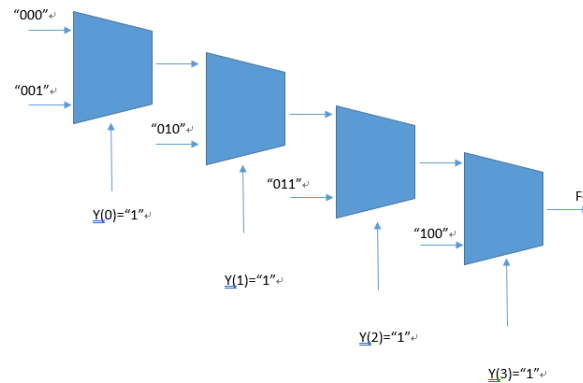


題目 1:

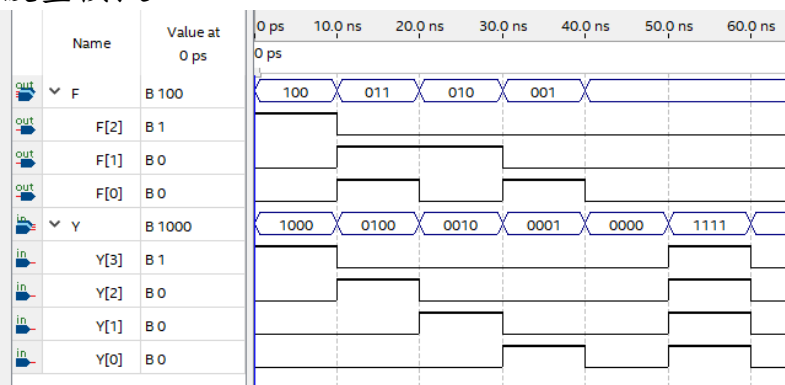
用 VHDL 語言 When else 方式，設計一個由序列最左邊'1'的位置決定輸出的電路。

VHDL code

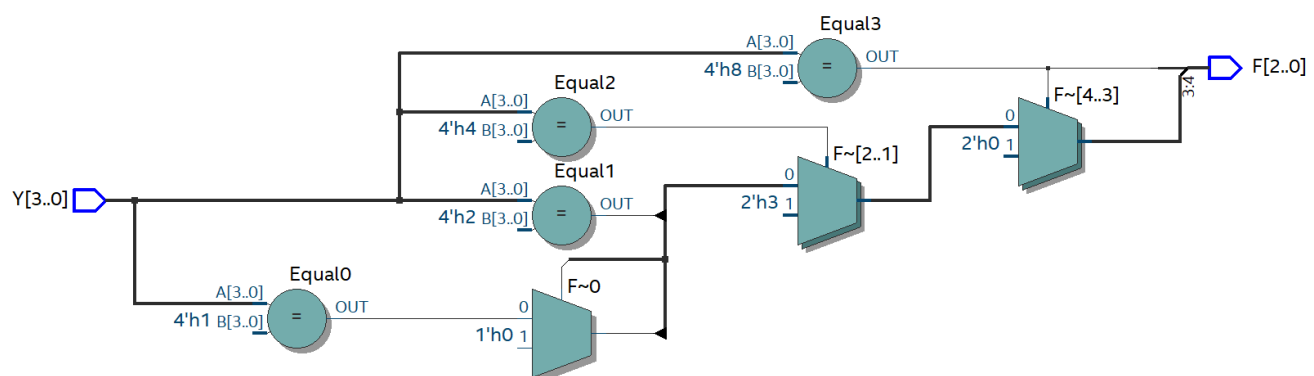
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity test1 is
port(Y:in std_logic_vector(3 downto 0);F:out std_logic_vector(2 downto 0));
end test1;
architecture a of test1 is
begin
    F<="100" when Y="1000" else
      "011" when Y="0100" else
      "010" when Y="0010" else
      "001" when Y="0001" else
      "000";
end a;
```



波型模擬



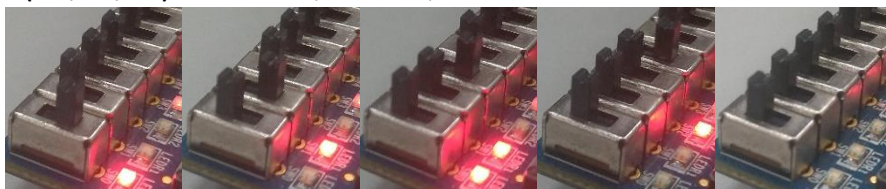
RTL 模擬



FPGA 狀態

Y(Y0,Y1,Y2,Y3)由 SW0, SW1, SW2, SW3 控制

F(F0,F1,F2)於 LEDR0, LEDR1, LEDR2 顯示



題目 2:

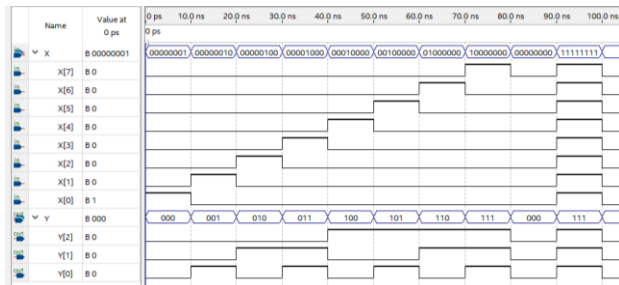
請設計一個八對三編碼器，用 With-Select-when 進行設計。

VHDL code

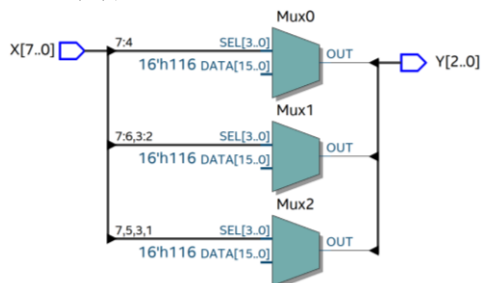
```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity test2 is
port(X: in std_logic_vector(7 downto 0);Y: out std_logic_vector(2 downto 0));
end test2;
architecture a of test2 is
begin
with X select
    Y<="000" when "00000001",
        "001" when "00000010",
        "010" when "00000100",
        "011" when "00001000",
        "100" when "00010000",
        "101" when "00100000",
        "110" when "01000000",
        "111" when "10000000",
        "XXX" when others;
end a;
```

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | M2 | M1 | M0 |
|----|----|----|----|----|----|----|----|----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

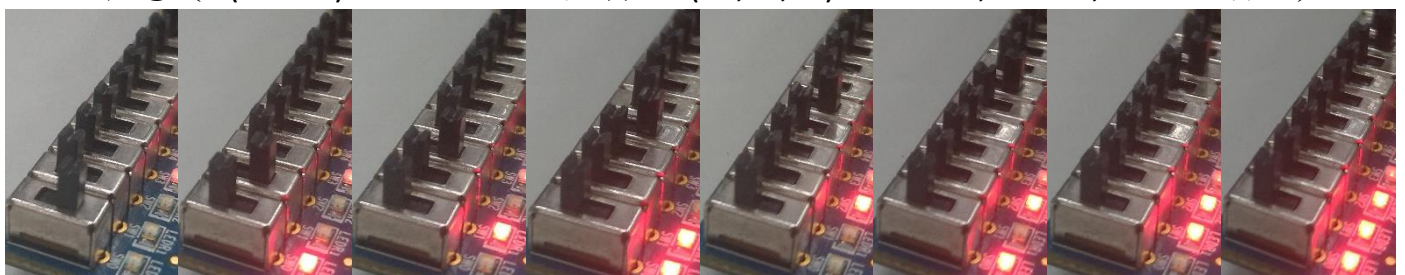
波形模擬



RTL 模擬



FPGA 狀態 (X(X0~X7)由 SW0~SW7 控制，Y(Y0,Y1,Y2)於 LEDR0, LEDR1, LEDR2 顯示)



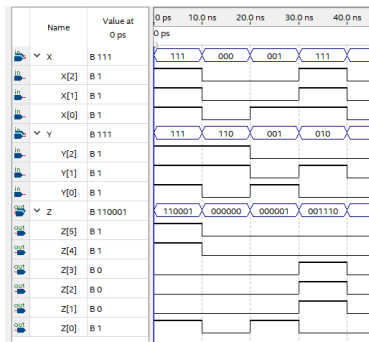
題目 3:

用 VHDL 語法設計一個 3*3 乘法器。

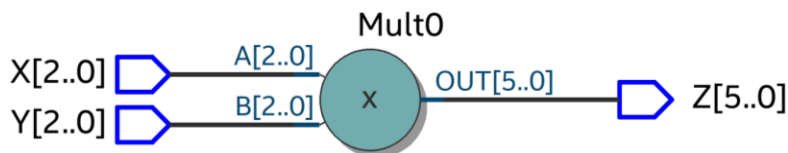
VHDL code

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use ieee.std_logic_unsigned.all;
entity test3 is
port(X,Y: in std_logic_vector(2 downto 0);Z: out std_logic_vector(5 downto 0));
end test3;
architecture a of test3 is
begin
    Z<=X*Y;
end a;
```

波型模擬

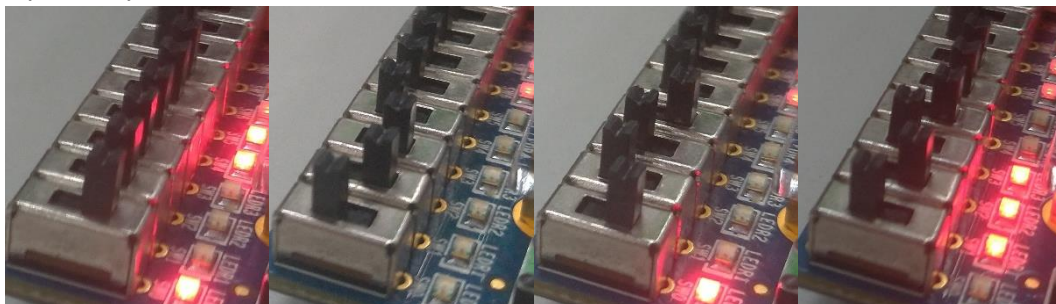


RTL 模擬



FPGA 狀態

X(X0,X1,X2)由 SW3, SW4, SW5 控制，Y(Y0,Y1,Y2)由 SW0, SW1, SW2 控制
Z(Z0~Z5)於 LEDR0~LEDR5 顯示



優質學生：助教！第三題一定要用題目提示的方法做喔？

助教：不用啦～結果對就可以了。

優質學生：痾…你確定嗎？……

助教：確定，因為這題是我改的，哈哈～

優質學生：喔好！謝謝！

助教：還有問題再叫我～

優(?)質學生：("Z<=X*Y" 诶嘿～…)