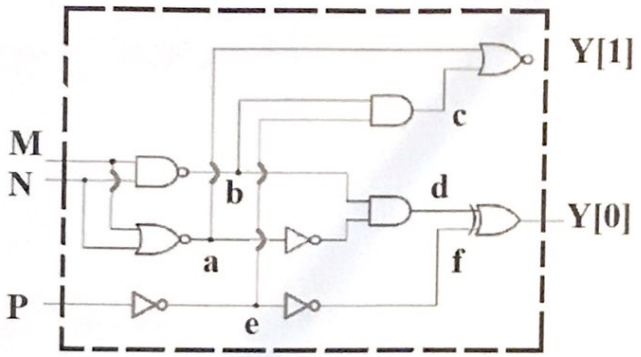
CSUS CPE166 Dummy Exercise Student Name: Xavier Howell

You need to upload the solution in multi-page PDF or WORD file format on the canvas course website.
You must write down your name on your solution sheets.

1. Complete the Verilog HDL design for the circuit below.




```
module ex1 ( M, N, P, Y );
input  M N P ;
output [1:0] Y ;
wire   a, b, c, d, e, f ;
assign a = ~M | N ;
assign b = ~M & N ;
assign c = b & e ;
assign d = b & ~a ;
assign e = ~P ;
assign f = ~e ;
assign Y[1] = ~a | c ;
assign Y[0] = d ^ f ;
endmodule
```

2. Write a testbench for the above circuit. You must generate testing cases for all possible values of M, N, and P.

```
module ex1_tb;
reg M,N,P;
wire [1:0] Y;

ex1 X1(.M(M),.N(N),.P(P),.Y(Y));

initial
began

    M=0; N=0;  P=0;
#5  M=0; N=0;  P=1;
#5  M=0; N=1;  P=0;
    M=0  N=1;  P=1;
    M=1  N=0;  P=0;
    M=1  N=0;  P=1;
    M=1  N=1;  P=0;
    M=1  N=1;  P=1;
    M=0  N=0;  P=0;

end

endmodule
```

3. Design a counter circuit in Veirlog. The counter counts from 0 to 220 and then repeats.

```
module counter (input, reset, move, output);
reg [8:0] movei;
always @(posedge clk or posedge rest)
  begin
    if (reset)
      move <= 9'h0;
    else if (~movei)
      move <= move + 9'd1;
    else
      move <= move - 9'd1;
  end
  assign counter = movei;
endmodule
```