# XMICRO Bus

Technical Specification



V0.5 2024-10-08

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- Multiple Masters
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- ATX Power Supply Compatibility
- Fully Open-source

## 1.2 Overview

The XMICRO Bus is a modular platform for building microcomputer systems. Discrete modules called “cards” communicate with one another through this bus over a backplane. Each card slot on the backplane is assigned a 256-byte address space and an interrupt request line. This uniform resource allocation allows most cards to be installed in the system with little or no special hardware configuration. Another advantage of this is the ability to use multiple identical cards in the same system without conflicts. The XMICRO Bus is designed to operate without reliance on any special CPU architecture features, such that most 8-bit microprocessors can be adapted to work with other devices designed for the bus.

An XMICRO system consists of the following elements:

- Backplane
- Primary Master
- Secondary Masters
- Slaves

A *Backplane* is the basis of any system. In its simplest form, the backplane handles power and signal distribution, decodes I/O addresses, and provides a power-on reset signal. Each backplane contains a number of *slots*, into which *cards* may be inserted to build and expand the system. More complex implementations may add significantly more functionality, including peripherals or an onboard CPU.

A *Primary Master* is a device which acts as the default system controller. Typically this will be the main CPU card. Primary masters must default to this operation unless the bus is requested by another device. Primary masters handle interrupt signals and bus requests. A system must have exactly one primary master installed.

A *Secondary Master* is a device with the ability to act as a temporary system controller. This is used for direct memory access by the secondary master.

A *Slave* is a device with no ability to control the system. Slaves are only capable of being read or written to under the command of a master.

Note: The master/slave designation is used only as a broad classification of the functionality of a device. It may be used to refer to either a discrete subsystem or a card as a whole. For example, a coprocessor card may have some control/status registers that can be accessed by the master. Those registers act as a slave device when being read or written to. When the coprocessor later takes control of the bus and directly accesses memory, it is acting as a master.

## 1.3 Definitions

### 1.3.1 System Terminology

Backplane: The central component of the system which provides bus power and signals to all devices

Motherboard: A subtype of backplane containing an integrated Primary Master

Extended backplane: Any backplane with greater than 8 slots

Slot: A uniquely identified position on a backplane where a card may be installed, and the associated set of allocated resources.

Card: A discrete module which interfaces with a backplane through a slot

Master: The current active system controller. This could be either the Primary Master or a Secondary Master

Slave: A device capable of being read or written to by the master.

### 1.3.2 Signal Notation

1) Active-low signals are denoted by an $\overline{\text{OVERLINE}}$.
2) A range of similar signals are referred to collectively using the format A<19..0>. This example is an abbreviation of signals A19 through A0.
3) *Table 1-1* lists the terminology used to describe signal states.

*Table 1-1: Signal State Terminology*

| Term | State (Active-high Signal) | State (Active-low Signal) |
|---|---|---|
| Asserted | 1, High | 0, Low |
| Deasserted | 0, Low | 1, High |
| Released | Z, High-impedance | Z, High-impedance |

### 1.3.3 Numerical Notation

1) All hexadecimal numbers are indicated by a leading dollar sign ($).
2) All address values are referenced using hexadecimal notation.
3) Numerical digits are substituted with “X” to indicate that any possible value is applicable.
4) I/O resource addresses use a two-digit hexadecimal value formatted as $X00, where X indicates a variable slot number. This notation is used because I/O devices only assess the least-significant eight address bits. See *3.1.2 I/O*.
5) Memory addresses use a 5-digit hexadecimal value corresponding to the values of A<19..0>. Example: $01234

# 2. Signaling

## 2.1 Signal Lines

### 2.1.1 Address Lines (A<19..0>)

Twenty unidirectional lines driven by the master to specify a memory or I/O location. Unused address lines must be held at a logic 0 state. Where a master implements bus arbitration (See *2.4 Bus Arbitration*), A<19..0> must be capable of entering a high-impedance state.

### 2.1.2 Data Lines (D<7..0>)

Eight bidirectional lines which carry information between master and slave devices. See *2.3 Data Transfers*.

### 2.1.3 Read Strobe (RD)

Asserted by the master to indicate that the addressed slave device may place data on the data lines. The data bus is read by the master at the rising edge of RD. See *2.3 Data Transfers*.

### 2.1.4 Write Strobe (WR)

Asserted by the master to indicate that it has placed data on the data lines. The data bus should be read by the addressed slave device at the rising edge of WR. See *2.3 Data Transfers*.

### 2.1.5 I/O Select (IOSEL)

Asserted by the master to access the backplane's card I/O address space. When asserted, A<19..8> determine which backplane slot is being addressed, and the backplane asserts the CSX signal for that slot. See *3.1 Address Spaces*.

### 2.1.6 Card Select – Slot X (CSX)

This slot-specific signal is driven by the backplane to indicate that the I/O address space is selected, and the current address is within the range of the slot's allocated I/O address space. While this signal is asserted, A<19..8> may be ignored by the slave card because their state is known. This is a discrete signal for each card slot. See *2.2 Address Signaling* and *3.1 Address Spaces*.

### 2.1.7 Main Memory Inhibit (INH)

This open-collector signal is used to inhibit general-purpose main memory. When INH is asserted, main memory must be prevented from reading or writing data, or driving the bus. This allows cards to make special-purpose memory available without reconfiguring or replacing the entire memory system. As this signal is typically derived from and therefore becomes stable after other Group A signals, its use may necessitate additional bus cycle time. INH has no effect on I/O operations. See *3.1.1 Memory*.

### 2.1.8 Wait (WAIT)

This open-collector line is asserted by the addressed slave device to indicate that the data transaction in progress is not yet ready to be completed. If WAIT is asserted concurrently with RD or WR, the master must hold all of its Group A signals in their current state until after WAIT is released. It is recommended that devices requiring greater than 100ns access time use this signal. See *2.3 Data Transfers*.

### 2.1.9 Reset (RST)

This open-collector signal resets the system and initializes it to a predictable state. During the power-on sequence, this signal should be asserted by the backplane until at least 100ms after all power supply rails have stabilized. RST may be used by any device for initialization.

### 2.1.1 Bus Request (BUSRQ)

This open-collector signal is asserted by a secondary master to request control of the bus. When the primary master is ready to release control of the bus, it will assert BUSAK. See *2.4 Bus Arbitration*.

### 2.1.2 Bus Acknowledge (BUSAK)

This signal is asserted by the primary master to indicate that it has released all Group A bus signals for control by a secondary master. The secondary master may only control the bus while this signal is asserted. See *2.4 Bus Arbitration*.

### 2.1.3 Halt (HALT)

This status line is asserted by the primary master to indicate to that it is in a halted state and waiting for an interrupt. Not to be confused with WAIT.

### 2.1.4 Interrupt Request – Slot X (IRQX)

This slot-specific line is asserted by a card to indicate that it requires the primary master's attention. This allows for interrupt vectoring and prioritization based on card position. This is a level-triggered interrupt signal. This is a discrete signal for each card slot. See *2.5.1 Level-triggered Interrupts*.

### 2.1.5 Summary Interrupt (SINT)

This open-collector signal is asserted by the backplane while any IRQX line is asserted. Therefore, this is a level-triggered interrupt signal. This signal is provided by the backplane and is not to be driven directly by a card.

### 2.1.6 Vectored Interrupt Lines (V<7..0>)

These eight lines correspond to the IRQX signal of slots 7..0 on a backplane. They are used by the primary master for interrupt prioritization and vectoring. A primary master may accept these signals as discrete interrupts from the first eight slots. These signals are provided by the backplane and are not to be driven directly by a card. See *3.3.1 Vectored Interrupts*.

### 2.1.7 Non-maskable Interrupt (NMI)

Open-collector edge-triggered interrupt signal. Its implementation may vary considerably between primary masters, so it is recommended that this signal be optional on any card using it. NMI should only be used for special signals requiring the immediate attention of the primary master and priority over all other interrupts. Some examples could be memory errors, power failure, or video timing. See *2.5.2 Edge-triggered Interrupts* and *3.3.2 Non-maskable Interrupt*.

### 2.1.8 System Clock (CLK)

This signal is the main system clock. Care should be taken to ensure it is a clean square wave. Its frequency and duty cycle are not defined. The primary master should typically provide this signal, however it may optionally be provided by another card such as a video card. It is recommended that primary masters do not strictly require externally generated clock signals to function. Any card capable of driving this signal must have an option to disable it, to prevent conflicts with other cards. Use of this signal for purposes that may restrict the system's compatibility with other devices is strongly discouraged.

### 2.1.9 Instruction Fetch (FETCH)

This signal is asserted by the primary master to indicate that the current read/write operation is an instruction fetch. This can be used by coprocessors or debuggers for synchronization and analysis. Implementation of this signal is optional.

### 2.1.10 Power Supply Rails (+12V, +5V, +5VSB +3.3V, 0V, -12V)

These non-signal lines supply power to the bus. Current capacity is defined by the individual backplane's specifications, as well as *4.2 Connectors*. See *4.3 Power Supply*.

*Table 2-1: Signal Sources*

| Group | Signal | Driver | Receiver |
|---|---|---|---|
| **A** *Information* | A<19..0> | Master | Any |
| | D<7..0> | Master (WR), Slave (RD) | Slave (WR), Master (RD) |
| | RD | Master | Any |
| | WR | Master | Any |
| | IOSEL | Master | Backplane, Memory Systems |
| | CSX | Backplane | Cards |
| | INH | Any | Memory Systems |
| **B** *Control* | WAIT | Slave | Master |
| | RST | Any | Any |
| | BUSRQ | Secondary Master | Primary Master |
| **C** *Status* | BUSAK | Primary Master | Secondary Master |
| | HALT | Primary Master | Any |
| | FETCH | Primary Master | Any |
| | CLK | Master (Typically) | Any |
| **D** *Interrupt* | IRQX | Any | Primary Master |
| | SINT | Backplane | Primary Master |
| | V<7..0> | Backplane | Primary Master |
| | NMI | Any | Primary Master |
| **E** *Supply* | +12V | Backplane | Any |
| | +5V | Backplane | Any |
| | +5VSB | Backplane | Any |
| | +3.3V | Backplane | Any |
| | 0V | Backplane | Any |
| | -12V | Backplane | Any |

## 2.2 Address Signaling

*Table 2-2* contains a sample of address signal relationships. A<19..0> and IOSEL are driven by the master, and CSX signals are asserted by the backplane in response. See *3.1 Address Spaces*.

*Table 2-2: Address Signal Relationships*

| A<19..0> | IOSEL | CSX (Slot 0) | CSX (Slot 1) | CSX (Slot 2) |
|---|---|---|---|---|
| $XXXXX | 1 | 1 | 1 | 1 |
| $000XX | 0 | 0 | 1 | 1 |
| $001XX | 0 | 1 | 0 | 1 |
| $002XX | 0 | 1 | 1 | 0 |

## 2.3 Data Transfers

Data are transferred asynchronously in 8-bit words (bytes). RD/WR may only be asserted while the address lines A<19..0>, IOSEL, and CSX are valid and stable, and must never be asserted simultaneously. During a read operation, the addressed slave places data on D<7..0>, which is read by the master at the rising edge of RD. During a write operation, the master places data on D<7..0>, which is read by the slave at the rising edge of WR.

The addressed slave may optionally assert WAIT during a data transfer to temporarily pause the sequence until it is ready to send or receive data. During this time, the master must not change the state of A<19..0>, IOSEL, CSX, RD, WR, or D<7..0>. When WAIT is high, the master may complete the transfer sequence.

*Table 2-3: Data Transfer Timing Parameters*

| No. | Symbol | Parameter | Min. | Max. |
|---|---|---|---|---|
| 1 | $T_{as}$ | Address setup time prior to $\overline{RD}$/$\overline{WR}$ falling edge | 10ns | — |
| 2 | $T_{ah}$ | Address hold time after $\overline{RD}$/$\overline{WR}$ rising edge | 10ns | — |
| 3 | $T_{ds}$ | Data setup time prior to $\overline{RD}$/$\overline{WR}$ rising edge | 20ns | — |
| 4 | $T_{dhr}$ | Data hold time after $\overline{RD}$ rising edge | 10ns | 30ns |
| 5 | $T_{dhw}$ | Data hold time after $\overline{WR}$ rising edge | 10ns | 30ns |
| 6 | $T_{wl}$ | $\overline{WAIT}$ falling edge delay after $\overline{RD}$/$\overline{WR}$ falling edge | 0ns | 40ns |
| 7 | $T_{wh}$ | $\overline{RD}$/$\overline{WR}$ rising edge delay after $\overline{WAIT}$ rising edge | 0ns | — |

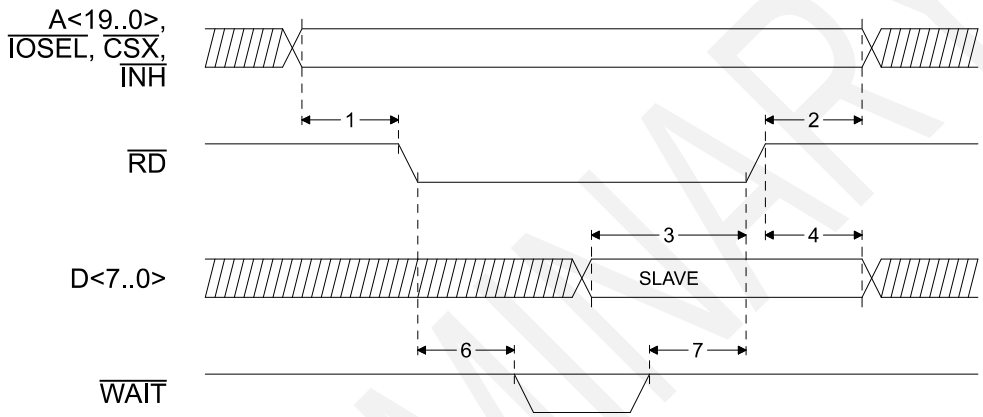


*Figure 2-1: Read Operation Timing*

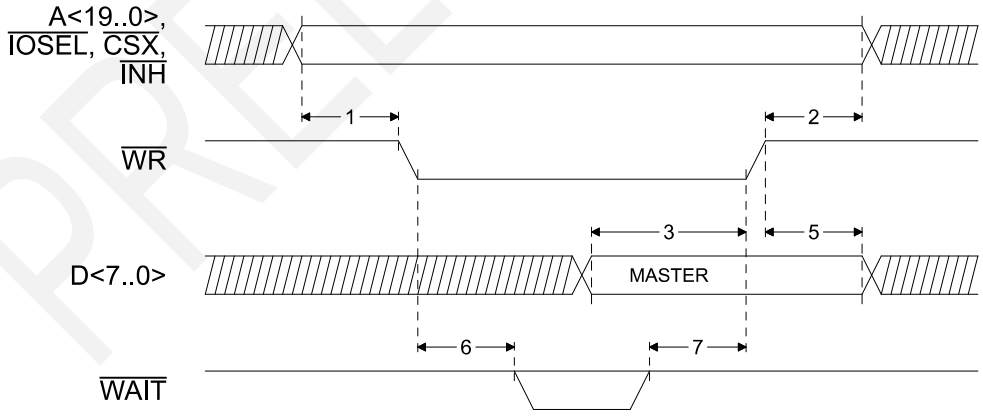


*Figure 2-2: Write Operation Timing*

## 2.4 Bus Arbitration

In the system's default state, the primary master has full control of the system bus. By asserting the $\overline{\text{BUSRQ}}$ line, a secondary master may request to temporarily take over control of some signals in order to directly access memory or I/O devices. When $\overline{\text{BUSRQ}}$ is asserted, the primary master gracefully hands over control of Group A signals.

The $\overline{\text{BUSAK}}$ signal indicates that the primary master has placed its Group A signals in a high-impedance state. These signals may be driven by a secondary master only while $\overline{\text{BUSAK}}$ is asserted. In order to prevent invalid data transfers, the primary master must remain in this high-impedance state until $\overline{\text{BUSRQ}}$ is released.

To avoid bus contention, secondary masters should wait for a command from the primary master before initiating a bus request, and must not initiate a bus request until the $\overline{\text{BUSRQ}}$ signal is no longer asserted by another device.

A typical bus arbitration sequence is as follows:

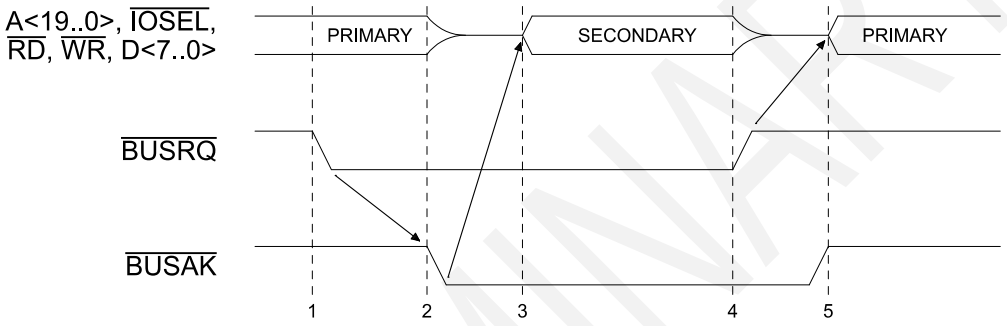


*Figure 2-3: Bus Arbitration Sequence*

1. A secondary master asserts the $\overline{\text{BUSRQ}}$ line.
2. The primary master, at its discretion, releases its Group A signals and asserts $\overline{\text{BUSAK}}$.
3. The secondary master begins driving its Group A signals.
4. The secondary master, at its discretion, releases its Group A signals and releases $\overline{\text{BUSRQ}}$.
5. The primary master deasserts $\overline{\text{BUSAK}}$ and resumes driving its Group A signals.

## 2.5 Interrupts

Each card's interrupt signals must default to a disabled state upon reset, such that they must be enabled through software before the card will assert them.

### 2.5.1 Level-triggered Interrupts

Level-triggered interrupt signals ($\overline{\text{IRQX}}$, $\overline{\text{V<7..0>}}$, $\overline{\text{SINT}}$) must be asserted by a device until it no longer requires the primary master's attention. A level-triggered interrupt signal which has been asserted and released before it was serviced may be disregarded.

### 2.5.2 Edge-triggered Interrupts

Edge-triggered interrupt signals ($\overline{\text{NMI}}$), as the name implies, are only sensitive to a falling edge. The state of the signal has no bearing on whether an edge-triggered interrupt should be serviced.

# 3. System Operation

## 3.1 Address Spaces

The system is divided into two discrete address spaces – “Memory” and “I/O”.

1) When $\overline{\text{IOSEL}}$ is not asserted, the memory address space is selected and read/write operations apply to memory devices.
2) When $\overline{\text{IOSEL}}$ is asserted, the I/O address space is selected and read/write operations apply to I/O devices.

### 3.1.1 Memory

There are two types of memory that can be added to a system:

1) “Main Memory” is memory that is accessible when $\overline{\text{INH}}$ is not asserted. It is recommended that only one device manages main memory in a system. Main memory is typically populated with general-purpose RAM.
2) “Override Memory”, when it is addressed, asserts the $\overline{\text{INH}}$ signal to disable main memory devices occupying the desired location. In this way, specialized memory devices may be added to a system without the need to reconfigure the main memory subsystem. In cases where $\overline{\text{INH}}$ is used, the main memory located at those addresses should be considered invalid.

### 3.1.2 I/O

1) Each card slot on a backplane is assigned 256 bytes of I/O address space, beginning at I/O address $00000. Each 256-byte block of I/O addresses is assigned to a slot number equal to the value of A<19..8>. For example, Slot 0 addresses are located from $00000-$000FF, Slot 1 from $00100-$001FF, etc.
2) When a slot’s I/O block is addressed by the master, the backplane asserts the $\overline{\text{CSX}}$ signal for that card.
3) $\overline{\text{CSX}}$ indicates to a slave that it is being addressed, and that A<7..0> contain the address to be accessed. Slave devices may only use A<7..0> for addressing purposes, and A<19..8> must be ignored by slaves during I/O operations.
4) A backplane’s I/O decoding logic must ignore any I/O address bits that are not required to access the number of implemented slots.

## 3.2 Reserved Addresses

Addresses $XFC-$XFF are reserved for special bus functions. These should not be used except as described in *Table 3-1*.

*Table 3-1: Reserved Addresses*

| Address | Purpose |
|---|---|
| $XFC | Reserved |
| $XFD | Reserved |
| $XFE | Reserved |
| $XFF | Card ID |

### 3.2.1 Card IDs

Each card should present an identification value at address $XFF which is unique to that type of card within the system. Identical cards should have identical IDs. Cards may be assigned a permanent ID as part of the XMICRO bus specification. Refer to *Appendix A* for Card ID assignments.

## 3.3 Interrupts

Interrupts provide cards with a means of requesting the attention of the primary master. Since interrupt schemes vary considerably between CPUs, the implementation of interrupts in an XMICRO system is relatively loosely defined.

When an interrupt signal is asserted, it is expected that the primary master will respond to it as soon as possible. Table 3-2 lists all interrupt signals on the bus, in order from highest to lowest priority. When multiple interrupt signals are being asserted simultaneously, they should be assessed in order from highest to lowest priority.

*Table 3-2: Interrupt Signal Priority*

| Signal | Priority |
|---|---|
| $\overline{\text{NMI}}$ | Highest |
| $\overline{\text{V0}}$ | |
| $\overline{\text{V1}}$ | |
| $\overline{\text{V2}}$ | |
| $\overline{\text{V3}}$ | |
| $\overline{\text{V4}}$ | |
| $\overline{\text{V5}}$ | |
| $\overline{\text{V6}}$ | |
| $\overline{\text{V7}}$ | |
| $\overline{\text{SINT}}$ | Lowest |

### 3.3.1 Vectored Interrupts

$\overline{\text{IRQX}}$ is asserted by cards as a general-purpose interrupt request. While any card's $\overline{\text{IRQX}}$ line is asserted, $\overline{\text{SINT}}$ is also asserted by the backplane as a summary of all interrupt requests.

Signals $\overline{\text{V<7..0>}}$ are connected on the backplane to the corresponding $\overline{\text{IRQX}}$ of slot 7..0. On extended backplanes, implementation of $\overline{\text{IRQX}}$ on slot 8 and higher is optional. The backplane may use $\overline{\text{IRQX}}$ on these slots to assert a summary interrupt ($\overline{\text{SINT}}$) with no vector signals ($\overline{\text{V<7..0>}}$) asserted.

### 3.3.2 Non-maskable Interrupt

$\overline{\text{NMI}}$ is a special interrupt intended for timing-sensitive operations. It has a higher priority than any other interrupt. Where possible, a primary master should immediately respond to an NMI, including interrupting an in-progress interrupt service routine. No other interrupts should interrupt an NMI service routine.

Due to hardware limitations, some primary masters may not be capable of overriding an interrupt routine in progress. In this case, $\overline{\text{NMI}}$ should be serviced as soon as possible.

# 4. Electrical Specifications

## 4.1 Signal Lines

### 4.1.1 Signal Characteristics

1) A receiver must recognize a voltage of ≤ 0.8V as a logic 0, and a voltage of ≥ 2.0V as a logic 1.

2) The minimum sink current capability of any driver on any line must be 20mA at 0.5V. Further, it is recommended that drivers with minimum source capability of 20mA at 2.4V be used.

*Table 4-1: Bus Driver and Receiver Characteristics*

| Signal | Driver Topology | Receiver Hysteresis |
|---|---|---|
| A<19..0> | Tri-state | Not Required |
| D<7..0> | Tri-state | Not Required |
| $\overline{RD}$ | Tri-state | Not Required |
| $\overline{WR}$ | Tri-state | Not Required |
| $\overline{IOSEL}$ | Tri-state | Not Required |
| $\overline{CSX}$ | Push-pull | Not Required |
| $\overline{BUSAK}$ | Push-pull | Not Required |
| $\overline{HALT}$ | Push-pull | Not Required |
| $\overline{FETCH}$ | Push-pull | Not Required |
| CLK | Push-pull | Not Required |
| $\overline{INH}$ | Open-collector | Required |
| $\overline{WAIT}$ | Open-collector | Required |
| $\overline{RST}$ | Open-collector | Required |
| $\overline{BUSRQ}$ | Open-collector | Required |
| $\overline{NMI}$ | Open-collector | Required |
| $\overline{IRQX}$ | Open-collector | Not Required |
| $\overline{SINT}$ | Open-collector | Not Required |
| $\overline{V}$<7..0> | Open-collector | Not Required |

### 4.1.2 Signal Integrity

For all signal lines, care must be taken to maintain high-speed signal integrity.

1) A card should add no more than 2” of total conductor length to any bus signal.

2) A card should present no more than 25pF capacitance to any bus signal.

### 4.1.3 Termination

1) When no device is driving a bus line, that line must be pulled to a high state by the backplane.

2) The combined DC current of all bus terminations must not exceed 22mA on any signal line.

3) The recommended active termination scheme for all bus signal lines is a 270Ω resistor to +2.85V at each end of the backplane.

## 4.2 Connectors

### 4.2.1 Backplane Interconnects

1) Backplanes must be fitted with female 62-position dual-row card edge connectors with a 0.1” contact pitch, designed for 0.0625” card thickness. TE Connectivity 7-5530843-0 or equivalent is recommended. Each of these connectors is considered a discrete slot.

2) Cards must be fitted with male card-edges compatible with the specified backplane connectors and conforming to physical specifications outlined in *5.1 Cards*.

3) The average current on any backplane connector pin must not exceed 2A. The recommended maximum current on backplane connectors is 1A for supply pins and 100mA for all other pins. If lower than these values, maximum design current for each rail must be specified in the included documentation for a backplane, or on the backplane PCB.

4) No XMICRO bus signal may be delivered between any two devices except by these backplane interconnects.

*Table 4-2: Backplane Interconnect Pinout*

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +12V | 2 | +3.3V |
| 3 | 0V | 4 | 0V |
| 5 | +5V | 6 | +5V |
| 7 | -12V | 8 | +5VSB |
| 9 | $\overline{\text{CSX}}$ | 10 | $\overline{\text{RST}}$ |
| 11 | $\overline{\text{BUSRQ}}$ | 12 | $\overline{\text{BUSAK}}$ |
| 13 | CLK | 14 | $\overline{\text{FETCH}}$ |
| 15 | $\overline{\text{HALT}}$ | 16 | $\overline{\text{WAIT}}$ |
| 17 | $\overline{\text{INH}}$ | 18 | $\overline{\text{IOSEL}}$ |
| 19 | $\overline{\text{RD}}$ | 20 | $\overline{\text{WR}}$ |
| 21 | 0V | 22 | A0 |
| 23 | A1 | 24 | A2 |
| 25 | A3 | 26 | A4 |
| 27 | A5 | 28 | A6 |
| 29 | A7 | 30 | A8 |
| 31 | A9 | 32 | A10 |
| 33 | A11 | 34 | A12 |
| 35 | A13 | 36 | A14 |
| 37 | A15 | 38 | A16 |
| 39 | A17 | 40 | A18 |
| 41 | A19 | 42 | 0V |
| 43 | D0 | 44 | D1 |
| 45 | D2 | 46 | D3 |
| 47 | D4 | 48 | D5 |
| 49 | D6 | 50 | D7 |
| 51 | $\overline{\text{SINT}}$ | 52 | $\overline{\text{IRQX}}$ |
| 53 | $\overline{\text{V0}}$ | 54 | $\overline{\text{V1}}$ |
| 55 | $\overline{\text{V2}}$ | 56 | $\overline{\text{V3}}$ |
| 57 | $\overline{\text{V4}}$ | 58 | $\overline{\text{V5}}$ |
| 59 | $\overline{\text{V6}}$ | 60 | $\overline{\text{V7}}$ |
| 61 | $\overline{\text{NMI}}$ | 62 | 0V |

### 4.2.2 Supplemental Power

Supplemental power may be delivered using TE Connectivity 174804-1 (Male) or equivalent installed on cards. Pinout and current limits match ATX standards for peripheral connectors.

*Table 4-3: Supplemental Power Connector Pinout*

| Pin | Signal |
|---|---|
| 1 | +12V |
| 2 | 0V |
| 3 | 0V |
| 4 | +5V |

## 4.3 Power Supply

### 4.3.1 Main Power Supply

1) A backplane must supply cards with the following voltages: +12V, +5V, +5VSB, 0V, -12V.
2) Specifications of the supply rails must meet ATX power supply standards.
3) The use of an ATX-compatible power supply is recommended.

### 4.3.2 Supplemental Power Supplies

Cards may use an additional connector to supplement the +12V, +5V, and 0V rails. Where such a connector is used, the following requirements apply:

1) All supplemental power rails must match the potential of the bus rails such that no significant current flows between them.
2) Supplemental power must be delivered using connectors as specified in *4.2.2 Supplemental Power*.

## 4.4 Grounding

### 4.4.1 Signal Ground

The 0V supply rail serves as the 0V reference and return path for all bus signals and supply rails.

### 4.4.2 Chassis Ground

1) A separate chassis ground must be maintained for conductive chassis members. The purpose of the chassis ground is to provide a safe, low-impedance return path for ESD and electrical faults, as well as to avoid stray ground paths between cards which could result in unpredictable operation.
2) Where mechanical mounting holes in cards can be used to make an electrical connection to chassis members or other cards, those holes must be isolated from the 0V supply rail. Mechanical mounting holes are not required to be electrically connected to each other.
3) Where connectors have a separate shield conductor that is not used as a signal ground, the shield should be tied to chassis ground. It is recommended that connector shields be electrically connected to the rear-edge mounting holes of the card.
4) Chassis ground should be tied to the signal ground at the backplane.

# 5. Physical Specifications

## 5.1 Cards

1) A card's dimensions must not exceed the overall dimensions shown in *Figure 5-1*.
2) Card edge connectors must match the dimensions shown in *Figure 5-1*.
3) Pin 1 of the edge connector must be indicated on the card.
4) Card edge connectors should be gold-plated for reliability. HASL or similar soft surface finishes are discouraged.
5) Card edge connectors should be chamfered for easier insertion.
6) The use of standard "full-size" and "half-size" card form-factors shown in *Figure 5-1* is strongly encouraged.
7) Standard card mounting holes should be isolated from the backplane's 0V pins and treated as a discrete chassis ground if conductive. See *4.4.2 Chassis Ground*.
8) External I/O connectors may only be placed on the rear edge.

## 5.2 Backplanes

1) Backplanes must conform to the measurements and orientation shown in *Figure 5-2*.
2) Pin 1 must be indicated on at least one slot.
3) Each slot's number must be indicated on the PCB
4) Maximum component height under cards may not exceed the edge connectors
5) All backplane slots must be capable of receiving maximum-dimension cards

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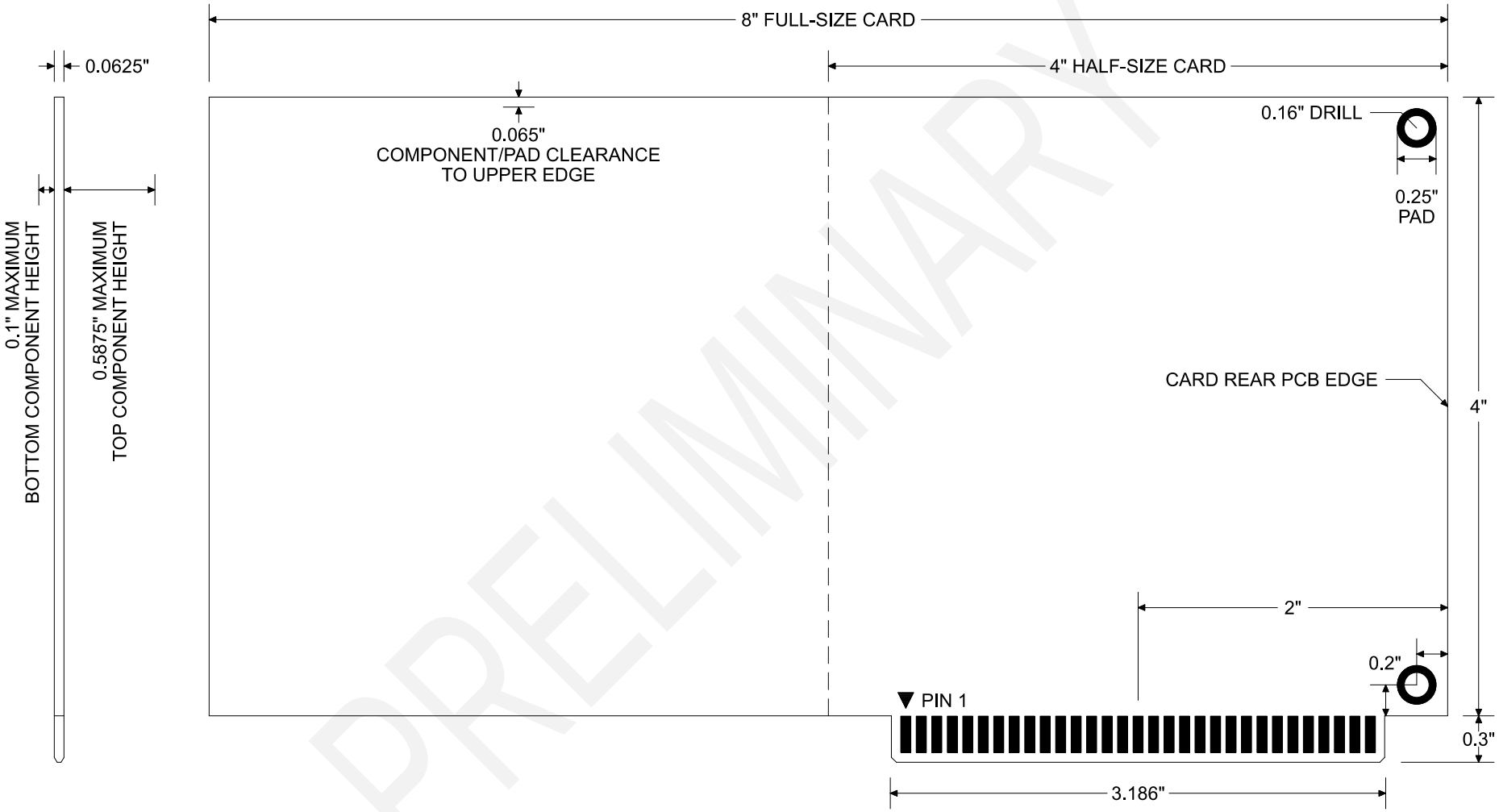


*Figure 5-1: Card Physical Dimensions*

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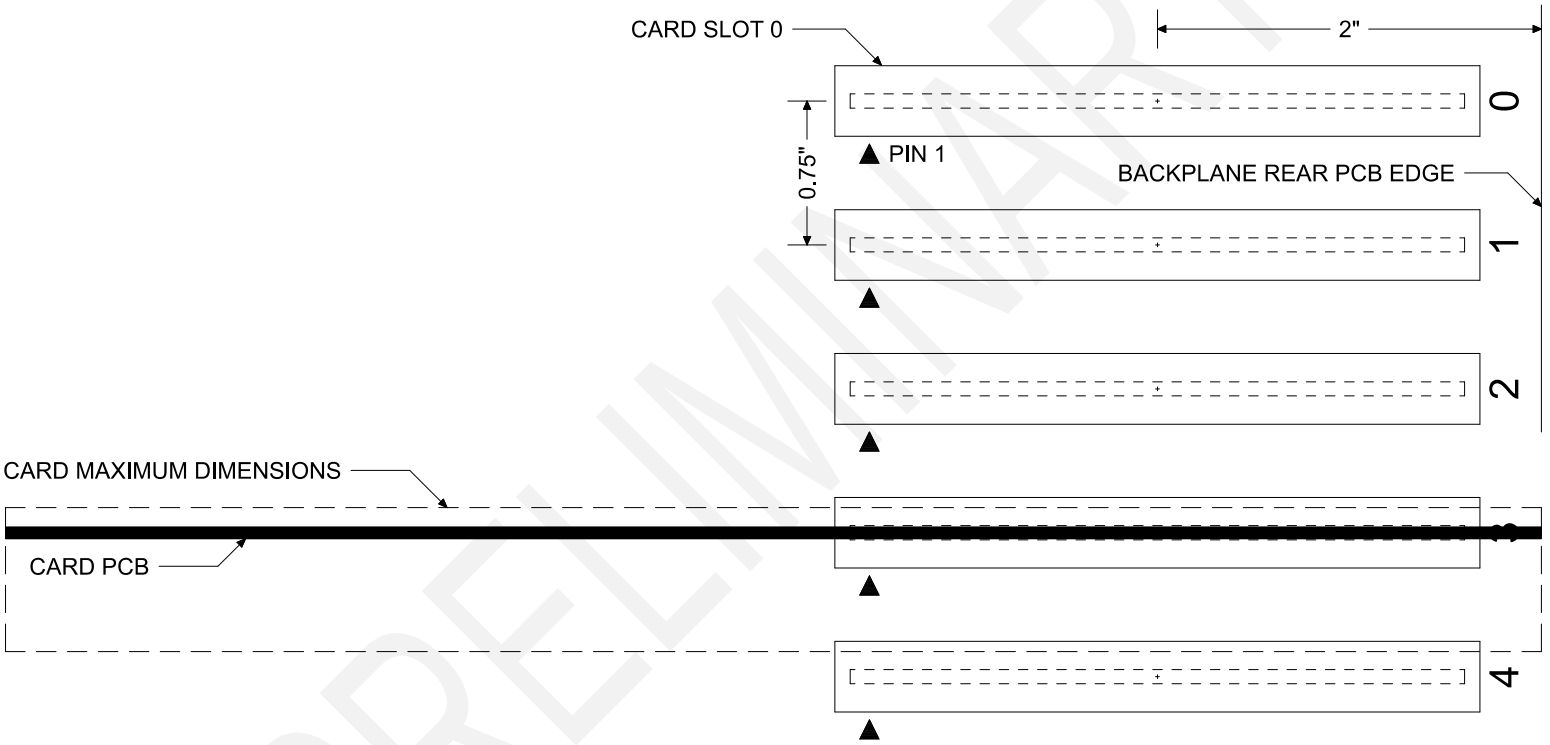


*Figure 5-2: Backplane Physical Dimensions*

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# Appendix A. Card IDs

1) IDs $00 and $FF are reserved to indicate that no card is installed in the addressed slot.
2) IDs $E0-$FE will not be assigned to any specific devices and may be used for any device that has not been granted a permanent ID.
3) Any ID not listed in Table *A-1* is not currently assigned and may not be used.

*Table A-1: Card ID Assignments*

| Value | Device |
|---|---|
| $00 | Reserved (No card detected) |
| $01 | XMICRO-6502 |
| $02 | XMICRO-MEMORY |
| $03 | XMICRO-CF |
| $04 | XMICRO-SERIAL |
| $05 | XMICRO-VDP |
| $06 | XMICRO-7SEG |
| $E0-$FE | Open for any use |
| $FF | Reserved (No card detected) |