1. General Description

The XMICRO-SERIAL is an XMICRO slave card which provides two high-speed RS-232 serial ports and a PS/2 interface for a keyboard or mouse.

1.1 Features

- Two RS-232 serial ports with 16C550 UARTs
- 115.2 kilobaud maximum symbol rate per serial port
- Interrupt-driven PS/2 interface
- Hardware compatible with upgraded 16Cx50 ICs

1.2 System Outline

Table 1: Card Memory Map

ADDRESS RANGE	FUNCTION
$X00-$X07	UART 1
$X08-$X0F	UART 2
$X10	PS/2 Data Register
$X11	Card Status Register (R)
$XFF	Card ID Register (R)

Table 2: Card Configuration

SETTING	FUNCTION
JP1	Enable wait states for all card accesses
JP2	Enable CF interrupts
JP3	Enable bus $\overline{\text{WAIT}}$ signal
JP4	Enable bus $\overline{\text{IRQ}}$ signal
JP5	Clear RTC NVRAM
JP6	Enable CF-generated wait states

2. UARTs

Two high performance 16C550 UARTs provide high-speed RS-232 communication through connectors J1 and J2. *Table 1* lists the locations of their internal register sets. UART operation is beyond the scope of this document and may be found in the 16C550 datasheet. A header next to UART 2 breaks out the two additional user-defined outputs which are otherwise unused.

Although the card was designed around the 16C550 UART, several compatible UARTs in the 16x50 series exist which may be used in its place for an improved feature set. The 16C850 is known to work with this card.

3. PS/2 Interface

3.1 Receiving Data

When a data byte is received from the connected device, the PS/2 Data Ready status bit (CSR bit 5) is set. This indicates that there is new data waiting in the PS/2 Data Register (PDR). When interrupts are enabled, the Data Ready bit also indicates an active PS/2 interrupt. The Data Ready bit is cleared when the PDR is read, which also signals to the device that it may send another byte.

3.2 Sending Data

Data may also be written to the PDR. During a write cycle, the PS/2 Write Status bit (CSR bit 3) is set. Data may only be written to the PDR when this bit is clear, indicating that no write cycle is in progress. The PDR cannot be written to when the Data Ready status bit (CSR bit 5) is set.

3.3 Interrupts

After a reset, PS/2 interrupts are not sent to the XMICRO bus by default. To enable PS/2 interrupts, UART 1's OP1 output must be set to logic 0. This is to avoid unknown interrupts before the system and drivers have been fully initialized. This setting has no effect on the operation of the PS/2 system, and the Data Ready bit may be polled if interrupts are not available/desired.

3.4 Parity Errors

If a parity error is detected in a received data byte, the PS/2 Error status bit (CSR bit 4) will be set. This indicates the data in the PDR is invalid and should not be read. In this case, a recovery may be attempted by performing the following procedure with minimal delay between steps:

1. Write a retransmit command to the PDR
2. Read the PDR and discard the data

This begins a write cycle, which keeps the PS/2 clock inhibited, preventing more data from being sent from the device. Reading the PDR then clears the Data Ready status, allowing the write cycle to proceed before the device attempts to send another byte. This procedure should also allow the receive circuit's shift registers to be cleared and resynchronized.

4. Onboard Registers

Table 3: Card Registers

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
$X11	UART 1 Interrupt	UART 2 Interrupt	PS/2 Data Ready	PS/2 Error	PS/2 Write Status	0	0	0
$XFF	Card ID $04 (R)							

4.1 Card Status Register ($X11)

The CSR is used to determine basic status of the card's functions in a single read operation. CSR bits indicate the following:

CSR Bit 7:
- 0: UART 1 interrupt is not asserted
- 1: UART 1 interrupt is asserted

CSR Bit 6:
- 0: UART 2 interrupt is not asserted
- 1: UART 2 interrupt is asserted

CSR Bit 5:
- 0: PS/2 data register is empty, interrupt is not asserted
- 1: PS/2 data register contains new data, interrupt is asserted

CSR Bit 4:
- 0: PS/2 data is good
- 1: PS/2 data is invalid (parity error)

CSR Bit 3:
- 0: PS/2 write cycle is not in progress
- 1: PS/2 write cycle is in progress

4.2 Card ID Register ($XFF)

The Card ID Register contains the ID value $04 as assigned in XMICRO Bus specification Appendix A. This register is used by the system to determine card types and locations.

5. Connector Shield

The connector shields are isolated from the rest of the card to provide flexibility for different system configurations. Ideally this should be isolated and tied to the system chassis, which should then have a good connection to mains-earth. When no other shielding solution is in place, JP4 should be shorted to connect the shields to the card's ground plane.

6. Theory of Operation

6.1 PS/2 Receive

Before data is received, the receive shift registers U12 and U13 are cleared to logic 0. When the PS/2 device sends a byte, it clocks the data into receive shift register pair U12 and U13. The data input to the shift registers is inverted, making the start bit 1. When the start bit reaches U13 output QB, it is detected by gate U3B which clocks the shift register data into U11 and U6A. Parity is calculated by U10 and compared to the received parity bit.

On the final clock pulse of the received data, the device sends the stop bit. This pushes the start bit to U13 output QC, which clears the input shift registers and prepares them for another byte. After clearing, U3B will no longer have an AND condition. This then clocks flip-flop U14B, which holds the PS/2 clock line low, preventing the device from sending more data, and asserts the PS/2 Data Ready bit in the CSR as well as the PS/2 interrupt.

When the data is read from the PDR (U18), U14A is clocked by the read operation and resets U14B, which then clears the Data Ready bit and interrupt, and releases the PS/2 clock line.

6.2 PS/2 Transmit

When data is written to the PDR (U20 and U21), flip-flop U5A is clocked. Its output asserts the PS/2 Write Cycle Status bit in the CSR. This WCS signal clocks flip-flop U6B and triggers a ~120µS low pulse on the PS/2 clock line. WCS simultaneously activates gate U7C, allowing shift register data to pass to the PS/2 data line. At this time, the data line will be held low, which will signal to the device that data is being transmitted at the rising edge of the 120µS clock pulse.

When the 120µS pulse ends, Q1 releases the PS/2 clock line, allowing the device to provide the clock signal for this transmission. Data in the transmit shift registers U20 and U21 are then clocked out of Q3 using the PS/2 clock signal provided by the device.

At the end of the cycle, the device acknowledges that the transmission is complete by pulling the PS/2 data line low. At this time, the output bit in the shift register is high, and this discrepancy causes gate U3C to output low. At the final clock rising edge, flip-flop U5B clocks U3C's low signal, which resets U5A and ends the write cycle.

6.3 UARTs

75185 driver/receiver ICs U28 and U29 translate signals between 5V TTL and TIA-232 compatible +/-12V signals. These ICs are the main bottleneck that puts the communication speed at 115200 baud. Faster drivers and a higher speed oscillator could potentially be substituted to provide faster communication, typically at the cost of maximum cable length and drive voltage. Alternatively, a TTL-level USB UART such as the FT232 could be connected directly to a 16C550 UART at its full speed.

DATA_BUS:D[0..7]

ADDRESS_BUS:A[0..4],$\overline{RD}$,$\overline{WR}$,$\overline{CSX}$

UART 1
$X00-$X07

U26 — 16C550

A0 A1 A2 $\overline{AS}$ $\overline{IOR}$ $\overline{IOW}$ IOR IOW CS0 CS1 $\overline{CS2}$ $\overline{DSR}$ $\overline{CTS}$ $\overline{CD}$ $\overline{RI}$ RESET XTAL1 XTAL2 RCLK

D0 D1 D2 D3 D4 D5 D6 D7 TX RX $\overline{TXRDY}$ $\overline{RXRDY}$ $\overline{DTR}$ $\overline{RTS}$ $\overline{DDIS}$ $\overline{OP1}$ $\overline{OP2}$ INT $\overline{BAUDOUT}$

U23A, U23B — 74HCT04N

RST/4.6D

Y1 — 1.8432MHz (VCC, OE, FO, GND; +5V, 0V)

U28 — 75185N

RY1 RY2 RY3 DA1 DA2 RY4 DA3 RY5 RA1 RA2 RA3 DY1 DY2 RA4 DY3 RA5 +5V VDD 0V VSS

J1 — DCD DSR RXD RTS TXD CTS DTR RI GND; CGND

+12V/4.3D -12V

KB_INT_ENABLE/2.1E

INT_UART1/5.5B

UART 2
$X08-$X0F

U27 — 16C550

A0 A1 A2 $\overline{AS}$ $\overline{IOR}$ $\overline{IOW}$ IOR IOW CS0 CS1 $\overline{CS2}$ $\overline{DSR}$ $\overline{CTS}$ $\overline{CD}$ $\overline{RI}$ RESET XTAL1 XTAL2 RCLK

D0 D1 D2 D3 D4 D5 D6 D7 TX RX $\overline{TXRDY}$ $\overline{RXRDY}$ $\overline{DTR}$ $\overline{RTS}$ $\overline{DDIS}$ $\overline{OP1}$ $\overline{OP2}$ INT $\overline{BAUDOUT}$

J4

U29 — 75185N

RY1 RY2 RY3 DA1 DA2 RY4 DA3 RY5 RA1 RA2 RA3 DY1 DY2 RA4 DY3 RA5 +5V VDD 0V VSS

J2 — DCD DSR RXD RTS TXD CTS DTR RI GND; CGND

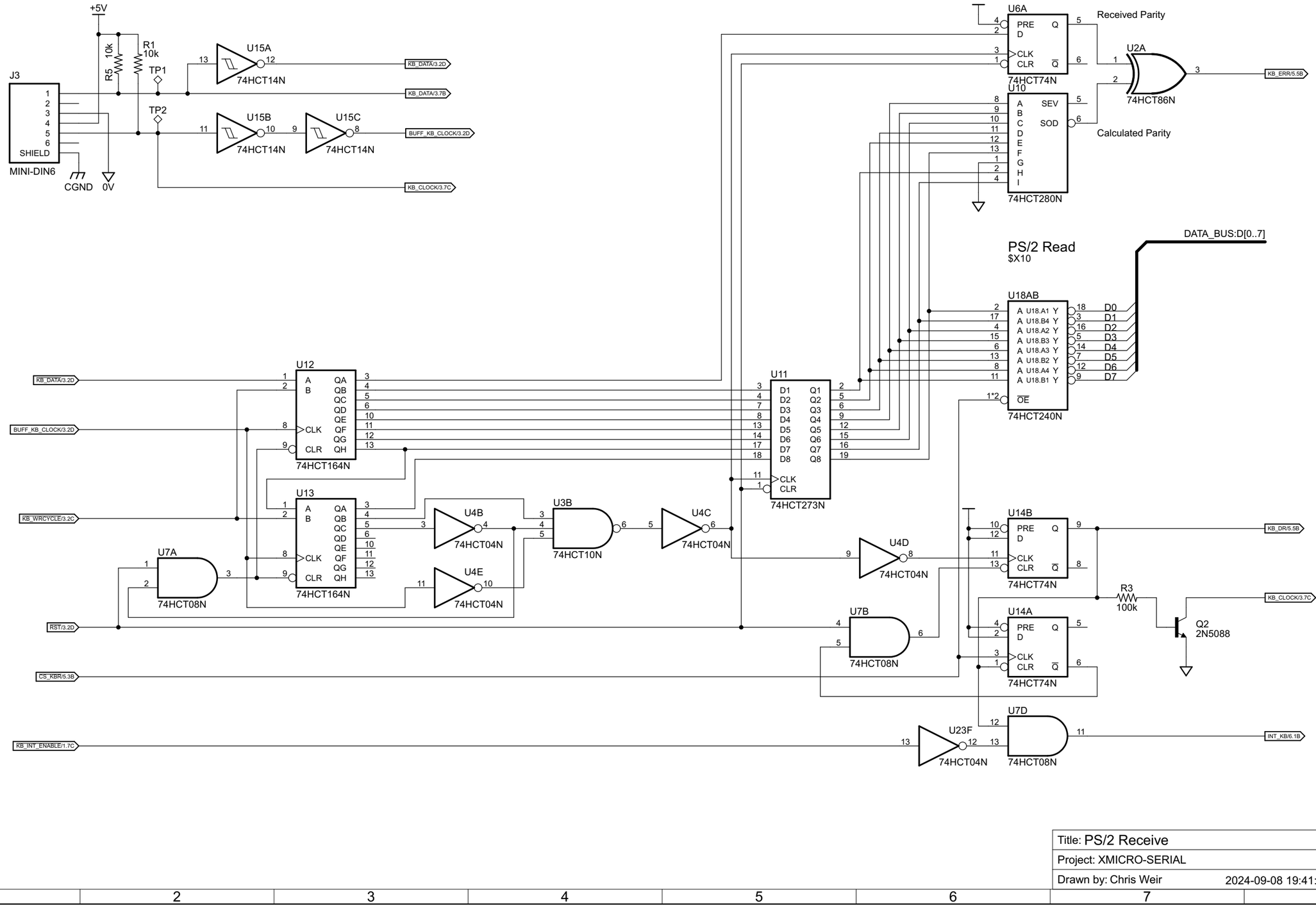
+12V/4.3D -12V INT_UART2/5.5B

U24 — TC962

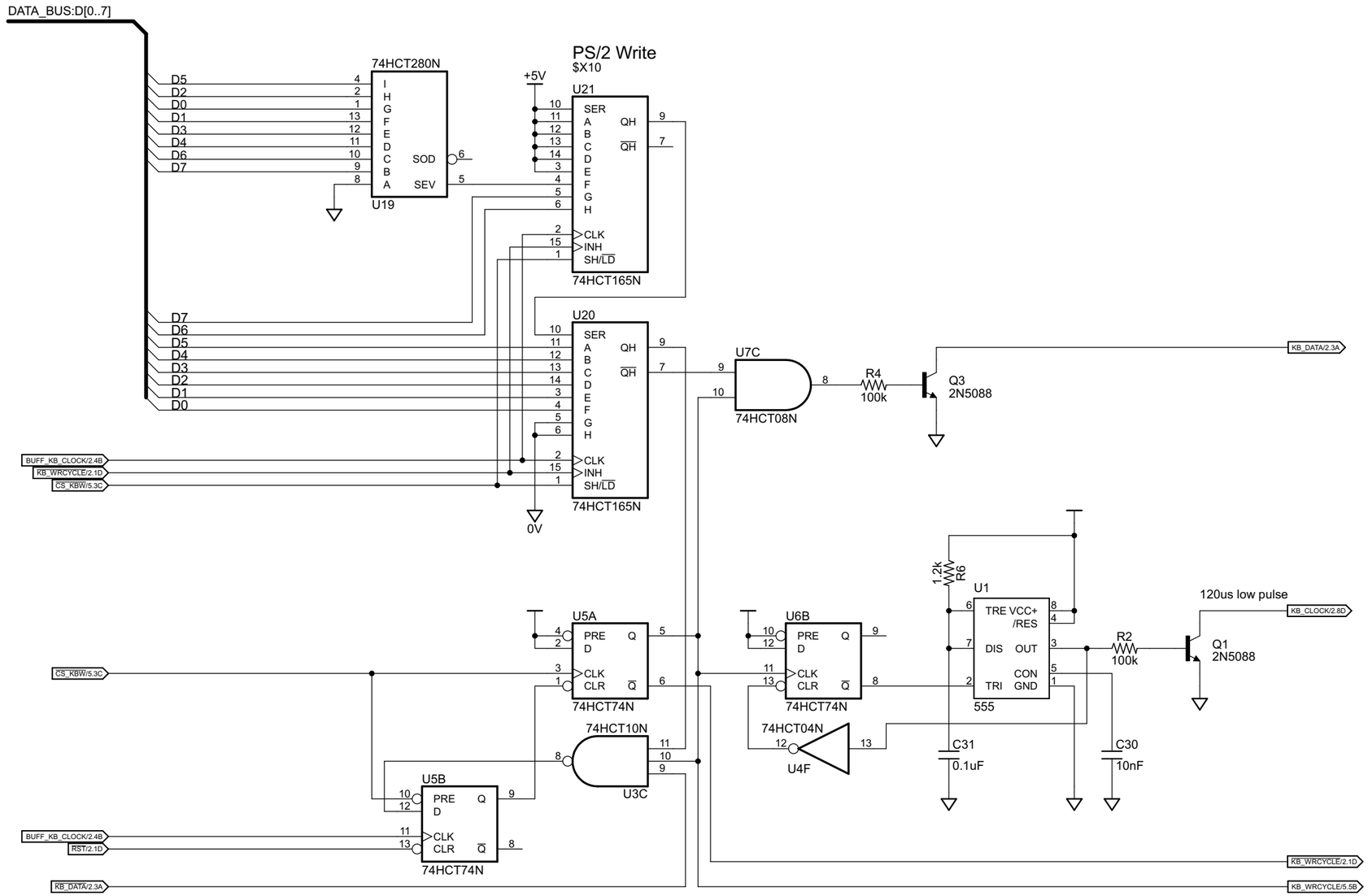
VDD 0V VOUT C+ C- FREQX2 OSC ZC

C33 10uF, C24 0.1uF, C35 10uF, C34 10uF

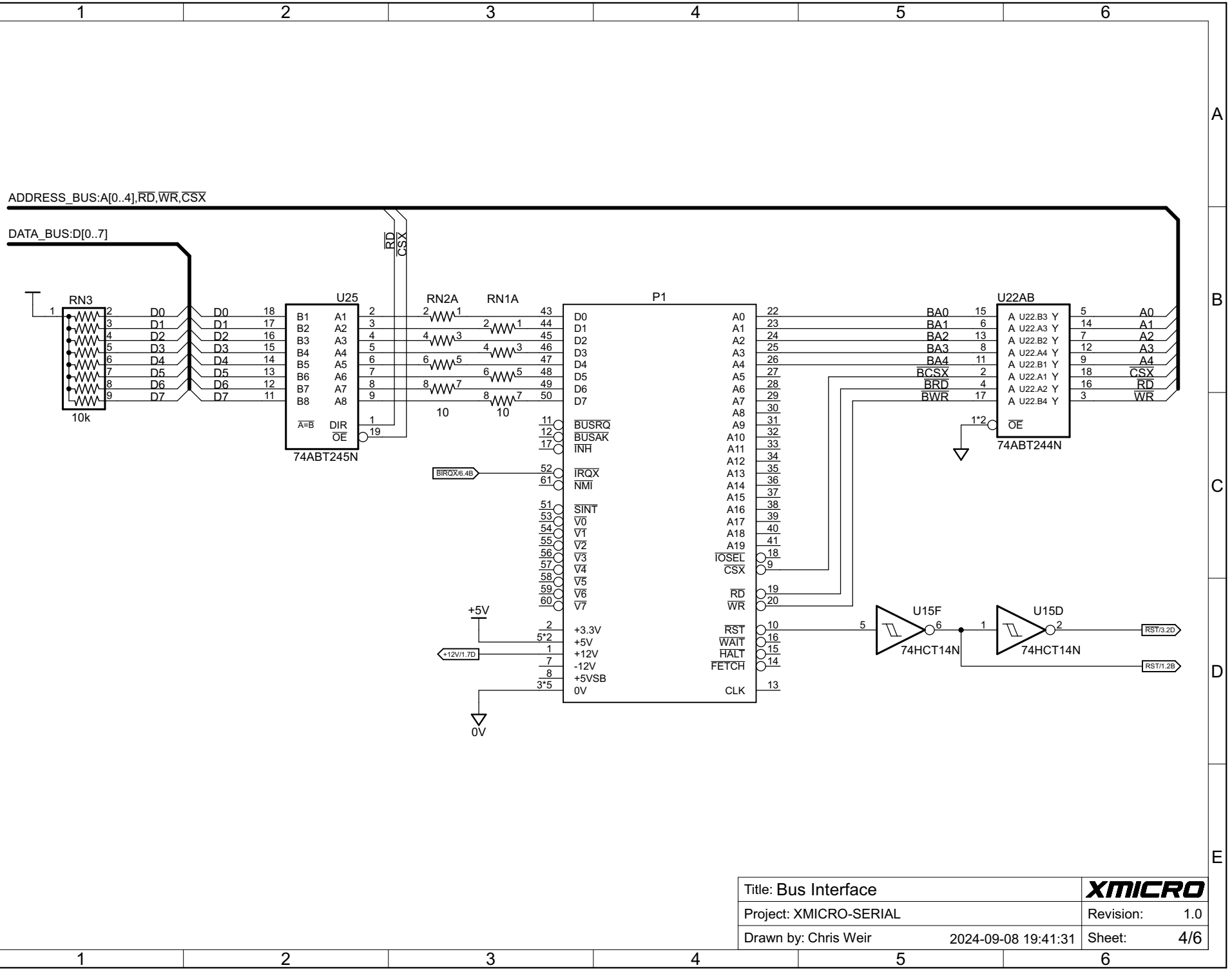
Title: RS232 Interfaces		XMICRO
Project: XMICRO-SERIAL		Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31	Sheet: 1/6



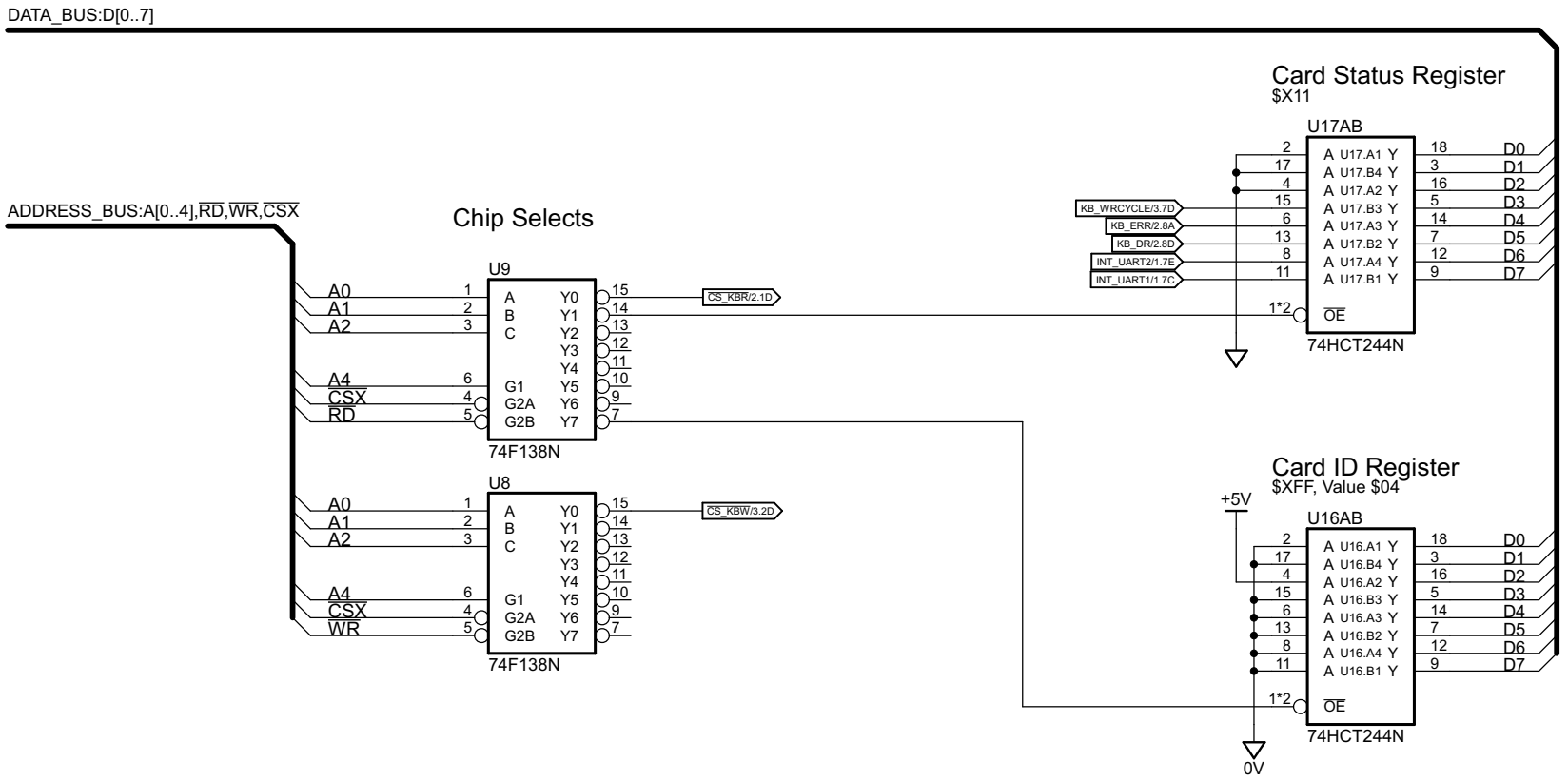
Title: PS/2 Receive		XMICRO
Project: XMICRO-SERIAL		Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31	Sheet: 2/6



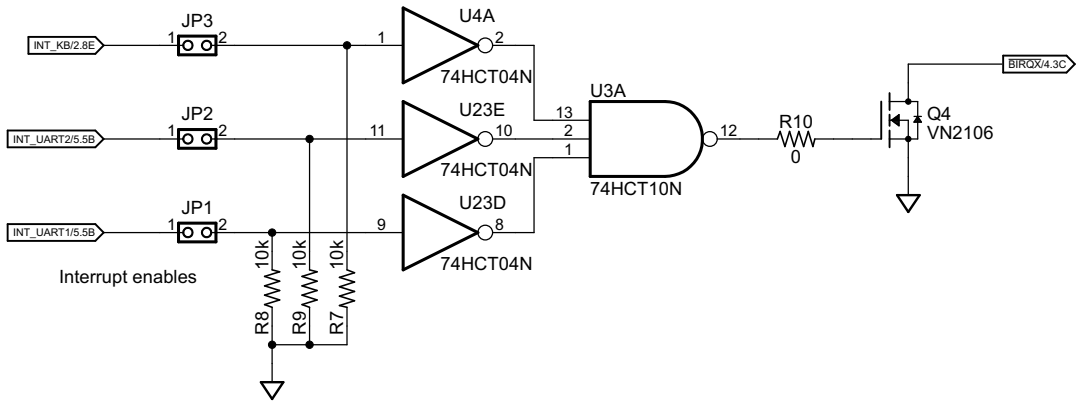
Title: PS/2 Transmit			XMICRO
Project: XMICRO-SERIAL			Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31		Sheet: 3/6

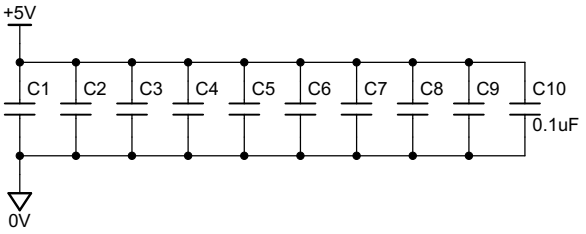


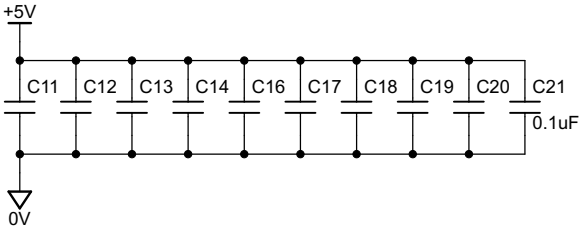
Title: Bus Interface		XMICRO
Project: XMICRO-SERIAL		Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31	Sheet: 4/6

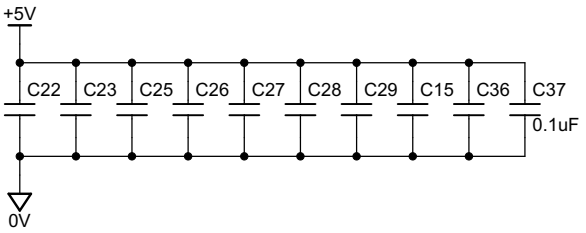


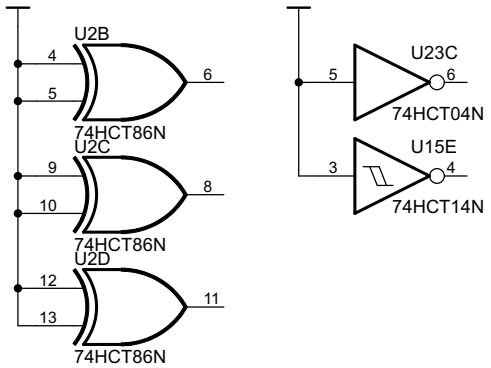
Title: Chip Selects/Registers		XMICRO
Project: XMICRO-SERIAL		Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31	Sheet: 5/6

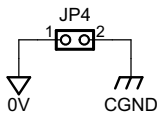


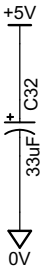












Title: Misc.		XMICRO
Project: XMICRO-SERIAL		Revision: 1.0
Drawn by: Chris Weir	2024-09-08 19:41:31	Sheet: 6/6