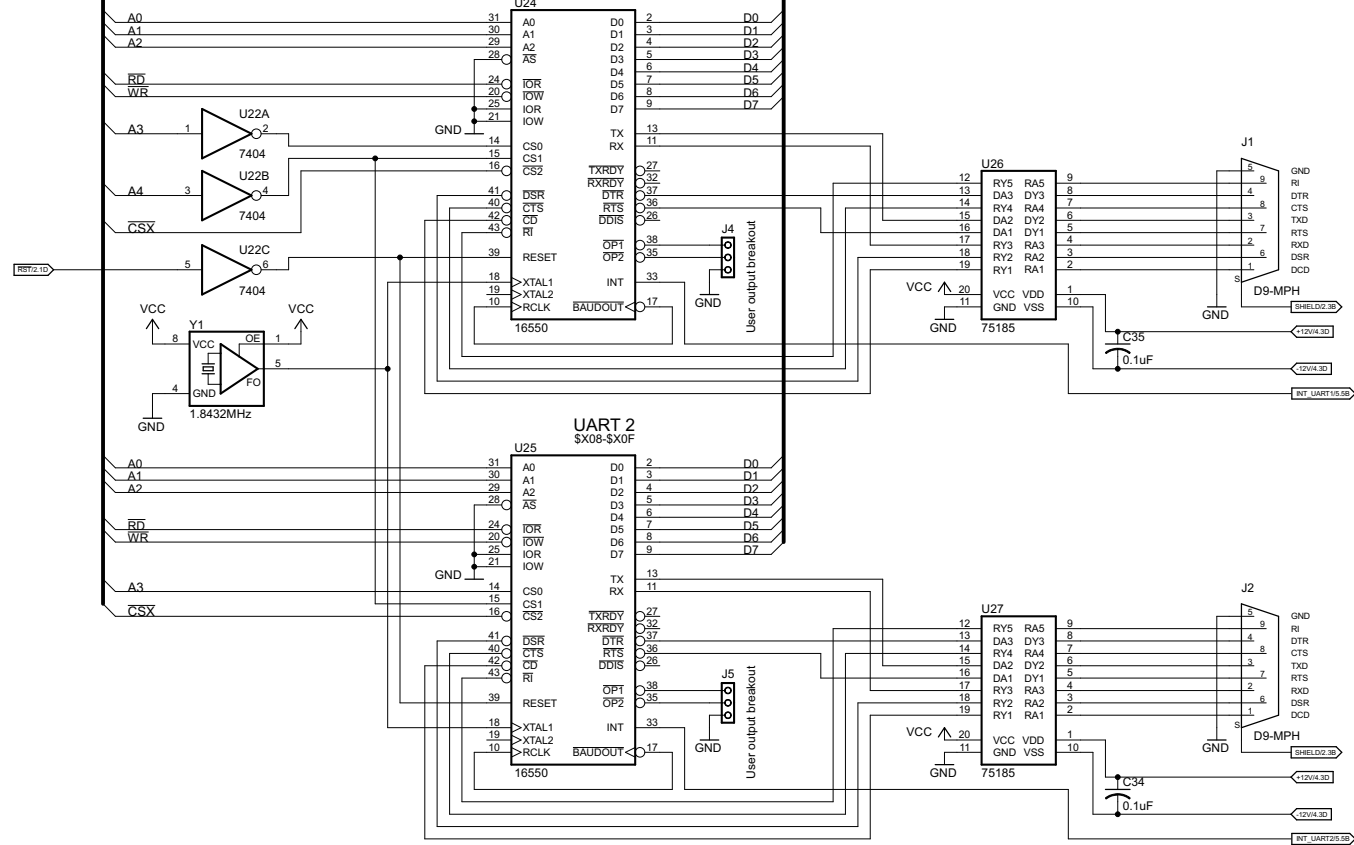


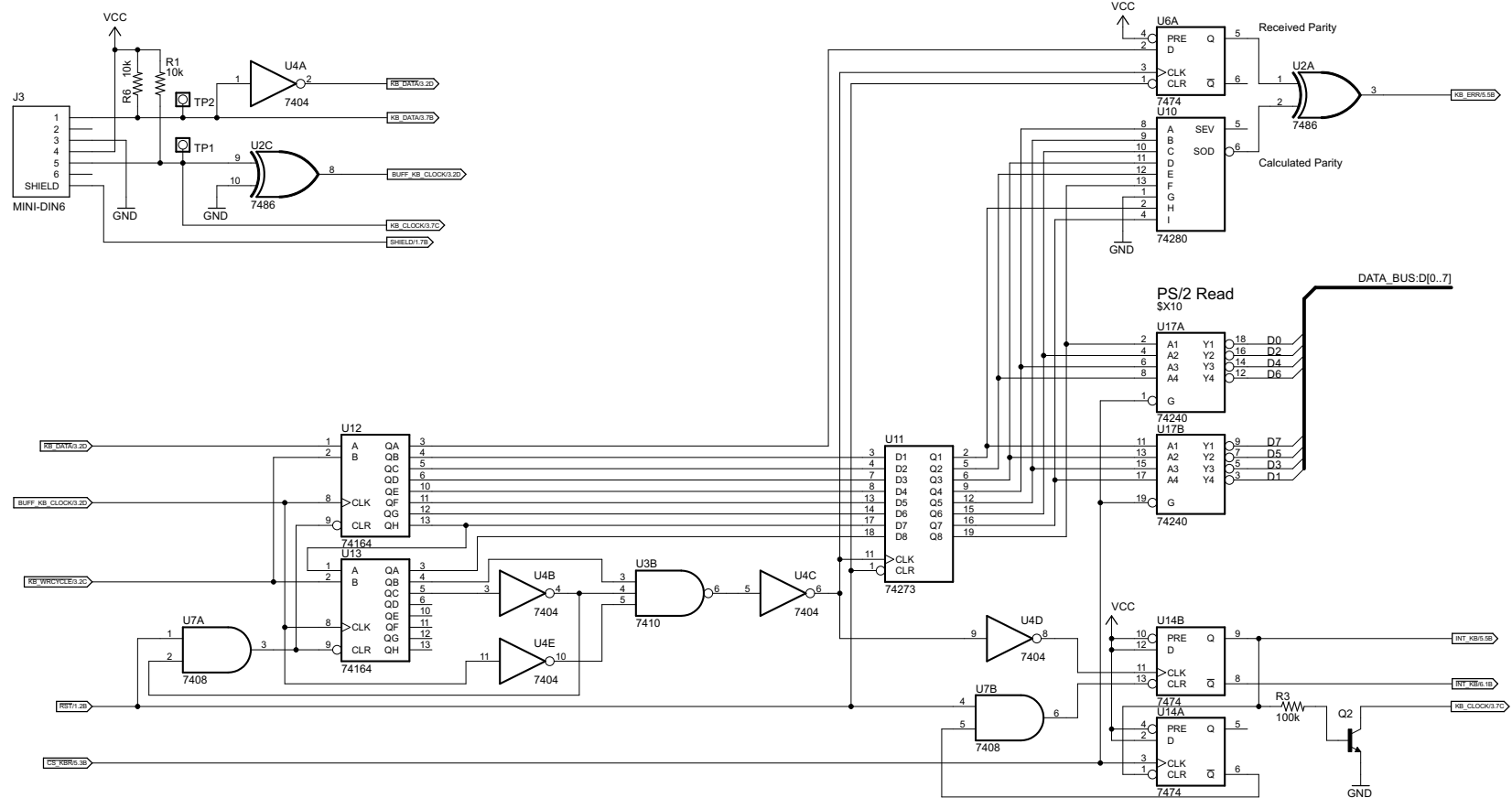
DATA_BUS:D[0..7]

ADDRESS_BUS:A[0..4]RD,WR,CSX

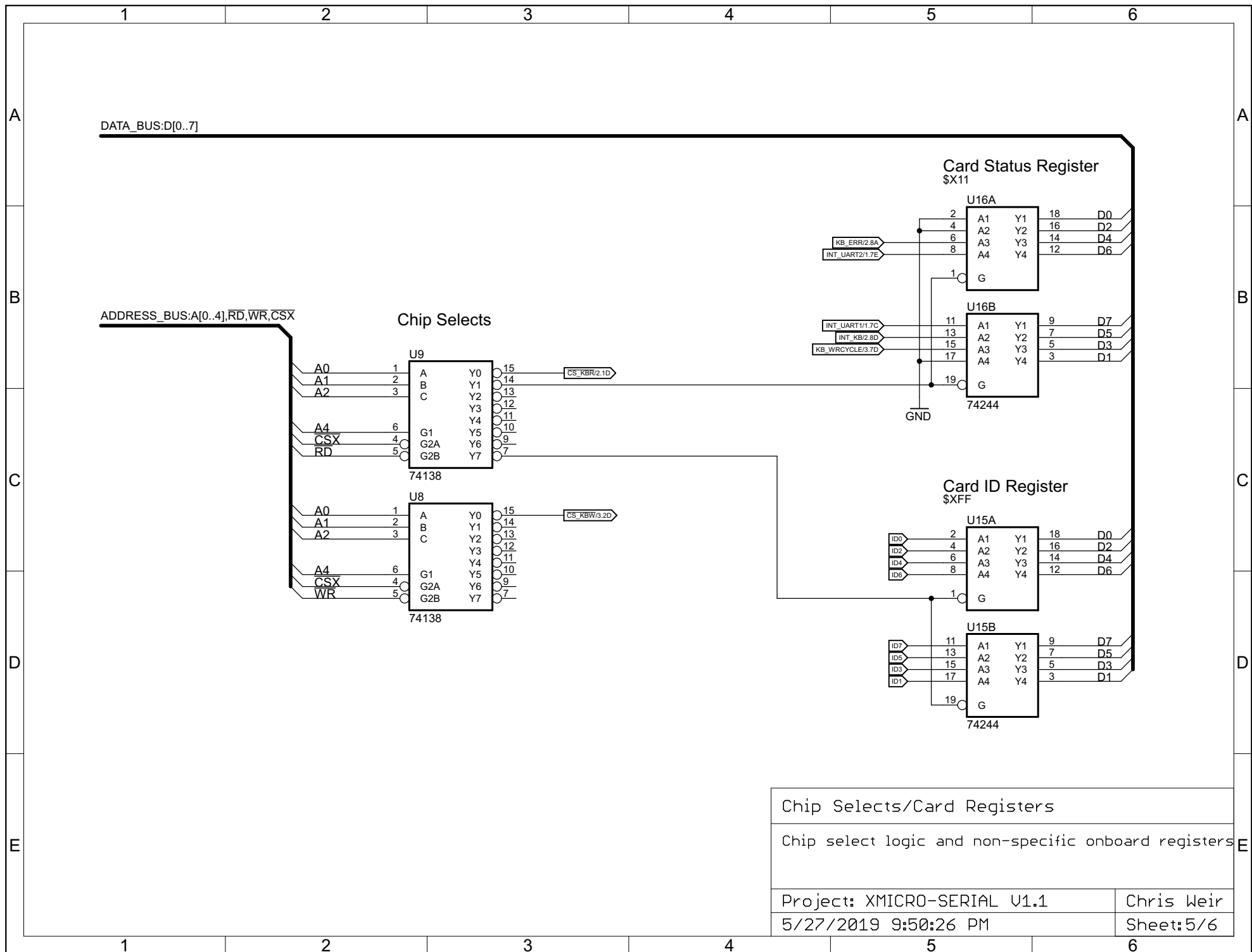


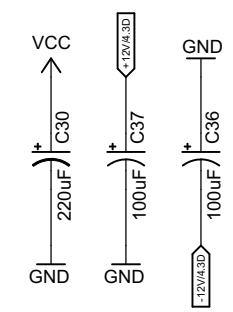
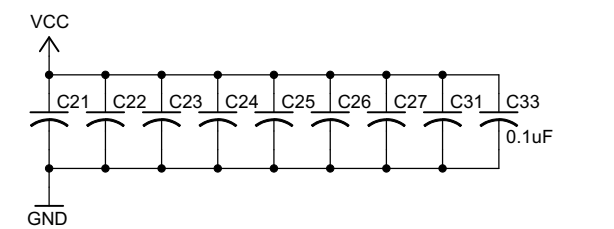
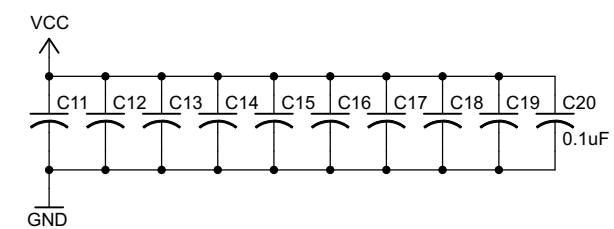
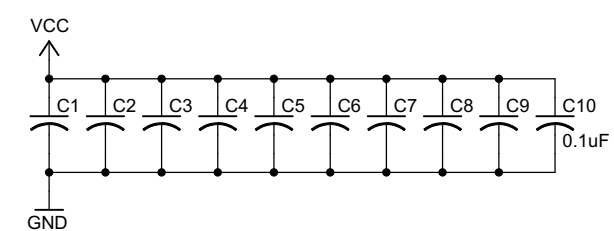
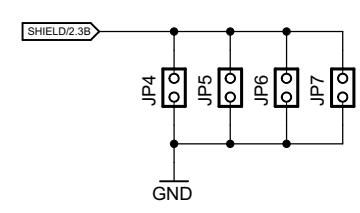
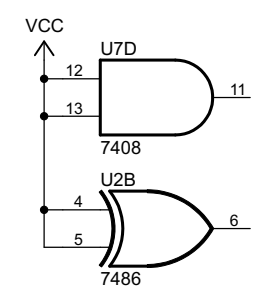
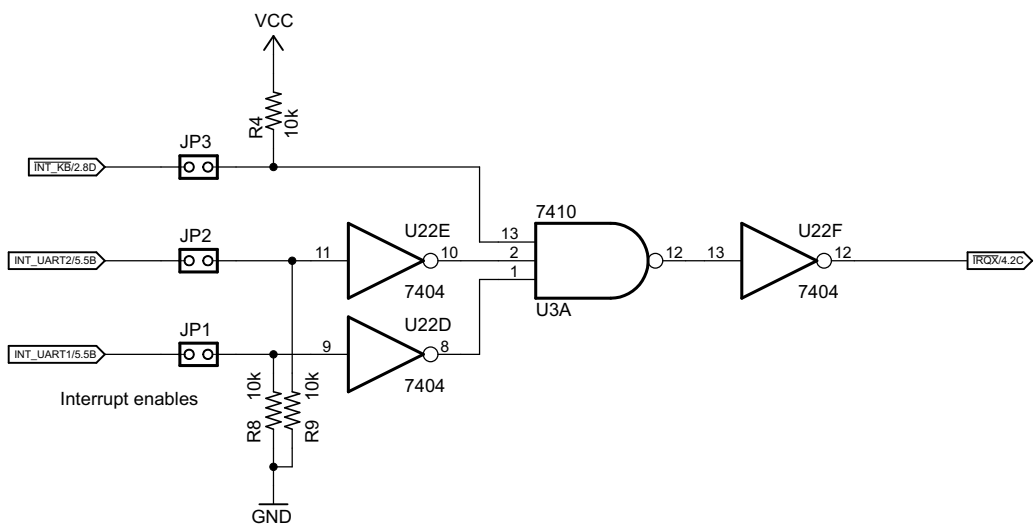
UARTs	
16C550 UARTs and RS-232 drivers	
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If a parity error is detected, software should wait for the keyboard to finish sending data before reading the data register. (approx. 1ms)
This inhibits the keyboard clock and allows the shift registers to resync with the next transmission, as they were reset when the interrupt was triggered.



PS/2 Read	
Receives data from PS/2 devices. An interrupt is generated when a byte is received and cleared when the data register is read by the CPU.	
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Misc.	
Interrupt combiner, bypass capacitors, extra gates, and shield jumpers.	
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