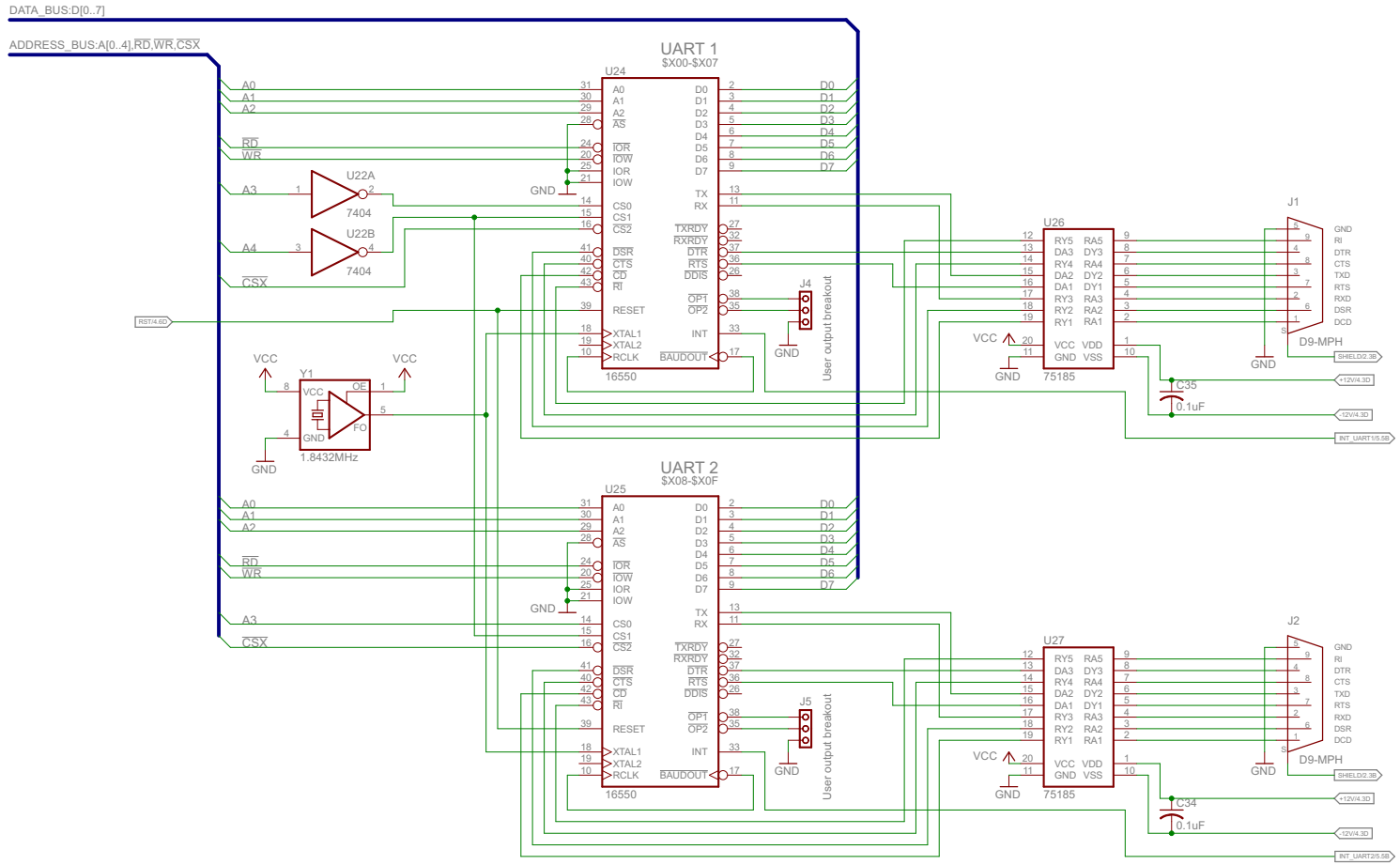

UARTs

16C550 UARTs and RS-232 drivers

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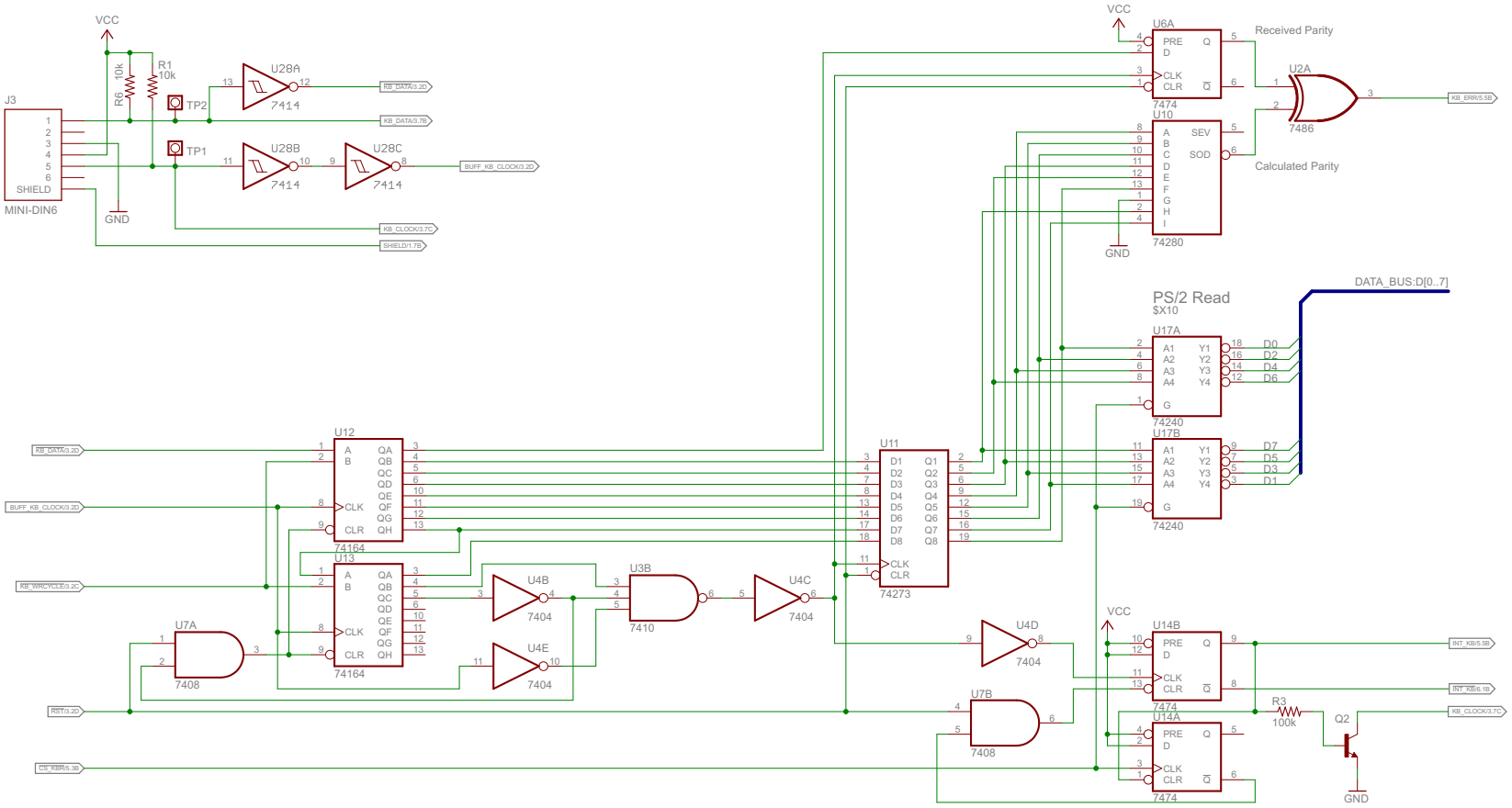
If a parity error is detected, software should wait for the keyboard to finish sending data before reading the data register. (approx. 1ms)
This inhibits the keyboard clock and allows the shift registers to resync with the next transmission, as they were reset when the interrupt was triggered.



PS/2 Read

Receives data from PS/2 devices. An interrupt is generated when a byte is received and cleared when the data register is read by the CPU.

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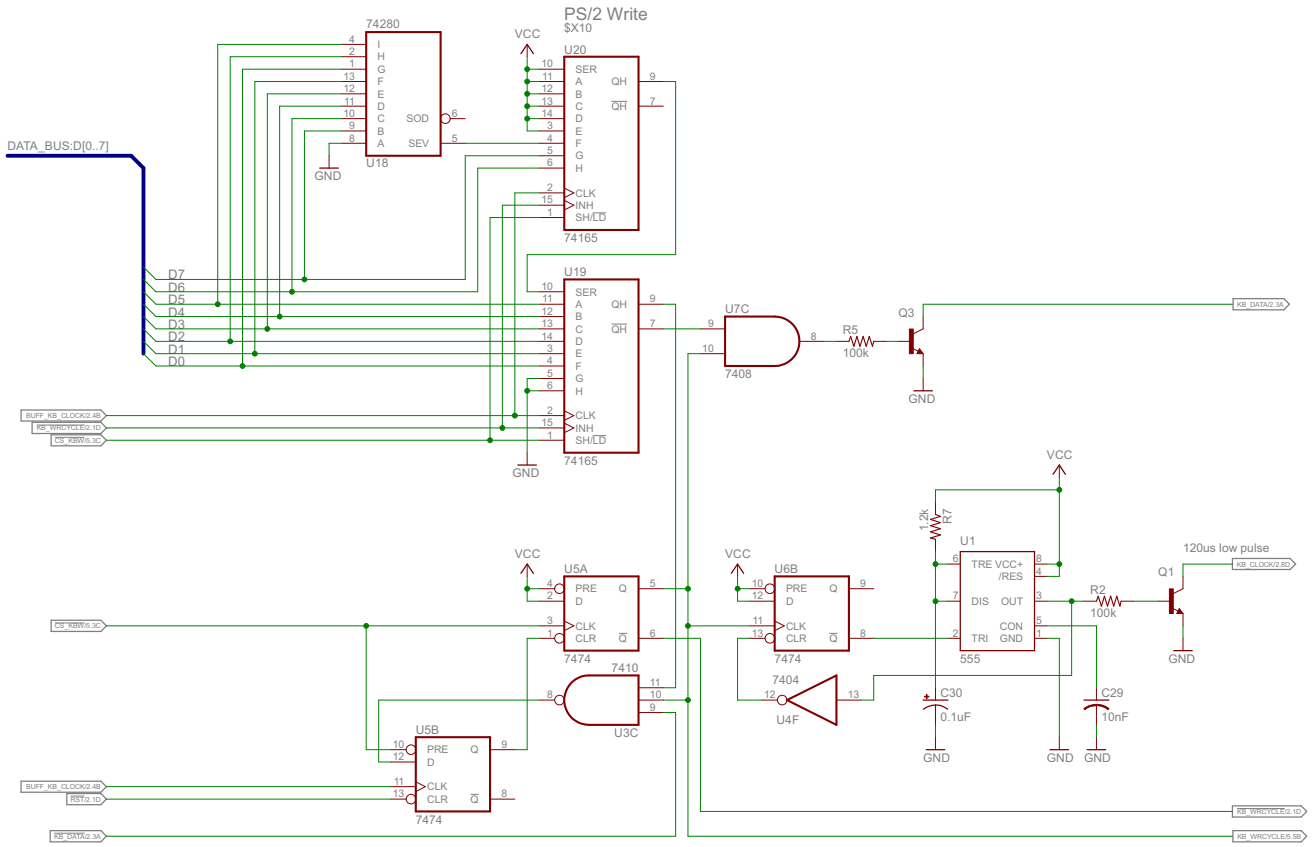

PS/2 Write

Sends data to PS/2 devices.

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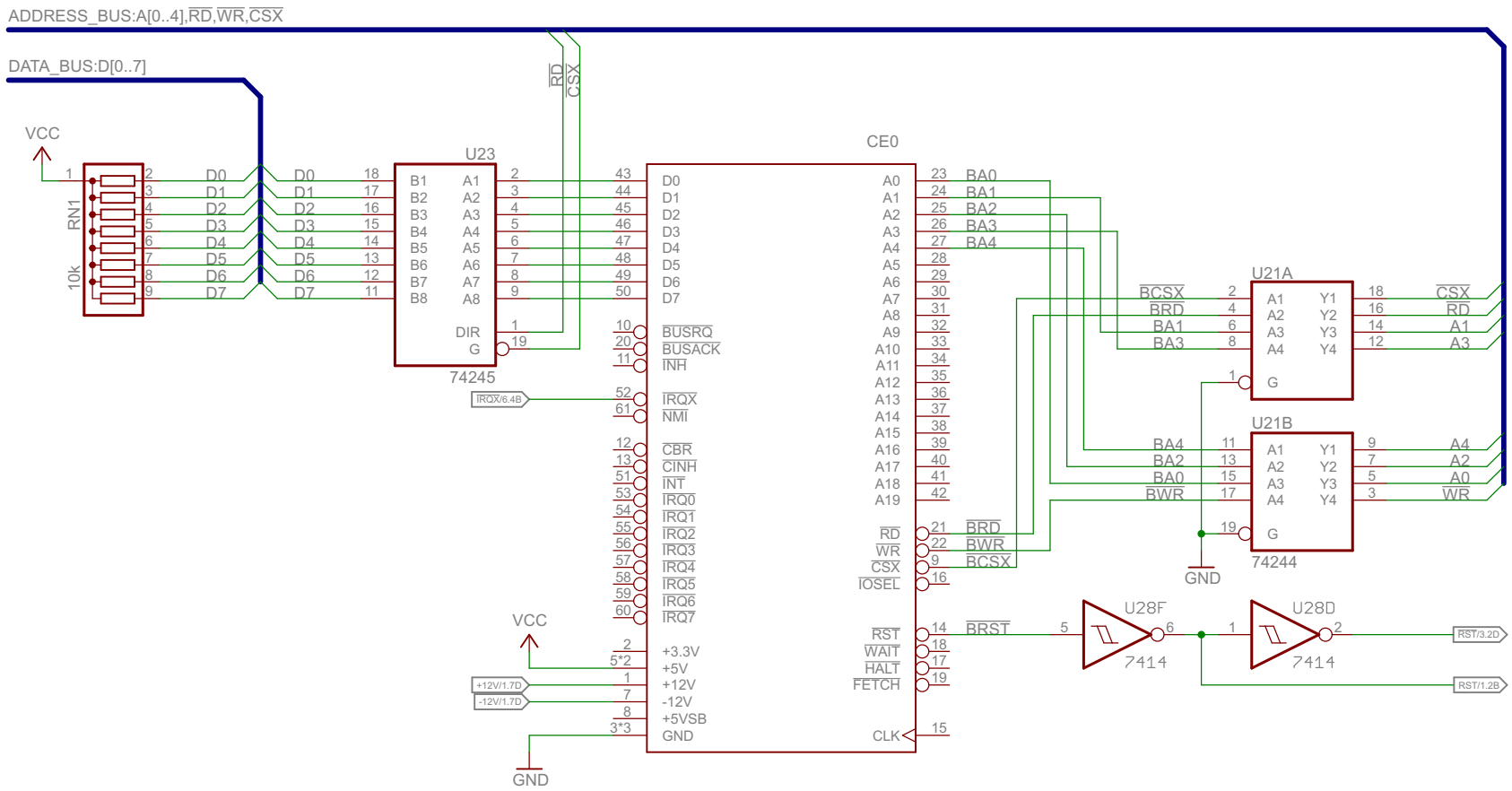

Bus Connector/Buffers

XMICRO bus interface. Buffers provide isolation and reduced loading on bus lines.

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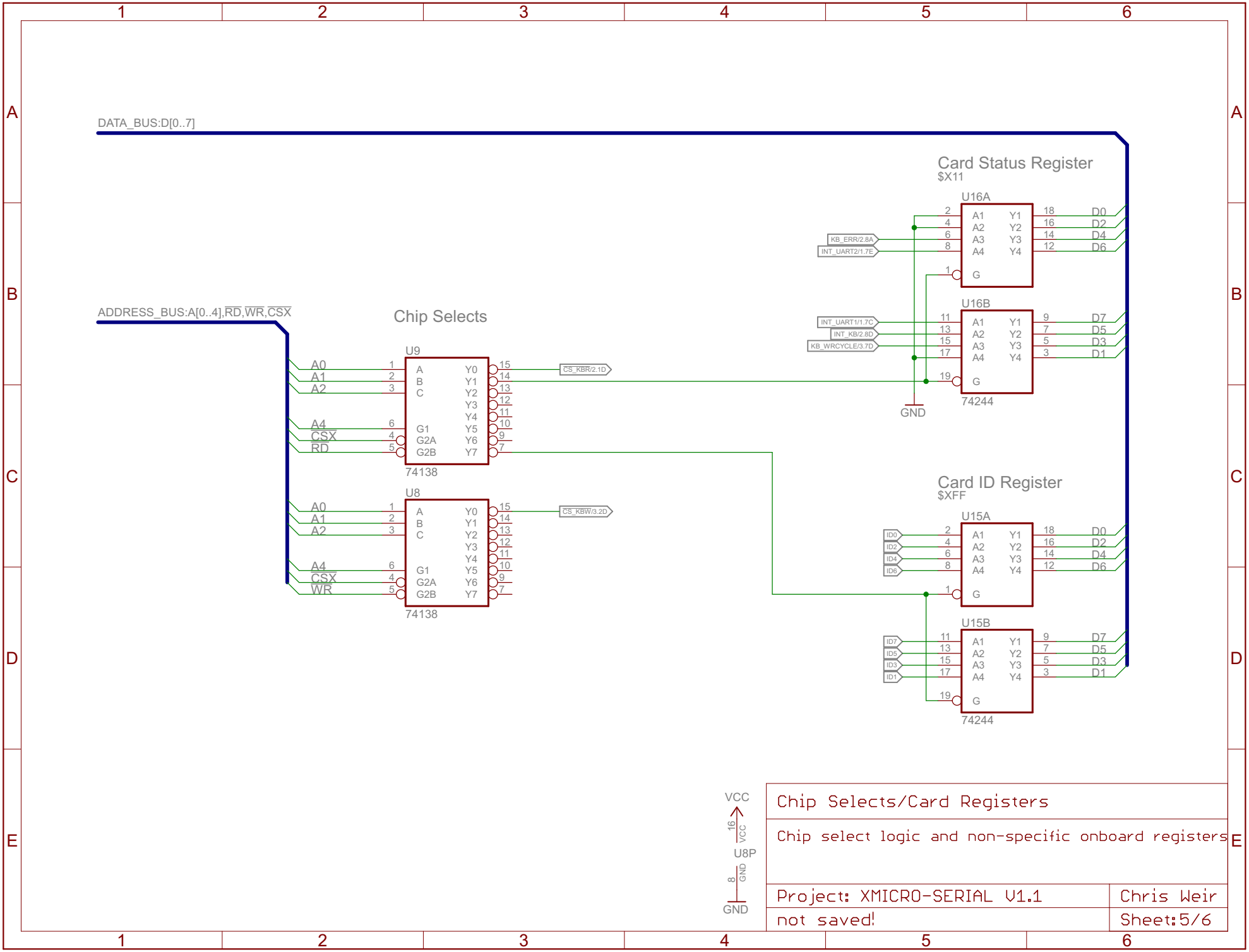
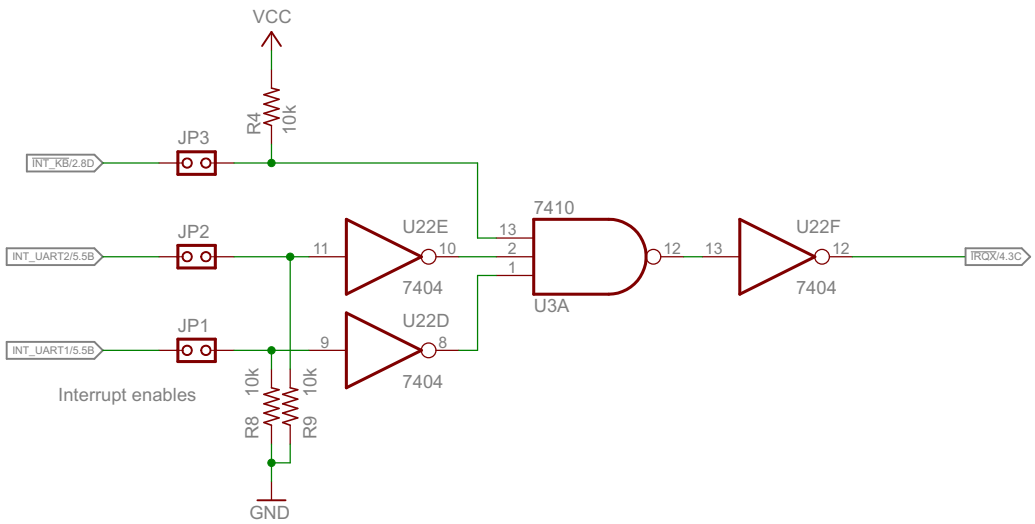
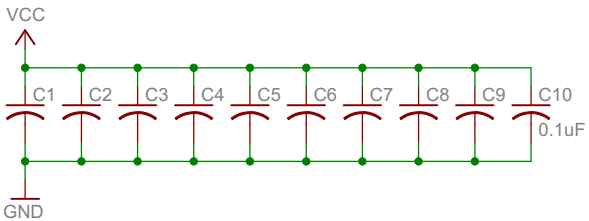
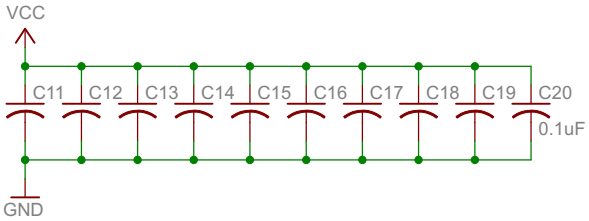
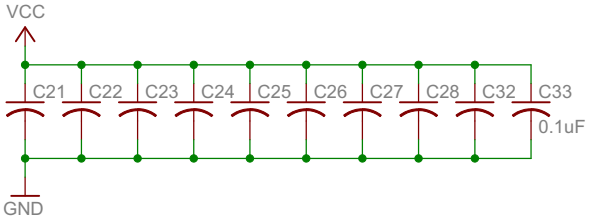
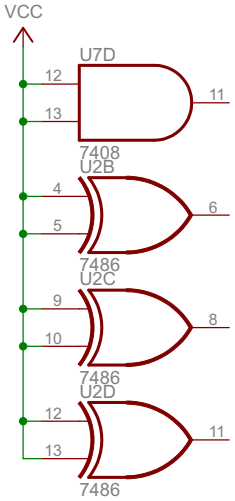

DATA_BUS:D[0..7]
ADDRESS_BUS:A[0..4],RD,WR,CSX
Chip Selects
U9
74138
U8
74138
A0
A1
A2
A4
CSX
RD
WR
CS_KBR/2.1D
CS_KBW/3.2D
Card Status Register
$X11
U16A
U16B
74244
KB_ERR/2.8A
INT_UART2/1.7E
INT_UART1/1.7C
INT_KB/2.8D
KB_WRCYCLE/3.7D
GND
Card ID Register
$XFF
U15A
U15B
74244
ID0
ID2
ID4
ID6
ID7
ID5
ID3
ID1
D0
D2
D4
D6
D7
D5
D3
D1
VCC
U8P
GND
Chip Selects/Card Registers
Chip select logic and non-specific onboard registers
Project: XMICRO-SERIAL V1.1
Chris Weir
not saved!
Sheet:5/6

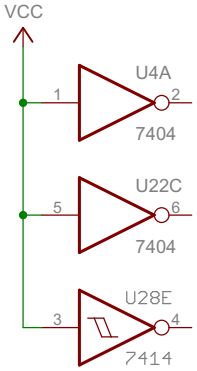


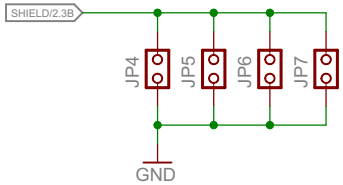


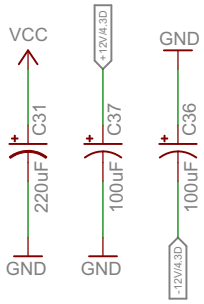












Misc.

Interrupt combiner, bypass capacitors, extra gates, and shield jumpers.

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