XMICRO-SERIAL

Technical Manual

V1.0 2019-03-23
Applies to hardware V1.1

Features:

- Two RS-232 serial ports with 16C550 UARTs
- 115.2 kilobaud maximum transfer speed
- Interrupt-driven PS/2 interface
- Card ID register for system self-configuration
- Fully open-source

Functional Description:

The XMICRO-SERIAL is an XMICRO slave card which provides two high speed RS-232 serial ports and a PS/2 interface for a keyboard or mouse. The 16C550 UARTs running the RS-232 ports provide a flexible and efficient interface for serial communications. The PS/2 interface uses no programmable or difficult to source ICs and provides full read/write functionality for PS/2 devices. The PS/2 interface also provides error detection, and a data-ready interrupt to minimize CPU overhead.

Tables of Information

Table 1 – Onboard Registers

Address	Function
$X00-$X07	16550 UART 1
$X08-$X0F	16550 UART 2
$X10	PS/2 Data Register (PDR)
$X11	Card Status Register (CSR)
$XFF	Card ID

Table 2 – Card Configuration

Setting	Function
JP1	Enable UART 1 Interrupt
JP2	Enable UART 2 Interrupt
JP3	Enable PS/2 Interrupt
JP4-7	Shield Ground

Table 4 – Card Status Register (CSR)

Address	D7	D6	D5	D4	D3	D2	D1	D0
$X11	UART 1 Interrupt	UART 2 Interrupt	PS/2 Interrupt	PS/2 Parity Error	PS/2 Write Cycle Active	0	0	0

UARTs

Two high performance 16C550 UARTs provide high-speed RS-232 communication through connectors J1 and J2. Table 1 lists the locations of their internal registers. The operation of these UARTs is beyond the scope of this document and may be found in the 16C550 datasheet. A header next to each UART breaks out the two additional user-defined outputs on each UART. These are otherwise not used on the card. Bits 7 and 6 of the CSR are set if there is an active interrupt from the UARTs.

75C185 driver/receiver ICs translate signals between TIA-232 compatible voltages and 5V TTL voltages. It is worth noting that these drivers are the main bottleneck that puts the maximum practical communication speed at 115200 baud. Faster drivers and a higher speed crystal could potentially be substituted to provide faster communication, typically at the cost of maximum cable length and driver voltage.

PS/2 Interface

When a data byte is received from a PS/2 device, the PS/2 interrupt is triggered. This is reflected in bit 5 of the CSR, which is set while there is an active interrupt, indicating that a new data byte is ready in the PDR. The PS/2 interrupt is cleared when the PDR is read, which also signals to the device that it may send another byte.

If a parity error is detected in the received data byte, bit 4 of the CSR will be set. In this case, software should wait approximately 1ms for the device to finish sending data before reading the data register. This inhibits the device clock for any remaining bytes and allows the shift registers to re-synchronize with the next transmission.

Data may also be written to the PDR. During a write cycle, bit 3 of the CSR is set. Data may only be written to the PS/2 data register when this bit is clear, indicating that the previous write is complete.

Connector Shield

The connector shields are isolated from the rest of the card to provide flexibility for different system configurations. Ideally this should be isolated and tied to the system chassis, which should then have a good connection to mains-earth. When no other shielding solution is in place, J4-J7 may be shorted to connect the shield net to the card’s ground plane.