XMICRO-VDP

Technical Manual

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Features:

- Yamaha V9958 Video Display Processor
- 192kB Video RAM
- Composite and S-Video Outputs
- Hardware configurable for NTSC or PAL operation
- Onboard wait-state generator for more transparent software interfacing
- VDP Interrupts
- Card ID register for system self-configuration
- Fully open-source

Functional Description:

The XMICRO-VDP is an XMICRO slave card which provides high resolution color video. Based on the Yamaha V9958 Video Display Processor (VDP), it has a rich feature set with text and graphics modes, sprites, and hardware video processing commands. The 192kB of onboard video RAM is accessed through the VDP and is independent of the main system RAM. A wait-state generator temporarily stops the system master when the VDP needs additional time for VRAM or register access, removing the need for time-sensitive wait loops in software. Programming the V9958 is beyond the scope of this document.

Tables of Information

Table 1 – Onboard Addresses

Address	Function	Description
$X00	VDP Port #0	VRAM Data (R/W)
$X01	VDP Port #1	Status Registers (R) VRAM Address (W) Register Setup (W)
$X02	VDP Port #2	Palette Registers (W)
$X03	VDP Port #3	Register Indirect Addressing (W)
$XFF	Card ID Register	

Table 2 – Card Configuration

Setting	Function
JP1	Enable wait on $\overline{CSX}$
JP2	Enable wait-states
JP3	Select IRQ or NMI interrupts

Table 3 – Card Connectors

Setting	Function
J1	Composite video output
J2	S-Video output
J3	RGB output breakout
J4	VDP color bus breakout
J5	Internal video signal breakout

Video Display Processor

The VDP interface is straightforward from a software perspective. Card addresses $X00-$X03 correspond to Ports #0-#3 on the VDP.

A wait-state is generated when the CPU accesses the card (Wait on $\overline{CSX}$). The length of these states is determined by the frequency of oscillator Y1 to ensure minimum access times to the VDP are met. The VDP can also be configured to generate its own wait-states for VRAM accesses by setting an internal register. When enabled, the VDP will make the CPU wait if the internal VRAM buffer is full and more time is required to access the current byte. See the V9958 datasheet for information on its wait function.

The VDP can be configured to generate interrupts. JP3 allows selecting between outputting a card-specific interrupt request ($\overline{IRQX}$) or a non-maskable interrupt ($\overline{NMI}$). Typically, $\overline{IRQX}$ should be selected. If VDP reads or writes occur in interrupt routines, care must be taken to ensure they can not conflict with in-progress read/write operations.

Analog Video

Analog video outputs are driven by a Sony CXA2075 video encoder. U18 takes the linear RGB signals from the VDP and encodes them into Composite and S-Video outputs capable of driving a 75Ω load such as a television. 75Ω-capable RGB outputs are also broken out on J3. NTSC and PAL operation are hardware-configured.

NTSC
- Populate R10 and R11, leave R12 and R13 open.
- Populate R15 with a 3.32k/1% resistor.

PAL
- Populate R12 and R13, leave R10 and R11 open.
- Populate R15 with a 2.61k/1% resistor.
- Oscillator Y1 must have a frequency of 4.43MHz to provide the PAL subcarrier.
- Note: PAL operation is currently untested.

Luma Trap
The luma trap reduces cross color on the composite video output. Typically U18's internal luma trap is used by populating R15, while leaving C30 and L1 open. Consult the CXA2075 datasheet for more details if a specialized luma trap is desired.

Programming Notes

- When using hardware wait-states, some jitter will always be present in read/write timing.
- Hardware wait-states do not account for the VDP's internal timing requirements. For example, when reading a status register, NOP instructions may be required between the register setup and the read operation. This is known to be critical for a stable reading of the S#0 status register.

Measured Interrupt Timing (NTSC TEXT1 Mode)

From Horizontal IRQ Assertion to:	
End of previous line (H.Blank)	6.9µS
Visible screen area (border)	17.2µS
Pattern area (characters)	21.5µS
From Vertical IRQ Assertion to:	
End of current field (border)	1,584µS
Next field (border)	2,804µS
Next field (characters)	4,460µS