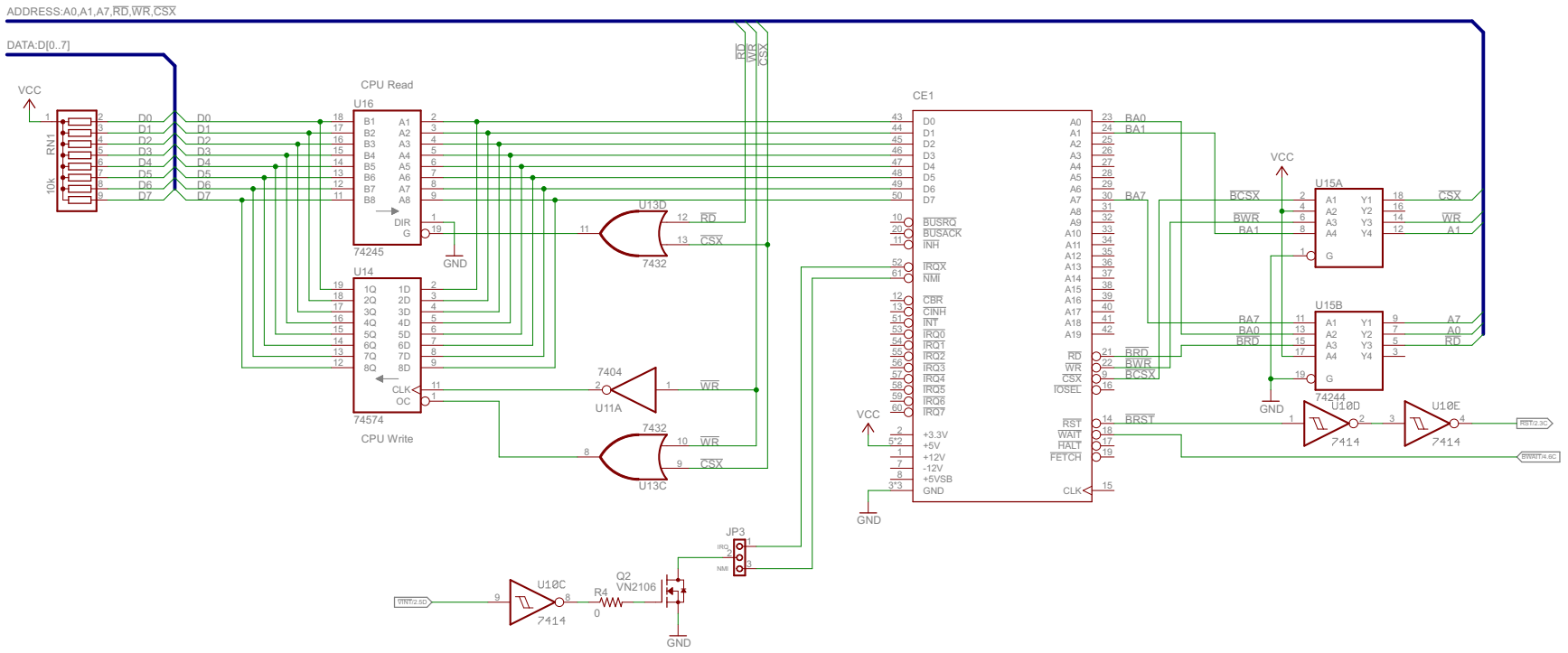
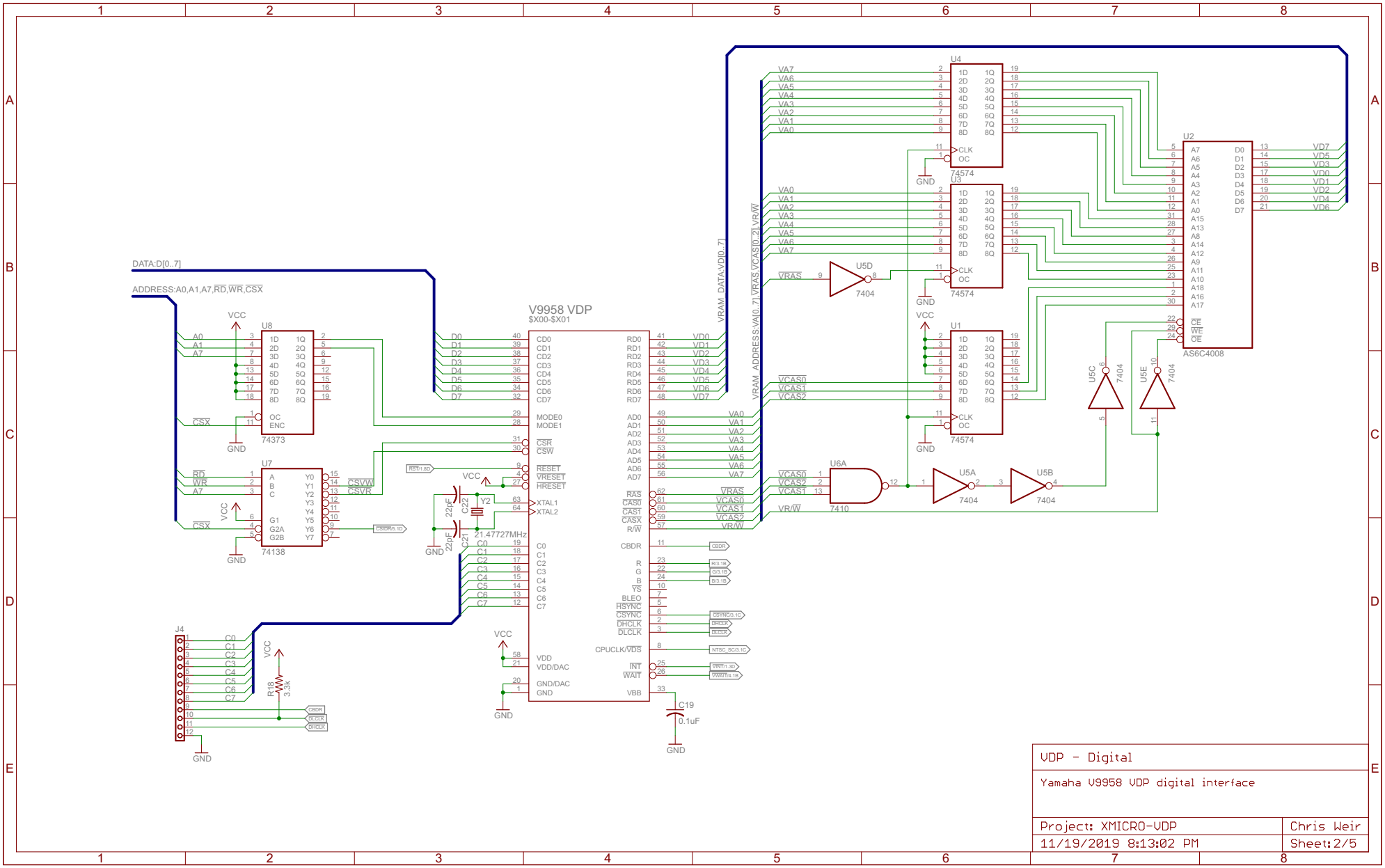
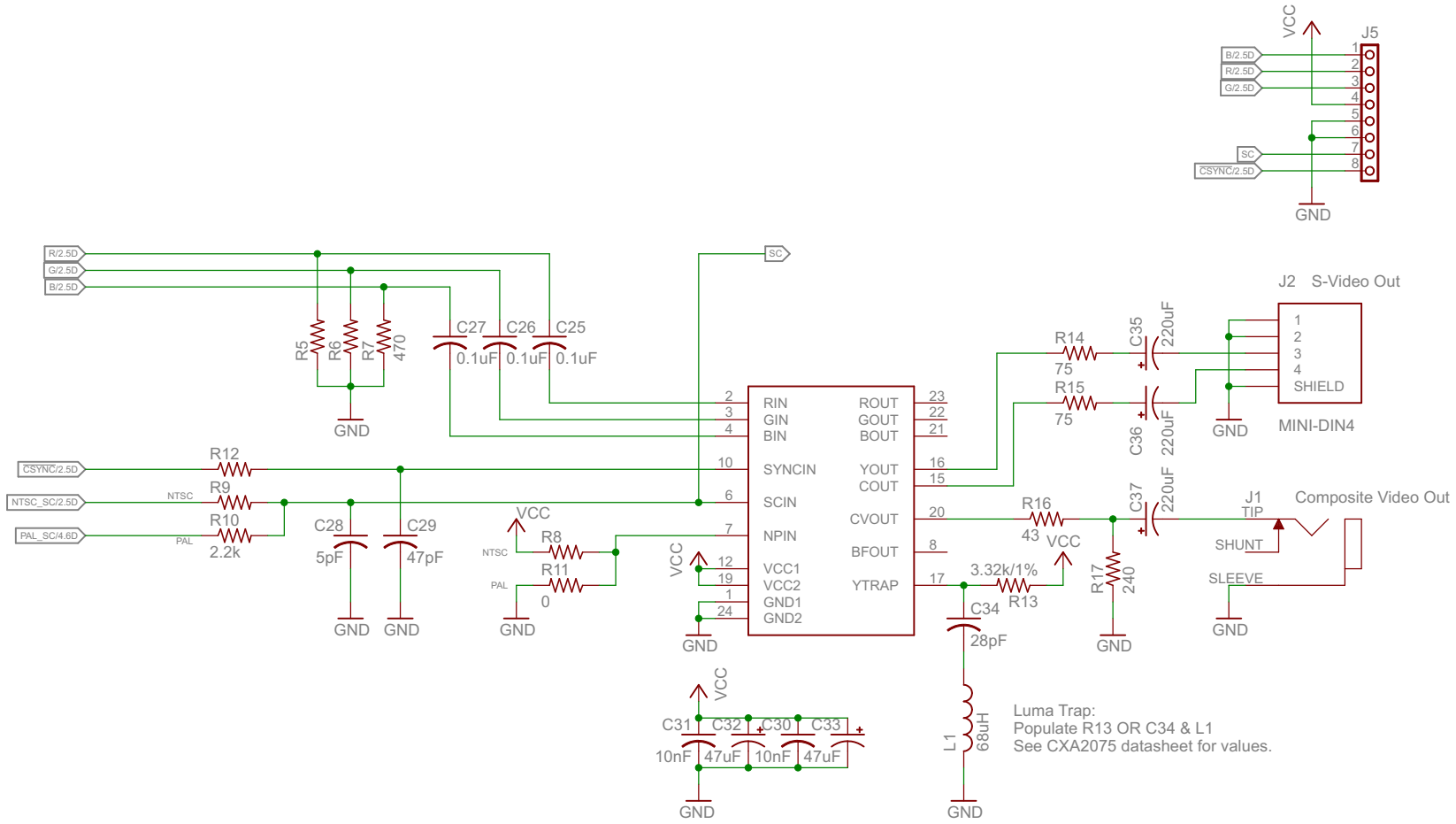
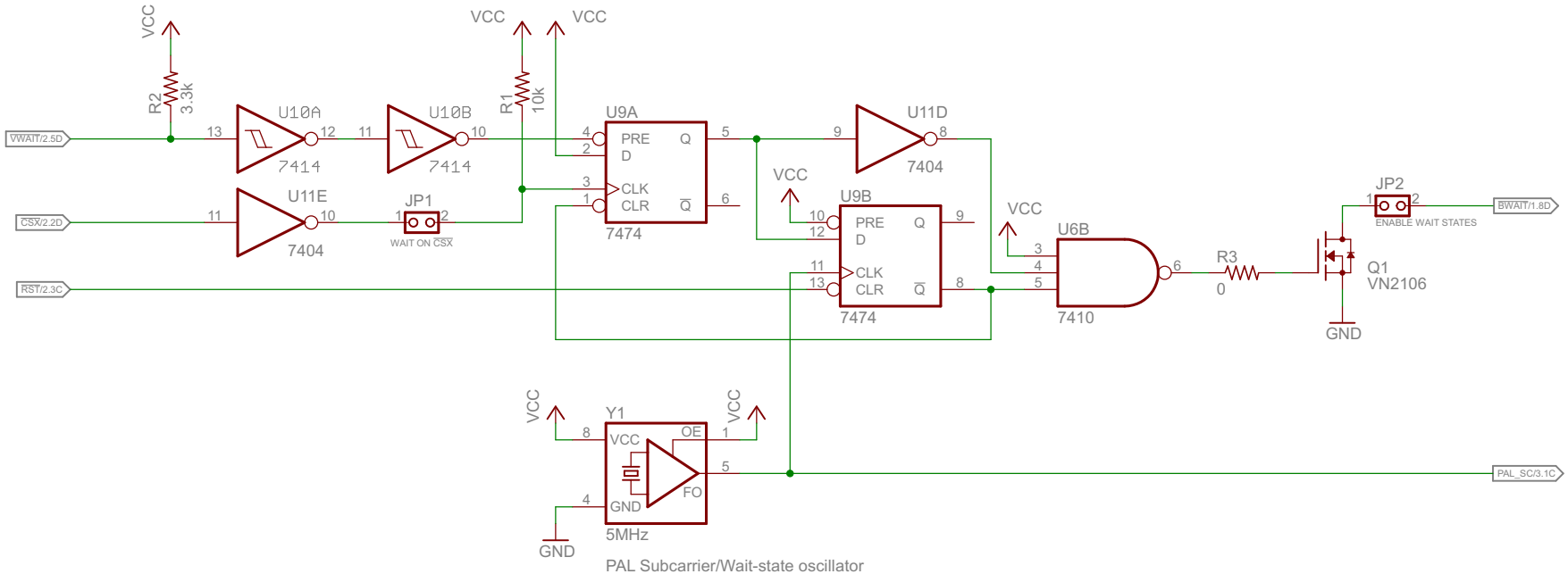



| | |
|---|---|
| Bus Connector/Buffers | |
| XMICRO bus interface. Buffers provide isolation and reduced loading on bus lines. | |
| Project: XMICRO-VDP | Chris Weir |
| 11/19/2019 8:13:02 PM | Sheet:1/5 |


DATA:D[0..7]
ADDRESS:A0,A1,A7,RD,WR,CSX
V9958 VDP
$X00-$X01
VRAM DATA:VD[0..7]
VRAM ADDRESS:VA[0..7],VRAS,VCAS[0..2],VR/W
74373
74138
74574
74574
74574
7404
7404
7404
7410
AS6C4008
21.47727MHz
0.1uF
3.3K
VDP - Digital
Yamaha V9958 VDP digital interface
Project: XMICRO-VDP
Chris Weir
11/19/2019 8:13:02 PM
Sheet:2/5




| Analog Video | |
|---|---|
| Analog video processing. Encodes VDP video signals into Composite and S-Video usable by TV sets.<br>Note: PAL operation is untested. | |
| Project: XMICRO-VDP | Chris Weir |
| 11/19/2019 8:13:02 PM | Sheet:3/5 |



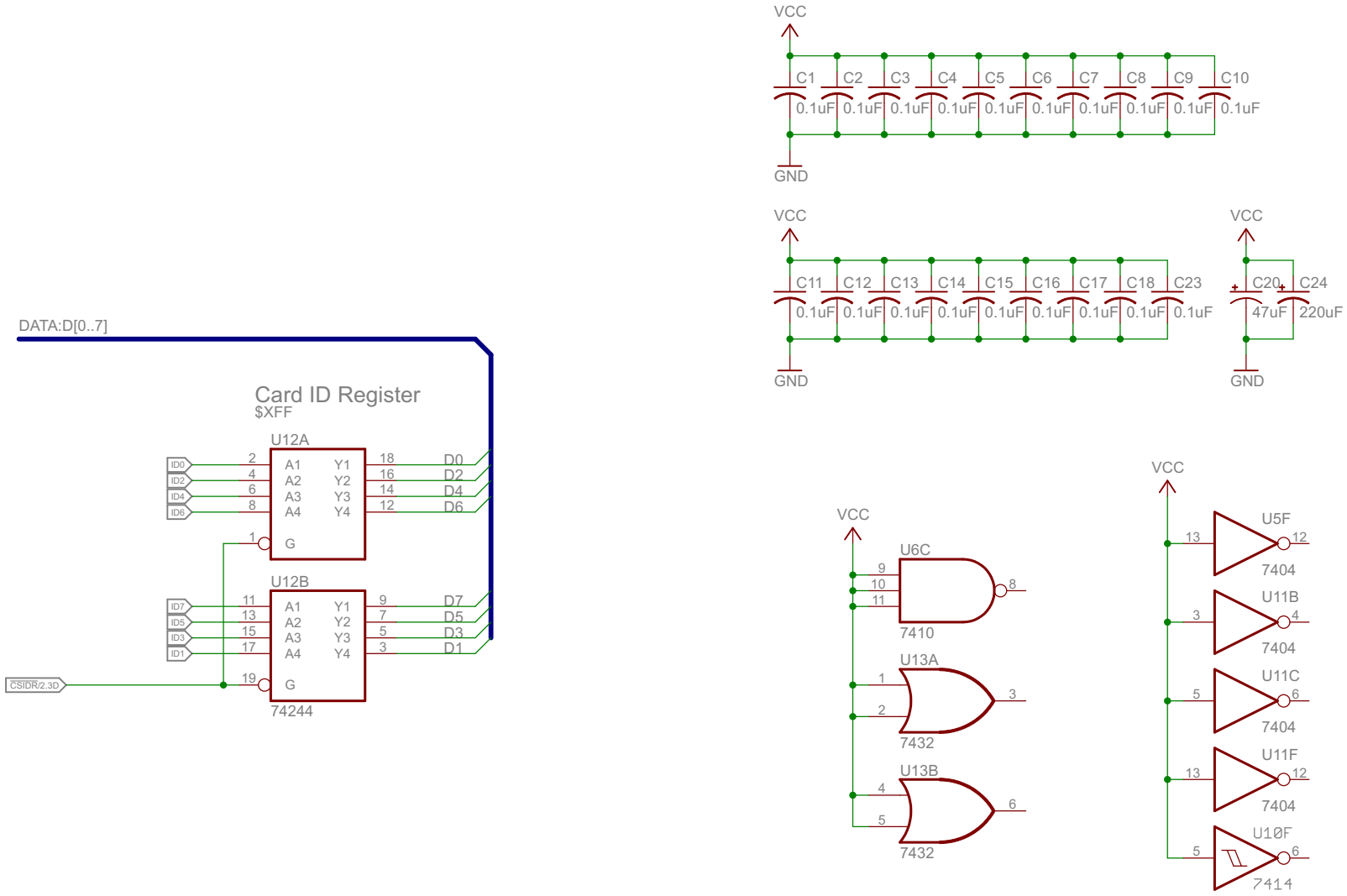

PAL Subcarrier/Wait-state oscillator
Higher frequency shortens wait states.
May be substituted with any frequency up to 5.5MHz on NTSC cards.
PAL cards require 4.43361875MHz

Wait State Generator Operation:
1. Assert $\overline{\text{WAIT}}$ on falling edge of chip select.
2. Hold it for at least one clock cycle.
3. Continue to assert $\overline{\text{WAIT}}$ as long as the VDP is asserting $\overline{\text{VWAIT}}$.
4. Deassert $\overline{\text{WAIT}}$ at least 1/2 cycle after $\overline{\text{VWAIT}}$ goes high.

## Wait-State Generator

Pauses the CPU until the VDP is ready to complete a read or write cycle.

| | |
|---|---|
| Project: XMICRO-VDP | Chris Weir |
| 11/19/2019 8:13:02 PM | Sheet: 4/5 |




| | |
|---|---|
| Misc. | |
| Card ID register, general bypass capacitors, and unused gates. | |
| Project: XMICRO-VDP | Chris Weir |
| 11/19/2019 8:13:02 PM | Sheet:5/5 |