Brac University
Department of Electrical and Electronic Engineering
EEE 412/ ECE 412
VLSI Design Laboratory, Summer 2021

Project:

Design a 4-bit ALU capable of performing 8 different arithmetic and logical operations using Verilog HDL and verify using timing diagram.

Specifications:

The ALU runs on 12-bit operation code. 4 least significant bits (OP0-OP3) signify register A, next 4 bits (OP7-OP4) signify register B and the most significant 4 bits (OP11-OP8) signify the operation to be performed. The output is of 4 bits. The output also contains carry, zero and sign flags. Carry is activated when the result of addition overflows. Sign is activated when Register B is greater than register A. Zero is activated when the result of an operation is zero.

Register A: 4-bit input 1

Register B: 4-bit input 2

ADD operation: Performs OUT=A+B (Carry if turned on if answer contains more than 4 bits)

MUL operation: Multiplies least significant 2 bits of A with least significant 2 bits of B

SUB operation: Performs OUT=A-B (Sign if turned on if answer is negative)

AND operation: Performs bitwise OUT=A&B

NAND operation: Performs bitwise OUT=A~&B

NOR operation: Performs bitwise OUT=A~|B

OR operation: Performs bitwise OUT=A|B

XNOR operation: Performs bitwise OUT=A~^B

XOR operation: Performs bitwise OUT=A^B

NOT operation: Performs OUT=~A

Example:

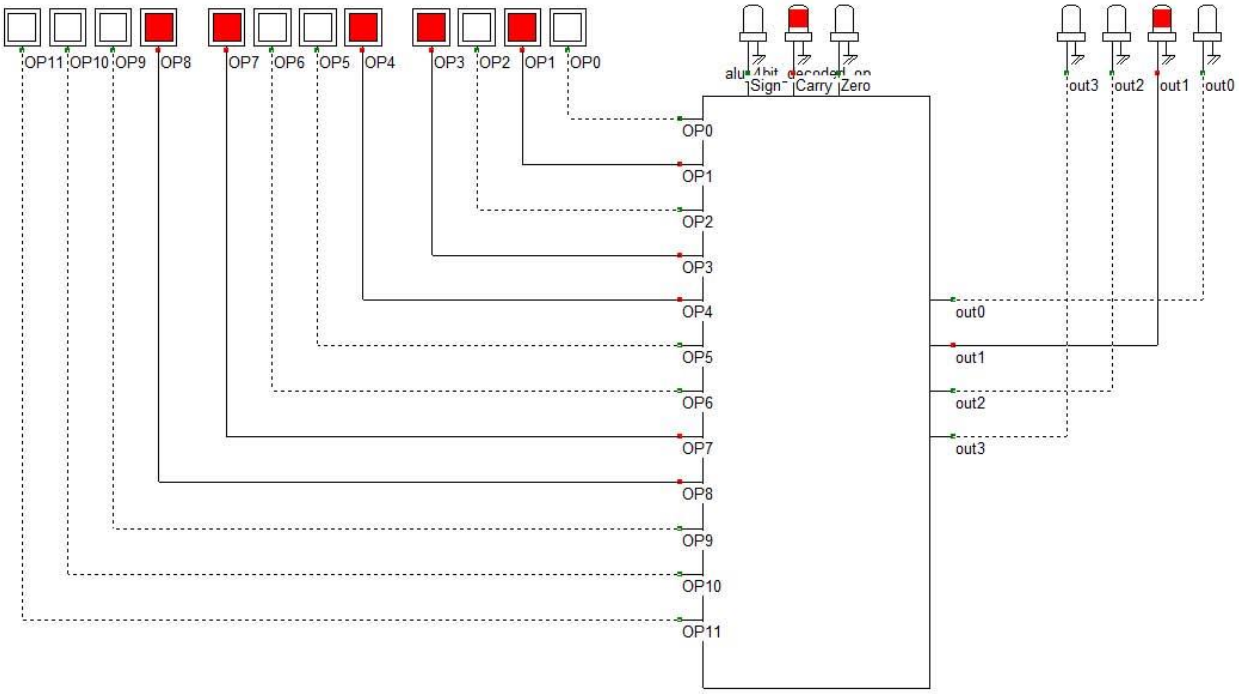
Let us take the sample OP CODE: xxxx 1001 1010

Let us suppose, following are the mapping of opcode, sample operation and output:

Code (xxxx)	Operation	OUT	Carry	Sign	Zero
0000	ADD	0011	1	-	0
0001	MUL	0010	-	-	0

0010	SUB	0001	-	0	0
0011	AND	1000	-	-	0
0100	NAND	0111	-	-	0
0101	NOR	0100	-	-	0
0110	OR	1011	-	-	0
0111	XNOR	1100	-	-	0
1000	XOR	0011	-	-	0
1001	NOT	0101	-	-	0

Following is a conceptual block diagram for you to understand the input and outputs of the ALU



Group 1:

Code (xxxx)	**Operation**
1010	NAND
1000	ADD
1110	OR
0100	SUB
0111	XOR
0001	NOT
1001	MUL
1101	NOR

For any other code, turn all the output pins to 0.

Group 2:

Code (xxxx)	Operation
1101	ADD
1001	AND
0101	MUL
0001	NOT
1100	NAND
0010	SUB
0011	XNOR
0110	NOR

For any other code, turn all the output pins to 0.

Group 3:

Code (xxxx)	Operation
1100	XOR
0100	NOT
1101	SUB
0110	NAND
1010	NOR
0111	ADD
0001	MUL
1110	XNOR

For any other code, turn all the output pins to 0.

Deadline: 2nd September 2021, 11:59 pm
Presentation: 5th September 2021 during class time.

Deliverables:

1. Detailed Project Report
2. Power Point Presentation

Project Report:

Report must contain the following:

1. Cover Page
2. Objective (You should write Problem Statement here)
3. Introduction (You should define the basic terminologies related to ALU here that is relevant to your design like OPCODE etc.)
4. Software Requirements
5. Working Procedure (How you went through with the design)
6. Verilog Code
7. Timing Diagram
8. Result and Observation (Here you explain your code and timing diagram. The timing diagram should contain all the eight OPCODE combinations of your group)

9. Discussion (Any issues with your design or what you've learnt doing the project)

Grading Criteria:

1. Completion of all Specifications
2. Efficiency of Code
3. Quality of Report
4. Quality of Presentation
5. Peer Evaluation (How your own groupmates rate your contribution) (out of 10)
6. Viva