

Department of Electrical and Electronic Engineering

Open Ended Lab Report

Semester: Fall 2020

Course Code: EEE208

Lab Section: 02

Name of the experiment: Frequency Response of Transistor Amplifier

Circuit

Group No: 11

Group Members:

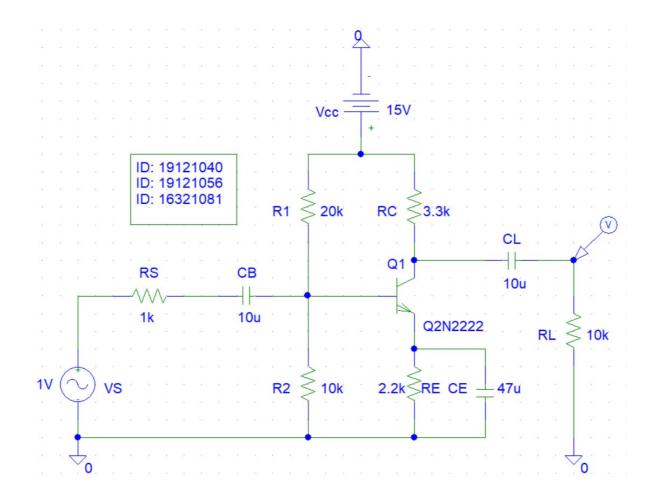
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Date of submission: 26th December, 2020

Objective:

Study of the frequency response of a transistor amplifier circuit

Single Stage BJT Amplifier Circuit



Gain vs Frequency graph:

Initially all the values are fixed. The peak of the graph is found to be 40.8 dB. The cutoff frequency would be 3 dB below the peak. Using that, the following data was obtained:

Lower Cutoff Frequency = 180 Hz

Upper Cutoff Frequency = 320 kHz

Bandwidth = 320 kHz

The unity gain is found at the 0 dB position.

Lower Frequency at unity gain = 2.11 Hz

Upper Frequency at unity gain = 34.66 MHz

Normal Circuit

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Date/Time run: 12/26/20 17:43:09 Temperature: 27.0 (A) Schematic2 (active) 60 (7.4989k, 40.846) (320.392K, 37.852) (180.170, 37.858)40 20 0 (34.656M, 44.255m) (2.1080, +34.600m)-20 100KHz 1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 10MHz 100MHz □ 20*LOG10(V(RL:2) / V(VS:+)) Frequency

Changing the value of RE:

The value of RE was varied from 1 k Ω to 100 k Ω . The following data was obtained:

RE (kΩ)	FL (Hz)	FH (MHz)	BW (MHz)	Gain (dB)
1	14.6	0.585	0.585	-13.0
5	97.4	0.649	0.649	35.5
10	53.4	1.10	1.10	30.3
50	12.2	2.74	2.74	17.1
100	6.75	3.42	3.42	11.2

From the data, we can see that when RE is set to 1 k Ω , the gain was negative, meaning there was no amplification. However, beyond 5 k Ω , the gain is positive. Increasing the RE beyond 5 k Ω would significantly decrease the gain, meaning a lower value is more preferable.

Changing RE

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Temperature: 27.0 Date/Time run: 12/26/20 14:49:31 (A) Schematic2 (active) 50 (5.1989K, \$5.527) (97.417,32.533) (649.382k,32.549) (5.1989K,30.301) (53.367, 27.297)(1.0959M, 27.303)(5.3367K, 17.071)(2.7384M,1<u>4.043)</u> (12.168/14.072)(5,407.0K,11.176) 6.7538,8.1545) (3.42Q5M, 8.1689) (5.0646K, -13.014)(584.851K, -16.016) (14.614, -16.034)**-**50 -1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 10MHz 100MHz $\square \diamond \nabla \triangle \circ 20*LOG10(V(RL:2)/V(VS:+))$ Frequency

Changing the value of CE:

The value of CE was varied from 10 μF to 100 μF . The following data was obtained:

CE (µF)	FL (Hz)	FH (kHz)	BW (MHz)	Gain (dB)
10	833			
15	555			40.0
25	333	320	320	40.8
50	169			
100	86.6			

From the data, we can see that changing CE has negligible impact on the upper cutoff frequency and gain. However, the lower cutoff frequency decreased slightly, meaning higher values of CE has slightly higher bandwidth.

Changing CE

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Date/Time run: 12/26/20 15:36:10 Temperature: 27.0 (A) Schematic2 (active) 60 (15.808K, 40.845) (320.392K, 37.860) 40 (832.635, 37.865) (555.032, 37.834)20 (333.217,37.831) (168.761,37.836)(86.596, 37.850) -20 1.0MHz 1.0KHz 10Hz 100Hz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20 * LOG10 (V(RL:2) / V(VS:+))$ Frequency

Changing the value of RL:

The value of RL was varied from 1 k Ω to 100 k Ω . The following data was obtained:

RL (kΩ)	FL (Hz)	FH (kHz)	BW (kHz)	Gain (dB)
1	190	832.6	832.4	31.0
5	185	384.8	384.6	39.0
10	180	320.4	320.2	40.8
50	176	266.8	266.6	42.6
100	176	266.8	266.6	42.9

From the data, the higher the load, the lower the bandwidth. However, the gain is significantly lower at low load. This is not preferrable as the gain should not change with load.

Changing RL

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Date/Time run: 12/26/20 15:43:06 Temperature: 27.0 (A) Schematic2 (active) 50 (266.770K,39.749) (266.770K, 39.618) (320.392к, 37.852 (384.793K,36.05 (175.517, 39.866) (10.132K,31.007) (832.6β5K**,**28.|Φ (175.517, 39.603) (10, 132K, 39.021)(180.170,37.858) (184.946, 36.096) (10\.132K,40.845) (189.849, 28.056) (10.132K, 42.642) (10.132K, 42.895) **-**50 -1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20*LOG10(V(RL:2)/V(VS:+))$ Frequency

Changing the value of RS:

The value of RS was varied from 1 k Ω to 100 k Ω . The following data was obtained:

RS (kΩ)	FL (Hz)	FH (kHz)	BW (kHz)	Gain (dB)
1	180	320.4	320.2	40.8
5	111	160.2	160.1	33.1
10	92.5	138.7	138.6	28.3
50	70.2	123.3	123.2	15.4
100	67.5	121.7	121.6	9.57

From the data, a higher value of RS significantly drops the gain. The bandwidth has also dropped significantly. Therefore, a lower value of RS is highly preferred.

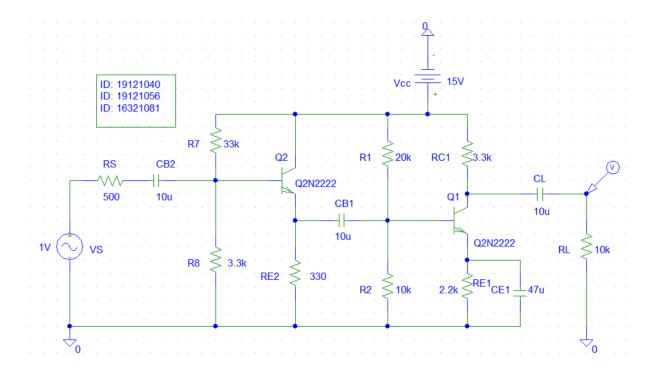
Changing RS

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic2.sch

Date/Time run: 12/26/20 16:00:50 Temperature: 27.0 (A) Schematic2 (active) 50 (7.0241K, 40.845) (18).170,37.858)(320.392K, 37.852) (7.0241K, 33.103) (11/1.034,30.090) (160.157K, 30.069) (7.0241K, 28.303) (138.690K, 25.295) (92.451,25.353) (7.0241k, 15.441)(70.241, 12.410)(123.285K, 12.412) (67.538, 6.5544) (121.682K, 6.5058) (7.0241 k, 9.570)**-**50 -1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20 * LOG10 (V(RL:2) / V(VS:+))$ Frequency

Dual Stage BJT Amplifier Circuit

A common collector amplifier is added before the previous amplifier.



Gain vs Frequency graph:

Initially all the values are fixed. The peak of the graph is found to be 42.9 dB. The cutoff frequency would be 3 dB below the peak. Using that, the following data was obtained:

Lower Cutoff Frequency = 243 Hz

Upper Cutoff Frequency = 6.16 MHz

Bandwidth = 6.16 MHz

Clearly, adding the CC amplifier has greatly increased the bandwidth. There is also a slight boost in the gain.

Dual Amplifier

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic3.sch

Date/Time run: 12/26/20 16:55:22 Temperature: 27.0 (C) Schematic3 (active) 50 (77.991K, 42.917) (243.424,39.910)(6.1627M, 40.888)-50 1.0KHz 100KHz 1.0MHz 1.0Hz 10Hz 100Hz 10KHz 10MHz 100MHz □ 20*LOG10(V(RL:2) / V(VS:+)) Frequency

Changing the value of RL:

The value of RL was varied from 1 k Ω to 100 k Ω . The following data was obtained:

RL (kΩ)	FL (Hz)	FH (MHz)	BW (MHz)	Gain (dB)
1	253	16.9	16.9	33.1
5	247	8.89	8.89	41.1
10	243	7.31	7.31	42.9
50	240	5.93	5.93	44.7
100	240	5.93	5.93	45.0

From the data, again, the higher the load, the lower the bandwidth. The gain is still significantly lower at low load. The gain should not vary with load.

Changing RL

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic3.sch

Date/Time run: 12/26/20 17:00:50 Temperature: 27.0 (A) Schematic3 (active) 50 (30.011K, 44.968) (240.260,41.976) (240.260, 41.713)(\$0.011K, 44.715)(24) .424, 39.910) (30).011K, 42.917) (246.630,38.095) (30.011K, 41.092)(253.168,30.070) (30.011K, 33.079) (5.9255M, 41.835) (5.9255M, 41.762) (7.3053M, 39.987)(8.8892M, 38.119) (16.876M, 30.133) **-**50 -1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20*LOG10(V(RL:2)/V(VS:+))$ Frequency

Changing the value of RS:

The value of RS was varied from 100 Ω to 10 $k\Omega$. The following data was obtained:

RS (kΩ)	FL (Hz)	FH (MHz)	BW (MHz)	Gain (dB)
0.1	247	6.67	6.67	44.0
0.5	243	7.31	7.31	42.9
1	243	6.84	6.84	41.7
5	243	5.06	5.06	35.5
10	243	4.61	4.61	31.2

From the data, again, a higher value of RS significantly drops the gain. The bandwidth has also dropped significantly. Therefore, a lower value of RS is highly preferred.

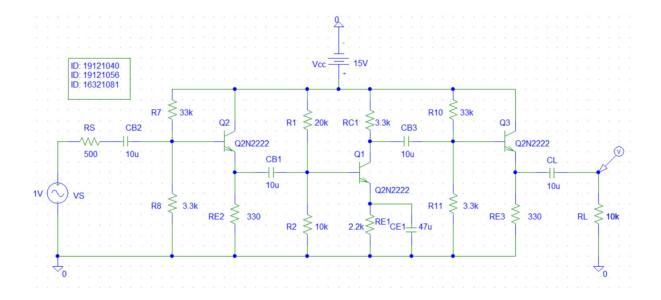
Changing RS

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic3.sch

Date/Time run: 12/26/20 17:29:40 Temperature: 27.0 (A) Schematic3 (active) 50 (30.011K, 44.020) (246.630,41.068) (30.011K, 42.917) (243.424,39.910) (\$0.011k,41.710) \(243.424,38.706) (30.011K, 35.526)(243.424,32.532) (30.011K, 31.247)(243.424,28.257) (6.6660M, 41.04/2) (7.3053M, 39.987)(6.8427M, 38.71/6)(5.0646M, 32.585)(4.6214M, 28.337)**-**50 -1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20 * LOG10 (V(RL:2) / V(VS:+))$ Frequency

Triple Stage BJT Amplifier Circuit

Another common collector amplifier is added after the dual stage amplifier.



Gain vs Frequency graph:

Initially all the values are fixed. The peak of the graph is found to be 38.6 dB. The cutoff frequency would be 3 dB below the peak. Using that, the following data was obtained:

Lower Cutoff Frequency = 250 Hz

Upper Cutoff Frequency = 7.70 MHz

Bandwidth = 7.70 MHz

There has been a slight drop in gain and slight increase in bandwidth.

Triple Amplifier

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic4.sch

Date/Time run: 12/26/20 17:54:34 Temperature: 27.0 (A) Schematic4 (active) 50 (57.725K, 38.596) (249.878, 35.593) (7.6978M, 35.599)-50 100KHz 1.0MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 10MHz 100MHz □ 20*LOG10(V(RL:2) / V(VS:+)) Frequency

Changing the value of RL:

The value of RL was varied from 1 k Ω to 100 k Ω . The following data was obtained:

RL (kΩ)	FL (Hz)	FH (MHz)	BW (MHz)	Gain (dB)
1				
5				
10	250	7.40	7.40	38.4
50				
100				

From the data, the graphs overlap. Changing the load does not affect the gain, thus triple gain amplifier is the best.

Changing RL

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Date/Time run: 12/26/20 17:57:09 Temperature: 27.0 (A) Schematic4 (active) 40 (30.011K,38.447) (249.878, 35.427) 20 (7.4015M, 35.437) -0 -20-**-**40--60-1.0MHz 1.0KHz 10Hz 100Hz 10KHz 100KHz 10MHz 100MHz $\Box \diamond \nabla \Delta \circ 20 * LOG10 (V(RL:2) / V(VS:+))$ Frequency

Changing the value of RS:

The value of RS was varied from 100 Ω to 10 $k\Omega$. The following data was obtained:

RS (kΩ)	FL (Hz)	FH (MHz)	BW (MHz)	Gain (dB)
0.1		6.93	6.93	39.7
0.5		7.70	7.70	38.6
1	250	7.40	7.40	37.4
5		5.70	5.70	31.2
10		5.70	5.70	26.9

From the data, again, a higher value of RS significantly drops the gain. The bandwidth has also dropped significantly. Therefore, a lower value of RS is highly preferred. The triple stage amplifier could not solve the RS issue.

Changing RS

* C:\Users\Asus\Desktop\Open Ended Lab\PSpice Files\Schematic4.sch

Date/Time run: 12/26/20 18:28:13 Temperature: 27.0 (A) Schematic4 (active) 50 (\$2.039K,39.699) (24).878,36.693) (249.878, 35.609) (32.039 K, 38.596)(249.878,34.405) (32.039K, 37.388)(249.878, 28.215) (32.039K, 31.205)(249.878, 23.956) (32).039K,26.926) (6.9328M, 36.692) (7.6978M, 35.59/9)(7.4015M, 34.44'1)(5.6975M, 28.258)(5.6975M, 22.914)**-**50 -100MHz 1.0Hz 10Hz 100Hz 1.0KHz 10KHz 100KHz 1.0MHz 10MHz $\Box \diamond \nabla \Delta \circ 20 * LOG10 (V(RL:2) / V(VS:+))$ Frequency

Discussion:

Initially, it was found that RE needs to be in a comprise value. Too low and there is no amplification. Too high, and the gain drops. The CE should be chosen small as the bandwidth is slightly higher. Not much significant effect. The RL would significantly affect the gain and bandwidth of the amplifier, even after adding a CC. It was after the second CC that the gain and bandwidth would remain constant no matter the gain. The second CC overcome the issue of varying RL. The RS would also affect the gain. All three amplifiers have the same issue, a lower value should be chosen for the gain to be high.