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GCAT486

TINY PC COMPATIBLE COMPUTER

TECHNICAL REFERENCE MANUAL

Revision B02 3 November 2000

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CONTENTS

TABLES

FIGURES

REVISION HISTORY

B00 This is the first revision of the GCAT486 Technical Reference Manual.

B01 Contains revisions reflecting enhancements made in the .B01 version of the BIOS. In particular, added text on graphics modes, PC Card and Compact Flash operation, GCAT486P2 operation, further advice on use as a super-component, corrected a number of typos and clarified text in a number of places.

B02 Contains revisions reflecting enhancements made in the .B02 version of the BIOS and the .B02 version of the printed circuit board. There are changes relating to keypad, BIOS patching and LCD graphics. Operation with the new TCDEVPLUSPLUS Development System is described. Further information is provided on GCAT486-specific BIOS interrupts. Corrected a number of typos and clarified text in a number of places.

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1 INTRODUCTION

1.1 OVERVIEW

To maintain our lead in advanced and highly integrated PC compatible computers, DSP Design have released a very small PC compatible computer. The GCAT486 is not much larger than a credit card and has been specially designed to allow low power operation. This makes it ideal for battery-powered operation in portable instruments and any application where space, weight and power consumption is important.

The GCAT486 can be used as a stand-alone single board computer, or as a plug-in module providing the PC compatible computer component for more complex systems.

This processor board is fitted with the AMD Elan SC400 high integration processor chip which operates at 66MHz. The chip integrates many of the functions commonly found in core logic chips on PC motherboards. It also provides a number of power-saving features, including the capability of reducing its clock speed under software control.

The board supports either 2M or 8M bytes of DRAM and either 256k, 512k, 1M, 2M, or 4M bytes of Flash memory. As standard 2M bytes of each are fitted. It also has three serial ports, an XT or key matrix keyboard interface, a number of general-purpose I/O lines and a speaker. In addition, an LCD controller in the Elan chip drives a variety of LCD modules, and a Vee negative voltage generator, required by many displays, is included on the board. An analog to digital converter is also provided.

The standard GCAT486 boards are provided with ROM-DOS pre-installed on the Flash File System. ROM-DOS is an MS-DOS “work-alike” operating system and with Flash File System software, which converts the on-board flash chip into a solid-state read/write disk drive.

A Compact Flash connector allows expansion by the addition of memory or I/O Compact Flash cards. One and two-slot add-in PC Card (PCMCIA) adapter boards are also available.

1.2 GCAT486 FEATURES

- High integration processor: a 66MHz AMD Elan SC400 is fitted.
- Very small – 65mm x 86mm.
- Very low power consumption from single 3.3V supply
- Draws as little as 800uA in suspend mode.
- ROM-DOS embedded in on-board Flash File System.
- Internal LCD graphics controller provides PC-compatible graphics for displays of 640 x 200 or smaller, and non-PC-compatible graphics for larger displays.
- Mono and STN colour LCDs supported.
- Microwindows graphical software package available.
- A Vee voltage generator provides the Vee and Vo voltages usually required by mono LCDs.

- A 5V power supply generator is provided, to allow the use of 5V LCD panels.
- Three RS-232 serial ports - COM2 is user-configurable as RS-485.
- The COM1 serial port can be optionally configured for IrDA-compatible infrared serial communications.
- Bi-directional Centronics parallel port is possible with the addition of external buffer chips. EPP compatible.
- 2M or 8M bytes of DRAM (default is 2M bytes).
- 256k, 512k, 1M, 2M or 4M byte flash memory for BIOS and solid state disk. A Flash File System is provided with every GCAT486, to provide a read-write logical disk drive. (By default 2M bytes are fitted).
- A Compact Flash connector is fitted, providing a built-in removable memory module. This socket can also accept Compact Flash I/O cards.
- Optional one and two-slot PC Card (PCMCIA) add-on boards are available, providing two PC Card slots.
- XT keyboard port. Alternatively, the GCAT486 interfaces to a matrix of keys of up to 14 x 8.
- A calendar/clock within the Elan processor uses an external battery.
- A 512-byte serial EEPROM is provided to retain set-up parameters in the absence of an external battery. Space is also available for user data.
- Reset, power supply monitor and watchdog timer circuitry.
- Up to 25 GPIO pins available to the user.
- Interface to other electronics is by way of an almost-full-function ISA bus interface, which is brought to two high-density connectors. Users can design their own motherboard fitted with mating connectors, and the GCAT486 can be plugged into the motherboard and used as a computer “super-component”.
- Most I/O signals are accessed through two 2mm-pitch connectors on the top side of the board, to which ribbon cables can be attached. These I/O signals are also taken to the two high-density connectors on the underside of the board.
- The TCDEVPLUS Development System provides all the facilities to get your GCAT486 running quickly, and is recommended for fast product development. This provides hard and floppy disk controllers and VGA graphics.

1.3 PC/AT COMPATIBILITY

The GCAT486 offers a high degree of compatibility with the PC family of computers. This compatibility extends from the MS-DOS level, through BIOS-level compatibility to register-level compatibility.

Users should note however that the GCAT486 lacks some features found on desktop PCs. The graphics is CGA compatible, not VGA compatible. There is no AT keyboard and mouse controller, only an XT keyboard interface. The Elan processor lacks a maths coprocessor. There are no floppy disk or IDE disk controllers.

The processor used on the GCAT486 board includes on-chip peripherals - timers, interrupt controller, DMA controller etc. These are software compatible with equivalent Intel peripheral chips used on the original IBM PC and PC/AT. The Elan chip provides other features. A calendar/clock circuit and speaker port are included, and the chip looks after clock generation, address decoding, expansion bus timing, memory mapping and various other functions.

The XT keyboard interface will connect to XT keyboards (though not AT keyboards). If the key matrix is used then a combination of hardware and software causes the key matrix keyboard to emulate a standard PC keyboard to a high level of compatibility.

The LCD controller provides CGA compatible graphics, so standard compilers and graphics libraries can be used to create display output. In graphics mode, the Elan display controller does not support any PC-compatible modes on displays with more than 200 lines, but does support such displays with non-PC-compatible graphics display modes. To provide a high-level graphics driver package for users who need graphics on a QVGA LCD we have ported the Microwindows graphics software package to the GCAT486

The three serial ports and optional printer port are PC compatible, and if one of the optional PC Card (PCMCIA) boards is used then it is also is PC compatible and is supported by Card and Socket Services drivers. (The PC Card adapter boards are the GCAT48P2 and the GCAT486P1. They are described in section 3.14).

While developing applications, the TCDEVPLUS Development System is recommended. This adds PC compatible floppy and IDE disk controllers and a full-screen VGA display controller.

1.4 ISA BUS EXPANSION

Users can operate the GCAT486 as a single board computer. It can also be treated as a "super-component" which can be plugged onto a motherboard designed by the user. In this case all of the I/O signals, plus an ISA bus (PC bus) are connected to the motherboard through two high-density two-part connectors. When mated the GCAT486 is just 3mm above the motherboard PCB.

The Elan chip provides an almost full-function 16-bit PC bus interface. Although the GCAT486 operates from 3.3V, most of its signals are 5V tolerant, so the GCAT486 can be used in a mixed 5V - 3.3V system with a minimum of additional circuitry.

Appendix H shows the circuit of the old GCAT486DEV Development System. This includes the data bus buffering circuit that can be copied by users who need to run a mixed voltage system. Although the GCAT486DEV is no longer supported, most of the circuitry has migrated to the TCDEVPLUS, and the circuit diagrams remain relevant for new designs.

1.5 THE GCAT486 ARCHITECTURE

The block diagram in Figure 1 shows the architecture of the GCAT486. The Elan processor accesses DRAM on a fast local bus. It also provides a slower PC bus (ISA bus), on which the Flash memory, serial comms and other I/O chips are located. The LCD graphics controller, keyboard interfaces and PC Card controllers are integrated within the Elan chip.

The Elan chip also performs a range of housekeeping and glue logic functions, as well as providing timer, interrupt, DMA, speaker and memory mapping facilities. Some of the Elan's GPIO pins are assigned specific functions onboard the GCAT486, such as accessing peripheral chips.

The GCAT486 has been designed to minimise power consumption, especially in Standby and Suspend modes. Signals are provided to place peripheral chips into a

low power state if they are not required. Both hardware and BIOS software work together to switch hardware into low power modes transparently to the user.

All timing is derived from a single 32.768kHz crystal. Phase locked loop oscillators within the Elan chip synthesise higher frequencies.

Connections are made to the GCAT486 through two 2mm-pitch pin headers or through two high-density two-part connectors, for applications where the GCAT486 is used as a plug-on PC component on a larger system.

This manual describes the operation of the B01 and B02 revisions of the GCAT486 PCB. There are a few minor differences between the two boards. The two PCB versions can be identified by looking for the text “165001.B01” or “166001.B02” which appears on the PCB.

Differences between the B01 and B02 PCB are minor. Enhancements added to the revision B02 PCB are:

- Extra pull-up and pull-down resistors are added on the .B02 board to minimise power consumption in Suspend mode.
- Extra pull-up and pull-down resistors are added to pull the COM2 status input signals to a defined state when operating in RS485 mode (this is discussed in section 3.6.2).
- A potential conflict on the PC Card Slot A Card Detect signal has been removed (this is discussed in section 3.14).
- A test point has been added to speed up DSP Design’s testing.

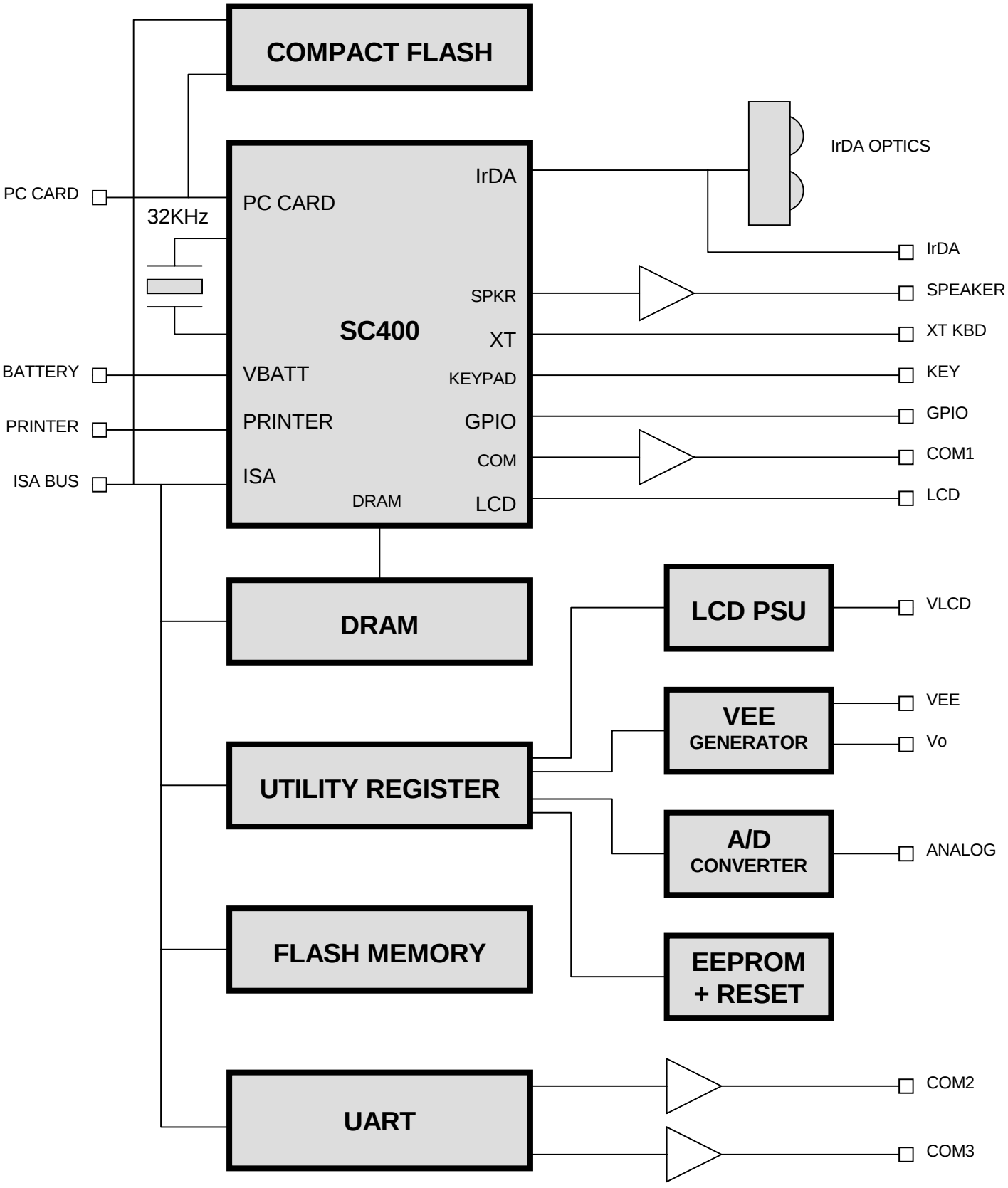


FIGURE 1 - GCAT486 BLOCK DIAGRAM

1.6 GETTING STARTED QUICKLY

This manual gives all of the information that most users will need in order to operate the GCAT486. This section gives a quick introduction to getting started. More details on configuring the board are given in Appendix B: GACT486 Setup Procedure. Those people who have special requirements may require further information. If this is the case our support engineers will be pleased to help you, but please read the manual first.

As well as reading this section, please read section 1.7, which identifies common problems.

1.6.1 TCDEVPLUS Development Systems

DSP Design strongly recommend developing with the TCDEVPLUS Development System, as in our experience this significantly reduces development time and users' technical problems.

The GCAT486 and the GCAT486P2 boards plug onto the TCDEVPLUS. The TCDEVPLUS provides considerable support circuitry and access to the GCAT486's I/O functions.

The TCDEVPLUS is a development platform that supports both the GCAT486 boards and PC/104 boards as well. It supercedes the TCDEV development system which many DSP Design's customers may already have. The TCDEV did not have sockets for the GCAT486, and instead an intermediate board, called the GCAT486DEV, was needed – the GCAT486 plugged into the GCAT486DEV, and the GCAT486DEV plugged into the TCDEV. This ungainly solution had a number of problems which have all been solved by the advent of the TCDEVPLUS. The GCAT486DEV has now been withdrawn (although its circuit is given in Appendix H as an example of motherboard design principles).

The features of the TCDEVPLUS include: an on-board VGA graphics controller with 15 pin VGA connector, a floppy and hard disk controller, a floppy drive plus cable, PC/AT and PC/104 slots for interfacing standard PC and PC/104 bus cards to the GCAT486's ISA bus. There is a battery to support the RTC and CMOS SRAM, power measurement circuitry, a forth serial port and diagnostic LEDs with programmable address decoding.

The TCDEVPLUS has all the standard PC connectors for interfacing to the outside world. These include serial port 9-way D-type connectors, a parallel port 25-way D-type connector, a VGA connector and PS/2 style keyboard and mouse connectors. It provides convenient options for connecting to 2.5" and 3.5" IDE drives, CD-ROM drives and Compact Flash cards. It also supports DSP Design's PC/104 range of embedded PC computers.

The TCDEVPLUS contains electronics specifically for the GCAT486: a DC-DC converter to provide 3.3V from 5V, buffers on the data bus, clock generation logic for the PC/104 bus and printer port electronics.

DSP Design also supply the TPPSU, which is a compact 45W power supply with cabling to make it easy to use with the TCDEVPLUS.

Most users will find getting started with the GCAT486 and TCDEVPLUS simplicity itself. The GCAT486 plugs directly onto the TCDEVPLUS. This links the COM1, COM2 and COM3 serial ports, parallel port, speaker and keyboard onto the TCDEVPLUS, and in turn to the PC compatible connectors mounted on the edge of the TCDEVPLUS board.

The TCDEVPLUS includes its own VGA, floppy and IDE disk controllers. It is possible to use either the VGA controller on the TCDEVPLUS or the LCD controllers on the GCAT486. These instructions assume that the VGA controller and floppy disk controller on the TCDEVPLUS are used initially, as this will be more convenient during early stages of development. Users can move to the GCAT486's on-board graphics controllers as the development process progresses.

The next sections describe using the TCDEVPLUS with the GCAT486.

1.6.2 Using the TCDEVPLUS Development System

Enable the floppy and IDE disk controllers and VGA graphics on the TCDEVPLUS. This is done by setting the jumpers at jumper areas E3, E4 and E5 to the "EN" position. The TCDEVPLUS COM4 UART may also be enabled at E8 if it is required. The battery back-up jumper should be set in the BATT position at E2. The status LED jumpers at E7 should both be set in the 1 - 2 position. At jumper area E6 set the C000 jumper to the "EN" position and the other seven jumpers to the "DIS" position. The speaker should be enabled by fitting a jumper at E1. The GCAT486 printer should be disabled at E9. Jumpers should be removed from E10 and E11.

Plug the GCAT486 onto the TCDEVPLUS. It plugs onto two 100-way connectors on the bottom left-hand corner of the PCB. The other two 100-way connectors are for the GCAT486PLUS.

Connect but do not switch on the TPPSU. (Note that the TPPSU power connector is polarized. Ensure that the locking tab on the power supply cable mates with the locking tab on the TCDEVPLUS connector). **Failure to connect the power supply cable assembly correctly may damage the equipment.**

Connect a keyboard and VGA monitor to the appropriate connectors. You will need an XT keyboard. Early PC keyboards had an XT/AT switch on the underside. If you do not have a keyboard which can operate in XT mode you will need to obtain one. DSP Design can supply you one – see Appendix D for ordering information. You will probably also need an adapter to convert the 5-pin DIN connector on the keyboard to the 6-pin mini-DIN socket on the TCDEVPLUS. An adapter is provided with the GCAT486PAK, or you can obtain one separately – see Appendix D.

Switch the power on. The GCAT486 should boot ROM-DOS from its on-board flash file system.

Try reading a floppy disk plugged into the TCDEVPLUS's disk drive. You can boot an operating system from the floppy as well as from the Flash File System.

Reset the computer using the reset switch on the TCDEVPLUS. This time hit the F2 key on the keyboard to enter the BIOS Setup menu. You should familiarise yourself with the Setup options (see section 6.2 for guidance). End by saving the settings to CMOS memory.

You will soon want to experiment with the GCAT486 on-board peripherals - LCD controller, solid state disks and matrix keyboard. The floppy and IDE disk controllers and VGA controller can be disabled with the E5, E4 and E3 respectively. To disable the TCDEVPLUS's VGA chip you must also set the E6 jumpers all to the "DIS" position.

When fitting an IDE disk drive on the TCDEVPLUS you will need to set the drive parameters using the Setup program. This is done using the Main/IDE Adapter 0 Master menu. Section 3.16 has more details on the IDE interface.

When development is complete the GCAT486 is removed from the TCDEVPLUS Development System. It can then operate stand-alone, or it can be plugged onto a motherboard of your own design.

Refer to the TCDEVPLUS Technical Reference Manual for full details of the TCDEVPLUS.

1.7 COMMON PROBLEMS

This section flags a number of common problems which have caused difficulties for some users. By being aware of these issues you should avoid the pitfalls.

The GCAT486 lacks some features found on desktop PCs, which may give rise to problems if programs are expecting these features. The graphics is CGA compatible, not VGA compatible. There is no AT keyboard and mouse controller, only an XT keyboard interface. The Elan processor lacks a maths coprocessor. There are no floppy disk or IDE disk controllers. Some of these compatibility issues may prevent some out-of-the-box operating systems or programs from running on the GCAT486.

There are some PC compatibility issues surrounding using graphics on displays with more than 200 lines. Users should ensure that they are aware of these. See sections 3.2.3, 3.2.6 and 3.2.8 for details. To provide a high-level graphics driver package for users who need graphics on a QVGA LCD we have ported the Microwindows graphics software package, which is described in section 3.2.8.

The COM1 serial port internal to the Elan chip suffers from a number of compatibility issues, particularly with respect to error reporting when FIFOs are enabled. These are described in the SC400 Errata, included on the GCAT486 Utility Disks. Most customers with simple serial comms requirements are unlikely to be bothered by these issues, but we would recommend that where sophisticated comms software is being used, then COM2 and COM3 should be used in preference to COM1. Some users have found that problems with the COM1 serial port can be eliminated by disabling the serial port’s FIFOs.

2 PROCESSOR AND MEMORY

The GCAT486 single board computer is based around the AMD Elan SC400 processor chip. There is one DRAM chip and one Flash memory chip soldered to the board.

2.1 PROCESSOR

The GCAT486 is based on the AMD Elan SC400 processor chip. This is a highly integrated chip that includes an x86 compatible processor and many integrated peripherals. It includes all of the motherboard support circuits used in PCs.

The processor is similar to the 80486, with an 8k write-back L1 cache. The Elan does not contain a floating-point processor. It runs at a range of speeds up to 66MHz (100MHz versions are available, subject to a minimum order quantity). The processor clock speed can be set to trade off computing power against power consumption.

The integrated peripherals include two 8237 compatible DMA control units (7 channels), one 8254 compatible timer control unit (3 channels), two 8259 compatible interrupt control units (15 interrupts), AT port logic and an MC146818 compatible calendar/clock and CMOS RAM. The majority of the peripheral functions are the same as on all PC/AT compatible computers. This includes the timers, interrupt controllers and DMA controllers as well as registers such as the NMI and speaker inhibit registers, fast reset and A20 gate registers. Software that accesses the PC/AT peripherals will have the same effect when running on the GCAT486, giving rise to a high degree of PC-compatibility.

The other housekeeping functions provided by the Elan are:

- Memory controller with on-board memory mapping registers
- DRAM memory controller
- Clock generation logic
- ISA bus interface and conversion logic
- Peripheral I/O address decoding
- Power management logic

The Elan includes a number of in-built peripheral circuits. These are:

- Real-Time Clock
- Serial port (COM1) with an optional IrDA mode
- LCD graphics controller
- Keypad interface
- XT keyboard controller
- PCMCIA controller
- Printer port
- GPIO pins

The Elan chip also includes a number of internal configuration registers. These registers are unique to the Elan chip. They control timing on the expansion bus, shadow RAM, DRAM configuration, memory mapping, power management and so

forth. They are initialized by the BIOS and will not normally need to be accessed by the user.

The performance of the GCAT486 may be gauged by the processor performance ratings produced by the Norton SI and the Byte Magazine Bytemark programs, as shown in Table 1. For comparison purposes the table also contains the measurements for a 100MHz 486DX4 (as used in DSP Design's TX486 board). This shows that at a comparable CPU speed the Elan processor delivers similar performance to the 486DX4.

CPU FREQUENCY	NORTON SI RATING	BYTEMARK RATING
8MHz	13	t.b.d.
16MHz	26	
33MHz	52	
66MHz	105	
100MHz	156	
486DX4 100MHz	156	

TABLE 1 - GCAT486 PERFORMANCE RATINGS

The above measurements were made with 2M bytes of DRAM. The programs were run using MS-DOS. Power management was switched off.

Users should make their own decision concerning cooling of the processor. Those who are running the processor at slow clock rates, and who are making use of the power management software will not need to worry too much about cooling, as the Elan will probably run cool. However, those who intend running the CPU at high clock speeds may need to consider cooling.

The processors will dissipate about 1.8W at 100MHz, 1.2W at 66MHz and about 700mW at 33MHz, and may get quite hot. AMD recommends a heatsink and/or a fan, at least when the processor runs at 100MHz and 66MHz, to keep the temperature of the processor down. In addition, the cooler a chip is the more reliable it will be. A heatsink or fan and heatsink combination can be fitted to the processor, or a fan could be provided in the enclosure along with the GCAT486. A Redpoint Thermalloy 2292B may be a suitable choice, glued on with suitable thermally conductive adhesive.

As an alternative the enclosure could be designed so that part of the enclosure acted as the heat sink. Thermal materials are available to provide a good thermal bond between the CPU and the case.

Another alternative is to use Chomerics T-Wing flexible heat spreader product.

The GCAT486 includes a built-in temperature sensor, which can be used to measure the temperature. This may be useful in formulating a temperature management strategy.

For data on the SC400, visit the AMD web site at:

http://www.amd.com/products/epd/processors/4.32bitcont/13.lan4xxfam/22.lansc400/index.html

Relevant data books are:

- Elan SC400 and Elan SC410 Data Sheet
- Elan SC400 and Elan SC410 User's Manual
- Elan SC400 Register Set Manual
- Elan SC400 Register Set Reference Manual Amendment

An errata lists the small number of outstanding bugs in the chip. This errata is not available on the AMD web site, but is included on the GCAT486 Utilities Disk.

2.2 CLOCK

The Elan includes a 32.786kHz oscillator circuit that is used for the real-time clock. This oscillator is used as the reference frequency for four phase-locked loop (PLL) clock synthesiser circuits that generate internal frequencies used by different sections of the Elan chip. The clock synthesisers are:

- Intermediate PLL - used to provide an input to the following the PLLs.
- Low-speed PLL - used for UART and timer.
- Graphics PLL - internal LCD graphics controller.
- High-speed PLL - used for CPU, DRAM, ISA bus controller.

The CPU itself runs as standard at 33MHz, but this frequency can be changed by software. The clock speed can be increased to 66MHz or 100MHz (so-called “Hyper-Speed” mode) to improve processing speed, using yet another PLL clock synthesiser. The clock speed can also be reduced, and even stopped, to save power. Frequencies of 16MHz, 8MHz, 4MHz, 2MHz and 1MHz are possible. These can be set by using the Setup menu.

Note that the standard GCAT486 is fitted with an Elan processor chip rated for 66MHz operation. Reliable operation at 100MHz with this chip cannot be guaranteed. The GCAT486 can be ordered with 100MHz processor chips by special order, subject to a minimum order quantity. See section 2.6 for a discussion of power supply voltage at 100MHz.

If automatic power saving is enabled then the clock speed will be adjusted automatically by software in order to reduce power consumption. Section 7 describes the clock changes.

The internal serial port baud rate generator is brought out of the Elan and used as the baud rate generator for the two external serial port UARTs.

The GCAT486 does not provide the two clocks that are sometimes required by ISA bus circuitry - the BUSCLOCK and OSC signals. These are generated on the TCDEVPLUS in case they are required. See Appendix H for details of the equivalent clock generation circuitry on the GCAT486DEV. See section 4.4 for further information.

2.3 DRAM

The main memory of the GCAT486 consists of a single Dynamic RAM (DRAM) chip. The chip is soldered to the board and cannot be changed. The memory is 16-bits wide. EDO parts are used for better speed. Two options are available: 2M bytes or 8M bytes. By default 2M bytes is fitted; the 8M byte capacity is subject to a minimum order quantity.

Note that only the first 640k bytes of DRAM are usually directly accessible by DOS. Some of the remaining DRAM is used to shadow the BIOS (see section 6.1) and the remainder is re-mapped above the 1M byte boundary, where it can be used by DOS extenders and by other operating systems.

The BIOS automatically determines the amount of DRAM present and configures the internal Elan registers accordingly.

Memory between C0000H and FFFFFH (the top of the 1M byte block) can be used to shadow BIOS code. This allows the BIOSes to run at the fast DRAM speed rather than the slow EPROM speed. Typically the system BIOS (from F0000H - FFFFFH) and the Flash File System (from CC000H - CFFFFH) driver are shadowed. If VGA graphics circuitry is used then its BIOS could be shadowed from C0000H - C7FFFH.

Memory beyond the 1M byte limit is available for DOS extenders and other protected mode operating systems.

2.4 FLASH MEMORY

The GCAT486 is designed to accept a range of Flash memory parts with the same footprint. Sizes available range from 256k bytes to 4M bytes. An 8M byte part may become available in the future. The default capacity is 2M bytes, implemented as a single AMD 29LV160 Flash memory chip. The board can also be supplied with other amounts of Flash memory, subject to a minimum order quantity.

Flash memory is non-volatile memory that can be programmed while it is soldered to the GCAT486. Data written to the Flash memory is retained after power is removed.

The Flash memory serves two purposes. Firstly, it contains the BIOS: machine-dependent software that is required to run an operating system.

The second function of the Flash memory is to provide a Flash File System for users who want a solid state disk.

The Flash memory device is divided into 64k byte sectors. Three of these are reserved for the BIOS. One 64k byte sector (at the top of the device) contains the first instruction of the BIOS, which is a jump to the BIOS itself, which is located halfway up the Flash chip. Two 64k byte sectors (128k bytes) of the Flash chip are used for the system BIOS and any BIOS extensions, such as the Flash File System BIOS extension. The GCAT486 comes pre-programmed with a system BIOS and a Flash File System BIOS extension. See section 2.5 for more information on memory mapping of the GCAT486, and section 6.3 for more information on BIOS extensions.

A Flash File System is provided with every GCAT486. This converts the remaining 1856k bytes of the 2M byte Flash chip into a non-volatile read-write logical disk drive.

This Flash disk can contain the ROM-DOS operating system as well as your application program. The Flash File System is described in section 6.6.

A utility program is provided on the GCAT486 Utility Disk, which allows the Flash chip to be programmed by the user. This allows the user to program various alternative BIOS image files into the Flash memory. This utility program is described in section 6.5.

The GCAT486 allows the Flash File System to access the large Flash chip through a small window in the 1M byte address space. Memory management logic in the Elan chip allows the high order address lines of the Flash chip to be changed by software. The Flash File System driver software controls the memory management logic transparently to the user's software.

The Flash File System is intended for ROM-DOS and MS-DOS. In principle Flash file systems could be created for other operating systems, such as Linux, QNX, OS/9 and VxWorks, but at the time of writing this work has not been done and DSP Design cannot support these operating systems. This situation may change in the future, so contact us if you have an interest in these operating systems.

The Flash chip resides on the eight-bit ISA bus data bus.

The BIOS makes use of "shadow RAM" in place of the Flash chip for greater speed. In this scheme the BIOS contained within the Flash chip is copied by the BIOS to DRAM at the same addresses. The Flash chip is then disabled and the BIOS is executed from the 16-bit wide DRAM, much faster than it would be from the Flash chip. Section 6.3 contains further information on BIOS extensions.

2.5 MEMORY ADDRESS MAP

Table 2 shows the memory map as configured by the standard BIOS of the GCAT486. This table shows the bottom 1M byte address space. Extra DRAM (1M byte or 7M bytes) is located immediately above the 1M byte boundary.

ADDRESS	MEMORY DEVICE DECODED	MEMORY SIZE
FFFFF F0000	BIOS in Flash Chip - copied to shadow DRAM memory during the boot sequence.	64K
EFFFF E0000	Some of this space is used by the BIOS during boot operations, after which it becomes free. Available for memory mapped circuitry on ISA bus.	64K
DFFFF D0000	Available for memory mapped boards on ISA bus. BIOS Extension code can be located here and optionally shadowed in DRAM.	64K
CFFFF CC000	The Flash File System BIOS extension is usually located here, shadowed into DRAM	16K
CBFFF C8000	Available for BIOS extension code contained in the Flash memory that can be shadowed to DRAM at this address.	16K
C7FFF C0000	Available for a VGA BIOS present external to the GCAT486. This can be copied from Flash chip to shadow DRAM at this address.	32K
BFFFF B0000	Parts of this region are used by the on-board LCD graphics controller, or by external VGA circuitry, if present.	64k
AFFFF A0000	Used by external VGA circuitry, if present. Used by Elan's display controller in some flat-mapped graphics modes. Otherwise available for memory mapped circuitry on ISA bus.	64K
9FFFF 00000	DRAM	640K

TABLE 2 - GCAT486 ADDRESS MAP - FIRST 1M BYTE

2.6 POWER SUPPLY VOLTAGE

The GCAT486 runs from a nominal 3.3V power supply. This should be in the range 3.0V to 3.6V. This voltage should be supplied to the GCAT486 through the connectors J1 and J2 (if operating as a stand-alone board) or through the two 100-way connectors J3 and J4 (if plugged onto a motherboard). In either case, connect as many as possible of the power supply pins on these connectors to the power supply. Keep wires or tracks to the power supply as short and thick as possible.

The +3.3V power supply should be connected between the pins named 3V3 and GND.

In special cases a separate power supply can be provided to the CPU core within the Elan chip. For this reason DSP Design have designed the GCAT486 with two power rails: one called VCC_CPU which connects to the VCC_CPU pins of the Elan processor and the other called 3V3 which connects to everything else. They are normally linked together on the GCAT486 by a solder link. This link can be removed and the VCC_CPU pins supplied by a different power supply voltage (See Appendix B for set-up options).

There are two reasons why a different power supply voltage may be required for the CPU core.

The first reason for a different VCC_CPU voltage is that AMD specifies a higher CPU core voltage for 100MHz operation. In this case the VCC_CPU power supply must be 3.45V +/- 0.15V (that is 3.3V - 3.6V).

Alternatively, users might take the view that by providing a tightly regulated 3.3V power supply to the whole board, and ensuring that this voltage did not fall below 3.3V then they would be supplying a legal voltage to the 100MHz CPU. A third alternative might be to supply the whole board (including the VCC_CPU pins) with a voltage of, say, 3.45V +/- 0.15V.

The second reason for a separate VCC_CPU voltage is to save power. At 33MHz or slower clock speeds the CPU core may be powered from a voltage as low as 2.7V, which will reduce power consumption. In this case DRAM timing must be slowed down. At present the BIOS does not support the slow DRAM timing.

The GCAT486 can operate with 3.3V and 5V peripheral circuitry, as most I/O pins on the Elan processor are 5V tolerant. The main exception to this is the 16-bit data bus, SD0-15. (Actually, the problem with these signals is not at the Elan itself, but at the Flash and UART chips which are attached to SD0-15 and which do not have 5V tolerant pins). Thus if connecting the GCAT486 to 5V logic a voltage translation buffer must be used on the SD0-15 bus. On the TCDEVPLUS Development System board DSP Design have used a 16-bit bi-directional CMOS switch, the PI5C162245 from Pericom Semiconductor, which can be used for this voltage translation. This circuit was used on the old GCAT486DEV, and is given in Appendix H.

Care must also be taken with PIRQ0 and PIRQ1 (configured as IRQ3 and IRQ5). These interrupt pins must not be driven higher than 3.3V, as they are also connected to the on-board UART chip, which does not have 5V tolerant inputs.

3 PERIPHERALS

This section describes the I/O address map and the on-board peripherals.

3.1 I/O ADDRESS MAP

The GCAT486 features a number of on-board I/O mapped resources, and supports access to I/O devices through an ISA bus interface. During development the GCAT486 accesses I/O devices on the TCDEVPLUS Development System.

All I/O mapped functions that are present on a standard PC are present at the same I/O addresses on the GCAT486. The GCAT486 is therefore compatible at the machine code or register level with a standard PC.

On-board I/O devices include registers within the Elan chip, the two external UARTs and the Utility Register.

The TCDEVPLUS floppy and IDE disk controllers and VGA graphics chip have I/O-mapped registers which are also present when the TCDEVPLUS is in use. The TCDEVPLUS has an optional COM4 serial port, and a programmable diagnostic LED address decoder. When Compact Flash or PC Card modules are installed then they will also have I/O-mapped registers in the I/O space. The PC Card controller chip programs the Compact Flash or PC Card modules with these resources.

The on-board I/O addresses are listed in Table 3. This table also includes the I/O addresses used on the TCDEVPLUS.

The GCAT486 can be used as a plug-in PC module on a motherboard designed by the user. This motherboard can have its own I/O resources. Those addresses that are not used on board the GCAT486 are available for peripheral devices on an external motherboard. I/O addressing of motherboard devices is reasonably straightforward: if an I/O address is not used by on-board resources then it can be allocated to a motherboard device. Putting this another way, the addresses of motherboard devices should be chosen to avoid the on-board I/O resources.

Users should be wary of partial decoding of the A0-A15 address lines. Partial decoding (not using A10-A15 for example) can result in “aliasing” - whereby a motherboard device can respond to more than one address. For example, a motherboard device at I/O address 200h when A10-A15 are not decoded will also respond at I/O addresses 600h, A00h, E00h and so on.

The Elan processor includes four programmable chip-select functional blocks – two for I/O space and two for memory space. The two I/O space chip-select generators are usually used for the COM2 and COM3 serial ports. However if either of these is unused then it may be possible to use the chip-select generators to generate a chip select for circuitry on the user’s motherboard. Contact DSP Design if this is necessary.

ADDRESS	I/O FUNCTION
00 - 0F	DMA Controller in Elan
20 - 21	Interrupt controller in Elan
22 - 23	Elan Chip Setup and Control (CSC) Registers
40 - 43	Timer Unit in Elan
60, 64	Keyboard controller in Elan
61	Port B Control/Status Port in Elan
70 - 71	Real-Time Clock and NMI enable in Elan.
80 - 8F	DMA Page Registers in Elan
92	Port A System Control Port in Elan
A0 - A1	Interrupt controller in Elan
C0 - DE (Even addresses only)	DMA Controller in Elan
EC	Utility Register (accessible only through BIOS)
EE	Alternate A20 Gate Control in Elan
EF	Alternate CPU Reset Control in Elan
102	Enable Register in TCDEVPLUS VGA chip.
1F0 - 1F7	IDE controller on TCDEVPLUS or Compact Flash card.
2E8 – 2EF	COM4: Serial port on TCDEVPLUS, if enabled.
2F8 - 2FF	COM2: Serial Port.
378 – 37A	Parallel Port in Elan, if used.
37B - 37F	Additional Parallel Port in Elan, if used in EPP mode.
3B4 - 3BF	Graphics controller registers, MDA or Hercules modes, if used.
3C0 - 3CF	Registers in VGA chip, if present.
3D0 - 3DF	Graphics controller registers, CGA mode or VGA chip.
3E0 - 3E1	PC Card controller in Elan.
3E8 - 3EF	COM3: Serial Port.
3F0 - 3F7	Floppy Disk Controller on TCDEVPLUS.
3F6 – 3F7	IDE controller on TCDEVPLUS or Compact Flash card.
3F8 - 3FF	COM1: Serial Port in Elan.
46E8	Enable Register in TCDEVPLUS VGA chip.
8022	Programmable Address Decoder for TCDEVPLUS LEDs.

TABLE 3 - ON-BOARD I/O DEVICES

3.2 LCD GRAPHICS

The Elan chip contains an internal graphics controller capable of supporting a variety of monochrome and STN colour LCD panels. Single-scan (4-bit data) and dual scan (8-bit data) displays are supported by the chip, with resolutions of up to 640 x 480. The BIOS is optimised to drive quarter VGA (320 x 240) panels and CGA panels (640 x 200). Other display sizes may be used, with certain restrictions, as described below.

The following sections describe the different display modes. Information which is specific to the GCAT486 is given below, as well as an overview of PC compatible display modes. The subject is rather complex, and for a fuller understanding of the subject readers should refer to the Elan manuals (see section 2.1 for references) and general texts on PC-compatible display modes.

Note that there are some PC compatibility issues surrounding using graphics on displays with more than 200 lines. Users should ensure that they are aware of these. See sections 3.2.3, 3.2.6 and 3.2.8 for details.

Note that the on-board LCD controller circuitry can be disabled completely, if necessary, thus freeing the memory and I/O space used by the LCD controller. This also reduces the power consumption, and so is useful in battery operated applications which do not require the LCD controller. This is done by the BIOS Setup program, in the Main / Video System menu.

3.2.1 General

The text and graphics memory, as well as fonts for text modes, are stored in part of the processor's DRAM. This is known as Unified Memory Architecture. Data is read from the DRAM and sent to the LCD controller. This may have an effect on processor performance, particularly with larger displays, as the time spent reading the display data is time during which the processor cannot access the DRAM.

Connection to flat panel displays is made through the J2 connector using a ribbon cable. (Users designing their own motherboard should remember that all the signals on the two ribbon cable connectors are also present on the two 100-way connectors which go to the motherboard.)

Mono LCDs require a Vee supply voltage, typically about -20V. This Vee is provided by the GCAT486, which has a Vee voltage generator on-board. The Vee voltage can be set by the variable resistor VR1. Some LCDs also require a second contrast adjust voltage, Vo. This can be supplied by the GCAT486, by adjusting VR2.

Hardware exists on the GCAT486 which allows the Vee voltage to be further adjusted by software around the mid-point value set by VR1. At the time of writing this function has not been supported by software, but it is the intention to allow this in future. See section 6.11 for information on GCAT486-specific BIOS interrupts.

STN colour LCDs are also supported. These usually require a positive Vee voltage, of around 20V. The GCAT486 cannot generate this voltage. However DSP Design have developed a circuit which generates a positive Vee voltage, which tracks the negative Vee voltage. Ask for details of this circuit if you need it.

Some LCDs require a 5V supply voltage, at a few milliamps. Other LCDs will operate with a 3.3V logic voltage. The GCAT486 can accommodate both of these supply voltages, and can switch the LCD supply voltage off to conserve power. The LCD logic supply voltage called VLCD, and is present on the J2 connector. A solder link determines whether it is 3.3V or 5V.

The GCAT486 drives the flat panel logic signals at 3.3V levels, rather than 5V levels. These 3.3V signals may possibly be of insufficient amplitude to drive displays

powered from 5V. We have found empirically that a 1k pull-up resistor connected between 5V (VLCD) and the DOTCLK pin was necessary for stable pictures on one 5V display. If you are planning to use 5V LCDs then you should consider this issue carefully.

To minimise power consumption the Vee and VLCD voltage generators are switched off when the display is not required. The Elan processor correctly sequences these supplies, both during power up and power down.

Following reset the BIOS searches for VGA circuitry on the ISA bus. If this circuitry is located then the off-board VGA chip is used instead of the on-board LCD controller. (The VGA BIOS extension must be shadowed in order for the VGA to operate correctly – this is the default in the Setup program). The on-board LCD controller circuitry can be disabled completely, if necessary, thus freeing the memory and I/O space used by the LCD controller. This is done by the BIOS Setup program. This also has the effect of reducing power consumption.

The BIOS setup program allows you to choose between three physical display types: CGA mono (640 x 200), QVGA mono and QVGA colour. In principle other size displays can also be used. This may require changes to the LCD controller timing registers, so that the LCD controller generates the correct number of pixels per line, and the correct number of lines per screen. The LCD timing is all table-driven, and tables in the BIOS can be patched by the user to suit alternative displays. See section 6.10 of this manual for information on patching the tables.

3.2.2 Display Modes

The Elan's graphics controller can be programmed to be MDA (monochrome Display Adapter), CGA (Colour Display Adapter) and HGA (Hercules Graphics Adapter) compatible. These are all PC standard graphics hardware and software standards. In addition it has proprietary modes of operation. Text and graphics modes are both supported. At the time of writing the BIOS does not support the MDA or Hercules modes.

Well-behaved DOS programs will make use of the BIOS to paint the screen. The BIOS can be told to place the display controller into a number of different display modes. The standard PC display modes are listed in Table 4. In some cases these modes have been implemented differently on the GCAT486, as will be explained in sections 3.2.3 to 3.2.6.

Modes 0 and 1 have identical resolutions, as do modes 2 and 3, and modes 4 and 5. However modes 1, 3 and 4 are colour, and modes 0, 2 and 5 are monochrome only. On a mono LCD the colours appear as different shades of gray. The screen resolution in graphics modes is expressed in pixels – horizontal by vertical. The resolution in text modes is expressed in characters (25 rows of 40 or 80 characters each) and also in pixels – the result of multiplying the character resolution by the font size (8 x 8 pixels or 9 x 14 pixels).

The different display modes can be selected by a BIOS interrupt 10h, function 0.

MODE	TEXT/GRAPHICS	CGA/MDA	RESOLUTION	COLOURS
0, 1	Text	CGA	40 x 25 (320 x 200)	16
2, 3	Text	CGA	80 x 25 (640 x 200)	16
4, 5	Graphics	CGA	320 x 200	4
6	Graphics	CGA	640 x 200	2
7	Text	MDA	80 x 25 (720 x 350)	Mono
(No number)	Graphics	Hercules	720 x 348	Mono

TABLE 4 - STANDARD PC DISPLAY MODES

The CGA modes include colour and monochrome capability. They include both text modes and graphics modes. The CGA standard is limited to 200 lines, and the Elan display controller complies with this restriction while in CGA mode. This creates problems when trying to use CGA modes with taller displays (such as the common QVGA display with 320 x 240 pixels). The problem can be overcome in text modes but not in graphics modes. See sections 3.2.3 and 3.2.6 for further details of the problem and the work-arounds.

The MDA mode is a monochrome-only, text-only mode. It displays 25 lines each of 80 characters. On the original PC each character was 9 x 14 pixels, which required a 720 x 350 pixel screen. On the GCAT486 the font size is modified so as to allow the use of displays 320 or 640 pixels wide and 200 or 240 pixels high. See section 3.2.4 for details. At the time of writing the BIOS does not support MDA operation.

The Hercules standard was a proprietary extension to the MDA standard that was popular in early days of the PC. It cannot be set by a BIOS call, but it became a defacto standard, and Hercules display drivers and graphics libraries exist. It is a graphics standard with 720 x 348 pixel resolution. It could offer an option to display graphics on QVGA displays in the future. At the time of writing the BIOS does not support Hercules operation. See section 3.2.5 for details.

The Elan display controller also provides a series of proprietary display modes, called flat-mapped modes. While these lack PC-compatible software support, they are more flexible than the PC-compatible modes and can provide an answer when PC-compatible modes fall short. Flat mapped modes are used to provide graphics on QVGA LCDs. See section 3.2.6 for details.

The BIOS is pre-configured to operate with either CGA (640 x 200) or QVGA (320 x 240) displays. Smaller displays can probably be connected without needing any BIOS changes. In most cases the smaller LCD will display the top left-hand part of the image that would have been displayed on the larger LCD. To achieve graphics on a QVGA display it is necessary to use no-PC compatible flat-mapped display modes. In some rare cases it may be necessary to change certain tables in the BIOS in order to program the display controller to support other LCDs. The mechanism exists to do this, should it prove necessary. Contact DSP Design for details.

3.2.3 CGA Display Modes

The CGA standard is an early colour display standard defined by IBM for their early PCs. Text and graphics modes are both supported.

The default BIOS is configured for 40-character CGA text operation (display mode 0), and assumes a QVGA LCD (320 x 240). Alternatives can be chosen using the BIOS Setup program (see section 6.2), and once you have booted any other CGA mode can be selected by a BIOS call.

The CGA display modes have native resolutions of 320 x 200 pixels or 640 x 200 pixels. In text modes these correspond to 40 x 25 characters, and 80 x 25 characters. In text modes the characters can be expanded vertically to match a 240 line LCD. CGA allows up to 16 foreground colours and 16 background colours. In mono displays this translates to an equivalent number of shades of gray.

In the text modes the BIOS writes a character byte plus an attribute byte to display memory. The display controller reads the character and generates appropriate signals for the LCD, based on a character generator look-up table. The standard CGA font size is 8x8 pixels, and since there are 25 lines of text this represents 200 pixels vertically. In text modes one byte defines the character and another defines the attribute. The attribute of a character defines its foreground and background colour, and whether or not the character blinks. There are 16 colour options for the foreground colours, depending on the settings of the red, green, blue and intensity bits in the attribute byte. There are two sets of eight background colours available, depending on the settings of red, green, blue bits in the attribute byte and on the setting of a bit in I/O register 3D8h.

The CGA graphics modes allow either one bit per pixel (and 640 x 200 resolution) or two bits per pixel (and 320 x 200 resolution). One bit per pixel allows a choice of two colours and two bits per pixel allow a choice of four colours. In one bit per pixel mode one colour is black and the other can be chosen from a palette of 16 (defined by values of red, green, blue and intensity bits in I/O register 3D9h). In two bits per pixel mode one colour (the “background” colour) can be chosen from the same palette of 16, and the other three colours (the “foreground” colours) are either green, red and yellow or cyan, magenta and white, and either “normal” or “intense”, depending on the settings of two further bits in I/O register 3D9h.

In CGA graphics modes your software may either write to any individual pixel (“all points addressable” or APA), or you may print text characters, in which case the BIOS uses the font look-up table to paint those pixels required to form the characters.

The BIOS setup program allows you to choose between three physical display types: CGA mono (640 x 200), QVGA mono and QVGA colour.

CGA LCDs are practically obsolete, but they are supported in the BIOS for those people who wish to use them, and those who wish to use smaller LCDs. Unsurprisingly, the BIOS supports CGA modes on CGA displays with no problems. In 320 pixels modes (modes 0, 1, 4 and 5) horizontal pixels are duplicated to ensure that the image fills the 640 pixel wide screen.

The default BIOS is optimised for quarter VGA LCDs (320 x 240 pixels), since these are readily available in both monochrome and colour. There is a problem to resolve here, since the CGA modes support only 200 vertical lines. The problem is resolved

in text modes by having the BIOS program the LCD controller timing registers to expand the font size to 8 x 9 pixels (by replicating the 8th row) and adding 15 blank rows at the bottom of the screen. This makes the 25 lines of text fit reasonably well onto the 240 line LCD.

However there is no solution in the CGA graphics modes. For this reason, when using physical QVGA displays, the graphics modes (modes 4, 5 and 6) cannot be CGA compatible. Instead the BIOS programs the display controller into “linear flat-mapped modes” in response to a BIOS request for modes 4, 5 or 6. The linear flat-mapped modes allow for graphical operation on QVGA displays. This is explained in section 3.2.6. To provide a high-level graphics driver package for users who need graphics on a QVGA LCD we have ported Microwindows, which is described in section 3.2.8.

In display modes 0 and 1 the screen is 40 characters wide. This matches the 320-pixel QVGA width exactly. As mentioned above, when using physical CGA LCDs in modes 0 and 1 horizontal pixels are duplicated to ensure that the image fills the 640 pixel wide screen.

In display modes 2 and 3 the screen is 80 characters wide. This is fine when using physical CGA displays, which are 640 pixels wide. On QVGA displays however there is a problem, since only 40 characters can be accommodated. Methods of displaying 80 characters on a 40-character QVGA screen are discussed in section 3.2.5.

3.2.4 MDA Display Mode

The MDA display mode is probably not particularly useful in the context of the GCAT486, and at the time of writing it is not supported by the BIOS.

MDA is a monochrome text display mode. On the standard PC it displays 25 rows of 80 characters each, as does the CGA text modes. On the original PC however, each character was 9 pixels by 14 pixels, in contrast to the 8 x 8 pixel resolution used in CGA mode. This was able to give a clearer image.

On the GCAT486 however, display controller register settings have been modified to match the physical LCD panels available. The character size would therefore need to be reduced to 8 x 8 pixels (when using the physical LCD panel) or 8 x 9 pixels (when using the QVGA displays). Thus the image quality is the same as for the CGA modes.

MDA mode is also only a black and white mode – no gray scales are possible.

3.2.5 Hercules Display Mode

Hercules mode could possibly offer a PC-compatible solution to displaying graphics on a QVGA display, since Hercules graphics provides APA (all points addressable) graphics operation with 348 lines. (You will recall that CGA graphics modes only support 200 line displays and so cannot be used with the 240 line QVGA displays).

At the time of writing the Hercules mode is not supported by the BIOS. Hercules mode may be supported at a later date.

3.2.6 Flat-Mapped Graphics

"Flat-mapped graphics" is the term given by AMD to the Elan's non-PC compatible display mode. In flat-mapped graphics mode the CPU views graphics memory as a flat, packed-pixel, linear map. This is in contrast to CGA graphics modes, where successive lines do not necessarily occupy successive memory locations.

Flat-mapped graphics is the simplest and most flexible display mode. It supports physical display sizes of up to 640 x 480 pixels. Colour depth can be either one, two or four bits per pixel (representing two colours, four colours or 16 colours, or the same number of gray scales).

Memory mapping is also fairly straightforward. In the case of one bit per pixel mode, the first pixel is located in the first byte of the display buffer, occupying bit 7. The next seven pixels occupy the remaining bits of the first byte, and the next pixel occupies bit 7 of the second byte in the display buffer. This pattern repeats until the end of the first display row; the first pixel of the second row occupies bit 7 of the next byte. The pattern is the same for two bits per pixel and four bits per pixel, except that the first pixel occupies bits 6 and 7 of the first byte in two bits per pixel mode, and the first pixel occupies bits 4 – 7 in four bits per pixel mode.

The display buffer is accessed through a 16k byte window at memory address B8000h.

Flat mapped graphics mode is used by the GCAT486 BIOS to resolve the problem of displaying graphics on a QVGA display. As explained in section 3.2.3, the CGA graphics modes cannot display more than 200 lines (there is a work around for text modes). Therefore, when using physical QVGA displays, the graphics modes (modes 4, 5 and 6) cannot be CGA compatible. Therefore DSP Design have modified the BIOS to place the display controller into flat-mapped mode in response to a BIOS request for modes 4, 5 or 6. (This only applies when the LCD Type has been set to QVGA in the BIOS Setup program, Main / LCD Options menu.) The linear flat-mapped modes allow for graphical operation on QVGA displays.

In this case the modes 4, 5 and 6 correspond to one bit per pixel, two bits per pixel and four bits per pixel respectively.

Table 5 shows the memory mapping for these modes, as they have been implemented for a QVGA display. The table lists the bytes per line (which provides the memory offset between pixels at the same position on two adjacent horizontal lines). Multiplying the bytes per line by 320 lines gives the number of bytes per screen. This gives rise to a complication for the 2 and 4 bits per pixel modes.

The base address of the display buffer is fixed at B8000h, and the memory window through which software can access the display buffer is fixed at 16k bytes, or 4000h bytes. As can be seen from Table 5, the 2 and 4 bits per pixel modes have screen sizes of greater than 16k bytes. Accessing the display buffer in these cases requires a page switching mechanism. There are actually 64k bytes of DRAM allocated to the display buffer. This memory is arranged as four 16k byte pages, and two page select bits make one of the pages accessible at memory address B8000h. The page select bits are in the display controller register at I/O address 3D4h/3D5h, at index 4Fh.

MODE	BITS PER PIXEL	PIXELS PER BYTE	BYTES PER LINE	SCREEN SIZE IN BYTES	NUMBER OF 16K PAGES PER SCREEN	NUMBER OF SCREENS AVAILABLE
4	1	8	28h	2580h	1	6
5	2	4	50h	4B00h	2	3
6	4	2	0A0h	9600h	3	1

TABLE 5 - FLAT-MAPPED DISPLAY MODES

The GCAT486 Utilities Disks contain three programs which fill the display buffers with simple patterns, corresponding to these three modes. The programs are called FILL1BPP, FILL2BPP and FILL4BPP. The screen is filled with horizontal stripes of different colours or gray scales (two, four or 16 stripes) and a diagonal line one pixel wide of a complementary colour is drawn from the top left-hand corner. The FILL2BPP and FILL4BPP programs illustrate the page switching.

To investigate these modes with a QVGA display you can use the three buffer fill programs to set up the patterns, and then the VMODE4, VMODE5 and VMODE6 programs to switch into the flat-mapped graphics modes. The program VMODE2 can be used to restore the GCAT486 to a text mode.

At the risk of adding further confusion, it is worth pointing out that, as with the PC compatible modes multiple display pages are available, at least for 1 and 2 bit per pixel modes. This is independent of the page switching, which is a mechanism for software to write to the display buffer. In the case of 1 bit per pixel mode, for example, six screens of 2580h bytes can be accommodated within the 64k byte display buffer. So six different images can be simultaneously resident within the 64k byte display buffer. By appropriately programming the display controller Start Address Registers (I/O addresses 3D4h and 3D5h, index 0Ch and 0Dh) it is possible to select any of these six as the page to be displayed.

3.2.7 Virtual Video

The BIOS supports “virtual video”, whereby a small physical screen can be used as a window into a larger logical screen. As an example, in display mode 2 the logical screen is 80 x 25 characters, and if a QVGA LCD is used the physical screen is 40 x 25 characters.

There are three modes supported – “Normal”, “Virtual” and “Track”.

Normal mode forces the logical display size to match the physical display size. For example, in display mode 2 (80 x 25 characters) with a QVGA LCD, the BIOS is told that the allowable number of characters per line is 40 rather than 80. When you are writing your own software then Normal mode will be the preferred mode.

In Virtual mode the BIOS assumes the usual screen size (see Table 4 above), and the LCD will display the top left-hand corner of this logical screen. An application program can be written to pan the physical screen around the logical screen as required. Sample programs to do this are included on the GCAT486 Utilities Disk.

In Track mode the BIOS uses the usual screen size. In this mode the physical screen is panned around the larger logical screen based on an algorithm where the panning follows the cursor position.

The virtual video mode is selected by the BIOS Setup program (see section 6.2). By default the virtual video mode is set to Normal. The virtual video mode may be changed after booting by BIOS calls. In Virtual mode the panning can also be set by BIOS calls. These are GCAT486-specific BIOS calls, which are further described in section 6.11. Sample programs for placing the GCAT486 into the various modes, and panning around the screen, are contained on the GCAT486 Utilities Disk.

3.2.8 Microwindows

As noted above, CGA graphics will not work on a 320 x 240 line LCD, since in CGA compatible mode the Elan hardware is restricted to 200 line LCDs. This led us to search for a graphic software package which we could offer that would support QVGA (320 x 240) displays. We have selected Microwindows and ported it to the GCAT486.

Information on Microwindows is available at http://www.microwindows.org/faq.html, from where this extract was taken:

> Microwindows is an Open Source project that brings some of the features of modern graphical windowing systems to the programming community not wanting or requiring the large disk and ram requirements of higher-end windowing systems like Microsoft Windows or the X Window System. Microwindows does not require any operating system or other graphics system support, as it writes directly to the display hardware, although it runs well on Linux frame buffer systems. Microwindows is designed to be portable, and can run in a wide variety of hardware and software environments. One the of more interesting targets is the emerging market of portable handheld and pocket PC's running Linux, also known as LinuxCE.

In the case of the GCAT486 Microwindows has been implemented for the QVGA displays in 1, 2 and 4 bit per pixel modes. Microwindows allows text and graphics to be written to the display from users' application software. The users must write application software in C that makes calls to the Microwindows APIs. The Microwindows code is linked with the user's code into a single executable program.

At the time of writing the Microwindows port is for DOS only, and QVGA sized screens only, but we expect that our Microwindows project will be on-going, and so users who are interested in Microwindows for other operating systems or other display sizes should contact DSP Design for the latest status.

Microwindows code and documentation will be available on the GCAT486 Utility Disks. If your version of the Utility Disks do not yet contain Microwindows then contact DSP Design for your copy.

The Microwindows package runs on VGA displays as well as the GCAT486. The GCAT486 Utilities Disk will contain the standard Microwindows release code, which is designed to run on VGA displays, plus additional files which are necessary for the GCAT486. Make files can be set up so that an application intended to run on the GCAT486 can be tested on a desk-top PC with a VGA screen, or on the GCAT486 with the VGA display on the TCDEVPLUS Development System.

3.3 VGA AND ALPHANUMERIC GRAPHICS

The GCAT486 has no VGA graphics system. However, there is a VGA graphics controller on the TCDEVPLUS. In addition, alphanumeric LCDs can be driven with GPIO pins.

Users will probably want to use the TCDEVPLUS VGA controller while using the TCDEVPLUS. To do this the TCDEVPLUS VGA controller must be enabled at jumper area E3 and the jumper area at E6 configured so that the C000 jumper is in the enabled position and all others are in the disabled position.

Users can add a VGA controller to a motherboard of their own design, if necessary.

Following reset the BIOS searches for VGA circuitry on the ISA bus. If this circuitry is located then the off-board VGA chip is used instead of the on-board LCD controller. The VGA BIOS extension code is shadowed. (The VGA BIOS extension must be shadowed in order for the VGA to operate correctly – this is the default in the Setup program).

Note that the on-board LCD controller circuitry can be disabled completely, if necessary, thus freeing the memory and I/O space used by the LCD controller. This also reduces the power consumption, and so is useful in battery operated applications which do not require the LCD controller. This is done by the BIOS Setup program, in the Main / Video System menu.

In practical applications users may want to use small alphanumeric LCDs. These are available in a range of sizes, from 1 line of 16 characters to 4 lines of 40 characters. These displays can be driven from the GCAT486's GPIO pins, and sample code for driving these displays is included on the GCAT486 Utility Disks.

3.4 XT KEYBOARD

The GCAT486 supports two types of keyboard - an XT keyboard and a key matrix keyboard.

By default the GCAT486 is configured to use an XT type keyboard. These were used on IBM PC and IBM XT computers, before the introduction of the IBM AT. The XT keyboard uses a 5-pin circular DIN connector of the same type as the AT keyboard which is used on most desk-top PCs, but the serial protocol is different.

Many older keyboards have a switch that allows them to operate in XT or AT mode. These keyboards are suitable for the GCAT486. Some keyboard suppliers can still supply XT compatible keyboards. An example is the Cherry G81-1800-HAG model, which can be supplied by DSP Design (DSP Design part number KBDXTAT). See Appendix D for ordering information.

The GCAT486 will work without a keyboard if required. In some circumstances the XT keyboard can operate simultaneously with the key matrix keyboard. See section 3.5 for details.

Users should avoid plugging in the keyboard when the GCAT486 is powered on.

The keyboard uses the IRQ1 interrupt, which is routed internally to the Elan chip. If you are using the TCDEVPLUS the keyboard is accessible through the keyboard connector.

An adapter will be required when using an XT keyboard with the TCDEVPLUS, since XT keyboards use the older 5-pin DIN connector while the TCDEVPLUS uses a 6-pin mini-DIN connector. A suitable adapter, the KBDATPS2 is provided as part of the GCAT486PAK and can be bought separately.

There is no PS/2 mouse port. If a mouse is required then a serial mouse must be used.

3.5 KEY MATRIX KEYBOARD

The second keyboard option is to use a key matrix. This is an array of keys arranged in rows and columns. At each intersection of a row and a column a key links the row line to a column line. The rows and columns are attached directly to the Elan chip, and the Elan is able to scan the key matrix under software control looking for key presses.

Many of the key matrix keys are multifunction pins (see section 8 for information). This means that key matrix row and column pins are only available if other functions are sacrificed. There are options for 1, 3, 6 or 8 columns, and 8 or 14 rows. This gives allowable key matrix sizes from 1 x 8 (8 keys) to 8 x 14 (112 keys). As more Elan pins are allocated to the key matrix, so their alternative functions are lost. Section 8 and Appendix F describes the multifunction pins.

The XT keyboard pins are two pins that can be re-deployed as key matrix column pins. If they are not re-deployed the XT keyboard will continue to operate. This means that the XT keyboard and the key matrix keyboard can coexist and operate simultaneously.

With a standard PC keyboard, when a key is pressed the processor is interrupted, and a “scan code” is read, indicating the key that has been pressed. A different scan code is generated when the key is released. In the case of the XT keyboard scan codes 0 - 7Fh indicate a key press. The scan code when the key is released is the same but with bit 7 set to 1.

The key matrix code in the BIOS closely emulates this XT keyboard operation. The BIOS regularly scans the key matrix, looking for key presses. The code debounces the key matrix and returns the appropriate scan code. The same interrupts occur – the BIOS makes a software INT 9 call, which is equivalent to the XT keyboard’s physical IRQ1 interrupt. In the case of special keys, such as the control and shift keys, the BIOS notes the key has been pressed and modifies future performance appropriately, and perhaps returning two scan codes.

The GCAT486 BIOS drives the key matrix via a series of tables within the BIOS. These tables define the physical rows and columns used, and provide a mapping from the X/Y key position to the scan code delivered, or special processing routines. Initially the key matrix tables are fixed, and optimised for a Cherry G84-4000 keyboard. It is possible however for the user to patch these tables, to customise the key matrix.

Appendix G describes the structure of these tables, and lists their default values. It goes into considerable detail about how to customise the key matrix. Section 6.10 describes the method of patching the GCAT486 BIOS tables.

In the default BIOS the key matrix keyboard is disabled. More accurately, the BIOS table which defines the key matrix size is set for a zero-sized keypad. All of the other tables that are necessary to support the Cherry G84-4000 keypad are present in the BIOS. To reconfigure the BIOS for this keypad, or a sub-set of this keypad, or other keypads, it is a matter of patching the BIOS, as described in Appendix G.

3.6 SERIAL PORTS

The GCAT486 features three RS-232 serial ports that are accessed as COM1, COM2 and COM3. Additionally, the COM2 port can be configured for RS-485 operation. COM1 can be configured as an IrDA (infra-red) serial port. **Note that COM1 suffers from some problems. See section 3.6.1 for details.**

3.6.1 Signals, Addressing and Interrupts

The serial ports are hardware and software compatible with the serial ports used on PCs, and all PC communications software packages should work with the serial ports. The UARTs are 16C550 compatible and thus provide a 16 byte transmit and receive FIFOs.

The COM1 UART is contained in the Elan processor chip. The COM2 and COM3 UARTs are contained within an external dual UART chip.

Connection is made to the serial ports via the 44-way J1 connector. A ribbon cable can be attached to J1. The serial ports are also accessible through the 100-way connector J3. If you are using a TCDEVPLUS then the COM1, COM2 and COM3 serial ports are available through the standard 9 pin D-type connectors on the TCDEVPLUS. These connectors are pin compatible with all PC computers.

The TCDEVPLUS incorporates its own serial port, set up for the COM4 address range. This port can be disabled at jumper area E8 if necessary. COM4 is of particular use to DSP Design during BIOS development, as it allows a serial debugger to be used before the BIOS has initialised the GCAT486 serial ports. Other users may also find it of use for remote debugging.

The serial ports provide the full complement of RS-232 signals. Transmit Data, Request To Send (RTS) and Data Terminal Ready (DTR) are outputs from the GCAT486. Receive Data, Data Carrier Detect (DCD), Data Set Ready (DSR), Clear to Send (CTS) and Ring Indicator (RI) are inputs to the GCAT486.

Following a reset of the GCAT486 the serial ports are initialized as 2400 baud, one stop bit, eight data bits and no parity. These parameters can be changed by the MS-DOS MODE command. The maximum baud rate is 115.2k baud.

The serial ports occupy the standard PC I/O addresses: 3F8h – 3FFh for COM1, 2F8h – 2FFh for COM2 and 3E8h – 3EFh for COM3. In principle these addresses

can be changed, since the BIOS is responsible for allocating the addresses, although this would be up to the user to do.

COM1 serial port uses interrupt level IRQ4 to interrupt the processor. The COM2 serial port uses interrupt level IRQ3. COM3 uses interrupt level IRQ5. Note that in some PC systems with three serial ports COM3 shares an interrupt with COM1. The GCAT486 design allows each serial port to have its own interrupt. (See section 4.5 for information on re-allocating interrupts).

It should be noted that the BIOS does not make use of serial port interrupts, but that most comms software packages enable the interrupts and make use of them to increase the speed of serial data transfer.

The COM1 serial port internal to the Elan chip suffers from a number of compatibility issues, particularly with respect to error reporting when FIFOs are enabled. These are described in the SC400 Errata, included on the GCAT486 Utility Disks. Most customers with simple serial comms requirements are unlikely to be bothered by these issues, but we would recommend that where sophisticated comms software is being used, then COM2 and COM3 should be used in preference to COM1. Some users have found that problems with the COM1 serial port can be eliminated by disabling the serial port's FIFOs.

3.6.2 RS-485 Operation

As an option COM2 can be re-configured as an RS-485 serial port. This is done with a solder link on the board - see Appendix B for configuration details.

The COM2 RS-485 port configuration provides either half-duplex or full-duplex interfaces. In full-duplex mode one twisted pair is used for transmission and another twisted pair is used for reception. Full-duplex mode would normally be used in point-to-point communication between two computers.

In half-duplex mode the transmit and receive twisted pairs must be connected together at the GCAT486. In this mode several boards can be connected to the single twisted pair, with no more than one board driving the cable at once. A suitable protocol needs to be agreed by all nodes on the twisted pair to ensure that only one computer transmits at any one time.

On the GCAT486 the RS-485 driver is controlled by the RTS bit of the on-board UART. When RTS is off (inactive) the RS-485 transceiver chip does not drive the transmit twisted pair cable. This is the default state after a GCAT486 reset. When RTS is set active the RS-485 transceiver does drive the transmit twisted pair cable and the GCAT486 can transmit. Note that the receiver part of the transceiver is always enabled. Thus in half-duplex mode COM2 will receive the characters that it transmits itself.

In RS-485 mode the DTR control output has no effect. On the revision B02 PCB the CTS, DCD, DSR and RI status inputs are all seen as asserted (logic 1 in the Modem Status Register at 2FEh). On the revision B01 PCB these inputs are undefined (they can be in either state, and software must not assume any particular values of these signals).

No RS-485 termination resistors are provided on the GCAT486. These must be provided externally if required. Normally an RS485 cable will be terminated at each end with a resistor across the two wires of the twisted pair. This is normally 100 ohms. A capacitor can be connected in series with the resistor to save power – DC current is blocked but the resistor is still seen by AC signals.

When operating as an RS-485 port the COM2 RS-232 signals are re-assigned RS-485 functions. Table E2 in Appendix E provides information on RS-485 pin assignments.

3.6.3 Disabling and Powering Down Serial Ports

The serial ports can be individually disabled by the BIOS Setup program (use the Advanced/Integrated Peripherals menu item). When both the COM2 and COM3 serial ports are disabled the baud rate generator clock from the Elan chip is switched off which reduces power consumption. When all three serial ports are disabled the RS-232 and RS-485 transceivers are also powered down, which can save a small amount of current. See section 6.2 for details of the Setup program.

An option also exists to place the RS-232 transceivers into an “auto-shutdown” mode. In this mode the transceivers shut themselves down when they do not detect a valid RS-232 signal level at their inputs. The auto-shutdown mode can be selected by the Setup program. Auto-shutdown applies only to the RS-232 transceivers, not the RS-485 transceiver.

Table 6 describes the RS-232 transceiver operating states. The /COMMOFF and FORCEON bits are in the Utility Register (see section 3.12). /COMMOFF can be controlled dynamically by the power management code, if the user has requested that the serial ports are turned off in Standby or Suspend modes. The FORCEON bit is set once only, depending on the auto-shutdown bit in the Setup menu.

/COMMOFF	FORCEON	TRANSCEIVER OPERATION
0	0	Shut down.
0	1	Shut down.
1	0	Auto-shutdown. Transceivers off when no valid incoming RS-232 levels present.
1	1	Normal operation – transceivers always on.

TABLE 6 - RS-232 TRANSCEIVER OPERATION

3.6.4 IrDA Operation

The COM1 serial port can also be configured to operate as an IrDA-compatible infrared serial comms port. The GCAT486 includes an on-board IrDA transceiver optics device.

To configure the COM1 serial port as an IrDA port you must use the Advanced/Integrated Peripherals menu within the BIOS Setup program (see section 6.2 for details of the Setup program). The IrDA standard defines a number of protocols. The GCAT486 supports the SIR format, with speeds of up to 115k baud.

The Elan chip also allows a higher speed MIR mode at 1.152M baud, although DSP Design do not provide software support for this, at the time of writing. Also, the TFDU4100 optical transceiver module is only designed for the SIR speed, so a faster optical device would have to be fitted for MIR operation.

The on-board IrDA transceiver module is located on one corner of the board. If the GCAT486 is suitably positioned in its enclosure then this module may be used to achieve infrared communication with other IrDA equipment. IrDA communication uses short pulses of high intensity infrared light. The Vishay Telefunken TFDU4100 IrDA optics device used on the GCAT486 calls for about 300mA to be supplied to the transmitter LED during these short pulses. To avoid having to supply this current from the regulated 3.3V power supply of the GCAT486, the positive terminal of the LED is taken out through the J1 and J3 connectors (as the VIRDA signal) to an external power supply which can source this current. The VIRDA signal should be connected to a positive supply (which would typically be a higher voltage than 3.3V) through a current limiting resistor. Since the LED has a forward voltage drop of about 1.5V the current limiting resistors can be chosen according to the following equation:

$$R = (Vs - 1.5) / Ipk$$

Where: Vs is the supply voltage
Ipk is the LED peak current (300mA)

The GCAT486 incorporates an on-board 10-ohm resistor, suitable for operation from power supplies of about 4.5V. Alternatively, a solder link on the board can be installed to short out this resistor, in which case an external resistor must be used.

To save power the IrDA transceiver can be powered on or off under software control. The POWER_IRDA bit in the Utility Register provides power to the transceiver. This pin can be permanently on or off, or can be dynamically switched by the GCAT486's power management software. See section 7 for details of power management.

If the on-board IrDA module is not fitted then an external IrDA optics module can be used instead. The IrDA transmit and receive data signals are available on the 44-way I/O connector J1 and on the 100-way connector J3. SIROUT is the transmit data (from the Elan to the IrDA module). SIRIN is the receive data (from the IrDA module to the Elan).

The data sheet of the TFDU4100 IrDA transceiver is included on the GCAT486 Utility Disks. For further information on the IrDA standards, see this web site:

www.irda.org

3.7 PRINTER PORT

The GCAT486 can optionally implement a full-function Centronics compatible printer port. This port is the MS-DOS PRN device. The printer can be implemented using a set of multi-function pins (see section 8). The default for these pins is for the printer port to be enabled. Alternative uses are as GPIO pins and as control signals for Slot B of a PC Card (PCMCIA) slot.

The printer port requires the use of two external buffer chips and some gates. These buffer chips are not present on the GCAT486, but are present on the TCDEVPLUS. Thus the printer port cannot be used when the GCAT486 is operating stand-alone, but can be used if the external chips are soldered to a motherboard into which the GCAT486 is plugged. If a unidirectional printer port is required then only the output latch chip is required.

This circuit is implemented on the TCDEVPLUS and also on the old GCAT486DEV board. A circuit of the old GCAT486DEV is given in Appendix H and the circuit can be copied. This is the circuit to be used for bi-directional and EPP modes. (Take care: when PCMCIA Slot B is used the printer signals assume new roles. The printer can not be used, and the /PPDWE and /PPOEN pins go low, so this circuit will cause trouble, by turning on the HCT245 chip during every I/O read cycle! Pull-up resistors on /PPDWE and /PPOEN will stop this happening).

For unidirectional mode the HCT245 chip is removed. The HCT373 is replaced by an HCT374 with its output enable pin (pin 1) tied low. The /PPDWE pin from the Elan processor connects directly to the clock pin (pin 11) of the HCT374.

The printer port features an 8-bit data port and the full compliment of control signals - four output signals and five input signals.

In applications where a printer is not required, the I/O signals on the printer port can be treated as general purpose digital input and output signals, and as such can be used for other applications (such as driving LEDs and polling switches, for example). When the printer port is enabled the nine control signals are always present, and a bi-directional 8-bit data bus can be provided by adding the two external buffer chips.

The 8-bit data port is normally used as an output port for driving a printer. Provided that the printer port is set up for bi-directional operation (which it is by default), then it can also be used as an input port. The default direction setting (after reset) is output. To configure the printer as an input bit 5 of the printer port Control Register must be set to 1. To re-configure as an output set bit 5 to 0. The Control Register is a read/write register located at I/O address 37AH.

The printer port signals are brought out on the 100-way connectors J3 and J4. Some of the control signals are also on J2 where they may be used as general-purpose I/O lines, if necessary. A typical use could be driving LEDs and polling switches. On the TCDEVPLUS the parallel port is accessed via a PC compatible 25 way female D-type connector.

The parallel port may be able to use interrupt IRQ7 to interrupt the processor. Users should note that the BIOS does not make use of interrupts for accessing the printer port, but other software drivers may do so. See section 4.5 for a discussion of interrupt allocation on the GCAT486.

The printer port can optionally be configured as an Enhanced Parallel Port (EPP). In EPP mode greater throughput is provided by automatically generating strobe signals. In EPP mode the control lines change function, and the I/O address range increases from three bytes (378h – 37Ah) to eight bytes (378h – 37Fh). Users must provide their own software for this mode. In EPP mode a 10us time-out can be enabled to ensure that an external peripheral does hang up the host.

The parallel port mode can be set with the BIOS Setup program (use the Advanced/Integrated Peripherals menu item). The port can also be disabled using this Setup program. See section 6.2 for details of the Setup program.

Note that the printer port uses multi-function pins. The same pins can be GPIO pins, or they can be the signals required to support Slot B of the PCMCIA controller. By default the PC Card Slot B pins are selected following a reset, and the printer function can be turned on by the BIOS Setup program. Section 8 describes multi-function pins.

Users should note the electrical characteristics of the printer port signals. The status input pins (/ERROR, PE, /ACK, BUSY and /SLCT) all have weak pull-up resistors attached (these are internal to the Elan chip). The control output pins (/STRB, /AFD, /SLCTIN and /INIT) are all open-drain with weak pull-up resistors (again, internal to the Elan). If the printer data port is set to be an input then the data pins will float unless pull-up or pull-down resistors are connected to them (note that on the TCDEVPLUS three lines - PD0-2 – have pull-up resistors and the rest have none).

3.8 SPEAKER

A PC compatible loudspeaker port is implemented within the Elan. This allows for production of tones, tunes, keyboard clicks etc. PC software that uses the speaker to generate sound will therefore operate as expected with the GCAT486. External speakers should be connected between the signal called SPKR (on J1 and J3) and the positive supply rail (3V3).

The circuit is very simple: the Elan's speaker output pin drives the gate of a MOSFET, whose source pin is connected to GND. The drain of the FET is connected through a 33-ohm resistor to the SPKR pin, and a speaker should be connected between this pin and the positive power supply (3.3V).

The TCDEVPLUS has a small loudspeaker mounted to it. It can be disabled at jumper area E1.

3.9 CALENDAR/CLOCK FUNCTIONS

Calendar/Clock facilities are provided in PC computers. The calendar/clock module is often known as the Real-Time Clock, or RTC. DOS time keeping occurs as a result of a regular interrupt from Counter/Timer 0. These two hardware elements are described below.

3.9.1 Real-Time Clock

The RTC functions of the Elan processor emulate those found in the Motorola MC146818 chip, and include time of day functions, calendar functions and CMOS RAM for storing setup parameters. An alarm facility is also provided; this allows an interrupt to be generated when a particular time is reached.

The calendar/clock chip may be accessed through the MS-DOS calls (interrupt 1AH) or with MS-DOS TIME and DATE commands. As well as the calendar clock functions there are 114 bytes of static RAM, which are backed up by the battery. This is used

to store configuration parameters used by the BIOS. A serial EEPROM fitted to the GCAT486 can be used to store these parameters in systems that have no battery - see section 6.7 for details.

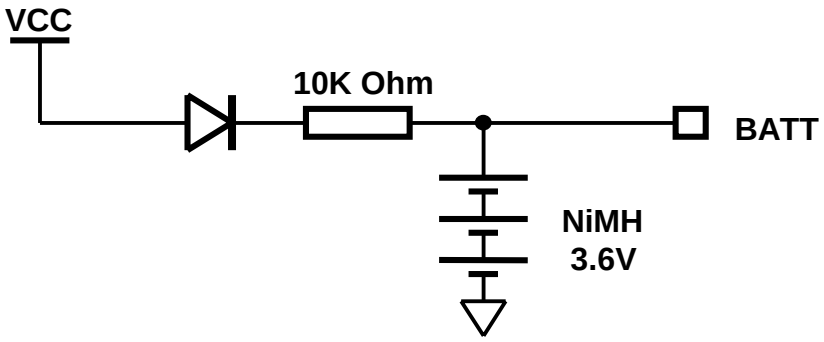
Users should note that in many operating systems, including MS-DOS and ROM-DOS, the RTC is read only as the computer boots. The RTC time and date is converted into an internal representation of the time and date, and the time is then updated based on an interrupt from Counter/Timer 0 (IRQ0, running at 18.2Hz in DOS). When applications request the time or date the result returned is based on this internal representation, not the RTC value. See 3.9.2 for details of this.

A battery can be used to provide power to maintain the clock and CMOS RAM when the main +3.3V power supply is not present. This external battery should be connected between the BATT input (on J2 and J4) and GND. The battery voltage should be between 3.0V and 3.6V and can be either be a rechargeable battery (e.g. NiMH) or a non-rechargeable battery (e.g. Lithium).

The Elan chip draws approximately 3uA from the battery when the GCAT486 is powered down and draws no current when operating normally (i.e. powered up). Note that if the battery voltage is higher than about 4V the battery will be supplying current even when the GCAT486 is powered on.

The TCDEVPLUS has a 3.6V NiMH rechargeable battery installed. This connects to the BATT input of the GCAT486 via a solder link, as described in Appendix H. The NiMH battery should be sufficient for the clock to operate for several months in the absence of the power supply.

Figure 2 gives a suitable circuit for a rechargeable battery back-up circuit.



NOTE: This circuit is suitable only when using a NiMH or Nicad battery of the type used on the TCDEVPLUS. The circuit shown in figure 2 is **not** suitable for Lithium or other non-rechargeable battery types. The diode and the resistor must be omitted if a lithium battery is used.

FIGURE 2 - RECOMMENDED BATTERY BACK-UP CIRCUIT

3.9.2 Timer Interrupt and Counter/Timer 0

Users should note that in many operating systems, including MS-DOS and ROM-DOS, the RTC is read only as the computer boots. The RTC time and date is converted into an internal representation of the time and date, and the time is then updated based on an interrupt from Counter/Timer 0 (IRQ0, running at 18.2Hz in

DOS). When applications request the time or date the result returned is based on this internal representation, not the RTC value.

This has a number of implications. Firstly, if interrupts are disabled for a long period, timer interrupts may be lost and the time may thus appear to be running slowly. Secondly, when the GCAT486 enters Suspend mode the timer stops running, and so the time will appear to be frozen.

Thirdly, the GCAT486 generates all of its internal clocks from a single 32kHz crystal, using phase-locked-loop clock multipliers to generate higher frequencies. The frequency of the clock which drives Counter/Timer 0, which in turn generates the IRQ0 timer interrupt, is not the exact 1.19318MHz used in standard PCs, but rather 1.1892MHz. To compensate for this the BIOS programs the Counter/Timer 0 divisor to be 0FF23h rather than the usual 0FFFFh. This will not normally cause any problems, but it is possible that some operating systems or applications may reprogram this register and thus receive interrupts at a slightly slow rate.

The same effect will apply to the other two Counter/Timer channels. Both of these will run at a slightly slow rate unless their divisor registers are compensated for the slower input clock. Counter/Timer 1 was traditionally used for DRAM refresh timing and Counter/Timer 2 generates tones for the speaker, so the slight differences are unlikely to be of significance.

3.10 SERIAL EEPROM

The GCAT486 has a serial EEPROM chip fitted. This is used primarily to store set-up parameters in systems that lack a battery to retain configuration data in the CMOS RAM. There is some space available in the serial EEPROM for users' data. The serial EEPROM chip also contains the watchdog timer, which is also accessed through the EEPROM's serial interface.

The BIOS includes a feature that checks to see if the contents of the CMOS memory are valid during the boot sequence. If the CMOS memory does not have valid contents (since there was no battery back-up, for instance) then the BIOS will check whether the serial EEPROM contains valid CMOS data. If it does then the data in the serial EEPROM memory will be copied into the CMOS memory and used.

See section 6.7 and 6.8 for information on using the serial EEPROM utility programs. See section 5.2 for details of the watchdog timer. See section 6.11 for information on GCAT486-specific BIOS interrupts which can be used to access the serial EEPROM and watchdog timer.

3.11 ANALOG TO DIGITAL CONVERTER

The GCAT486 includes a four channel 12-bit analog to digital converter chip. The converter allows analog signals to be monitored.

The analog to digital converter is a Maxim MAX1247 device. Communication with the A/D chip is through a serial link that is implemented partly in the Utility Register and partly with Elan GPIO pins. Using this communications link the processor may configure the A/D converter, place it in a low power mode, or make conversions.

The A/D converter has four inputs, called ADC0, ADC1, ADC2 and ADC3. These inputs can be between 0V and +3.3V. The input voltages must not extend beyond this range, or else internal protection diodes will begin conducting. If there is a chance of the supply voltages exceeding the supply rails then current limiting resistors must be added external to the GCAT486, to limit this current to 4mA. This same restriction applies when the power is switched off - if the analog voltage is still applied to the A/D chip when the GCAT486 is powered off then the internal protection diodes will conduct, and so the current limiting resistors must be used.

The voltages are measured as a proportion of a reference voltage, VREF. VREF defines the input voltage that provides the full-scale digital reading. The VREF pin on the A/D chip can be driven from an external voltage source, or from the on-board 3.3V supply voltage. A solder link allows this selection to be made. The accuracy of the measurement of course will be limited by the accuracy of the VREF voltage. By default the solder link connects VREF to 3.3V.

Measurements can be made as “single-ended” or “differential” measurements, as programmable options. In single-ended mode each of the four inputs are measured with respect to the AGND (0V) pin. (AGND is connected to the digital GND at a single point on the GCAT486). In differential mode the difference between two inputs is measured. The difference between ADC0 and ADC1 can be measured, as can the difference between ADC2 and ADC3.

Measurements can also be made as unipolar or bipolar, as programmable options. In unipolar mode an input voltage of AGND will give a digital output of 0000h, and an input voltage of VREF will give a digital output of 0FFFh.

In this case the voltage measured may be determined by this equation:

$$V = VREF \times n / 4096$$

where n is the binary number read from the MAX1247 (in the range 0 to 4095).

In bipolar mode an input voltage of VREF/2 will give a digital output of 0000h, an input voltage of VREF will give a digital output of 07FFh, and an input voltage of 0V will give a digital output of 800h. Voltages between 0V and VREF/2 are treated as negative voltages, and converted into twos complement negative numbers. It is probably only sensible to use bipolar mode in conjunction with differential mode, where the difference between two inputs can be negative as well as positive.

Sample software for the A/D converter is provided on the GCAT486 Utilities Disk. This software makes measurements using the A/D converter. The software may be used as a guide to users who wish to write their own A/D code. Note that this sample software shows the A/D converter being accessed through BIOS interrupt calls. See section 6.11 for information on GCAT486-specific BIOS interrupts which can be used to access the A/D converter.

A temperature sensor is provided on the GCAT486. This is mounted close to the Elan chip, and thus measures a temperature, which will be close to that of the Elan package. Thus the temperature of the Elan can be estimated. In principle this could allow the power management software to slow the processor down if it got too hot. At the time of writing this power management feature has not been implemented.

The temperature sensor is connected via a solder link to ADC3. If ADC3 is required to measure an off-board voltage then the solder link can be removed.

The temperature sensor is the National Semiconductor LM60C. It has a voltage output given by:

$$V = (T \times 0.00625) + 0.424$$

where T is temperature in degrees C.

Expressed differently, the output is 6.25mV per degree C, with an offset such that 0 degrees C gives 424mV.

Alternatively:

$$T = (V - 0.424) \times 160$$

Substituting the earlier equation for V we get:

$$T = ((VREF \times n / 4096) - 0.424) \times 160$$

To save power the A/D converter and the temperature sensor are powered on or off under software control. The /ADCOFF bit in the Utility Register is responsible for this. The A/D converter can be enabled or disabled by using the Integrated Peripherals section of the BIOS Setup program. If it is enabled, then the Power Management section of the Setup program can be used to determine whether the A/D converter should be powered off when the GCAT486 enters the Standby or Suspend states.

The Utilities Disk also includes the data sheet for the MAX1247 and the LM60.

3.12 UTILITY REGISTER

The GCAT486 has a Utility Register, which controls a number of peripheral functions including the serial EEPROM, analog to digital converter interface and power management. The Utility Register is an 8-bit write-only latch in the I/O address space at addresses 0ECh.

The Utility Register is used extensively by power management code, the Flash File System driver software and the serial EEPROM software, and will not normally be accessed by the user.

Table 7 gives the function of each bit in the Utility Register. Following reset all bits are set to logic 0. Users should not change bits they do not understand, or the GCAT486 may stop working.

The Utility Register can only be accessed by a complex address mapping scheme involving re-programming a number of the Elan's internal registers. This allows the register to temporarily appear in I/O space at address 0ECh. To avoid burdening the user with the details of this re-programming process the Utility Register can be accessed through a GCAT486-specific BIOS interrupt call, which does the re-programming transparently to the user. See section 6.11 for details.

BIT	FUNCTION
0	/ADCOFF (Disables A/D converter when logic 0).
1	SK (Clock to serial EEPROM and A/D Converter).
2	CSADC (chip select for the A/D converter – active high).
3	ADJVEE (Each pulse increases Vee amplitude).
4	POWER_IRDA (powers on the IrDA transceiver when logic 1).
5	ENFLASH (Enables access to the Flash memory chip when 1).
6	FORCEON (RS232 transceivers in auto-shutdown when logic 0).
7	/COMMOFF (RS232 transceiver off when logic 0).

TABLE 7 - UTILITY REGISTER BIT ALLOCATIONS

3.13 COMPACT FLASH SOCKET

The GCAT486 includes a Compact Flash connector. This can be used to accommodate any 3.3V Compact Flash card. The Compact Flash connector is controlled by the Slot A port of the Elan's in-built PCMCIA controller.

Compact Flash memory cards are commonly used for storage in digital cameras. Flash memory cards are available with capacities of several hundreds of megabytes, and mechanical hard disk drives in Compact Flash format are also available with capacities in the Giga-byte region. DSP Design is able to supply Compact Flash cards and a reader to allow the cards to be read on a desktop PC. This allows the GCAT486 to exchange data with desktop PCs.

Most users will want to use flash memory cards as a form of removable mass storage. However a range of peripheral cards is becoming available, which will offer a convenient way of adding I/O expansion to the GCAT486. Peripheral cards include modems, Ethernet LAN cards, interfaces to GSM phones and others.

From a software point of view, Compact Flash cards are the same as the physically larger PC Cards (PCMCIA cards). They thus (usually) require the same software stack to operate – a "Socket Services" layer which is hardware specific, a "Card Services" layer, which is machine independent, and device drivers specific to the card being used. When used in this fashion the Card and Socket Services software, and associated drivers, allow a full range of memory and I/O cards to be installed and used. The PCMCIA software is provided on the GCAT486 Utilities Disks.

The Compact Flash socket can be used in another way – as an IDE disk drive, without the need for Card and Socket Services. In this case the Elan's PCMCIA controller sub-system is programmed for the I/O address range and interrupt required by an IDE disk drive. A Compact Flash memory card is installed and is configured by the BIOS to appear as a standard IDE disk drive, normally appearing as the C: or D: disk drive.

When used in this mode, you must enter the BIOS Setup program (Main/Embedded Features menu) and enable the Compact Flash socket to operate as a disk drive. Then you must exit from Setup, and re-enter a second time. On the second time the IDE Adapter 0 Master menu item is selected, and can be used to auto-size the Compact Flash disk. **LBA should be disabled.**

When using a Compact Flash card as an IDE disk drive the Compact Flash memory card must be installed whenever the BIOS Setup program expects an IDE drive. If the card is removed without re-running the BIOS setup program to disable the IDE disk drive then the computer will report a failure in the IDE drive which it is expecting to be present. In practice, a card should always be present when the GCAT486 is powered on, only removed when it is powered off, and replaced before the GCAT486 is powered on again.

With Card and Socket Services the software is less demanding – the software will automatically detect the presence of a memory card and install the appropriate drivers only if the card is present. The absence of a card is not treated as an error condition. The Card and Socket Services software is discussed further in section 6.12

Because of board space limitations, the Compact Flash connector is directly attached to the GCAT486 data and address bus, and is not buffered. This means that it is not recommended that you install or remove cards while the GCAT486 is powered on. The cards should not be inserted or removed while the GCAT486 is powered on ("hot-plugged"), or you may run the risk of crashing the computer. Having said this, we have found that in practise most cards can usually be removed and installed without causing any trouble. Thus while we recommend that cards are not hot-plugged, users may decide that they are happy to do so.

Because the Compact Flash connector is directly connected to the GCAT486 internal signals and power supply, only Compact Flash cards which can operate from a 3.3V power supply may be used. Most cards will operate from 3.3V.

The Compact Flash connector is connected to the Elan's PCMCIA controller slot A. This means that it cannot be used while the GCAT486P2 or GCAT486P1 PC Card adapter board is installed.

3.14 PC CARD SOCKETS

PC cards were previously known as PCMCIA cards. They provide a convenient way of adding a wide range of removable memory and I/O functions to the GCAT486.

The Elan chip includes a two-port PCMCIA controller. This allows the GCAT486 to support two PC Cards (PCMCIA cards) using external PC Card connectors and buffer circuitry. These connectors and buffers are provided by the GCAT486P2 adapter board, or may be added by users to a motherboard of their own design.

The GCAT486P2 is a PCB the same size and shape as the GCAT486, with two 100-way connectors which mate with the J3 and J4 connectors on the GCAT486. Thus the GCAT486P2 may be plugged onto the GCAT486.

The GCAT486P2 provides two buffered PC Card connectors. The lower connector, closest to the PCB, is Slot A. The upper connector is slot B. Any combination of Type I, Type II and Type III cards may be used, with the sole restriction that if a Type III card is installed in Slot A then Slot B cannot be occupied.

A partially populated version of the GCAT486P2, called the GCAT486P1, is also available, although this may be subject to a minimum order quantity. This includes only the connector and circuitry for the Slot A card.

Unlike the Compact Flash socket, the circuitry on the GCAT486P2 includes buffers, which allows for PC cards to be installed and removed while the GCAT486 is powered on. Both 3.3V and 5V cards may be used, although 5V cards require an external 5V power supply.

The voltage selection is done with solder links, and there are other solder links on the GCAT486P2 as well. The configuration of the GCAT486P2 is described in Appendix B.

The GCAT486P2 also requires certain BIOS Setup settings, since some of the PC Card control signals are multi-function pins, and the appropriate function of these pins must be selected if the GCAT486P2 is to operate correctly. In the Advanced/Integrated Peripherals menu are two entries for the PCMCIA Slot A and Slot B control. These bits must be set to the “PCM-A” and “PCM-B” settings for the GCAT486P2 to operate, thus setting the multi-function pins into their PC Card control modes. If you are using the GCAT486P1 board, which has only the Slot A circuitry installed, then the slot B pins may be used for GPIO or as the printer. The multi-function pins are set to support the GCAT486P2 by default.

PC Cards require a software stack to operate – a “Socket Services” layer which is hardware specific, a “Card Services” layer, which is machine independent, and device drivers specific to the card being used. The PCMCIA software is provided on the GCAT486 Utilities Disks and discussed in section 6.12.

The Compact Flash connector is connected to the PCMCIA controller slot A. This means that it cannot be used while the GCAT486P2 or GCAT486P1 is installed.

Users who want to add the PC card circuitry to motherboards of their own design should request the circuit of the GCAT486P2 from DSP Design.

In Rev B01 PCBs the Compact Flash card detect signals and the GCAT486P2 card detect signal both drive the Elan’s card detect pin, causing a conflict. In practice this is not noticeable, but it is bad form, and a track on the GCAT486 PCB should be cut to avoid this conflict if the GCAT486 is to be used with a GCAT486P2. Contact DSP Design if you intend using the GCAT486P2 with a Rev B01 GCAT486. The problem was removed with the Rev B02 PCB.

3.15 FLOPPY DISK DRIVE

The GCAT486 does not have a floppy disk controller on-board. However, the TCDEVPLUS development system incorporates a complete floppy system, including a floppy diskette drive and cable. Connection to the GCAT486 is via the ISA bus on the two 100-way connectors J3 and J4.

Users will probably want to use the TCDEVPLUS floppy drive while using the TCDEVPLUS. To do this the TCDEVPLUS floppy disk controller must be enabled at jumper area E5.

The floppy disk circuit uses an interrupt (IRQ6) and a DMA channel (channel 2). These can be re-assigned to other uses if the floppy disk controller is not used. If a floppy disk drive is required on a motherboard design then, clearly, the BIOS support is available for it.

3.16 IDE DISK DRIVE

The GCAT486 does not have an IDE disk controller on-board. However, the TCDEVPLUS development system incorporates an IDE disk controller. Connection to the GCAT486 is via the ISA bus on the two 100-way connectors J3 and J4.

Users may want to use the TCDEVPLUS IDE controller while using the TCDEVPLUS. To do this the TCDEVPLUS IDE controller must be enabled at jumper area E4.

The TCDEVPLUS IDE controller connects to two 44-way 2mm connectors (for 2.5" IDE drives), a 40-way 0.1" connector (for 3.5" IDE drives and CD-ROM drives) and a Compact Flash connector (for Compact Flash cards operating as solid-state disk drives). See the TCDEVPLUS Technical Reference Manual for details.

The GCAT486 BIOS can identify the type and parameters of attached disk drives. This is done in the BIOS Setup program. Use the Main/IDE Adapter 0 Master menu item. The parameters should then be saved.

The IDE disk circuit uses an interrupt (IRQ14). If an IDE drive is required on a motherboard design then, clearly, the BIOS support is available for it. CDROMs are also supported.

A Compact Flash memory card can be used as a solid-state IDE disk drive. See section 3.13 for details. When the Compact Flash card is used as an IDE disk drive an external IDE drive cannot be used, and the TCDEVPLUS E4 jumper must be set to the disabled position.

4 STAND-ALONE AND SUPER-COMPONENT OPERATION

The GCAT486 will operate as a stand-alone single board computer, or it can be used as a “super-component”, using the two 100-way connectors to interface with circuitry on other printed circuit boards. This section of the manual describes first the stand-alone operation and then operation as a component plugged into a motherboard.

4.1 STAND-ALONE OPERATION

The GCAT486 will operate as a single board computer with the addition of the appropriate peripherals and a single +3.3V power supply. In stand-alone operation the GCAT486 need not be plugged into a motherboard, and the two 100-way connectors are not used.

In stand-alone mode connections are made to the GCAT486 through two 2mm ribbon cables which mate with connectors J1 and J2. J1 is a 44-way connector and J2 is a 50-way connector. Pin assignments for these connectors are given in Appendix E. The pin assignments have been chosen so that most signals which will be used in stand-alone modes are available on these two connectors. These signals are mainly serial ports, keyboard and display signals.

The GCAT486 requires a +3.3V power supply. Power is supplied through the two 2mm pitch ribbon cables which connect to the J1 and J2 connectors of the GCAT486. Each connector has a number of +3.3V and GND pins. All 3.3V pins and all GND pins are connected to the power rails on the GCAT486, so are electrically equivalent.

Users should take care to provide power to the GCAT486 through cables which are as short and thick as possible, and to make use of as many of the power and ground pins as possible, connecting them in parallel. This is to minimise the voltage drop which will occur through the resistance of the power cables.

4.2 SUPER-COMPONENT OPERATION

The GCAT486 can be used as a PC computer super-component, and can be plugged into motherboards designed by DSP Design’s customers. The GCAT486 plugs in using the two high-density 100-way connectors J3 and J4. These two connectors include the signals usually found on the PC and AT bus (the ISA bus). In addition to the ISA bus signals, all of the I/O signals which are on the J1 and J2 2mm pitch connectors are also present on the 100-way connectors. This allows users to design a motherboard to route the I/O signals to required locations, without the need for ribbon cable connections.

There are pull-up or pull-down resistors (internal to the Elan chip) on the ISA bus signals. In many cases the state of these pull-up or pull-down resistors is programmable, which can be of use for minimising power particularly if the ISA bus is to be powered off during Suspend. The default pull-up and pull-down resistors are defined as follows: The SD0-15 has pull-down resistors. The DREQ signals have pull-down resistors. The interrupt signals have pull-up resistors.

Note that most PCs have pull-up resistors on SD0-15, which means that reads from an unoccupied address will return 0FFh. The GCAT486 has weak pull-down resistors and so will often return 00h from an unoccupied address. However, if the data bus had recently been driven with another data value, the pull-down resistors may not have yet pulled the data bus back to 00h, and so in fact any data value could be read from an unoccupied address. This could possibly confuse some programs. Users may elect to add their own pull-up resistors on their own motherboard designs. Values of around 1k will usually be suitable. Note that this may increase current consumption in the lowest power suspend state.

The IOCHRDY, /IOCS16 and /MEMCS16 signals are not used on-board the GCAT486. They have pull-up resistors in the Elan chip, but the value of these resistors may be too high for these signals to pull up fast enough if driven by user-defined circuitry. Accordingly we would recommend that users add pull-up resistors on the range 330R to 1K if these signals are used on a motherboard design. (As an example of this, pull-up resistors have been added to /IOCS16 and /MEMCS16 on the TCDEVPLUS, since without them an IDE drive on the TCDEVPLUS will not operate correctly.)

As described in section 4.3, the Elan processor does not implement a full ISA bus interface. Some signals are missing or partially implemented. These restrictions are unlikely to cause problems in most circumstances.

Note however that some ISA bus signals are multi-function pins, and their functions will disappear if their alternative function is used. See section 8 for details. By default all such pins default to their ISA bus function.

Power is provided to the GCAT486 through the J3 and J4 connectors. The two 100-way connectors include a number of +3.3V and GND pins. All of these pins should be connected in parallel on the motherboard. A multi-layer PCB design should be used, with power and ground planes. As mentioned in section 2.6, the VCC_CPU pins are also normally connected to the +3.3V plane. Unless you need to drive VCC_CORE from a different voltage you should also connect VCC_CORE pins to 3.3V on your motherboard.

The GCAT486 can operate with 3.3V and 5V peripheral circuitry, as most I/O pins on the Elan processor are 5V tolerant. The main exception to this is the 16-bit data bus, SD0-15 (actually, the problem with these signals is not at the Elan itself, but at the Flash and UART chips which are attached to SD0-15 and which do not have 5V tolerant pins). Thus if connecting the GCAT486 to 5V logic a voltage translation buffer must be used on the SD0-15 bus. On the TCDEVPLUS Development System board DSP Design have used a 16-bit bi-directional CMOS switch, the PI5C162245 from Pericom Semiconductor, which can be used for this voltage translation. This circuit was used on the old GCAT486DEV, and is given in Appendix H.

Care must also be taken with PIRQ0 and PIRQ1 (configured as IRQ3 and IRQ5). These interrupt pins must not be driven higher than 3.3V, as they are connected to the on-board UART chip, which does not have 5V tolerant inputs.

The GPIO_CS2, GPIO_CS3, GPIO13 to GPIO19, SIRIN, SIROUT, KBD_ROW0-6, /BL1, /BL2, SUS_RES and /RESET pins are also not 5V tolerant

4.3 ISA BUS LIMITATIONS

The Elan chip does not support a full ISA bus interface. The limitations are as follows:

The ZEROWS-, IOCHCHK- (NMI), REFRESH- and MASTER- signals are not provided.

The two clocks BUSCLK (running typically at 8MHz and in sync with the bus timing signals) and OSC (a free running 14.318MHz signal sometimes used as a reference) are not provided by the Elan. DSP Design have added extra circuitry to provide both of these on the TCDEVPLUS board, so that these clocks will be available on the ISA slot and PC/104 bus slot on the TCDEVPLUS Development Systems. Note that in this case BUSCLK will be running asynchronously with respect to the bus cycles. Section 4.4 contains more information on clocks.

The SMEMR- and SMEMW- signals are not provided by the Elan. These two signals are active on the ISA bus only during accesses to the bottom 1M byte of the address space. The MEMR- and MEMW- signals, which are active during all ISA bus memory read and write cycles, are generated by the Elan and may usually be used in place of SMEMR- and SMEMW-. Note that MEMR- and MEMW- are not asserted during accesses to the Flash chip.

Note that some ISA bus signals are multi-function pins, and their functions will disappear if their alternative function is used. See section 8 for details. By default all such pins default to their ISA bus function.

Although the Elan includes a full interrupt controller internally, only eight interrupt request pins are provided on the Elan package. The eight physical pins can be allocated by software to any of the 15 interrupt channels supported by the internal interrupt controller logic. In practice, the BIOS programs two pins to on-board serial ports which require interrupts. These pins are also routed to the 100-way connectors, where they can be accessed if the on-board serial ports are not using the signals. Section 4.5 includes more information on interrupts.

Although the Elan includes a full DMA controller internally, only two DMA channels are provided with pins on the Elan package. That is, there are two physical DMA channels external to the Elan, each with a DMA request pin and a DMA acknowledge pin. These two pairs of pins can be allocated to any of the seven channels found on the ISA bus, under software control. Section 4.6 contains more information on DMA.

Note that most PCs have pull-up resistors on SD0-15, which means that reads from an unoccupied address will return 0FFh. The GCAT486 has only weak pull-down resistors, and any value may be returned. See section 4.2 for a fuller description of this issue.

4.4 CLOCK AND RESET SIGNALS

In most ISA bus computers the bus data transfer cycles are synchronised with the BUSCLK clock, which runs at approximately 8MHz. Additionally there is a 14.318MHz clock called OSC, often used by graphics cards. The Elan's internal ISA clock is not brought out of the chip to be used as BUSCLK, and there is no OSC signal generated on the GCAT486 either. Neither of these signals is required by the GCAT486.

However, these are generated by additional clock circuitry on the TCDEVPLUS board, and routed to the appropriate pins on the TCDEVPLUS ISA bus slot and PC/104 bus connectors, where they can be used for necessary tasks, such as for clock synthesisers on VGA graphics cards. The BUSCLK runs at 8.0MHz. The OSC signal is a clock running at 14.3181MHz. The BUSCLK clock is not synchronised to the ISA bus cycles. This is unlikely to be a problem for most users, since only very few ISA bus peripherals will require the BUSCLK signal at all, let alone a clock which needs to be synchronised with the ISA bus cycle.

If either of these signals is required on motherboard designs then users must generate these signals themselves.

The GCAT486 can generate a reset signal for motherboard circuitry. See section 5 for details. The GCAT486 drives the ISA bus RESETDRV signal but cannot be reset by the RESETDRV signal.

The GCAT486 can be reset by issuing a low going pulse on the /RESET line of the J1 or J3 connectors. In this way a system reset can be generated by an external signal or switch. The GCAT486 will then force the ISA bus RESETDRV signal to be driven. The TCDEVPLUS has a push button switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

The Elan processor itself contains two registers that can be used to force a reset of the Elan processor. These are at I/O addresses 92h and EFh. The port 92h register is common to most PC compatible computers. The port EFh register however is unique to the Elan. Reading from port EFh will force the processor to reset. Users must therefore avoid reading from this address.

Neither of the internal reset ports will cause the RESETDRV signal to be asserted, nor will any of the on-board peripherals receive a physical reset.

4.5 INTERRUPTS

The Elan processor contains the same interrupt controller circuit as is present on all PC computers. This consists of two 8259 type interrupt circuits, each with eight interrupt inputs. One 8259 is connected in cascade with the other, leaving 15 interrupts available.

Some of these fifteen interrupts can be used internally to the Elan chip for functions such as the timer interrupt and the COM1 serial port interrupt. Due to a lack of pins on the Elan chip, only eight interrupt signals are brought out of the chip to be connected to peripherals on the GCAT486 and on a motherboard. However, so as to provide the greatest flexibility, these eight interrupt request pins are programmable. That is, each of the eight interrupt pins can be programmed to be routed to any of the fifteen normal PC interrupts. This has been done by the BIOS, but these defaults can be over-ridden by user's software if necessary.

All eight of the programmable interrupt pins (PIRQ0 - PIRQ7) are taken to the two 100-way connectors. This allows them to be used for motherboard interrupts. PIRQ0 and PIRQ1 are taken to the GCAT486 COM2 and COM3 UARTs, respectively, where they can be used as serial port interrupts if required. If the UART interrupts are not enabled then PIRQ0 and PIRQ1 can be used on the motherboard.

Note that six of the programmable interrupt pins (PIRQ2-7) are on Elan multi-function pins. They have an alternative function, that of key matrix keyboard pins. There is thus a trade-off between the number of interrupts available and the size of a keyboard matrix. Section 8 describes the multi-function pins.

Table 8 shows how the interrupts are assigned. The 16 entries in the table are the "usual" PC interrupts. The next column is either marked "internal", indicating that the interrupt is routed entirely within the Elan chip, or else indicates which one of the eight programmable pins (PIRQ0-7) is normally used to provide external access to that interrupt. Those IRQ levels marked "Not Used" do not have any interrupt source allocated to them, either internally within the Elan or externally via the programmable PIRQ0-7 pins.

PC IRQ	INTERNAL/ EXTERNAL	ALLOCATION
0	Internal	Timer in Elan.
1	Internal	Keyboard in Elan.
2	Internal	Cascades second 8259 chip.
3	PIRQ0	COM2 in external UART chip.
4	Internal	COM1 in Elan chip.
5	PIRQ1	COM3 in external UART chip.
6	PIRQ6	Floppy Disk drive on TCDEVPLUS, or available on ISA bus.
7	Internal	Printer in Elan chip.
8	Internal	Alarm interrupt from RTC in Elan chip.
9	PIRQ3	Available for ISA bus interrupts
10	PIRQ4	Available for ISA bus interrupts
11	Not Used	-
12	PIRQ2	Available for ISA bus interrupts.
13	Not Used	-
14	PIRQ7	IDE Disk Drive on TCDEVPLUS, or available on ISA bus.
15	PIRQ5	Available for ISA bus interrupts.

TABLE 8 - INTERRUPT ALLOCATION

Note that the serial ports have individual interrupt enable bits, within their register sets. The default is for these interrupts to be disabled. This means that IRQ3 and IRQ5 can be used by other motherboard chips if the interrupts are not being used by the COM2 and COM3 ports.

Registers internal to the Elan chip map the eight physical pins (PIRQ0-7) to the familiar PC interrupt request levels (IRQ0-15). It should not be necessary for users to need to change this mapping, but be aware that it is possible, if it is necessary.

4.6 DMA

The Elan processor contains the same DMA controller circuit as is present on all PC computers. This consists of two 8237 type interrupt circuits, each with four DMA Request (DREQ) inputs and four DMA acknowledge (DACK) outputs. One 8259 is connected in cascade with the other, leaving seven DMA channels available.

Although the Elan includes a full DMA controller internally, only two DMA channels are provided with pins on the Elan package. That is, there are two physical DMA channels external to the Elan, each with a DREQ pin and a DACK pin. These two pairs of pins can be allocated to any of the seven channels found on the ISA bus, under software control.

One pair of DMA pins (PDRQ0 and /PDACK0) is normally programmed by the BIOS to be DMA channel 2, and is intended for use with the floppy disk controller on the TCDEVPLUS Development System. If the floppy disk controller is disabled then these pins can be used for DMA devices a motherboard. A Setup menu option allows this pair to be programmed for DMA Channels 0, 2 or 7.

The other pair of DMA pins (PDRQ1 and /PDACK1) has no fixed allocation, and is programmed by default to be DMA channel 5. A Setup menu option allows this pair to be programmed for DMA Channels 1 or 5.

The GCAT486 DMA channels are wired to DMA channels 2 and 5 on the TCDEVPLUS ISA bus and PC/104 bus connectors.

DMA channels 0, 1 and 2 can be used for 8-bit DMA transfers, and DMA channels 5 and 7 can be used for 16-bit DMA transfers. Thus the options provided should allow users to have two 8-bit channels in operation, or two 16-bit channels, or one of each.

Note that PDRQ1, /PDACK1, AEN and TC are on Elan multi-function pins. They have an alternative functions. If the alternative function is used then obviously the DMA function is no longer available. Section 8 describes the multi-function pins.

5 HARDWARE RESET OPTIONS

A full set of hardware reset options exist for the GCAT486. The reset circuit is built around the X5043 serial EEPROM chip, which provides reset functions as well as memory. This chip includes a power supply monitor and a watchdog timer. To avoid glitches on the reset signal the X5043 will always hold the reset signal asserted for approximately 200ms. This ensures all circuitry is properly reset.

The X5043 resets the Elan chip, and on-board circuitry. The Elan responds to its reset by driving the RESETDRV signal high. The data sheet of the X5043 is on the GCAT486 Utilities Disks.

5.1 POWER SUPPLY MONITOR

The X5043 monitors the +3.3V supply voltage. When the supply drops below about 2.7V the X5043 will assert the GCAT486 reset signal. Once the power supply returns to within specification, the reset signal will be released after further 200ms. This circuit prevents power “brown-out” causing unpredictable behavior.

Users should note that if the voltage drop across the cables that link the power supply to the GCAT486 is excessive then the power supply monitor might reset the GCAT486. This may also happen if there are noise spikes on the power supply. It is recommended that all power supply cables be as thick and short as possible to minimize the voltage drop across them.

5.2 ONBOARD WATCHDOG TIMER

A watchdog timer exists on the X5043. The function of a watchdog timer is to reset a computer if the software has crashed. The correct operation of the timer relies on software to access the watchdog timer hardware on a regular basis. If the software crashes, the watchdog timer will not be “kicked” and so eventually it will time-out and reset the computer. The watchdog timer function is accessed via the Utility Register and GPIO bits within the Elan chip.

The Utility Register is a multi-function register that among other things gives access to the clock pin of the X5043 serial EEPROM. The Utility Register is described in section 3.12. The GPIO pins of the Elan are described in section 8.

The watchdog is enabled by writing an enable command to the X5043 via the Utility Register and Elan GPIO pins. Once this has been initiated, an internal clock to the X5043 starts counting and will continue to count until it times out, until the watchdog timer is “kicked” by the user’s application software, or until the watchdog timer is disabled by a disable command sent to the X5043.

The watchdog timer period can be set to approximately 1.4s, 600ms or 200ms, or it can be disabled, by writing different command words to the serial EEPROM status register. Once it has been enabled the watchdog timer must be accessed repeatedly by the user’s software. If the watchdog timer is allowed to time out the X5043 chip will issue a hardware reset to the GCAT486 (and to the ISA bus).

The watchdog timer is “kicked” by taking its chip select (/CS) pin low then high. The /CS pin is driven by the GPIO20 pin of the Elan processor. The GCAT486 Utility Disk has documented sample code illustrating the use of the watchdog function. Note that it is the responsibility of the user to design code that will reliably kick the watchdog timer.

The BIOS includes code which disables the watchdog timer immediately after a reset, and thus if a watchdog time-out occurs the watchdog timer is disabled until after the operating system is loaded and the application software re-enables it. See section 6.7 for further information on the watchdog timer.

The watchdog timer is disabled prior to entering Standby or Suspend modes. After resuming operation the watchdog timer is restored to its previous state.

5.3 RESET SWITCH

The GCAT486 can be reset by issuing a low going pulse on the /RESET line on the J1 or J3 connectors. In this way a system reset can be generated by an external signal or switch. The reset switch connects between J1 pins 39 and 40. (Pin 40 is the /RESET input, and pin 39 is a GND pin). The GCAT486 will then force the RESETDRV signal of the ISA bus to be driven.

The TCDEVPLUS has a push button switch connected between /RESET and GND. Pressing this switch momentarily will reset the system.

5.4 RESETTING THE ISA BUS

The GCAT486 always resets the ISA bus via the RESETDRV signal. The active high RESETDRV signal is asserted whenever the X5043 is driving the GCAT486 on-board reset signal - that is, in response to a power failure, watchdog timer time-out, or a low going pulse on the /RESET line of the J1 or J3 I/O connectors.

The RESETDRV signal should be used to reset circuitry on a user-designed motherboard.

It is not possible to reset the GCAT486 by driving the RESETDRV signal on the ISA bus.

5.5 INTERNAL RESET SOURCES

The Elan processor itself contains two registers that can be used to force a reset of the Elan processor. These are at I/O addresses 92h and EFh. The port 92h register is common to most PC compatible computers. The port EFh register however is unique to the Elan. Reading from port EFh will force the processor to reset. Users must therefore avoid reading from this address.

Neither of the internal reset ports will cause the RESETDRV signal to be asserted, nor will any of the on-board peripherals receive a physical reset.

6 SOFTWARE

The GCAT486 offers a high degree of PC compatibility. A substantial body of software (both operating systems and applications software) which will run on any other PC will also run satisfactorily on the GCAT486.

The GCAT486 lacks some features found on desktop PCs, which may give rise to problems if programs are expecting these features. The graphics is CGA compatible, not VGA compatible. There is no AT keyboard and mouse controller, only an XT keyboard interface. The Elan processor lacks a maths coprocessor. There are no floppy disk or IDE disk controllers. Some of these compatibility issues may prevent some out-of-the-box operating systems or programs from running on the GCAT486.

Most users will wish to use the ROM-DOS operating system (booting from a hard disk, floppy disk or Flash File System) and then run off-the-shelf software, or their own application. Although in principle Linux, VxWorks, QNX, Windows CE and other operating systems can be made to run on the GCAT486, at the time of writing DSP Design cannot support these operating systems. This situation may change in the future, so contact us if you have an interest in these operating systems.

6.1 SYSTEM BIOS

The system BIOS is a program that interfaces between the GCAT486 hardware, the operating system and application code. It is responsible for controlling the GCAT486 hardware and providing a standard interface to the higher levels of software. The BIOS also deals with functions such as testing and initialisation of the GCAT486 hardware following power-on.

The GCAT486 uses a system BIOS supplied by Phoenix Technologies. Users should note that the BIOS is the copyright of Phoenix.

The BIOS has an in-built Setup program, which can be invoked by typing the F2 key at the keyboard during the boot sequence. Section 6.2 contains more information on the Setup program.

The BIOS is programmed into the Flash memory chip as part of the manufacturing process. Note that the system BIOS and BIOS extensions are combined in a single 128k byte file, which is programmed into the 2M byte Flash memory chip. The contents of the Flash memory chip can be changed by the user if necessary, as described in section 6.5. The default is for a system BIOS and the Flash File System BIOS Extension to be programmed into the Flash memory.

A number of pre-configured BIOS files are available on the GCAT486 Utility Disks. These differ in whether or not they contain the Flash File System BIOS extension, and in other respects. See the README.TXT file in the BIOS directory of the GCAT486 Utility Disks for further details.

Under some circumstances the GCAT486 BIOS may need to be modified or additional BIOS code may need to be added to the BIOS EPROM. Tools exist to deal with these issues, so contact DSP Design for details.

6.2 BIOS SETUP PROGRAM

The BIOS has an in-built Setup program, which can be invoked by typing the F2 key at the keyboard during the boot sequence. The setup program allows many system parameters to be changed, and then stored in CMOS memory. Amongst the parameters which can be changed are the current time and date, disk drive types, enabling and disabling peripheral devices, security and power management.

The Setup Utility is menu driven, and its operation should be self-explanatory. Users must not change parameters that they do not understand. The standard BIOS has a full-screen Setup screen with help information displayed. Since this screen is too large to be displayed on QVGA LCDs, alternative BIOSes are provided on the GCAT486 Utilities Disks which do not include the help information. See the BIOS directory of the Utilities Disks for further information.

A number of default settings will be loaded the first time the GCAT486 is re-booted after a CMOS battery backup failure. This will load in the default values suitable for operation with the TCDEVPLUS Development System. The default values can also be restored by an option in the Setup program's Exit menu. In addition, the F9 key can also be used to reset only those settings on the currently displayed Setup menu.

The GCAT486's on-board peripheral devices can be enabled or disabled by the Setup program, mostly in the Advanced/Integrated Peripherals menu (the LCD controller is disabled in the Main menu, in the Video System section). When peripherals are disabled they are placed into a low power mode. In the case of the on-board serial ports and LCD graphics controller, their I/O addresses and interrupt signals become available for other motherboard devices.

Setup parameters are stored in the on-board CMOS memory, and it is backed-up if an external battery is provided. If no external battery is present then the Setup parameters can be stored in an on-board serial EEPROM, as described in section 6.7.

The Setup menu includes a security menu. This allows access to the Setup program, floppy disk and hard disk boot sector to be password protected. Care should be taken with this, as if the password is forgotten the battery on the CMOS RAM must be removed to reset the password protection. Worse still (or better still!), if the serial EEPROM is being used to save the CMOS settings in the event of battery failure, the EEPROM will need to be erased or removed before the password protection can be removed.

The Setup program also provides control of the power management features of the GCAT486. This is described in detail in section 7.

6.3 BIOS EXTENSIONS

As well as the system BIOS, the Flash memory chip can (and usually does) contain at least one other BIOS extension. This is the Flash File System BIOS extension. Other BIOS extensions can in be added into the BIOS image by the user, and further BIOS extensions may reside outside the GCAT486.

6.3.1 Principles of Operation

The system BIOS and the BIOS extensions are combined into a single 128k byte file, which is programmed into the Flash memory chip using a Flash programming utility, as described in section 6.5. A number of these pre-configured BIOS image files are present on the GCAT486 Utilities Disk. The pre-configured files include options with and without the Flash File System driver.

If these pre-configured BIOS image files are not suitable, (for example if other BIOS extensions must be copied into the Flash memory) then a utility program is available for generating new 128k byte BIOS image files. This program is called CRUNCH.EXE, and is provided on the GCAT486 Utilities Disk. A CRUNCH.TXT file on the disk describes the operation of this program.

As well as executing BIOS extensions contained within the Flash chip, the BIOS also searches the ISA bus for BIOS extension EPROMs which might be present elsewhere in the system. The BIOS searches on every 2k byte boundary from C0000h to just below the system BIOS at F0000h. If valid BIOS extension EPROMs are found on the ISA bus then they are executed.

If a VGA graphics controller is enabled on the TCDEVPLUS then this search will locate the VGA BIOS extension. This will also apply if VGA circuitry is located on the user's motherboard.

The system BIOS is shadowed, and BIOS extension code in the Flash chip, such as the Flash File System BIOS extension, is also shadowed. BIOS extensions which may reside on the user's motherboard (such as VGA controllers or LAN controllers) may also be shadowed. This shadowing is enabled or disabled by the GCAT486 Setup program, in the Main/Memory Shadow menu.

Note that if the Flash File System is used then the 64k bytes of memory at address C0000h must be shadowed. Note also that since the Elan chip can only enable shadow memory in 64k byte blocks, if any memory in the 64k byte segment at C0000h is shadowed then all of the 64k byte block will be mapped as shadow RAM. The same applies to the 64k byte segments at D0000h and E0000h.

6.3.2 The Flash File System BIOS Extension

The standard GCAT486 boards are shipped with a BIOS image that includes one BIOS extension. This is the Flash File System BIOS extension. The FFS BIOS Extension is 16k bytes in size and is located at address CC000h.

The Flash File System device allows the Flash memory to be configured as a disk drive, as described in section 6.6.

The Flash File System is designed for MS-DOS, ROM-DOS and related operating systems. It is likely that the Flash File System BIOS extension will not operate with some other operating systems, and may need to be removed. A suitable BIOS image, without the Flash File System, exists on the GCAT486 Utilities Disk.

6.3.3 The VGA BIOS Extension

There is a special case relating to VGA BIOS extensions. Before the GCAT486 BIOS initialises its on-chip LCD graphics controller, it first examines the ISA bus, looking for any VGA BIOS which may be present. If a VGA BIOS exists (because the user is using the TCDEVPLUS VGA controller, for instance) then this VGA BIOS extension is executed, enabling the external VGA hardware. The on-board graphics sub-system is disabled.

6.4 ROM-DOS AND OTHER OPERATING SYSTEMS

The standard GCAT486 is supplied with a copy of Datalight's ROM-DOS 6.22 operating system installed in the Flash File system. This is an MS-DOS "work-alike". ROM-DOS is also present on the GCAT486 Utility Disks, which contain more information on this operating system and its utilities.

Most users will wish to use the ROM-DOS operating system (booting from a hard disk, floppy disk or Flash File System) and then run off-the-shelf software, or their own application. Although in principle Linux, VxWorks, QNX, Windows CE and other operating systems can be made to run on the GCAT486, at the time of writing DSP Design cannot support these operating systems. This situation may change in the future, so contact us if you have an interest in these operating systems.

The minimal nature of the GCAT486 hardware may cause problems to some out-of-the box operating systems. For example, Microsoft Windows will expect VGA graphics. Even if VGA was provided, it may still object to the lack of AT keyboard controller. We expect that most embedded operating systems will work with the GCAT486, although some customisation and configuration may be required.

Users who are running non-DOS operating systems may need to remove the Flash File System BIOS Extension from the BIOS image. See section 6.3.2 for details.

6.5 FLASH MEMORY PROGRAMMING

Flash programming utility programs provide facilities for programming data into the Flash memory chip on the GCAT486. The programs can erase some or all of the Flash chip, and can write a file from disk to the Flash chip. The most common use of these programs is to safely program the BIOS image file into the Flash memory chip.

The Flash programming utility is normally used to write a new BIOS to the Flash memory. It is not required to create the Flash File System disk in the Flash chip. Care must be taken when using this program to program the Flash chip, since an error can erase the BIOS, which means the GCAT486 will stop working. Should this happen the TCDEVPLUS Development System can be used to restore the contents of the Flash chip. See the TCDEVPLUS Technical Reference Manual for details.

The following describes the process of programming the AMD Am29LV160 chip installed as standard on the GCAT486.

The 29LV160 flash device is arranged as 32 sectors of 64k bytes each. Each block is erased separately, and it is not possible to erase less than 64k bytes at a time. The

GC4LV160.EXE programming utility used to program the 29LV160 device is available on the GCAT486 Utility Disk.

Users should be aware of where the BIOS resides. The 128k byte image occupies the region from E0000h to FFFFFh. In addition, a single JMPF (jump far) instruction is located at the very top of the chip, at 1FFFF0h. This jump is executed at a hardware reset and forces a jump into the 128k byte image. The top 64k byte block where the JMPF instruction resides in unusable for the Flash File System, so in effect three 64k byte blocks of the Flash memory are used by the BIOS.

The program can be run two ways - most commonly to safely program a BIOS image file into the Flash chip, and also in a more flexible way, to allow any file to be programmed at any location in the Flash chip.

In the safe BIOS programming mode GC4LV160 is run with the following single parameter:

GC4LV160 -u<filename>

u -u<filename> (u for 'update BIOS'). Program the specified BIOS image file into the device. In this safe mode the program checks to see if the file is present on the disk, and is a plausible BIOS image (i.e. it is 128k bytes in size). The program then erases the 128k bytes required by the BIOS image in the Flash memory, and programs and verifies the file. It also checks the JMPF instruction, and will erase the top sector and program that instruction, if necessary.

In the flexible mode GC4LV160 is run with any or all of the following parameters:

GC4LV160 -e -sxx -p<filename> -v<filename> -oxxxxx -lxxxxx -q -dxxxxx -h

e If -e is specified the entire device will be erased. If -e is not specified the device will not be erased. The default is to not erase.

s If -sxx is specified then the sector specified by xx is erased. The value for xx is a hexadecimal number between 0 and 1F. The BIOS is in sectors 0E and 0F. The JMPF instruction is in sector 1F.

p -p<filename> program the specified file into the device. This parameter defaults to "do not program".

v -v<filename> verifies the contents of the flash device against the data in the file specified by <filename>. If the chip and the file differ the address of the first byte that differs is printed, together with the values of the differing bytes. The default is not to verify.

o -oxxxxxx. Start programming the file at this offset from the start of the flash device. xxxxxx is a 21 bit (6 hex digit) hexadecimal number. This parameter defaults to 0. For programming the 128k byte BIOS image file you should use the parameter -oE0000.

l -lxxxxxx. This is the maximum number of bytes of data to program into the Flash chip. The number of bytes programmed will be the either the file length or the number of bytes specified by this parameter, whichever is the smaller.

This parameter defaults to the size of the Flash device (200000h bytes in the case of the 29LV160).

q Quiet. This parameter minimizes screen output. The default is “not quiet”.

d -dxxxxxx. This option displays the contents of the Flash chip at the 21-bit (6 hex digit) hexadecimal address xxxxxx. The output is 16 lines each of 16 hex bytes. The default is not to print data.

h Displays a help menu.

The GC4LV160.EXE program can be used to write one or more files to the Flash chip, by running the program several times with different -p, -s and -o options each time.

Once you have re-programmed your system BIOS there are several steps that MUST be undertaken to complete the BIOS update process. These steps are listed below.

1. Re-program the system BIOS as discussed above.

2. Re-boot by powering the GCAT486 system off and on or use the push button reset on the TCDEVPLUS. Do not use a CTRL-ALT-DEL reset.

3. Enter the Setup program by pressing the F2 key.

4. Once in Setup load the default settings (in the Exit menu) and then make whatever changes are appropriate.

5. If you have a hard disk, ensure you set the correct drive parameters.

6. Save the new settings to CMOS memory and exit. This will cause the GCAT486 to re-boot using the new BIOS parameters.

7. If you have previously run GC4EE.EXE -C (to save CMOS to EEPROM), then you MUST do this again to save the new BIOS parameters into the serial EEPROM.

6.6 FLASH FILE SYSTEM

This section describes the Flash File System, or FFS.

The Flash File system works well with MS-DOS and ROM-DOS. In principle Flash file systems could be created for other operating systems, such as Linux, QNX, OS/9 and VxWorks, but at the time of writing this work has not been done and DSP Design cannot support these operating systems. This situation may change in the future, so contact us if you have an interest in these operating systems.

6.6.1 Overview

The ability to operate without mechanical disk drives is a key feature of the GCAT486. To do this you can make use of the Flash File System (FFS) which is provided with every GCAT486. As well as being more robust than mechanical drives

they are also faster, at least for read operations. The Compact Flash socket can also be used as a solid-state disk drive.

The FFS provided with the GCAT486 is the FlashFX product from Datalight Inc. DSP Design have paid a license fee for every standard GCAT486, so you may use the Flash File System on every standard GCAT486 you buy. (Some volume users who do not require the FFS may ask for GCAT486 boards without the license, to reduce costs).

The Flash File System driver is implemented as a BIOS extension or as a loadable device driver. In order to boot the operating system from the Flash File System disk drive the BIOS Extension option must be chosen, since a loadable device driver can only be loaded after DOS has booted from another disk (such as a floppy disk). However, the loadable device driver option can be used when another device (an IDE drive for instance) is the boot device. The loadable device driver is also required during the initial formatting of the Flash disk.

The Flash File System driver is normally implemented as a BIOS extension. This driver must be programmed into the Flash memory, and then it is located every time the GCAT486 boots. The standard GCAT486 is shipped with the FFS device driver already present in the Flash memory as a BIOS extension, and with the disk formatted. There are two versions of the BIOS extension driver, as will be explained below.

The loadable device driver requires the driver to be placed on the boot disk, and it is activated by an appropriate entry in the CONFIG.SYS file.

In normal use you should use either the BIOS extension or the loadable device driver - not both. The only time it is permissible to use both is during initial formatting as explained in section 6.6.2.

In either case, the FFS driver operates by intercepting calls to the BIOS disk drive sub-system, which uses software interrupt INT13h. Calls that are not intended for the FFS are passed through to the BIOS. Calls that are intended for the FFS are performed by the FFS driver.

The FFS BIOS extension requires 16k bytes of memory, from CC000H - CFFFFH. A small amount of RAM within the 640k bytes available to ROM-DOS is also used by the FFS.

The Flash File System is designed for MS-DOS, ROM-DOS and related operating systems. It is likely that the Flash File System BIOS extension will not operate with some other operating systems, and may need to be removed. A suitable BIOS image without a Flash File System exists on the GCAT486 Utilities Disk.

6.6.2 Operation of the Flash File System

The standard GCAT486 is shipped from DSP Design with the FFS BIOS Extension installed in the Flash memory, the Flash disk already formatted, and ROM-DOS installed on the Flash disk. Thus most of this section is for information only, as all of the steps below have already been performed.

The Flash File System software referred to here is on the GCAT486 Utility Disk, in the FFS directory.

To operate with a Flash File System, perform the steps below:

1 Confirm that you have the FFS BIOS extension programmed in the Flash memory along with the system BIOS. If not, suitable BIOS files are present on the GCAT486 Utility Disk. The standard BIOS includes the FFS BIOS extension.

2 Boot your computer with ROM-DOS (or MS-DOS) from a floppy disk containing the FFS driver in its loadable device driver form and a suitable entry in the CONFIG.SYS file. The loadable device driver is FGC4LV16.SYS and the corresponding entry in CONFIG.SYS is:

```
DEVICE=FGC4LV16.SYS
```

When the Flash File System driver loads it will display a sign-on message to confirm that it has been located.

3 Before the Flash File System can be used the Flash disk must be formatted, using a dedicated formatting program called FXFMT.EXE. The syntax of the FXFMT program is:

```
FXFMT <drive> [/options]
```

<drive> is the drive letter, usually C:

[/options] can be any or all of the following:

/C This is an optional parameter, and tells the program to format the drive without prompting the user for input (not recommended).
/V This is an optional parameter and allows a volume label to be placed on the disk. After a format, the program will prompt the user for a volume name.
/T Do not use this parameter.
/M Do not use this parameter.

Most users will simply type:

```
FXFMT C:
```

4 At this point you have a functioning Flash disk, although the disk will not be bootable and will have no files on it.

5 Now the DEVICE=FGC4LV16.SYS entry should be removed from the CONFIG.SYS file on the boot disk.

6 Once the Flash disk has been formatted the user can use the DOS SYS command to place ROM-DOS (or MS-DOS) on the Flash disk. (Note this step is optional, but the operating system must be added if the Flash disk is to be the boot disk). To copy the ROM-DOS (or MS-DOS) operating system to the Flash Disk type:

```
SYS C:
```

7 At this point the GCAT486 can be re-booted. If all has gone well the Flash File System BIOS Extension will print a sign-on message and the GCAT486 will boot DOS from the Flash disk.

In a system without hard disk drives the Flash disk will be allocated the drive letter C:. It will be the boot disk (provided that the boot sequence in the Setup menu has C: selected as the boot disk).

If IDE drives are included in the system then there are two options. Either the Flash disk will be the first drive in the sequence (C:, with the IDE drives following on as D: etc), or it will be the last drive in the sequence (D: if there is just a single IDE drive). The option selected is determined by which version of the FFS BIOS extension is incorporated into the BIOS image. The file FGC4LF16.ROM places the Flash drive as the first drive (C:) always and the file FGC4LV16.ROM places the Flash drive as the final drive. In systems with no IDE drives both BIOS extensions will make the Flash drive C:.

Any additional PC Card disk drives present in the GCAT486P2 will be allocated successive drive letters.

The FFS implements a wear-leveling algorithm, to ensure that all parts of the Flash chip are equally used.

6.6.3 Write Operations and Garbage Collection

Writes to the Flash disk take longer than reads. This is due to the time taken by the Flash memory chip itself to write data into its memory cells.

When files are deleted the FFS driver does not immediately erase the corresponding Flash memory. Instead, it marks that memory as being “garbage”, and when the Flash memory approaches its capacity the FFS performs a garbage collection process, in which data which is still required is copied into a spare 64k byte block, freeing another block to be erased. The nature of the Flash memory is that it can only be erased in 64k byte blocks. The FFS driver thus has the task of allocating logical disk sectors to physical areas of Flash memory.

As a consequence of the garbage collection process, some writes will take longer than others, if they force the FFS to perform its garbage collection operation. This garbage collection process during Flash writes can increase write time by as much as sixty percent, as the number of garbage areas grow. The Datalight web site (at www.datalight.com/wp-flashfx-perform.htm) provides a fuller explanation of performance issues.

The GCAT486 Utilities Disk contains a garbage collection utility called FXRECLM.EXE. This utility can be used to force the FlashFX FFS to perform a garbage collection operation at any time, when executed. Placing an appropriate entry in autoexec.bat would force garbage collection each time the GCAT486 boots, helping to keep the flash array performance higher than normal.

FXRECLM.EXE usage:

FXRECLM.EXE <drive> [<count>]

Where <drive> is the drive letter of the flash disk (e.g. C:), and
<count> is the number of successive garbage collection operations to perform on the flash disk. One garbage collection operation will reclaim one 64k block of flash memory.

The FXRECLM.EXE utility stops the garbage collection process either when <count> has been reached or when there is no more flash memory to recover, whichever comes first.

For 2Mbyte of flash memory there are 32 blocks of 64k bytes each, three of which are reserved for system BIOS use. The remaining 29 blocks are available for flash disk use. Thus to perform garbage collection on all 29 64k byte blocks of flash disk memory use the FXRECLM.EXE utility as follows:

FXRECLM C: 29

6.6.4 Flash File System Statistics

The GCAT486 Utilities Disk also contains a useful utility for reporting the status of the flash disk. It can be used to find out how much flash memory is available, has been used, and is recoverable through the garbage collection process.

FXINFO.EXE usage:

FXINFO.EXE <drive>

Where <drive> is the drive letter of the flash disk (e.g. C:)

The FXINFO utility provides a detailed flash disk report, most of which is of little use to GCAT486 users. However the final section (an example of which is displayed below), is of use in determining flash memory usage, in particular the 'Recoverable Space', information.

The following is an extract from a typical FXINFO display:

```
        ...
Media Usage
Data Used           : 1528K
Free Space          : 58K
Recoverable Space   : 177K
```

The recoverable space is the amount of memory that can be recovered through the garbage collection process. In the example above the recoverable space is reported at 177Kbytes.

6.7 SAVING CMOS RAM DATA IN THE SERIAL EEPROM

A serial EEPROM chip on the GCAT486 provides non-volatile memory storage and also incorporates a watchdog timer. The non-volatile memory can be used to back-up the CMOS SRAM, in systems without batteries, or where the battery may go flat. The serial EEPROM chip used is the Xicor X5043. This chip contains 512 bytes of non-volatile serial EEPROM. The serial EEPROM is accessed through the Utility Register and Elan GPIO pins.

The BIOS includes a feature that checks to see if the contents of the CMOS memory are valid during the boot sequence. If the CMOS memory does not have valid contents (since there was no battery back-up, for instance) then the BIOS will check whether the serial EEPROM contains valid CMOS data. If it does then the data in the serial EEPROM memory will be copied into the CMOS memory and used.

It is the responsibility of the user to program the serial EEPROM. A utility program is provided to do this. It is called GC4EE.EXE and is available on the GCAT486 Utility Disk. It should be run with the -C parameter, like this:

```
GC4EE -C
```

(Note that the GC4EE program has other uses - see 6.8 and 6.9).

The GC4EE program should be run once the CMOS memory contains valid data - after running the BIOS Setup program for instance. The contents of the CMOS registers are then copied into the serial EEPROM. These values will be returned to the CMOS memory by the BIOS if the CMOS memory contains invalid data during subsequent boot operations.

When the GC4EE.EXE program is run all of the 128 locations in the CMOS SRAM module are copied to the EEPROM. Note the 128 locations are made up of 114 CMOS RAM locations, ten real-time clock time and date registers and four control registers. All 128 are copied to the serial EEPROM.

During the restore process, when the contents of the serial EEPROM are copied back to the CMOS RAM, all 128 bytes are copied. This restores the time and date, the control registers and the memory locations containing data.

The BIOS makes use of all of the CMOS memory locations – there are none available for the user.

Although only 128 locations in the serial EEPROM are currently used by the BIOS to store the CMOS registers, DSP Design strongly recommends that 256 locations in the serial EEPROM up to and including address 0FFh are reserved for possible future BIOS use. This leaves a further 256 bytes in the serial EEPROM (at addresses 100h - 1FFh) available for users. Section 6.8 describes a program that can be used to read and write CMOS EEPROM locations.

6.8 SERIAL EEPROM PROGRAMMING

The X5043 serial EEPROM has 512 (200h) bytes on non-volatile memory. Section 6.7 describes using the serial EEPROM for saving CMOS RAM settings. Addresses 00h - 7Fh in the serial EEPROM are reserved for holding CMOS RAM data, and addresses 80h - FFH are reserved for future DSP Design use. Addresses 100h - 1FFh remain available for users.

The GC4EE.EXE program allows individual bytes in the EEPROM to be written and read. It also provides a way of testing the EEPROM, enabling and testing the watchdog timer, and copying the CMOS SRAM into the EEPROM. It has the following parameters:

rxxx -r reads the data from the serial EEPROM at the address <xxx>, and displays it on the screen. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

wxxx -w writes data into the serial EEPROM at the address defined by the <xxx> parameter. The data written is the hexadecimal byte specified by the -d parameter. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

dxx -d defines the data value to be written to the serial EEPROM by the -w parameter. The xx parameter is a hexadecimal number in the range 0 - FFh.

t -t tests the serial EEPROM, by writing to every location. This destroys the previous contents of the EEPROM.

c -c copies the contents of the CMOS SRAM into the serial EEPROM.

s -s saves the contents of the serial EEPROM into a file on the current drive called GC4CMOS.DAT. All 512 bytes are saved. Together with the –p command this can be used to save and restore known CMOS memory configurations prior to putting GCAT486 systems into production.

p -p programs the serial EEPROM with the contents of a file on the current drive called GC4CMOS.DAT. All 512 bytes are written. Together with the –s command this can be used to save and restore known CMOS memory configurations prior to putting GCAT486 systems into production.

e -e enables the watchdog timer. The GCAT486 will be reset unless the watchdog is kicked (see the -k parameter). This is only used for testing purposes.

kxx -k kicks the watchdog timer for <xxx> seconds. The xxx parameter is a hexadecimal number in the range 0 - 1FFh.

The serial EEPROM can also be accessed through the GCAT486-specific BIOS calls, as described in section 6.11. In fact, this is how the GC4EE program accesses the serial EEPROM. Users who need to use these functions should read the XR5043 data sheet, which is contained on the GCAT486 Utility Disks.

6.9 WATCHDOG TIMER PROGRAMMING

The watchdog timer is contained within the serial EEPROM chip and is controlled through pins of the Utility Register and Elan GPIO pins. Once it is enabled, the watchdog timer will reset the GCAT486 if it is not accessed (or “kicked”) regularly. It is up to the user to write code to enable and kick the watchdog timer. As an example, the source code of a watchdog timer test program is included on the GCAT486 Utility Disk. The test program is called GC4WD.EXE.

The general-purpose serial EEPROM program, GC4EE.EXE, can also be used to test the watchdog timer - see section 6.8. The watchdog timer can also be accessed through the GCAT486-specific BIOS calls, as described in section 6.11. In fact, this is how the GC4WD program accesses the watchdog timer register in the serial EEPROM chip. Users who need to use this function should read the XR5043 data sheet, which is contained on the GCAT486 Utility Disks.

The watchdog timer is kicked by the toggling of its chip select pin (/CS), which is driven by the Elan chip GPIO20 pin. Users should consider where in their program the watchdog timer is to be kicked, in order to reduce the likelihood that a crashed program ends up executing a small loop containing the watchdog kick. Similarly, the watchdog accesses should not be part of a timer-based interrupt service routine, since a program could possibly crash and leave a timer interrupt correctly operating.

Care needs to be taken if the GCAT486 power management is to be used. Power management can slow down the processor clock, or even stop it, so that software loops will execute slowly, or even stop entirely. Thus the possibility exists that watchdog timer would time out.

Consequently, the BIOS disables the watchdog timer before entering Standby and Suspend modes, and re-enables it after resuming high-speed operation. Users must be aware of this. In low speed mode the watchdog timer remains operational. Users must confirm that the slow CPU speed still allows the watchdog to be kicked.

6.10 PATCHING THE BIOS TABLES

Many of the BIOS configuration options may be set using the BIOS Setup program. For some options however it is impractical to provide a BIOS Setup mechanism. Instead, the BIOS image itself may be patched, so as to change certain tables and data structures. This section describes how this is done.

The tables include:

- Key matrix tables defining the Elan key matrix row and column pins that are to be used.
- Key matrix tables for translating from a given X/Y coordinate to a scan code, or to a special key processing routine.
- LCD controller configuration tables, which may need to be changed if different LCDs are used.
- Others may be added later.

All of these BIOS tables are prefixed by a unique ASCII string. It is possible for a patching program to search for these strings, so as to discover the location of the tables that follow the identifying text. The program is then able to replace the data in the table with data from another file. The program then updates a checksum and writes back a new version of the BIOS image, which can then be programmed into the GCAT486.

The BIOS patching process is done by a program called GC4PATCH.EXE, which is present on the GCAT486 Utility Disks. The BIOS must first be “uncrunched” by the CRUNCH program (see section 6.3.1 and the Utility Disks). The program is run from the DOS command line. It can be run with the –p switch or the –d switch, but not both:

GC4PATCH -p<filename> or GC4PATCH –dx

p -p<filename> Defines a file containing data to be patched into the BIOS image.

d -dx Locates patch point x and dumps the contents of the patch point to the screen (or to a file if redirected).

h Displays a help menu.

A batch file called PATCHIT.BAT uncrunches a BIOS, runs GC4PATCH, then runs CRUNCH again to re-create a BIOS image. This is explained in further detail on the GCAT486 Utility Disks. The Utility Disks contain details of the tables that may be patched, including the contents of the default tables.

6.11 GCAT486 BIOS INTERRUPT

6.11.1 Introduction

Users of the GCAT486 will potentially need to access hardware and the BIOS in order to configure the GCAT486 for their purposes, and to access low-level hardware functions such as the Utility Register. In order to provide these functions without exposing the user to complexities of the Elan registers we have provided a set of BIOS extensions which will allow users to perform the functions they need in a safe and simple fashion.

Functions provided by the GCAT486 BIOS call include these, as well as others:

- Accessing the A/D converter
- Accessing the serial EEPROM
- Controlling the Elan's GPIO pins
- Accessing the Utility Register
- Making A/D conversions
- Kicking the watchdog timer
- Controlling the LCD Virtual Screen
- Accessing the Elan processor's Chip Setup and Control (CSC) Registers

For a full description of the GCAT486 BIOS call, see the GCAT486 Utility Disks. As well as providing a full description of the BIOS call and its parameters, the Utility Disks contain practical examples of programs which make use of the BIOS call – the A/D converter program and watchdog timer program in particular. This section in the Technical Reference Manual provides an overview.

6.11.2 BIOS Call Parameters

The functions can be accessed by making a software interrupt call. The BIOS will then perform the required function for the user.

The interrupt called is INT 15h.

The AX register must always contain 0BF00h.

The BX register must always contain 04754h (ASCII "GT").

The function required is specified in the CH register.

Parameters are passed in the CL and DX registers.

Results are returned in the AL and DX registers.

A successful result is indicated by the carry flag being cleared. An unsuccessful result is indicated by the carry flag being set.

An example of a software interrupt being called from assembler code follows. This is extracted from the PANL.ASM program in the LCD directory of the GCAT486 Utility Disks. It pans the screen left by one character width in virtual mode. It actually makes two calls – one to get the current screen position and the other to change the position.

```
mov   ax, 0BF00h ; Identifies GCAT486 BIOS call
mov   bx, 4754h  ; Identifies GCAT486 BIOS call
mov   cx, 1400h  ; Function = GCAT486GetVirScrnPos
int   15h        ; on return dl = column

cmp   dl, 0
jz    no_need    ; if dl=0 then can't pan further left
dec   dl         ; move one left

mov   ax, 0Bf00h
mov   bx, 4754h
mov   cx, 1500h  ; Function = GCAT486SetVirScrnPos
int   15h
```

The next example shows the software interrupt being called from a Borland Turbo C program. This is a function call which can be made to kick the watchdog timer. It is taken from the GC4WDOG.C program in the UTILS directory of the GCAT486 Utility Disks.

```
void GCAT486_Watchdog(int Command)
{
   union REGS regs;
   regs.h.ah = 0xBF;    // AX must always be set to 0xBF00
   regs.h.al = 0x00;
   regs.h.bh = 0x47;    // BX must always be set to 0x4754
   regs.h.bl = 0x54;
   regs.h.dl = Command; // Command to set 1.4s timeout
   regs.h.ch = 0x0A;    // Select INT15 function 0Ah
   int86(0x15, &regs, &regs);  // Perform INT 15 interrupt
}
```

6.11.3 Overview of Function calls

The functions are summarised in Table 9. The functions are liable to change and users should refer to the GCAT486 Utility Disks for up to date information.

At the time of writing not all of these functions have yet been implemented. These include the high-level functions to control the Vee generator. Accesses to these functions should (for the time being) be performed by functions 0 to 7. However, the higher level functions will be implemented in due course. Some functions have been included for DSP Design's internal development program and may be omitted in later versions. These calls are identified below and should not be used.

CH Value	Function Name	Description
0	GCAT486InitUtil	Clears the Utility Register
1	GCAT486ReadUtil	Reads a bit from the Utility register
2	GCAT486WriteUtil	Writes a bit to the Utility Register
3	GCAT486GPIOInit	Initialises Elan GPIO Pins
4	GCAT486GPIOGetDirection	Reads direction of an Elan GPIO Pin
5	GCAT486GPIOSetDirection	Sets the direction of an Elan GPIO Pin
6	GCAT486GPIORead	Reads current value of an Elan GPIO Pin
7	GCAT486GPIOWrite	Writes to an Elan GPIO Pin
8	GCAT486ReadEEPROMStatus	Reads EEPROM status
9	GCAT486ReadEEPROMData	Reads EEPROM byte
0Ah	GCAT486WriteEEPROMCmd	Writes an EEPROM command
0Bh	GCAT486WriteEEPROMData	Writes an EEPROM data byte
0Ch	GCAT486A2Dstart	Start A/D conversion
0Dh	GCAT486A2Dread	Read A/D data
0Eh	GCAT486VeeReset	Reset Vee Generator to mid-point
0Fh	GCAT486VeeInc	Increment Vee voltage gen.
10h	GCAT486VeeDec	Decrement Vee Voltage Generator
11h	GCAT486VeeSet	Set Vee generator to a level
12h	GCAT486GetCSC	Reads Elan CSC register
13h	GCAT486SetCSC	Writes Elan CSC register
14h	GCAT486GetVirScrnPos	Gets virtual scrn position (pan position)
15h	GCAT486SetVirScrnPos	Sets virtual screen position (pans)
16h	GCAT486SetVirScrnMod	Sets virtual screen mode
17h	GCAT486GetScrnSize	Gets Logical or Physical Screen size
18h	GCAT486FlashLights	Flashes port 80h LEDs (for debug only)
19h	GCAT486KickWatchdog	Kicks Watchdog Timer
1Ah	GCAT486ReadShadow	Read GPIO Shadow Register (for debug)
1Bh	GCAT486WriteShadow	Write GPIO Shadow Register (for debug)
1Ch	GCAT486FillStack	Fills Stack with n words (for debug only)

TABLE 9 - GCAT486 BIOS INTERRUPT CALLS

6.12 PICOCARD PC CARD SOFTWARE

The GCAT486 is provided with PC Card (PCMCIA) support software, which can be found on the GCAT486 Utilities Disks. This is the PicoCard software from Phoenix Technologies, and consists primarily of Card and Socket Services, and device drivers for different PC card types.

The PicoCard software is required when using the GCAT486P2 PC Card adapter. Note that Compact Flash cards are software compatible with PC Cards, and so this section applies to Compact Flash cards plugged into the Compact Flash socket on the GCAT486.

PicoCard software is loaded by entries in the CONFIG.SYS file as ROM-DOS or MS-DOS boots. The required drivers include Socket Services (which provides the hardware-specific software), Card Services (which manages the sockets) and one or more device drivers, which are selected depending on what PC Cards are to be installed. A PCM.INI file provides additional information to the various drivers, and it must also be present on your boot disk.

Principle drivers are the PCMATA.SYS, which supports ATA (IDE) hard disk drives, and PCMSCD for I/O cards such as modems.

The GCAT486 Utilities Disk includes all of these drivers, a sample CONFIG.SYS file, further explanatory notes, and a PicoCard User's Manual.

In a typical system ROM-DOS would boot from the Flash File System, and a CONFIG.SYS file on the Flash disk would then load the appropriate drivers for the GCAT486P2 (or Compact Flash cards).

7 POWER MANAGEMENT

The GCAT486 includes sophisticated power management hardware and software, which allows the power consumption of the GCAT486 to be reduced at times when the full performance of the board is not required. This can extend battery life in battery-operated systems and allow for cooler operation, and thus greater product reliability.

The BIOS can manage power autonomously, without intervention from higher levels of software. It is also compliant with the Advanced Power Management (APM) specification, version 1.2, which can allow APM-aware applications and operating systems to influence the power management of the GCAT486.

The BIOS default is for the power management to be disabled. Users who do not need power management can ignore this section. Users who do need to save power or to reduce heat should understand this section, and make appropriate settings in the BIOS Setup program.

7.1 OVERVIEW OF POWER MANAGEMENT

The power management on the GCAT486 relies on a combination of hardware within the Elan processor chip, hardware control of the peripheral functions on the GCAT486, and power management software.

The way the power management normally operates is as follows.

The user chooses a normal processor clock speed, and determines which peripheral functions are switched on in normal operation. From that point on, hardware within the Elan checks to see whether the computer is doing useful work (as determined by monitoring interrupts, accesses to peripheral functions and so on.) Activities that indicate that the processor is busy constantly reset hardware timers within the Elan. Unless these timers time-out the, Elan processor is kept at the selected speed, and the selected peripherals remain powered on.

However, during periods of inactivity (while the computer is waiting for user input for example) the activity timers count down and eventually time-out. At this point the GCAT486 is switched into a lower power mode. (The timers force a System Management Interrupt, or SMI, and the SMI code is responsible for switching to a lower power mode). As longer periods of inactivity occur the GCAT486 is switched into lower and lower power modes. At certain points various peripherals can be switched off, and eventually the processor itself is switched off.

The ultimate stage is reached when the processor and most of the peripherals are switched off. At this point the GCAT486 may draw as little as 800uA from the +3.3V power supply.

At any point there are a variety of activities that will cause the GCAT486 to switch back to a higher level of operation. To the user the switch is usually imperceptible.

7.2 ELAN POWER MANAGEMENT FEATURES

The Elan processor has been designed with a wealth of power saving features. The features are to a large extent programmable - they can be invoked in one of a number of ways under software control. Some of these features are described here.

The Elan can be thought of as a 486 processor, or CPU, surrounded by peripherals (serial port, LCD controller, interrupt controllers etc). The CPU can be set to execute instructions at a variety of clock speeds. The higher the clock speed the higher the power consumption, and vice versa. The clock can be stopped entirely, so that no instructions are executed. At this point the CPU draws almost no current. Other elements of the Elan can still be operational at this stage - in particular the power management circuitry stays operating, waiting to bring the CPU back to life by starting its clock.

The CPU runs at several clock speeds. In “High-Speed” mode the CPU can run at 33MHz, 16MHz or 8MHz - these frequencies being software selectable. In “Hyper-Speed” mode the 33MHz clock is doubled (or tripled) to 66MHz (or 100MHz) by a phase locked loop (PLL) clock multiplier. This mode gives the highest performance but also the highest power consumption. (Note that the GCAT486 is not designed to run at 100MHz, since it is fitted with a 66MHz processor as standard, and reliable operation at this frequency cannot be guaranteed with the 66MHz processor).

Then there is “Low-Speed” mode - programmable as 8MHz, 4MHz, 2MHz or 1MHz. This mode is suitable when not much processing is required, but the CPU must not be shut down entirely.

Then there is “Standby” mode and “Suspend” mode. In these modes the CPU clock is stopped entirely. The main difference between the two modes is that normally the Elan’s phase locked loop clock synthesisers are switched off in Suspend mode for lowest power consumption. When leaving Suspend mode the PLLs must be restarted, which takes a little time. Thus it takes longer to leave Suspend mode for normal operation than it does to leave Standby mode.

Lastly there is “Temporary Low-Speed” mode. On occurrence of certain activities the CPU can be taken from Standby mode to Temporary Low-Speed mode in order to execute a relatively small number of instructions, at a low clock rate, before dropping back to Standby mode. In the case of the GCAT486, Temporary Low-Speed mode is used to service the timer interrupt when it occurs, thus allowing the GCAT486 to keep track of the DOS time and date, and other routines which may be linked to the timer.

In Suspend mode the timer interrupt does not occur, and so the time and data will remain frozen for the duration of the suspended period. It is up to the user to update the time and date (by performing a BIOS or operating system call) on return from Suspend.

Other Elan features support power management. There are several timers, with programmable time-out periods. If enabled, the expiry of a certain timer will cause the Elan to switch to a lower power mode, or will cause a System Management Interrupt (SMI, see below). The timers are reset to their maximum count if various activities are detected by the Elan. These activities, which are programmable, include interrupts and software accesses to selected memory or I/O addresses. While these activities are occurring the timer cannot time out, and the CPU stays at its current clock speed.

Finally, the internal peripheral functions of the Elan can be shut down when not required, to save power.

The System Management Interrupt, or SMI, is a very high priority interrupt. It is available to allow power management hardware to interrupt the processor in order to request changes to the power management regime. In the case of the GCAT486, an SMI is generated when the activity timers time out, and when certain other hardware activities are detected. It is the SMI handling code which forces a switch to a different power state.

While in Suspend state the DRAM is refreshed by timing circuitry driven by the 32kHz clock. This allows other clocks internal to the Elan to be turned off. The 32kHz clock also provides timing for the power management timers and an internal state machine within the Elan processor.

7.3 PERIPHERAL POWER MANAGEMENT FEATURES

Most of the peripherals on the GCAT486 can be placed into a low power mode by a combination of hardware and software. The Setup program in the BIOS allows many peripherals to be switched off permanently, or selectively, as the GCAT486 enters either Standby or Suspend modes.

The COM1 UART is contained within the Elan chip itself, and can be disabled by software. Other sections of the Elan circuitry will be placed into low power modes as the Elan enters standby or suspend modes.

The on-board LCD controller can be shut down under software control, and automatically shuts down the Vee and VLCD power supplies when it does so.

Key to much of the power saving in the peripheral devices is the Utility Register. Several of the eight bits in this port are used to shut down peripheral hardware. These are described below, and also in section 3.12.

Two signals can be used to shut down the RS-232 and RS-485 transceivers on the serial ports. One signal (/COMMOFF) shuts down the transceivers. Another signal, FORCEON places the RS-232 transceivers in an “auto-shutdown” mode (see section 3.6.3).

A signal /ADCOFF shuts down the analog to digital converter and the temperature sensor.

A signal POWER_IRDA shuts down the IrDA transceiver.

7.4 DETAILED OPERATION

The Setup program includes three main menus that influence power consumption.

The first, the Advanced/Integrated Peripherals menu, allows unused peripherals to be turned off permanently. With the peripheral switched off in this menu the BIOS places the device in the lowest possible power state. Its I/O addresses and interrupt become available for other devices on the PC/104 bus. Once off the peripheral remains off, and is not dynamically controlled by the power management process.

For technical reasons the LCD display controller must be disabled in the second menu, which is the Main menu, under the Video System heading.

The third menu, the Power menu, defines the dynamic power saving operation.

In the Power menu, the Power Savings item allows dynamic power management to be switched off, or placed in one of two pre-configured modes (termed Maximum Performance and Maximum Power Savings), or customised. The pre-configured and customised modes enable a number of timers. In the customised mode the periods of these timers can be adjusted.

These timers define the amount of time that elapses before the GCAT486 is switched into the next lowest power mode, in the absence of activities that act to reset the timers. For example, in the “Maximum Power Saving” setting, assuming that the computer is running DOS and waiting for user input from the keyboard, the following will occur.

One second after the last keyboard activity the GCAT486 will switch from Hyper-Speed mode to High-Speed (assuming that it has been operating at Hyper-speed - 66MHz or 100MHz). One second later it will switch from High-Speed mode to Low-Speed mode. One minute later it will switch into Standby mode (the CPU clock is stopped except to service the timer interrupt). Finally, two minutes later, the GCAT486 will switch into Suspend mode (not even the timer interrupt is serviced).

Note that the GCAT486 will only be in the Hyper-Speed mode if the CPU Clock has been set to 66MHz (or 100MHz) in the Advanced/Advanced Chipset Control menu. Otherwise the highest speed mode will be the High-Speed mode.

If one of the timers is set to “off” then the timer will never time out, and the next lowest state will not be entered. For example, if the Low Speed timer is set to “off” the GCAT486 will power down to the High-Speed mode, but will not enter the Low-Speed mode, nor will it enter the lower power modes: Standby mode and Suspend mode.

Table 10 lists the power modes and describes the activities in each state.

The menu called Device Power Down allows the user to determine which peripherals are switched off when the GCAT486 enters Standby mode, and which are switched off when the GCAT486 enters Suspend mode.

Certain activities can cause the GCAT486 to switch from one mode to another. These activities are such things as interrupts, software accesses to peripheral I/O locations and inputs on some I/O signals.

Some activities cause the GCAT486 to remain in Hyper-Speed mode or High-Speed mode. Other activities can cause the GCAT486 to return to Hyper-Speed mode or High-Speed mode from the Low-Speed mode. Still other activities can cause the GCAT486 to return to Hyper-Speed mode or High-Speed mode from the Standby or Suspend states. Some of these activities are permanently selected by the BIOS, and will always cause a change of mode. Other activities can be selected by the Wakeup Activities menus to cause a change of mode. Table 11 lists activities that can cause state transitions in each mode.

MODE	CPU CLOCK	CPU ACTIVITY	PERIPHERAL ACTIVITY
Hyper-Speed	66MHz or 100MHz	CPU fully operational, at highest speed.	Peripherals are on.
High-Speed	33MHz or 16MHz or 8MHz	CPU fully operational, at relatively high speed.	Peripherals are on.
Low-Speed	8MHz or 4MHz or 2MHz or 1MHz	CPU fully operational, but processor speed is low.	Peripherals are on.
Standby	Stopped	CPU clock stopped, except to service timer interrupts. (Elan enters Temporary Low Speed mode to service the timer.)	Many peripherals can be shut down. These are selected by the Setup program.
Suspend	Stopped	CPU clock stopped, PLL synthesisers stopped. Timer interrupt not serviced.	Many peripherals can be shut down. These are selected by the Setup program.
Temporary Low-Speed	8MHz	Elan enters this state on a timer interrupt. It remains in this state for a fixed time before returning to Standby.	Same as for Standby mode.

TABLE 10 - POWER MODES

For example, the first entry in Table 11 shows that keyboard activity will always keep the GCAT486 in Hyper-Speed mode. Additional activities (hard and floppy disk activity, serial and parallel port activity) can be programmed to keep the GCAT486 in the Hyper-Speed mode. The additional modes are enabled using the Setup program's Power/Wakeup Activities High/Low Speed menu.

To use COM2 or COM3 to force a resume from standby the serial port must be programmed to generate an interrupt. It is the arrival of the interrupt that forces the resume. The programmable interrupt controller (PIC) must also be programmed to accept the interrupt, and the interrupt must be unmasked. COM1 activities include active edges on the RxD and RI pins as well as interrupts. Table 12 summarises serial port capabilities.

COM2 and COM3 cannot be used to force a wakeup from Suspend. This is because in Suspend mode the clocks to the UART are turned off, which prevents the UART from generating an interrupt.

It is possible to use an RTC alarm interrupt to force a resume from Standby or Suspend. This allows the user to set the alarm for some time in the next 24 hours, force a switch to Standby or Suspend, and then expect to resume again at the pre-arranged time. The programmable interrupt controller (PIC) must also be programmed to accept the interrupt, and the interrupt must be unmasked. Sample code on the GCAT486 Utilities Disk gives an example of how to do this.

Please read section 7.5 for important information on interrupts in Standby mode.

Where Table 11 refers to interrupts as wake-up activities, this excludes the timer interrupt, IRQ0, which is handled separately. Where Table 11 refers to accesses to various peripherals (disk, serial ports etc), this means software reads or writes to the I/O addresses associated with these peripherals.

A suspend/resume signal on the Elan processor can also be used to force entry into the Suspend state, and force a suspended system to return to high-speed mode. The SUS_RES signal is available on connectors J2 and J4. A de-bounced switch on the TCDEVPLUS drives this signal. The SUS_RES signal can be programmed to operate in a number of ways – these options are evident in the BIOS Setup program. For example, the SUS_RES signal can force a suspend, a resume or both, and can operate such that one logic level forces a suspend and the other a resume, or such that a pulse forces a suspend and another pulse forces a resume. (At the time of writing the BIOS does not yet support the SUS_RES signal.)

The XT keyboard is a special case. This is because the Elan's XT keyboard controller circuitry requires the Elan's clocks to be running in order to operate correctly. These clocks, however, are switched off in Standby and Suspend states, thus disabling the keyboard controller. Thus in Standby or Suspend modes the keyboard cannot be used to resume the GCAT486. (In Standby the clocks are switched on briefly every time the DOS timer interrupt occurs; the Elan enters Temporary Low Speed mode. This means that the keyboard controller is enabled from time to time in Standby mode, and so will appear to respond to a small proportion of key presses.)

Users should be aware that in Suspend mode the timer interrupt is not serviced, which will have an effect on any software which expects a regular timer tick. In particular, the ROM-DOS time will appear to be frozen while the GCAT486 is in Suspend.

In Standby mode the timer interrupt is regularly serviced, so the DOS time and date is updated. Note that in the case of Standby, after the timer interrupt has been serviced control will be returned to the background program, until the Elan's clock turns off again. Thus the background program will continue to execute, albeit very slowly.

CURRENT MODE	NEXT MODE	ACTIVITY CAUSING CHANGE (ALWAYS)	ACTIVITY CAUSING CHANGE (OPTIONAL)
Hyper-Speed	Hyper-Speed	Keyboard activity will keep Elan in this mode.	Activities enabled in Wakeup Activities High/Low Speed menu: disk drives, COM1, COM2 and printer activity.
	High-Speed	None.	High Speed Timer times out.
	Standby	APM Standby request	None.
	Suspend	APM Suspend request	None.
High-Speed	Hyper-Speed if enabled, else High-Speed.	Keyboard activity.	Events enabled in Wakeup Activities High/Low Speed menu: disk drives, COM1, COM2 and printer activity.
	Low-Speed	None.	Low Speed Timer times out.
	Standby	APM Standby request	None.
	Suspend	APM Suspend request	None.
Low-Speed	Hyper-Speed if enabled, else High-Speed.	Keyboard activity.	Activities enabled in Wakeup Activities High/Low Speed menu: disk drives, COM1, COM2 and printer activity.
	Standby	APM Standby request	Standby Timer times out.
	Suspend	APM Suspend request	None
Standby	Hyper-Speed if enabled, else High-Speed.	Keyboard activity.	Activities enabled in Wakeup Activities Standby/Suspend Speed menu: COM1, COM2 activity.
	Suspend	None.	Suspend Timer times out.
	Temporary Low-Speed	Timer Interrupt (IRQ0)	None.
Suspend	Hyper-Speed if enabled, else High-Speed.	Keyboard activity.	Activities enabled in Wakeup Activities Standby/Suspend Speed menu: COM1 or RTC activity.
Temporary Low-Speed	Standby	Timer times out.	None

TABLE 11 - ACTIVITIES WHICH CAUSE A MODE CHANGE

Table 12 summarises the abilities of the three serial ports to wake up the GCAT486 from Standby or Suspend modes. Users who need to use the serial ports to wake up the GCAT486 will need to study this table and plan the use of the three serial ports to match their system requirements.

CURRENT MODE	COM1	COM2	COM3
Standby	Program accesses COM1 I/O addresses. Interrupt from COM1 (if interrupt is enabled by software). Signals on RI or RxD pins (if enabled by Setup Wakeup Activities menu).	Program accesses COM2 I/O addresses. Interrupt from COM2 (if interrupt is enabled by software).	Interrupt from COM3 (if interrupt is enabled by software). See section 7.5 for a special warning concerning interrupts in Standby Mode.
Suspend	Interrupt from COM1 (if interrupt is enabled by software). Signals on RI or RxD pins (if enabled by Setup Wakeup Activities menu).	Cannot cause a wakeup, since clocks are turned off.	Cannot cause a wakeup, since clocks are turned off.

TABLE 12 - SERIAL PORT ACTIVITIES CAUSING A WAKEUP

7.5 INTERRUPTS IN STANDBY MODE

Under some circumstances a problem can occur if interrupts occur while the GCAT486 is in Standby mode. The reason for this is explained first, and then a discussion of work-arounds is presented.

When in Standby mode, incoming interrupts will cause the Elan chip hardware to leave the Standby mode (clocks stopped) and enter High-Speed or Hyper-Speed mode. It is important that when this happens the power management software in the BIOS gets to know that the hardware has resumed execution, so it can switch back on peripheral hardware that may have been switched off, and perform other housekeeping tasks. The power management software is notified of the hardware resume by an SMI (System Management Interrupt) which is generated by some activity corresponding to the interrupt.

For example, when a key on the keyboard is pressed the resulting interrupt (IRQ1) switches the processor clock back on, and in due course the keyboard interrupt service routine accesses the I/O registers of the keyboard controller. It is this access to the keyboard controller registers that cause the SMI. The SMI in turn informs the power management software that the interrupt has occurred, and the power management software then synchronises itself with the hardware - i.e. it is notified that the Elan hardware is now in High-Speed or Hyper-Speed mode.

The same principles apply to COM1 and COM2 serial port activity (IRQ4 and IRQ3). (These principles would apply to the printer, floppy disk and IDE disk drive, but it is difficult to envisage circumstances where these devices would spontaneously

generate interrupts while the GCAT486 is in Standby mode). Note that it is the I/O access within the interrupt service routine that causes the SMI.

There is potentially a problem with all other interrupts however. The interrupt will cause the processor clock to switch on, and software execution will resume. However, no SMI will occur and so the power management software is not informed of this transition, and does not switch back on peripherals, for example. In other words, the hardware and software get out of sync.

This is potentially dangerous and must not be allowed to occur.

Possible interrupts that could cause problems are the COM3 serial port and any interrupts from users' hardware.

A number of solutions are possible.

- Ensure at the system design level that interrupts that do not cause SMIs do not occur.

- Do not use Standby mode. Prevent the BIOS from automatically switching you into Standby mode by setting the Standby Timeout to Off in the Setup program. If you are using APM calls from within your application then switch directly to Suspend mode, avoiding Standby mode. (The problem does not occur in Suspend mode).

- If you are using APM calls from within your own application to switch to Standby, then disable the interrupts for the devices which do not cause SMIs before switching to Standby.

- If you have written your own interrupt service routine then add code within your interrupt service routine to access an I/O location known to cause an SMI. The I/O access we recommend is a read from the printer data port. This is harmless, and will force an SMI.

- If you have not written your own interrupt service routine then you may be able to chain interrupt service routines. This involves forcing the processor to execute your own small interrupt service routine before moving onto the real interrupt service routine. Your own code needs to include the read from the printer port (or other I/O access that causes an SMI).

Users should be confident that they understand what their operating system does with interrupt service routines. ROM-DOS is simple and predictable, but many operating systems will add layers of code which virtualise the interrupts, preventing the users from directly controlling the interrupt service process.

7.6 APM SOFTWARE INTERFACE

The GCAT486 power management can be controlled by application software. This is done by use of the Advanced Power Management (APM) interface. APM code is included in the BIOS. Application programs can communicate with the APM code by making BIOS calls. This allows the application to move the GCAT486 from one power mode to another.

The APM specification can be obtained at:

http://www.microsoft.com/hwdev/busbios/amp_12.htm

A sample program, together with source code, is included on the GCAT486 Utilities Disks showing how to force the GCAT486 into Standby or Suspend from within an application program. This code is in the UTILS directory.

Note that this sample program can be run from ROM-DOS, but not from more sophisticated operating systems that may include their own power management drivers. As can be seen from the APM specification, the proper way for an application to control power management is through a driver, which in turn communicates with other applications that may also be requesting power management control, and with the operating system.

In simple embedded applications where the operating system is not controlling power management, and where there are no other applications running, it may be acceptable for the application to make calls directly to the APM in the BIOS. The GCAT486 Utilities Disks contain further discussion of some limitations of this approach.

Users should be aware that if the application requests the BIOS to enter Standby mode, this will not occur immediately. Some code following the APM BIOS call will be executed before the Elan's clock switches off. Furthermore, the user's code will continue to be executed, little by little, every time the timer interrupt occurs. A call to enter Suspend mode, however, switches off the processor's clock almost immediately, and the next instruction following the APM BIOS call will not be executed until the GCAT486 has resumed normal operation.

7.7 POWER MANAGEMENT OF PC CARDS

Power management of the PC Cards is a special case. The GCAT486P2 circuitry has the ability to remove power from either or both of the PC Card slots during standby or suspend, which can produce considerable power savings in battery operated systems.

However, it is essential that power is sequenced in an intelligent fashion, as PC Card drivers must participate in the process, in particular so that they may save the state of the cards before power is removed from them, and restore the state afterwards. Otherwise the card could be powered down and back on again, with all of its registers set to the power-on reset state.

In order for this power management to occur, the MS-DOS POWER.EXE APM driver must be installed. This driver acts as an intermediary between the APM part of the BIOS and the device drivers for each of the PC Cards. A sample CONFIG.SYS file is present on the GCAT486 Utilities disk, showing how to load the POWER.EXE program and power manage the PC Cards.

Unfortunately, the ROM-DOS POWER.EXE does not work correctly for this function and cannot be used. Although MS-DOS POWER.EXE appears to work with both MS-DOS and ROM-DOS, users should ensure that they do not use MS-DOS POWER.EXE with ROM-DOS, as this is likely to violate Microsoft’s license terms.

7.8 POWER CONSUMPTION MEASUREMENTS

The power consumption of the GCAT486 depends mainly on the speed of the processor clock, and which peripherals are powered on. The processor clock speed can be fixed using the Setup program, and the power management software can vary the processor clock dynamically. The peripherals can be powered on or off permanently using the Setup program, or dynamically under the control of the power management software.

There are other factors that also affect the power consumption. The program being executed will affect power consumption - some instruction sequences cause the processor and memory to draw more current than other sequences. And of course peripheral devices and external circuitry will also draw current, and will influence the current taken by the GCAT486 itself.

The figures given in this section are therefore only “typical” figures - measurements in real-world applications are likely to vary somewhat.

The measurements given here were made with a GCAT486 running in stand-alone mode (not plugged into a development system). Unless otherwise noted the configuration was as follows. Two megabytes of DRAM and 2M bytes of flash memory were fitted. The COM1, COM2 and COM3 UARTs enabled and the RS-232 transceivers were on. The A/D converter and IrDA transceiver were off. No keyboard was used when the measurements were made. One variable was the LCD – a quarter VGA (320 x 240) mono LCD was either fitted or not, as is explained below.

The GCAT486 was allowed to boot MS-DOS from the Flash File System, and measurements were taken with the computer sitting at the C: prompt waiting for keyboard input. The power management software was then allowed to switch the GCAT486 into progressively lower power states, and power measurements were taken.

In addition, peripherals were switched off, either permanently or dynamically, and this allowed us to determine approximately the power consumption of each of the peripheral devices. Note that, with the exceptions of the LCD, no peripherals were connected. It is possible that power consumption could vary if real peripherals were connected to the GCAT486. For example, an RS-232 transceiver is likely to draw more current if it is connected to a peripheral than if it is unused.

Table 13 gives the current consumption for the GCAT486 in milliamps, in a number of power states. For power consumption in milliwatts, multiply the current figure by 3.3V. The figures are typical measurements, for the most part rounded to the nearest 5mA.

The three right-hand columns show consumption with and without the LCD controller in action. The first of these columns is the total consumption of the GCAT486 and a quarter VGA mono LCD – the GCAT486 is providing both logic and Vee power to the LCD. The next column is with the LCD disconnected, but with the LCD controller still active, which therefore separates the current consumed by the GCAT486 from that consumed by the LCD. The third column is with the LCD controller within the Elan processor switched off. The LCD is switched off in suspend mode. The LCD can thus be seen to add about 30mA and the LCD controller sub-system within the Elan about 15mA (taking the rounding errors into account). The contribution of the LCD thus

remains independent of clock speed and so becomes an increasing proportion of total power as the processor speed reduces.

In standby mode the processor clock is stopped for most of the time, but the system enters temporary low speed mode to service the timer interrupt, at an 8MHz clock speed.

In suspend mode the bottom row is the consumption with all peripherals off. The row above is with the RS-232 transceivers switched on.

MODE	CLOCK SPEED	LCD CONT. ON, WITH LCD	LCD CONT. ON, NO LCD	LCD CONT. OFF, NO LCD
Hyper-Speed	100MHz	620mA	590mA	580mA
	66MHz	470mA	440mA	430mA
High-Speed	33MHz	285mA	260mA	245mA
	16MHz	175mA	145mA	135mA
	8MHz	125mA	95mA	80mA
Low Speed	8MHz	125mA	95mA	80mA
	4MHz	100mA	70mA	55mA
	2MHz	85mA	55mA	40mA
	1MHz	80mA	50mA	35mA
Standby	Stopped / 8MHz	65mA	35mA	22mA
Suspend	Stopped, RS232 on	1.8mA	1.8mA	1.8mA
	Stopped	0.8mA	0.8mA	0.8mA

TABLE 13 - GCAT486 CURRENT CONSUMPTION

Table 14 provides typical power consumption of each of the elements of the GCAT486 that may be independently enabled or disabled. It allows an estimate to be made of power consumption with a particular mix of peripherals. Figures are given in mA and mW.

ELEMENT	CURRENT CONSUMPTION	POWER CONSUMPTION
Elan and memory running at 33MHz	241mA	795mW
LCD Controller	13mA	43mW
LCD panel (QVGA)	28mA	92mW
COM2 & COM3 UARTs	<<1mA	<<1mW
RS232 Transceivers	1mA	3mW
A/D converter	1mA	3mW
IrDA transceiver	1mA	3mW
TOTAL	285mA	940mW

TABLE 14 - POWER CONSUMPTION OF GCAT486 ELEMENTS

8 MULTI-FUNCTION PINS

The Elan processor has many pins that can assume two or even three functions, depending on the setting of internal configuration registers. The GCAT486 assigns default functions to these pins, but the user may change many of these pins to suit the application.

8.1 DEFAULT AND ALTERNATIVE FUNCTIONS

Table 15 below lists the groups of pins that may be assigned alternative functions on the GCAT486. Each group is controlled by a single bit (or field) within the Elan Pin Configuration Registers. Note that for some pins changing a bit in an Elan register will change the function of a single pin. In most cases however changing one bit will change the function of several pins.

The functions of the pins are normally set by the BIOS. Options in the BIOS Setup program allow the user to change the function of each group of pins. (At the time of writing the BIOS does not yet allow alternative functions to be programmed for all of the multi-function pins.)

Table 15 describes the default function of the pins. This is the function that the BIOS will normally give to the pins. This use is the function that is of most use when the GCAT486 is plugged into the TCDEVPLUS Development System. You will note that in this case most of the pins are given ISA bus functions, or XT keyboard functions, or are left as general purpose I/O pins. The matrix keyboard is not selected by default. However, the PC Card functions are selected by default, since if the printer functions are selected this may interfere with the PC Card Slot B circuitry if a GCAT486P2 module is plugged in.

Appendix F gives a pin by pin description of the multi-function pins.

The pin names on the connectors given in Appendix E and F are names that reflect the default function. For example, a pin is called /IOCS16, reflecting its ISA bus use, rather than GPIO_CS5, which is its alternative function.

Note that there are some other multi-function pins which are not listed here or in Appendix F. These are pins which are performing a particular fixed task on the GCAT486, and whose function must not be changed.

GROUP	DEFAULT FUNCTION	ALTERNATIVE FUNCTIONS	ELAN REGISTER AND BIT
1	ISA Bus: /IOCS16	GPIO_CS5	38h[4]
2	ISA Bus: IOCHRDY	GPIO_CS6	38h[3]
3	ISA Bus: PIRQ1 (IRQ5)	GPIO_CS7	38h[2]
4	ISA Bus: PIRQ0 (IRQ3)	GPIO_CS8	38h[1]
5	ISA Bus: PDRQ0, /PDACK0, AEN, TC	GPIO_CS12 - 9	38h[0]
6	PC Card Slot B VPP, VCC Power Control	GPIO_18, GPIO_17, GPIO_16	39h[6]
7	PC Card Slot A VPP, VCC Power Control	GPIO_15, GPIO_14, GPIO_13	39h[5]
8	XT Keyboard	Matrix Keyboard Columns 0, 1	39h[3]
9	ISA Bus: /MEMCS16, /SBHE, BALE, PIRQ2 (IRQ12), PDRQ1, /PDACK1	Matrix Keyboard Rows 12 - 7	39h[2]
10	PC Card Slot B Control Signals	Printer Port Control and status, or GPIO_31 - 21	39h[1, 0]
11	ISA Bus: PIRQ7 – 3	Matrix Keyboard Columns 2 - 6	3Ah[1]

TABLE 15 - GROUPS OF MULTI-FUNCTION PINS

8.2 GENERAL PURPOSE I/O PINS

The Elan provides 32 pins that can be used for a variety of uses. These are the General Purpose I/O (GPIO) pins. All of them (except two) are multi-function pins as described in section 8.1, and therefore cannot be used as GPIO pins if their alternative function has been selected. Some others are performing particular fixed tasks on the GCAT486. Those remaining – as many as 25 - can be used as GPIO pins if required by the user.

Examples of the uses to which the GPIO pins can be put are:

- Digital inputs
- Digital outputs
- I/O address decode outputs
- Memory address decode outputs
- Output of an internal ROMCS2 address decoder.
- Signals that switch state when the Elan changes power management state.
- Wakeup activity inputs
- SMI and NMI interrupt inputs
- Programmable chip selects
- Power mode state indicators

The use of the GPIO pins is beyond the scope of this manual. Users should refer to AMD's Elan documentation to understand how to program the GPIO pins. Note that

the I/O address decoders are used by the BIOS for COM2 and COM3, and cannot be used to drive users' GPIO pins unless these serial ports are disabled.

Table 16 lists the uses to which the GPIO pins can be put. Those pins that are not on a connector have dedicated on-board functions. The remaining pins may be used as GPIO pins so long as they are not required for their other function. The GPIO pins have pull-up or pull-down resistors that operate when they are not driven as outputs. The table specifies whether they have pull-up or pull-down resistors.

Those multi-function pins which are in their GPIO mode may be used for user applications. This involves the operations of writing to a GPIO pin, reading from a GPIO pin and setting its direction as an input or an output. These functions are performed by a special GCAT486-specific BIOS call. This is documented in section 6.11, and on the GCAT486 Utility Disks.

PIN	FUNCTION	PULL-UP/DOWN RESISTOR	AVAILABLE ON CONNECTOR?
GPIO_CS0	Chip select for COM2 UART	p.u.	No
GPIO_CS1	Chip select for COM3 UART	p.u.	No
GPIO_CS2	Chip Select for Utility Register	p.u.	No
GPIO_CS3	Data input from A/D Converter	p.u.	No
GPIO_CS4	Reserved for BIOS use.	p.u.	No
GPIO_CS5	ISA Bus /IOCS16	p.u.	Yes
GPIO_CS6	ISA Bus IOCHRDY	p.u.	Yes
GPIO_CS7	ISA Bus PIRQ1	p.u.	Yes
GPIO_CS8	ISA Bus PIRQ0	p.u.	Yes
GPIO_CS9	ISA Bus TC	p.u.	Yes
GPIO_CS10	ISA Bus AEN	p.u.	Yes
GPIO_CS11	ISA Bus /PDACK0	p.u.	Yes
GPIO_CS12	ISA Bus PRDQ0	p.d.	Yes
GPIO_CS13	PC Card /PCMA_VCC	p.d.	Yes
GPIO_CS14	PC Card PCMA_VPP1	p.d.	Yes
GPIO_15	PC Card PCMA_VPP2	p.d.	Yes
GPIO_16	PC Card PCMB_VCC	p.d.	Yes
GPIO_17	PC Card PCMB_VPP1	p.d.	Yes
GPIO_18	PC Card PCMB_VPP2	p.d.	Yes
GPIO_19	Serial EEPROM /CS pin	p.u.	No
GPIO_20	Serial EEPROM Data I/O, and output to A/D converter.	p.u.	No
GPIO_21	Printer Port Data Latch, /PPDWE	p.u.	Yes
GPIO_22	Printer Port Output Enable, /PPOEN	p.u.	Yes
GPIO_23	Printer SLCT or PC Card WP_B	p.u.	Yes
GPIO_24	Printer BUSY or PC Card BVD2_B	p.u.	Yes – J2
GPIO_25	Printer /ACK or PC Card BVD1_B	p.u.	Yes – J2
GPIO_26	Printer PE or PC Card /RDY_B	p.u.	Yes – J2
GPIO_27	Printer /ERROR or PC Card /CD_B	p.u.	Yes – J2
GPIO_28	Printer /INIT or PC Card /REG_B	p.u.	Yes – J2
GPIO_29	Printer /SLCTIN or PC Card RST_B	p.u.	Yes – J2
GPIO_30	Printer /AFD or PC Card /MCEH_B	p.u.	Yes – J2
GPIO_31	Printer /STRB or PC Card /MCEL_B	p.u.	Yes

TABLE 16 - GPIO PINS

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APPENDIX A: SPECIFICATION

Product:	GCAT486
Description:	Very small, low power, single board PC compatible computer.
Processor:	AMD Elan SC400. Clock speed of 66MHz, maximum, with many lower clock speeds available for power savings. 100MHz processor available on special order.
DRAM:	2M or 8M bytes DRAM (EDO). 2M fitted as standard.
Flash Memory:	2M byte of AMD 29LV160 Flash memory. Options for 4M bytes of Flash memory.
Graphics:	LCD controller capable of driving mono and colour STN LCDs up to 640 x 480 pixels. Default BIOS support for 320 x 240 pixels.
Serial interface:	RS-232 (COM1, COM2 and COM3). RS-485 full-duplex or half-duplex option for COM2.
Printer port:	Centronics compatible (PRN). Bi-directional. EPP compatible. – requires external chips.
Keyboard port:	XT compatible.
Matrix Keypad:	Option for key matrix of up to 14 x 8 keys.
Speaker port:	PC compatible. Drives an external speaker.
Analog to Digital Converter:	Four-channel, 12-bits. External reference. 0V to +3.3V input range. Optionally connected to on-board temperature sensor.
Reset circuit:	Power supply monitor, ISA bus reset, watchdog timer and external reset switch capability.
Bus interface:	ISA V2.3 16-bit (on proprietary connectors).
Interrupts:	Standard PC and PC/AT interrupts are available for on-board peripherals or the ISA bus. Eight interrupts available: IRQ3, IRQ5, IRQ6, IRQ9, IRQ10, IRQ12, IRQ14, IRQ15.
DMA:	Standard PC and PC/AT DMA request and acknowledge pairs available on ISA bus. Two DMA channels are available; channel numbers are software-selectable. Multiple bus masters (using the /MASTER signal) are not supported.

Connectors:	I/O uses 44-way and 50-way 2mm pitch pin headers for ribbon cables. ISA bus, PCMCIA and I/O uses two 100-way Hirose FX8 connectors for connection to a motherboard.
Dimensions:	PCB – 2.55 inches * 3.4 inches, (64.8mm * 86.4mm). Maximum component height on the component side of the PCB is 6.0mm (cables not connected) and 11.5mm (2mm cables connected). Maximum height below the under side of the PCB is 2.7mm (3mm between boards when plugged into a motherboard).
Weight:	40g Approx.
Operating temperature:	0 - 70 degrees C.
Humidity:	10% - 90% non-condensing.
Power Supplies:	+3.3V only required. 300mA typ. (33MHz, all peripherals on) 60mA typ. (8MHz, LCD off) 800uA typ. (Suspended, all peripherals off) See section 7.6 for power consumption of other configurations.

APPENDIX B: GCAT486 SET-UP PROCEDURE.

This appendix describes solder link settings for the GCAT486 and also for the GCAT486P2.

The component placement diagrams in Appendix C may be of help in locating the solder links referred to in this appendix.

A number of functions can be configured with solder links on the GCAT486 board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers, as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced. Default settings are noted below.

B.1 GCAT486 SET-UP

LK1 Boot from Compact Flash Card

This link can be fitted to allow the GCAT486 to boot from a Compact Flash card. This feature has not yet been tested and should not be used. The link should not be fitted.

LK2 /BL2 Pin

This link determines the source of the Elan's /BL2 pin. This is a power management pin and at the time of writing there is no software support for it. It is linked 1 – 2 at the factory and should not be changed.

LK3 /BL1 Pin

This link determines the source of the Elan's /BL1 pin. This is a power management pin and at the time of writing there is no software support for it. It is fitted (linked 4 – 5) at the factory and should not be changed.

LK4 VCC_CPU Source

This link is used to connect the 3V3 and VCC_CPU power rails, as described in section 2.6.

VCC_CPU is connected to 3V3:	Fit link. (Default setting)
VCC_CPU is powered separately:	Omit link.

LK5 IrDA Series Resistor

This link allows shorts out the 10-ohm resistor in series with the IrDA transceiver power supply pin. It should be shorted if an alternative series resistor is fitted externally.

10-ohm resistor present on board:	Omit link (Default setting)
No resistor present on board:	Fit link.

LK6 A/D Converter Input ADC3

This link is used to connect the analog to digital converter input ADC3 to the on-board temperature sensor.

ADC3 is connected to on-board temperature sensor:	Install link (default setting)
ADC3 may be supplied externally:	Omit link.

LK7 COM2 RS-232/RS-485 Selection

This link is used to select whether COM2 is RS-232 or RS-485.

RS-232:	Link 1 - 2 (Default setting)
RS-485:	Link 2 - 3

LK8 Remote Bootstrap

This link needs to be set according to the location of the BIOS. It is normally only used in the manufacturing process.

BIOS is in the Flash memory:	Link 1 - 2. (Default setting)
BIOS is in off-board EPROM:	Link 2 - 3.

LK9 Flash Memory Pin 13

This pin may be used in the future to route the A22 address pin to an 8M byte Flash memory chip. At present it is not used and should not be connected.

LK10 LCD Voltage Selection

An on-board voltage generator produces a power supply for LCD panels. Both 3.3V and 5V supplies can be generated.

LCD uses 3.3V:	Link 1 – 2
LCD uses 5V:	Link 2 – 3 (Default setting)

LK11 A/D Converter Reference

This link is used to select the source of the VREF input voltage to the analog to digital converter.

VREF is supplied by on-board +3.3V: Link 1 - 2.
VREF is supplied from an external source: Link 2 - 3.
VREF is supplied by on-board +3.3V and +3.3V is taken out to external circuitry on VREF pin: Link 1, 2 and 3 (Default setting)

LK12 UART Divisor

This link may be used to select UART clock speeds at some point in the future, when alternative UART chip may be fitted. At present it has no function, and is left with no connection made.

B.2 GCAT486P2 SETUP

LK1 Slot B Enable

This link disables some Slot B circuitry for the GCAT486P1 (no Slot B). It is factory set and should not be changed.

GCAT486P1:	Link 2 – 3
GCAT486P2:	Link 1 – 2 (default setting)

LK2 Frame Grounding

This link routes the metal frame of the PC Card socket either to signal GND (0V) or to a chassis ground (for systems with a separate chassis ground). The chassis ground (if available) is connected to the GCAT486P2 through pin 1 of the three-way connector J3.

Use Signal Ground:	Link 1 – 2 (default setting)
Use chassis ground	Link 2 – 3

LK3 Slot B Enable

This link disables some more Slot B circuitry for the GCAT486P1 (no Slot B). It is factory set and should not be changed.

GCAT486P1:	Omit link
GCAT486P2:	Fit link (default setting)

LK4 Slot A Enable

This link disables some Slot A circuitry for a (hypothetical) version of the GCAT496P2 with no slot A. It is factory set and should not be changed.

GCAT486P2:	Fit link (default setting)

LK5 Slot B Power Supply

This link selects the power source for Slot B PC Card. Either the main 3.3V supply of the GCAT486 or an external +5V supply can be used. An external +5V supply is provided through the three-pin connector J3, and is required when using PC Cards which cannot operate from 3.3V. Pin 2 is the +5V pin and pin 3 is GND.

+3.3V supply:	Link 1 – 2 (default setting)
+5V supply	Link 2 – 3

LK6 Slot A Power Supply

This link selects the power source for Slot A PC Card. Either the main 3.3V supply of the GCAT486 or an external +5V supply can be used. An external +5V supply is provided through the three-pin connector J3, and is required when using PC Cards which cannot operate from 3.3V. Pin 2 is the +5V pin and pin 3 is GND.

+3.3V supply:	Link 1 – 2 (default setting)
+5V supply	Link 2 – 3

B.3 CUT TRACK ON REVISION B01 PCB

In Rev B01 PCBs the Compact Flash card detect signals and the GCAT486P2 card detect signal both drive the Elan's card detect pin, causing a conflict. In practise this is not noticeable, but it is bad form, and a track on the GCAT486 PCB should be cut to avoid this conflict if the GCAT486 is to be used with a GCAT486P2. Contact DSP Design if you intend using the GCAT486P2 with a Rev B01 GCAT486. The problem was removed with the Rev B02 PCB.

APPENDIX C: MECHANICAL DRAWINGS

The two component placement diagrams which follow (one for each side of the GCAT486) may be of help in locating the solder links referred to in Appendix B. The dimensioned drawings will be of assistance to users who need to design an enclosure, or who need to design a motherboard PCB onto which the GCAT486 will plug. The drawings are also included as Acrobat .PDF files on the GCAT486 Utility Disks.

(The diagrams are of the Rev B01 PCB, which differs only in some minor details from the Rev B02 version).

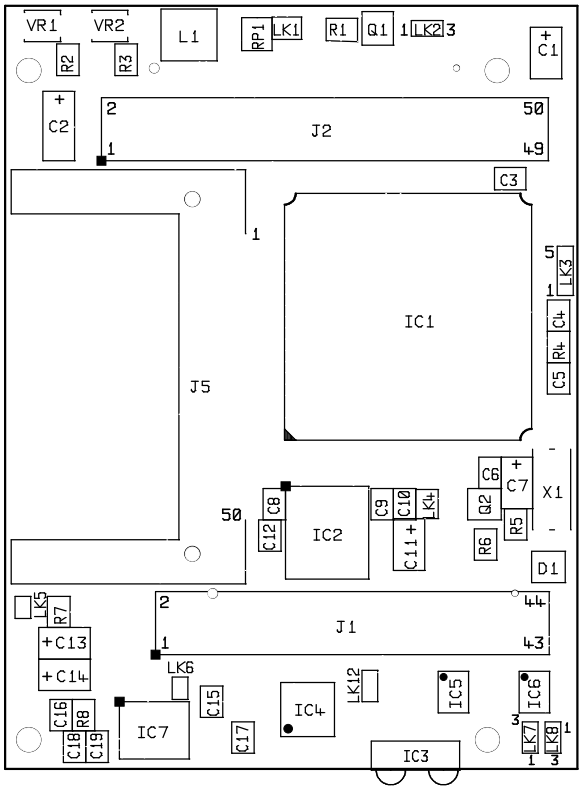


FIGURE C1 - TOP COMPONENT PLACEMENT DIAGRAM

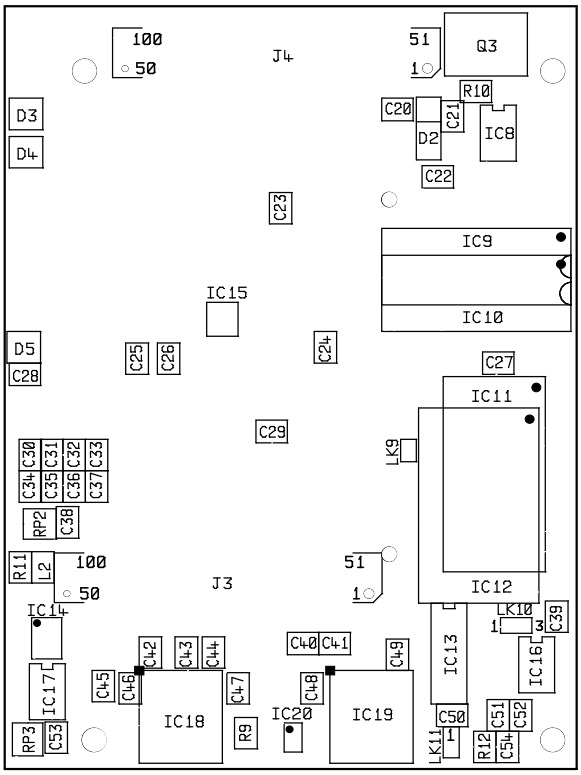
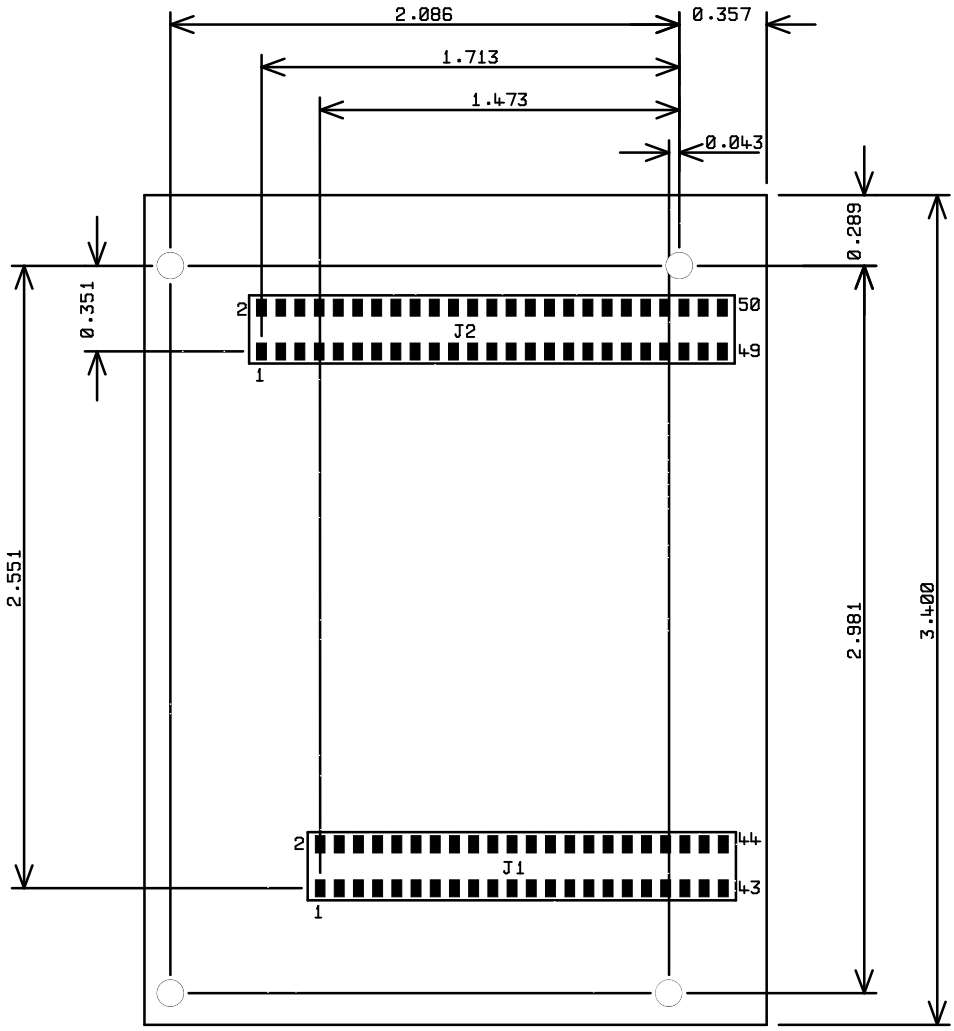


FIGURE C2 - BOTTOM COMPONENT PLACEMENT DIAGRAM

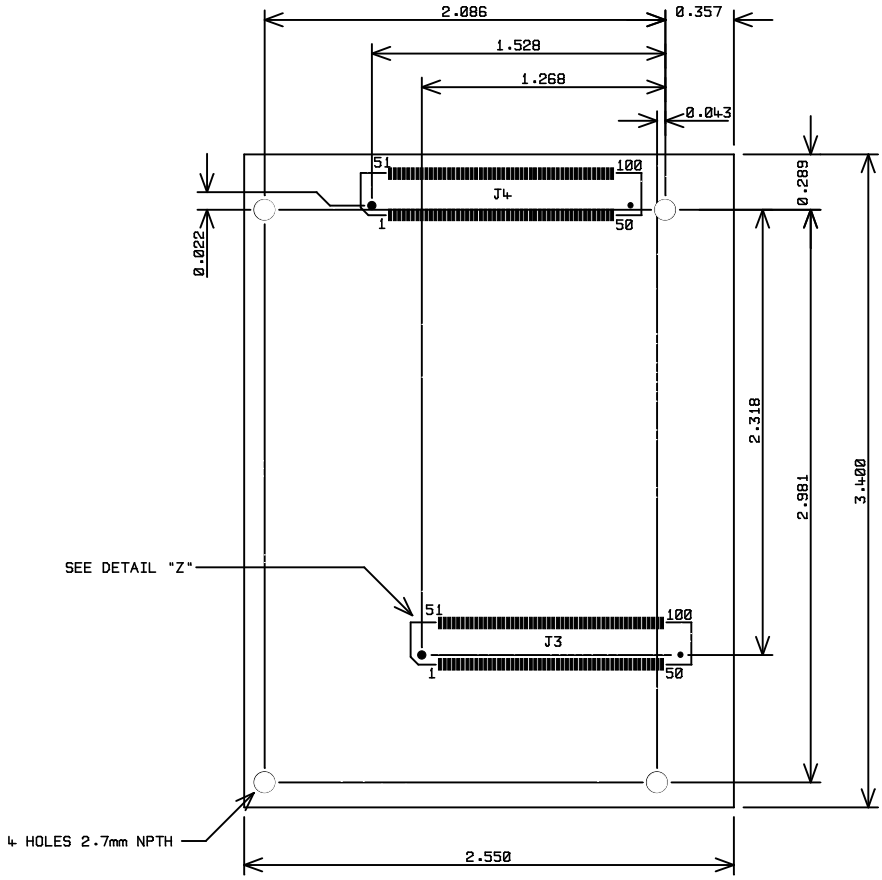


VIEW FROM PROCESSOR SIDE

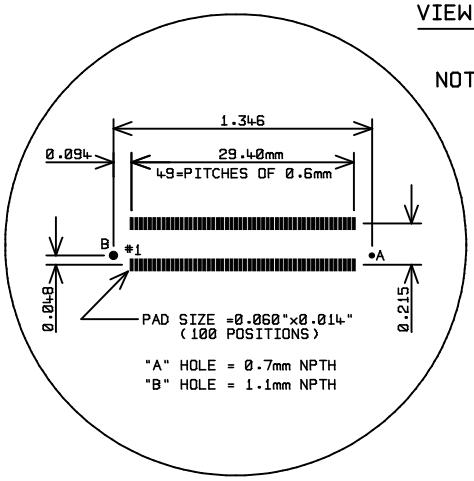
NOTES:-

1. J1 & J2 ARE MOUNTED ON PROCESSOR SIDE OF BOARD

FIGURE C3 - BOARD DIMENSIONS AND CONNECTOR POSITIONS



VIEW FROM PROCESSOR SIDE



DETAIL "Z"

2 POSITIONS

(FOOTPRINT OF J3 & J4 MATING HALF)

NOTES:-

1. J3 & J4 ARE MOUNTED ON UNDERSIDE OF BOARD
2. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE STATED

FIGURE C4 - MOTHERBOARD PCB LAYOUT DIMENSIONS

APPENDIX D: OPTIONS AND ORDERING INFORMATION

This Appendix lists some of the products related to the GCAT486. Note that as new products are being released all the time this list may not be complete. Contact DSP Design for a full price list.

D.1 BOARDS

Table D1 lists the GCAT486 boards that are available.

ITEM	DESCRIPTION
GCAT486	Standard GCAT486 processor board.
GCAT486P2	Two slot PC Card adapter board.
GCAT486P1	Single slot PC Card adapter board (Minimum order quantity may apply).

TABLE D1 - BOARDS

D.2 GCAT486 PROCESSOR SUPPORT PACK

The best way of starting a GCAT486 development project is to buy a GCAT486PAK, which is one of a family of “PAK” products. Each “PAK” product includes the processor itself, the TCDEVPLUS Development System board, a TPPSU power supply and a comprehensive set of manuals, disks, and cable assemblies optimized to that particular processor. The PAK products provide most customers with all that they need for their development process, but there are still other accessories which may be of use, and which will need to be ordered separately.

The contents of the GCAT486PAK product are defined in Table D2. The first five items in the table are common to all of the PAK products.

ITEM	DESCRIPTION
TCDEVPLUS	Development System
TPPSU	45W power supply
PSU-xxLEAD	Mains Power Lead for TPPSU (specify your country so we can provide the correct lead)
TRM-TCDEVPLUS	Technical Reference Manual
TCDEVPLUS-UTILS	Floppy disk containing software
GCAT486	Processor board
TRM-GCAT486	Technical Reference Manual
GCAT486-UTILS	Utility Disks
KBDATPS2	5-pin DIN to 6-pin mini-DIN adapter

TABLE D2 - CONTENTS OF THE GCAT486PAK

Note: Customers may also need to order a KBDXTAT if they do not have an XT keyboard. They may also want to order a GCAT486P2 and Compact Flash cards.

D.3 ACCESSORIES

Table D3 lists some or all of the following items may be of use during your development process. Some of the items are included in the GCAT486PAK product.

ITEM	DESCRIPTION
GCAT486PAK	Starter pack for GCAT486. See section D.3 for full details. The individual items in Table D3 can also be ordered separately.
GCAT486-UTILS	Set of floppy disks containing BIOSes and support software.
TRM-GCAT486	Technical Reference Manual for GCAT486.
TCDISK-6000	6G byte 2.5 inch IDE drive
EC586-IDECA	Cable to connect the TP300 to 2.5 inch IDE drives
IDE-3020	Cable to convert 2.5inch IDE connector to 3.5-inch IDE connector and vice-versa.
LCDQVGA	320 X 240 mono LCD and cable to plug into the TCDEVPLUS.
KBDXTAT	Cherry G81-1800-HAG (or G80-1000) XT/AT keyboard.
KBDATPS2	Adapter to allow 5-pin mini-DIN keyboard to plug into the 6-pin mini-DIN keyboard connector.

TABLE D3 - GCAT486 ACCESSORIES

D.4 COMPACT FLASH

The GCAT486 has a socket for Compact Flash memory cards, which can be used in place of IDE disk drives. Compact Flash cards are also a useful alternative to IDE drives and floppy disks during development. They are reasonably high capacity, and if you equip your PC with the CFREADER product you are able to transfer files between your development machine and the GCAT486. Compact Flash cards with larger capacities than those mentioned in Table D4 are also available. The CFREADER is a Compact Flash reader/writer unit that plugs into the printer port of a PC.

ITEM	DESCRIPTION
CF4M	4M byte Compact Flash memory card
CF8M	8M byte Compact Flash memory card
CF16M	16M byte Compact Flash memory card
CF32M	32M byte Compact Flash memory card
CF48M	48M byte Compact Flash memory card
CF80M	80M byte Compact Flash memory card
CF128M	128M byte Compact Flash memory card
CFREADER	Compact Flash reader/writer unit that plugs into the printer port of a PC.
CF100-EKIT	Ejector for the Compact Flash socket

TABLE D4 - COMPACT FLASH ACCESSORIES

APPENDIX E: CONNECTOR PIN ASSIGNMENTS

E.1 OVERVIEW OF CONNECTORS

J1 and J2 are the two ribbon cable connectors on the GCAT486. The connectors are on 2mm pitch, so takes 1mm pitch ribbon cable. J1 is a 44-way connector and J2 is a 50-way connector.

The ribbon cable connectors provide access to most peripherals which would be used in stand-alone configurations: keyboards, displays, serial ports, A/D converter, power supplies and some other signals.

Connectors J3 and J4 are 100-way pin connectors. They allow the GCAT486 to plug onto a motherboard, which can contain the user's circuitry. The connector on the GCAT486 is a Hirose FX8-100S-SV. The connector required on the motherboard is a Hirose FX8-100P-SV (3mm board spacing) or FX8-100P-SV1 (4mm board spacing). The signals on these connectors contain all of the signals on the ribbon cable connectors, plus signals required for PC Cards and ISA bus expansion.

All of the signals on the ribbon cable connectors are also present on the 100-way connectors, so if the GCAT486 is plugged into a motherboard there is no need to make use of the ribbon cable connectors.

Note that many of the pins on the Elan processor can be configured for two or even three alternative uses. For the most part, the signal names given below are the default uses for the signals. Appendix F and section 8 give alternative functions for these pins.

The pin numbering of the connectors is indicated by text on the PCB.

Pin assignments for the connectors are given below.

E.2 J1 44-WAY RIBBON CABLE CONNECTOR

PIN	SIGNAL	PERIPHERAL	PIN	SIGNAL	PERIPHERAL
1	3V3	Power	2	GND	Power
3	ADC0	A/D Converter	4	ADC1	A/D Converter
5	ADC2	A/D Converter	6	ADC3	A/D Converter
7	AGND	A/D Converter	8	VREF	A/D Converter
9	VIrDA	IrDA	10	SIROUT	IrDA
11	SIRIN	IrDA	12	GND	IrDA
13	DCD1	COM1	14	DSR1	COM1
15	RXD1	COM1	16	RTS1	COM1
17	TXD1	COM1	18	CTS1	COM1
19	DTR1	COM1	20	RI1	COM1
21	GND	COM1	22	DCD2	COM2
23	DSR2	COM2	24	RXD2	COM2
25	RTS2 *	COM2	26	TXD2 *	COM2
27	CTS2 *	COM2	28	DTR2 *	COM2
29	RI2	COM2	30	GND	COM2
31	DCD3	COM3	32	DSR3	COM3
33	RXD3	COM3	34	RTS3	COM3
35	TXD3	COM3	36	CTS3	COM3
37	DTR3	COM3	38	RI3	COM3
39	GND	COM3	40	/RESET	Reset Switch
41	GND	Power	42	3V3	Power
43	3V3	Speaker	44	SPKR	Speaker

*** Note**: See Table E2 for the function of these pins when COM2 operates as an RS485 port.

TABLE E1 - J1 44-WAY RIBBON CABLE PIN ASSIGNMENTS

RS-232 SIGNAL	RS485 SIGNAL	J1 PIN	J3 PIN
RTS2	RxD, non-inverting	25	83
TXD2	RxD, inverting	26	79
CTS2	TXD, non-inverting	27	85
DTR2	TXD, inverting	28	82

TABLE E2 - COM2 RS-485 PIN ASSIGNMENTS

E.3 J2 50-WAY RIBBON CABLE CONNECTOR

PIN	SIGNAL	PERIPHERAL	PIN	SIGNAL	PERIPHERAL
1	VEE	Graphical LCD	2	VO	Graphical LCD
3	GND	Graphical LCD	4	DOTCLK	Graphical LCD
5	VLCD	Graphical LCD	6	LP	Graphical LCD
7	FLM	Graphical LCD	8	M	Graphical LCD
9	LCDD7	Graphical LCD	10	LCDD6	Graphical LCD
11	LCDD5	Graphical LCD	12	LCDD4	Graphical LCD
13	LCDD3	Graphical LCD	14	LCDD2	Graphical LCD
15	LCDD1	Graphical LCD	16	LCDD0	Graphical LCD
17	BATT	Battery	18	GND	Battery
19	SUS_RES	Suspend Switch	20	KBDROW13	Key Matrix
21	KBDROW12 *	Key Matrix	22	KBDROW11 *	Key Matrix
23	KBDROW10 *	Key Matrix	24	KBDROW9 *	Key Matrix
25	KBDROW8 *	Key Matrix	26	KBDROW7 *	Key Matrix
27	KBDROW6	Key Matrix	28	KBDROW5	Key Matrix
29	KBDROW4	Key Matrix	30	KBDROW3	Key Matrix
31	KBDROW2	Key Matrix	32	KBDROW1	Key Matrix
33	KBDROW0	Key Matrix	34	KBDCOL7	Key Matrix
35	KBDCOL6 *	Key Matrix	36	KBDCOL5 *	Key Matrix
37	KBDCOL4 *	Key Matrix	38	KBDCOL3 *	Key Matrix
39	KBDCOL2 *	Key Matrix	40	KBDCOL0 *	Key Matrix
41	KBDCOL1 *	Key Matrix	42	GPIO_30 *	Alpha LCD
43	GPIO_29 *	Alpha LCD	44	GPIO_28 *	Alpha LCD
45	GPIO_27 *	Alpha LCD	46	GPIO_26 *	Alpha LCD
47	GPIO_25 *	Alpha LCD	48	GPIO_24 *	Alpha LCD
49	3V3	Alpha LCD	50	GND	Alpha LCD

* NOTE: These pins have multiple functions. The names given here represent the functions when the signals are connected to key matrix and alphanumeric LCD. These are not the default functions for these signals. See Appendix F for details of their alternative functions.

TABLE E3 - J2 50-WAY RIBBON CABLE PIN ASSIGNMENTS

E.4 J3 100-WAY INTER-BOARD CONNECTOR

PIN	SIGNAL	PERIPHERAL	PIN	SIGNAL	PERIPHERAL
1	AGND	A/D Converter	51	ADC1	A/D Converter
2	ADC0	A/D Converter	52	AGND	A/D Converter
3	AGND	A/D Converter	53	ADC3	A/D Converter
4	ADC2	A/D Converter	54	AGND	A/D Converter
5	AGND	A/D Converter	55	VREF	A/D Converter
6	VIRDA	IrDA	56	AGND	A/D Converter
7	3V3	Power	57	SIROUT	IrDA
8	SA21	ISA Bus	58	SD0	ISA Bus
9	GND	Power	59	SD4	ISA Bus
10	SIRIN	IrDA	60	SD8	ISA Bus
11	3V3	Power	61	SD6	ISA Bus
12	RTS1	COM1	62	SD3	ISA Bus
13	SD1	ISA Bus	63	SD5	ISA Bus
14	SD2	ISA Bus	64	DSR1	COM1
15	GND	Power	65	SD7	ISA Bus
16	TXD1	COM1	66	SD10	ISA Bus
17	CTS1	COM1	67	DCD1	COM1
18	RXD1	COM1	68	SD9	ISA Bus
19	PIRQ0 *	ISA Bus	69	3V3	Power
20	DTR1	COM1	70	RI1	COM1
21	DCD2	COM2	71	SD11	ISA Bus
22	GND	Power	72	SD12	ISA Bus
23	SA22	ISA Bus	73	SD13	ISA Bus
24	SA0	ISA Bus	74	/PCMWE	PC Card
25	SA1	ISA Bus	75	SD14	ISA Bus
26	RXD2	COM2	76	/REG_A	PC Card
27	SA2	ISA Bus	77	RDY_A	PC Card
28	GND	Power	78	/PCMOE	PC Card
29	TXD2	COM2	79	/CD_A	PC Card
30	DSR2	COM2	80	VCC_CPU	Power
31	3V3	Power	81	RST_A	PC Card
32	DTR2	COM2	82	VCC_CPU	Power
33	RTS2	COM2	83	BVD2_A	PC Card
34	GND	Power	84	WP_A	PC Card
35	CTS2	COM2	85	VCC_CPU	Power
36	/ROMRD	EPROM	86	/WAIT_AB	PC Card
37	RI2	COM2	87	WP_B *	PC Card
38	/IORD	ISA Bus	88	GND	Power
39	DSR3	COM3	89	VCC_CPU	Power
40	PIRQ1 *	ISA Bus	90	/MCEL_B *	PC Card
41	DCD3	COM3	91	BVD1_A	PC Card
42	RESETDRV	ISA Bus	92	/PPDWE *	Printer Control
43	/RESET	Reset Switch	93	SD15	ISA Bus
44	RXD3	COM3	94	/IOWR	ISA Bus
45	/ENFLASH	EPROM Control	95	ICDIR	PC Card
46	3V3	Power	96	SA25	ISA Bus
47	TXD3	COM3	97	RTS3	COM3
48	GND	Power	98	CTS3	COM3
49	DTR3	COM3	99	RI3	COM3
50	/ROMCS0	EPROM	100	SPKR	Speaker

* Note: These pins have multiple functions. For the most part, the names given here indicate the default functions. See Appendix F for details of their alternative functions.

TABLE E4 - J3 100-WAY INTER-BOARD CONNECTOR

E.5 J4 100-WAY INTER-BOARD CONNECTOR

PIN	SIGNAL	PERIPHERAL	PIN	SIGNAL	PERIPHERAL
1	VLCD	Graphics LCD	51	LP	Graphics LCD
2	GND	Graphics LCD	52	DOTCLK	Graphics LCD
3	VEE	Graphics LCD	53	/BL1	Power Management
4	FLM	Graphics LCD	54	VO	Graphics LCD
5	LCDD7	Graphics LCD	55	M	Graphics LCD
6	LCDD5	Graphics LCD	56	LCDD6	Graphics LCD
7	SA24	ISA Bus	57	LCDD4	Graphics LCD
8	LCDD3	Graphics LCD	58	LCDD2	Graphics LCD
9	LCDD1	Graphics LCD	59	LCDD0	Graphics LCD
10	SUS_RES	Suspend Switch	60	KBDROW13	Key Matrix
11	SA11	ISA Bus	61	/SBHE *	ISA Bus
12	SA13	ISA Bus	62	GND	Power
13	BATT	Battery	63	SA3	ISA Bus
14	BALE *	ISA Bus	64	PIRQ2 *	ISA Bus
15	SA16	ISA Bus	65	SA12	ISA Bus
16	PIRQ3 *	ISA Bus	66	/PDACK1 *	ISA Bus
17	SA15	ISA Bus	67	KBDROW5	Key Matrix
18	PDRQ1 *	ISA Bus	68	SA7	ISA Bus
19	/MEMCS16 *	ISA Bus	69	SA8	ISA Bus
20	KBDROW6	Key Matrix	70	3V3	Power
21	PIRQ7 *	ISA Bus	71	KBDROW1	Key Matrix
22	MA2	Boot Control	72	GND	Power
23	SA10	ISA Bus	73	SA5	ISA Bus
24	/ROMCS1	EPROM	74	KBDROW3	Key Matrix
25	KBDROW2	Key Matrix	75	/PCMA_VCC *	PC Card Power
26	GND	Power	76	SA6	ISA Bus
27	KBDROW0	Key Matrix	77	AEN *	ISA Bus
28	PCMB_VCC *	PC Card Power	78	KBDCOL7	Key Matrix
29	/ROMWR	EPROM	79	IOCHRDY *	ISA Bus
30	GND	Power	80	PCMA_VPP2 *	PC Card Power
31	KBDROW4	Key Matrix	81	PIRQ6 *	ISA Bus
32	3V3	Power	82	/IOCS16 *	ISA Bus
33	/MEMR	ISA Bus	83	TC *	ISA Bus
34	PIRQ5 *	ISA Bus	84	ATCLK	AT Keyboard
35	3V3	Power	85	PIRQ4 *	ISA Bus
36	PCMA_VPP1 *	PC Card Power	86	/PDACK0 *	ISA Bus
37	SA23	ISA Bus	87	XTCLK *	XT Keyboard
38	SA20	ISA Bus	88	PDRQ0 *	ISA Bus
39	SA18	ISA Bus	89	PCMB_VPP1 *	PC Card Power
40	SA14	ISA Bus	90	PCMB_VPP2 *	PC Card Power
41	SA19	ISA Bus	91	XTDATA *	XT Keyboard
42	3V3	Power	92	GND	Power
43	SA17	ISA Bus	93	/MCEH_B *	PC Card
44	SA9	ISA Bus	94	/REG_B *	PC Card
45	/MCEL_A	PC Card	95	/PPOEN *	Printer Port Control
46	/RST_B *	PC Card	96	/CD_B *	PC Card
47	SA4	ISA Bus	97	RDY_B *	PC Card
48	/MEMW	ISA Bus	98	/BL2	Power Management
49	GND	Power	99	BVD2_B *	PC Card
50	/MCEH_A	PC Card	100	BVD1_B *	PC Card

* Note: These pins have multiple functions. For the most part, the names given here indicate the default functions. See Appendix F for details of their alternative functions.

TABLE E5 - J4 100-WAY INTER-BOARD CONNECTOR

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APPENDIX F: MULTI-FUNCTION PINS

Many pins on the Elan processor can have two or even three functions. The different functions are selected by changing pin configuration registers within the Elan chip. This is normally done by the BIOS. For some pins changing a bit in an Elan register will change the function of a single pin. In most cases however changing one bit will change the function of several pins.

This appendix describes the alternative functions of the multi-function pins.

GROUP	DEFAULT FUNCTION	ALTERNATIVE FUNCTIONS	ELAN REGISTER AND BIT
1	ISA Bus: /IOCS16	GPIO_CS5	38h[4]
2	ISA Bus: IOCHRDY	GPIO_CS6	38h[3]
3	ISA Bus: PIRQ1 (IRQ5)	GPIO_CS7	38h[2]
4	ISA Bus: PIRQ0 (IRQ3)	GPIO_CS8	38h[1]
5	ISA Bus: PDRQ0, /PDACK0, AEN, TC	GPIO_CS12 - 9	38h[0]
6	PCMCIA Slot B VPP, VCC Power Control	GPIO_18, GPIO_17, GPIO_16	39h[6]
7	PCMCIA Slot A VPP, VCC Power Control	GPIO_15, GPIO_14, GPIO_13	39h[5]
8	XT Keyboard	Matrix Keyboard Columns 0, 1	39h[3]
9	ISA Bus: /MEMCS16, /SBHE, BALE, PIRQ2 (IRQ12), PDRQ1, /PDACK1	Matrix Keyboard Rows 12 - 7	39h[2]
10	PCMCIA Slot B Control Signals	Printer Port Control and status, or GPIO_31 - 21	39h[1, 0]
11	ISA Bus: PIRQ7 - 3	Matrix Keyboard Columns 2 - 6	3Ah[1]

TABLE F1 - GROUPS OF MULTI-FUNCTION PINS

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
/IOCS16	ISA Bus Signal - I/O is 16 Bits	GPIO_CS5

TABLE F2 - FUNCTIONS OF GROUP 1

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
IOCHRDY	ISA Bus Signal - Insert Wait States	GPIO_CS6

TABLE F3 - FUNCTIONS OF GROUP 2

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
PIRQ1	ISA Bus Signal - IRQ5	GPIO_CS7

TABLE F4 - FUNCTIONS OF GROUP 3

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
PIRQ0	ISA Bus Signal - IRQ3	GPIO_CS8

TABLE F5 - FUNCTIONS OF GROUP 4

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
PDRQ0	ISA Bus: DMA Request	GPIO_CS12
/PDACK0	ISA Bus: DMA Acknowledge	GPIO_CS11
AEN	ISA Bus: DMA Cycle Indicator	GPIO_CS10
TC	ISA Bus: DMA Terminal Count	GPIO_CS9

TABLE F6 - FUNCTIONS OF GROUP 5

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
GPIO_18	PCMCIA Slot B VPP Control	GPIO_18
GPIO_17	PCMCIA Slot B VPP Control	GPIO_17
GPIO_16	PCMCIA Slot B VCC Control	GPIO_16

TABLE F7 - FUNCTIONS OF GROUP 6

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
GPIO_15	PCMCIA Slot A VPP Control	GPIO_15
GPIO_14	PCMCIA Slot A VPP Control	GPIO_14
GPIO_13	PCMCIA Slot A VCC Control	GPIO_13

TABLE F8 - FUNCTIONS OF GROUP 7

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
XTDATA	XT Keyboard Data	Key Matrix Keyboard Column 0
XTCLK	XT Keyboard Clock	Key Matrix Keyboard Column 1

TABLE F9 - FUNCTIONS OF GROUP 8

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
/PDACK1	ISA bus: DMA Acknowledge	Key Matrix Keyboard Row 7
PDRQ1	ISA bus: DMA Request	Key Matrix Keyboard Row 8
PIRQ2	Interrupt PIRQ2 (IRQ12)	Key Matrix Keyboard Row 9
BALE	BALE (ISA Bus Signal)	Key Matrix Keyboard Row 10
/SBHE	/SBHE (ISA Bus Signal)	Key Matrix Keyboard Row 11
/MEMCS16	/MEMCS16 (ISA Bus Signal)	Key Matrix Keyboard Row 12

TABLE F10 - FUNCTIONS OF GROUP 9

SIGNAL NAME	DEFAULT FUNCTION (PC CARD)	ALTERNATIVE FUNCTION (PRN)	ALTERNATIVE FUNCTION (GPIO)
/PPDWE	Tri-state, (p.d.)	Printer /PPDWE	GPIO_21 (p.u.)
/PPOEN	Tri-State, (p.d.)	Printer /PPOEN	GPIO_22 (p.u.)
SLCT	WP for PCMCIA Slot B	Printer SLCT	GPIO_23 (p.u.)
BUSY	BVD2 for PCMCIA Slot B	Printer BUSY	GPIO_24 (p.u.)
/ACK	BVD1 for PCMCIA Slot B	Printer /ACK	GPIO_25 (p.u.)
PE	RDY for PCMCIA Slot B	Printer PE	GPIO_26 (p.u.)
/ERROR	/CD for PCMCIA Slot B	Printer /ERROR	GPIO_27 (p.u.)
/INIT	/REG for PCMCIA Slot B	Printer /INIT	GPIO_28 (p.u.)
/SLCTIN	RST for PCMCIA Slot B	Printer /SLCTIN	GPIO_29 (p.u.)
/AFD	/MCEH for PCMCIA Slot B	Printer /AFD	GPIO_30 (p.u.)
/STRB	/MCEL for PCMCIA Slot B	Printer /STRB	GPIO_31 (p.u.)

TABLE F11 - FUNCTIONS OF GROUP 10

SIGNAL NAME	DEFAULT FUNCTION	ALTERNATIVE FUNCTION
PIRQ3	Interrupt PIRQ3 (IRQ9)	Key Matrix Keyboard Column 2
PIRQ4	Interrupt PIRQ4 (IRQ10)	Key Matrix Keyboard Column 3
PIRQ5	Interrupt PIRQ5 (IRQ15)	Key Matrix Keyboard Column 4
PIRQ6	Interrupt PIRQ6 (IRQ6)	Key Matrix Keyboard Column 5
PIRQ7	Interrupt PIRQ7 (IRQ14)	Key Matrix Keyboard Column 6

TABLE F12 - FUNCTIONS OF GROUP 11

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APPENDIX G: DEFINING GCAT486 KEYPADS

G.1 INTRODUCTION

This Appendix describes the tables associated with the key matrix keyboard, and the process of patching them to customise the BIOS for keypads of different sizes and different arrangements of keys.

A keyboard can be implemented as a matrix of switches, in a grid of rows and columns. Software within the GCAT486 BIOS can scan this key matrix and pass key press information to other parts of the BIOS, and on to the operating system and applications program as though the key had been pressed on a conventional XT keyboard. The key matrix software is responsible for scanning the key matrix, debouncing key presses, handling special cases and generating a "scan code" to pass to higher levels of the BIOS.

The function of the key matrix software is to return "scan codes", which correspond to a particular key. The scan codes generated are compatible with an XT keyboard. One scan code is generated when a key is pressed and another when the key is released. In most cases the scan code for the key release is the same but with bit 7 set. Note that the scan codes are not the same as ASCII characters – the ASCII characters are translated from the scan codes by higher levels of BIOS software

The operation is table-driven – tables within the BIOS define the size of the key matrix and the key associated with each intersection of rows and columns. GCAT486 users may modify these tables to suit their application.

The key matrix tables are somewhat complex – this is necessary to provide maximum flexibility. There are seven tables which may be patched – six for the key matrix and one for LCDs. These are listed in Table G1. (The odd sounding names are those given by Phoenix in the BIOS source code).

NUMBER	NAME	DESCRIPTION
1	MtrxScanIndex	This is actually a group of three tables that are placed one after the other. These are MtrxScanIndex, MtrxRtnIndex and regMtrxTbl. Together they define the number of rows and columns in use, and switch multi-function pins to their keyboard functions.
2	EkbXlatTable1	This converts the X/Y key position to an index which accesses one of the next four tables.
3	ScanTBL	This returns a simple scan code.
4	KeyTBL	This results in a call to a subroutine that processes special keys.
5	KeyTBL1	This returns one scan code if the "Fn" key is not pressed, and a different scan code if it is. This allows for keys to be given dual functions.
6	KeyTBL2	This returns one scan code if the "NumLock" key is not pressed, and a different scan code if it is. This allows for keys to be given dual functions.
7	LCDtable	This table defines timing registers for the LCD controller.

TABLE G1 - BIOS TABLES SUPPORTING MATRIX KEYBOARD

G.2 KEY MATRIX SIZES

As explained in Appendix F, many pins on the Elan processor have multiple functions. One function or another is selected in software. Amongst these multi-function pins are the pins which can operate as the rows and columns of a key matrix. As Elan pins are allocated key matrix functions, the other functions are lost. It is the job of the system designer to consider which pins may be used for the key matrix, and which are to be used for their other function.

In practise it turns out that there are two options for key matrix rows (eight or 14 rows) and seven options for key matrix columns (from one to eight columns).

(In theory the Elan's SUS_RES pin can be reconfigured as a 15th key matrix row, but software support for this does not exist at present).

The MtrxScanIndex table in the BIOS defines which pins are to be used for which function. If the key is not used for the key matrix function then it is assigned to the alternative function by this table.

DSP Design has prepared 15 files which can be placed in this table – all of the 14 combinations of two row options and seven column options, plus a table which defines no key matrix at all. These files are on the GCAT486 Utilities Disks, in the directory BIOS/TABLES. The files and their rows and columns are listed below. They may be patched into the MtrxScanIndex table as explained in the section on the GC4PATCH program.

The files and the rows and columns that they use are listed in Table G2. A dot indicates the rows and columns used by each file.

FILE NAME	ROW 0-6	ROW 7-12	ROW 13	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7
R_NONE.TXT											
RALL_C01.TXT	•	•	•	•	•						
RALL_C06.TXT	•	•	•	•	•	•	•	•	•		
RALL_C07.TXT	•	•	•	•	•	•	•	•	•	•	•
RALL_C26.TXT	•	•	•			•	•	•	•	•	
RALL_C27.TXT	•	•	•			•	•	•	•	•	•
RALL_C7.TXT	•	•	•								•
RALLC017.TXT	•	•	•	•	•						•
RLIM_C01.TXT	•		•	•	•						
RLIM_C06.TXT	•		•	•	•	•	•	•	•		
RLIM_C07.TXT	•		•	•	•	•	•	•	•	•	•
RLIM_C26.TXT	•		•			•	•	•	•	•	
RLIM_C27.TXT	•		•			•	•	•	•	•	•
RLIM_C7.TXT	•		•								•
RLIMC017.TXT	•		•	•	•						•

TABLE G2 – KEY MATRIX SIZES

G.3 KEY ALLOCATIONS

The default tables have been set up to suit the Cherry G84-4000 QWERTY keypad. This is available from RS Components and other Cherry suppliers. The arrangement of this keypad is described in Table G3. Table G3 shows the key text at each position on the Cherry keypad. The table also shows the Elan pin that is connected to the rows and columns of the keypad, and the alternative function of the pin. Note that there are many row/column intersections which do not have an associated key – these are shown shaded in Table G3.

ROW:	**COLUMN:**	**COL0**	**COL1**	**COL2**	**COL3**	**COL4**	**COL5**	**COL6**	**COL7**
	Alt. Function	XTDAT	XTCLK	PIRQ3	PIRQ4	PIRQ5	PIRQ6	PIRQ7	(none)
ROW 0	(none)	F2	F3	F7	F6	F1	F4	F5	ESC
ROW 1	(none)	3 / £	4 / $	8 / *	7 / &	2 / "	5 / %	6 / ^	1 / !
ROW 2	(none)		Ins	, / <	. / >	End	Del	? / /	Space
ROW 3	(none)	Enter		K	L	PgDn	' / @	; / :	Left Arrow
ROW 4	(none)	# / ~	] / }	I	O	PgUp	[/ {	P	Up Arrow
ROW 5	(none)		Back Sp	9 / (	0 /)	Home	= / +	- / _	Dn Arrow
ROW 6	(none)	Scrl Lock	Prt Scr	F8	F9	Brk / Pause	Num Lock	F10	Right Arrow
ROW 7	/PDACK1	W	E	U	Y	Q	R	T	Tab
ROW 8	PDRQ1	S	D	J	H	A	F	G	Cap Lock
ROW 9	PIRQ2	X	C	M	N	Z	V	B	\ / |
ROW 10	BALE								Left Ctrl
ROW 11	/SBHE								Left Alt
ROW 12	/MEMCS16								Right Shift
ROW 13	(none)								Left Shift

TABLE G3 - CHERRY KEYPAD CONNECTIONS

Any other keypad will have different keys at each row/column intersection, and so another table will need to be patched. This is the table called EkbXlatTable1. The default EkbXlatTable1 is contained on the GCAT486 Utilities disk, in a file called XLAT.TXT. This file can be used for reference, and can be used edited and so

transformed into a table for any other arrangement of keys. The contents of this table is summarised in Table G4 below.

	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7
ROW0	0C1h	004h	002h	00Bh	0C0h	00Ch	003h	076h
ROW1	026h	025h	03Eh	03Dh	01Eh	02Eh	036h	016h
ROW2	0BFh	070h	041h	049h	069h	071h	04Ah	029h
ROW3	05Ah	0BFh	042h	04Bh	07Ah	01Eh	04Ch	06Bh
ROW4	00Eh	05Bh	043h	044h	07Dh	054h	04Dh	075h
ROW5	0BFh	066h	046h	045h	06Ch	055h	04Eh	072h
ROW6	07Eh	0CAh	00Ah	001h	089h	077h	009h	074h
ROW7	01Dh	024h	03Ch	035h	015h	02Dh	02Ch	00Dh
ROW8	01Bh	023h	03Bh	033h	01Ch	02Bh	034h	058h
ROW9	022h	021h	03Ah	031h	01Ah	02Ah	032h	05Dh
ROW10	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	014h
ROW11	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	011h
ROW12	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	059h
ROW13	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	012h
ROW14	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh
ROW15	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh	0BFh

TABLE G4 - CONTENTS OF DEFAULT EkbXlatTable1 (AND XLAT.TXT)

Each entry in the EkbXlatTable1 table (and hence the XLAT.TXT file) corresponds to the intersection of a row and column of the keypad. The rows in the XLAT.TXT file correspond to rows on the key matrix, starting from row 0. The entries in each row provides an index value for each column position, starting with column 0, so the arrangement of data in the XLAT.TXT file is in the same sequence as in Table G3 and Table G4.

Positions where there is no physical key are given a code 0BFh. Note that the table has 16 rows even though the GCAT486 only supports 14. All entries in rows 14 and 15 are set to 0BFh.

The value at each row/column position of EkbXlatTable1 is an index into one of four other tables: ScanTBL, KeyTBL, KeyTBL1 and KeyTBL2. Most simple keys will provide a single scan code to the BIOS. These scan codes are located in the table called ScanTBL, which is described in Table G5. Table G5 has entries for index values in the range 00h to 7Fh. Against the index value is the scan code returned by that value, and the key associated with that scan code.

For example, the row0/column1 position of the keypad corresponds to the F3 key on the keypad, as can be seen in Table G3. Table G4 shows that the row0/column1 position has an index value of 04h. This value 04h is an index into the 5th entry in the ScanTBL table, described in Table 5, where it results in the scan code 3Dh being returned. This is the standard PC scan code for the F3 key.

Keys with an index value in EkbXlatTable1 of greater than 80h represent an index into one of the other tables: KeyTBL, KeyTBL1 and KeyTBL2. These tables are described in Table G6, Table G7 and Table G8 respectively.

Table G6 contains the index values for keys that require software routines to be run. These routines either set flags for use by the keyboard scanning software, or return multiple scan codes. Examples of this are the Function and Function Lock keys, used with tables G7 and G8. (More information on this table will be supplied in the next issue of this manual or on the next Utility Disks).

Tables G7 and G8 allow some keys to be given two different functions, depending on the state of a “Function” or “NumLock” key. An example for this would be a QWERTY keypad which had a numeric keypad laid over it, with the numeric functions becoming active when a Function key was depressed. The GCAT486 offers two options. Table G7 delivers an alternative key while the Function key is held down. Table G8 is used with a toggling NumLock key – the alternative key is delivered when the NumLock key is depressed once, and the normal key is delivered when the NumLock key is pressed a second time.

The “press and hold” Function key should be given an index value of 97h (which also delivers its own “Fn” scan code of 55h) or 96h (which will not deliver a scan code of its own). The “NumLock” Function key should be given an index value 9Ah (which also delivers its own “NumLock” scan code of 45h) or 98h (which will not deliver a scan code of its own). Both the press and hold Function key and the NumLock key could be used in the same system, if necessary.

A key which has two functions controlled by the “press and hold” Function key should be given an index value in the range 0C0h – 0DFh. The two entries in KeyTBL1 are then chosen from Table G5 or Table G6.

A key which has two functions controlled by the “NumLock” Function key should be given an index value in the range 0E0h – 0FFh. The two entries in KeyTBL2 are then chosen from Table G5, Table G6 or Table G7. Note that this option of a Table G7 index value allows for the possibility of a key with three functions – a normal key, a key when the NumLock key is active and a key when both the NumLock and Function keys are active.

For example, the row0/column0 position of the keypad corresponds to the F2/F12 key on the keypad, as can be seen in Table G3. Table G4 shows that the row0/column0 position has an index value of 0C1h. This value C1h is an index into the 2nd entry in the KeyTBL1 table, described in Table G7, where either the scan code for the F2 key (006h) or the F12 key (007h) is returned, depending on the state of the Function key.

INDEX	SCAN CODE	KEY	INDEX	SCAN CODE	KEY	INDEX	SCAN CODE	KEY	INDEX	SCAN CODE	KEY
00	FF	Error	20	67	Res.	40	6B	Res.	60	55	Fn
01	43	F9	21	2E	C	41	33	< ,	61	56	Fn Lock
02	41	F7	22	2D	X	42	25	K	62	77	Res.
03	3F	F5	23	20	D	43	17	I	63	78	Res.
04	3D	F3	24	12	E	44	18	O	64	79	Res.
05	3B	F1	25	05	$ 4	45	0B	) 0	65	7A	Res.
06	3C	F2	26	04	# 3	46	0A	(9	66	0E	Back space
07	58	F12	27	5C	Res.	47	60	Res.	67	7B	Res.
08	64	Res.	28	68	Res.	48	6C	Res.	68	7C	Res.
09	44	F10	29	39	Space	49	34	> .	69	4F	1 End
0A	42	F8	2A	2F	V	4A	35	? /	6A	7D	Res.
0B	40	F6	2B	21	F	4B	26	L	6B	4B	4 Left Arrow
0C	3E	F4	2C	14	T	4C	27	: ;	6C	47	7 Home
0D	0F	Tab	2D	13	R	4D	19	P	6D	7E	Res.
0E	29	~ '	2E	06	% 5	4E	0C	_ -	6E	7F	Res.
0F	59	Res.	2F	5D	Res.	4F	61	Res.	6F	6F	Res.
10	65	Res.	30	69	Res.	50	6D	Res.	70	52	0 Ins
11	38	Left Alt	31	31	N	51	73	Res.	71	53	. Del
12	2A	Left Shift	32	30	B	52	28	" '	72	50	2 Down Arrow
13	70	Res.	33	23	H	53	74	Res.	73	4C	5
14	1D	Left Ctrl	34	22	G	54	1A	{ [	74	4D	6 Right Arrow
15	10	Q	35	15	Y	55	0D	+ =	75	48	8 Up Arrow
16	02	! 1	36	07	^ 6	56	62	Res.	76	01	Esc
17	5A	Res.	37	5E	Res.	57	6E	Res.	77	45	Num Lock
18	66	Res.	38	6A	Res.	58	3A	Caps Lock	78	57	F11
19	71	Res.	39	72	Res.	59	36	Right Shift	79	4E	+
1A	2C	Z	3A	32	M	5A	1C	Return	7A	51	3 PgDn
1B	1F	S	3B	24	J	5B	1B	}]	7B	4A	-
1C	1E	A	3C	16	U	5C	75	Res.	7C	37	*
1D	11	W	3D	08	& 7	5D	2B	| \	7D	49	9 PgUp
1E	03	@ 2	3E	09	* 8	5E	63	Res.	7E	46	Scroll Lock
1F	5B	Res.	3F	5F	Res.	5F	76	Res.	7F	54	Sys Req

Note : index and scan code values in hex

TABLE G5 - ScanTBL

INDEX	KEY	INDEX	KEY	INDEX	KEY	INDEX	KEY
80	L Shift	90	Up Arrow	A0	Res.	B0	Res.
81	L Ctrl	91	L Arrow	A1	Res.	B1	Res.
82	L Alt	92	Dn Arrow	A2	Res.	B2	Res.
83	F7	93	R Arrow	A3	Res.	B3	Res.
84	SysReq	94	B Slash	A4	Res.	B4	Res.
85	R Shift	95	Enter	A5	Res.	B5	Res.
86	R Ctrl	96	Fn1	A6	Res.	B6	Res.
87	R Alt	97	Fn2	A7	Res.	B7	Res.
88	PrtScrn	98	FnLk1	A8	Res.	B8	Res.
89	Pause	99	FnLk2	A9	Res.	B9	Res.
8A	Insert	9A	Num Lk	AA	Res.	BA	Res.
8B	Home	9B	Setup	AB	Res.	BB	Res.
8C	Pg Up	9C	Res.	AC	Res.	BC	Res.
8D	Delete	9D	Res.	AD	Res.	BD	Res.
8E	End	9E	Res.	AE	Res.	BE	Res.
8F	Pg Dn	9F	Res.	AF	Res.	BF	Res.

Note : index values in hex

TABLE G6 - KEYTBL (Routines for processing special keys)

INDEX	NORMAL KEY	SHIFTED KEY	NORMAL INDEX	SHIFTED INDEX
C0	F1	F11	05	78
C1	F2	F12	06	07
C2	L Arrow	Home	91	8B
C3	Up Arrow	Pg Up	90	8C
C4	Down Arrow	Pg Dn	92	8F
C5	Right Arrow	End	93	8E
C6	Left Ctrl	Right Ctrl	14	86
C7	Left Alt	Right Alt	11	87
C8	Insert	Num Lock	8A	9A
C9	Delete	Scroll Lock	8D	7E
CA	PrtScn	SysReq	88	84
CB	Scroll Lock	F11	7E	78
CC	Num Lock	F12	77	07
CD	Num Lock	Fn Lock (no #)	77	98
CE	Num Lock	Fn Lock (Scan #)	77	99
CF	F1	Setup	05	9B
D0	1	F1	16	05
D1	2	F2	1E	06
D2	3	F3	26	04
D3	4	F4	25	0C
D4	5	F5	2E	03
D5	6	F6	36	0B
D6	7	F7	3D	02
D7	8	F8	3E	0A
D8	9	F9	46	01
D9	0	F10	45	09
DA	-	Num Lock	4E	9A
DB	=	BS	55	66
DC	P	INS	4D	8A
DD	[	Pause	54	89
DE	]	Scr Lock	5B	7E
DF	;	Prt Scr	4C	88

Note : index values in hex

TABLE G7 - KEYTBL1 (Keys with two functions, depending on Fn)

INDEX	NORMAL KEY	NUMLOCK KEY	STANDARD INDEX	NUMLOCK INDEX
E0	7	7	D6	6C
E1	8	8	D7	75
E2	9	9	D8	7D
E3	0	*	D9	7C
E4	U	4	3C	6B
E5	I	5	43	73
E6	O	6	44	74
E7	P	-	DC	7B
E8	J	1	3B	69
E9	K	2	42	72
EA	L	3	4B	7A
EB	;	+	DF	79
EC	M	0	3A	70
ED	.	.	49	71
EE	/	/	4A	94
EF – FF	Res.	Res.	00	00

Note : index values in hex

TABLE G8 - KEYTBL2 (Keys with two functions, depending on NumLock)

G.4 MODIFYING THE TABLES FOR OTHER KEYPADS

The standard BIOS, as shipped with the GCAT486, has no key matrix enabled. In fact, the “R_NONE.TXT” file from Table G2 is active in the BIOS. To activate the full key matrix for the Cherry G84-4000 keypad you will need to patch the BIOS with the “RALL_C07.TXT” file. To configure the BIOS for other keypads there will be other files to modify and patches to make.

G.4.1 Changing the Tables

If you are using the Cherry keypad and a BIOS which selects the maximum number of rows and columns then you will not need to change the tables – just enable the key matrix with the RALL_C07.TXT file. If you want to retain the alternative functions for some of the Elan pins then you must change the definition of the key matrix size. Then you will have a keypad that will operate like a cut-down version of the Cherry keypad, with only some keys responding. If you can work with the resulting set of keys then you will have nothing more to do, but if you want to change the key at a particular X/Y position then you will need to patch the table EkbXlatTable1. Only if you wish to have two scan codes on the same key position will you need to modify KeyTBL1 and KeyTBL2. There should be no need to have to change the ScanTBL or KeyTBL tables.

We suggest you follow the following steps.

First select the key matrix size you require, using Table 2, and noting that you will loose the alternative function of the multi-function pin as it becomes a key matrix key.

To begin with you are advised to select a key matrix which does not use column 0 or 1, since the XT keyboard uses these, and the XT keyboard will remain operational while these pins are excluded from the key matrix. Note also that the floppy disk controller uses PIRQ6, which is multiplexed with column 5, so you must disable the Development System floppy disk controller when incorporating column 5 in your key matrix.

Use the GC4PATCH program (described below) to patch a BIOS with the desired key matrix size file from Table G2. Test the new BIOS, checking that characters appear on the screen corresponding to the rows and columns you have enabled.

Then re-map each row/column intersection to the key that you require, using (primarily) Table G5. To do this, edit a copy of the XLAT.TXT file, inserting the index values from Table G5 that correspond to the scan codes and keys on your keyboard. For example, if you want the key at row0/column0 to return the scan code for "B", replace the current 0C1h code with 32h. Patch and test a new BIOS image.

Finally, if required, provide support for the Function and NumLock keys. Modify your copy of XLAT.TXT by inserting index values in the range 0C0h – 0DFh (for Function keys) an in the range 0E0h – 0FFh (for NumLock keys). You may need to modify the KeyTBL1 (Function) and KeyTBL2 (NumLock) tables as well – if so, GC4PATCH can be used to extract the current versions of these tables from the standard BIOS, for you to edit.

G.4.2 The Patching Tools

The tools for patching the BIOS tables are a program called GC4PATCH.EXE and a batch program called PATCHIT.BAT, both of which are on the GCAT486 Utilities Disks. PATCHIT.BAT uses the program CRUNCH.EXE which is also on the GCAT486 Utilities Disks. We urge users to understand the operation of the GC4PATCH program and PATCHIT batch file – type out the PATCHIT.BAT file and examine it, and run the GC4PATCH program with the –h switch which will cause the program to print its help menu. The CRUNCH.TXT file in the BIOS directory should also be read.

In summary, the programs operate as follows.

GC4PATCH.EXE can extract a given table from the GCAT486 BIOS, and write a new table into the BIOS, from a text file. GC4PATCH works on the file BIOS.ROM, which is extracted from the 128k byte BIOS image file by the program called CRUNCH.EXE. That is where the PATCHIT.BAT program comes in – it runs CRUNCH a first time to break down a BIOS image file into its constituent parts, including BIOS.ROM. PATCHIT then runs GC4PATCH to make the required change to BIOS.ROM, then CRUNCH is run again to recombine the constituent files into a new BIOS image file, which is then programmed into the GCAT486 by the program GC4LV160.EXE.

Normally the process operates as follows. If you want to change the size of the key matrix to, say, eight columns by five rows, and you are starting with a BIOS image file called 165013B2.ROM, then you would type this:

```
PATCHIT   165013B2.ROM   MYBIOS1.ROM   RLIM_C26.TXT
```

This results in a new BIOS image file, called MYBIOS1.ROM, with the table defining the key matrix size patched with the contents of the RLIM_C26.TXT file.

The other common patching operation will be to change the key assignments on the keypad. Choose as a starting point the file XLAT.TXT, which is on the GCAT486 Utilities Disk. This file contains the default ekbXlatTable1 corresponding to the Cherry G84-4000 keypad. Make a copy of this file to, say, MYXLAT.TXT, edit the file to supply index values corresponding to the keys at each row/column intersection, and then patch the resulting table into the BIOS image by typing this:

```
PATCHIT   MYBIOS1.ROM   MYBIOS2.ROM   MYXLAT.TXT
```

G.5 SETUP

A quick note follows on the BIOS Setup program. On the standard XT keyboard, the BIOS Setup program can be entered by typing the F2 key at the appropriate time during POST. Because of the structure of the BIOS it was not possible to emulate this exactly with the key matrix. Instead, Setup is entered if any key is being held down at the point during POST when the BIOS searches for the F2 key.

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APPENDIX H: GCAT486DEV DEVELOPMENT SYSTEM

This appendix describes the GCAT486DEV Development System. The GCAT486DEV once formed part of the GCAT486 development environment, and was used in conjunction with the TCDEV Development System. This pair of boards is superceded by the TCDEVPLUS, and the GCAT486DEV is no longer available.

However, the circuit of the GCAT486DEV can be used as the basis of a custom-designed motherboard. It is useful because it illustrates power supply, 5V to 3.3V buffering, printer port circuitry and clock generation. The appendix includes the circuit diagram of the GCAT486DEV and a description of parts of its circuit.

H.1 OVERVIEW

The GCAT486DEV was designed to assist with development of GCAT486 systems.

The GCAT486 plugged onto the GCAT486DEV, which in turn plugged into our old PC/104 development system, the TCDEV. The GCAT486DEV therefore effectively turned the GCAT486 into a PC/104 board, and allowed our old PC/104 development platform to be used for GCAT486 development as well. The GCAT486DEV was able to be used by itself with a number of limitations – in particular disk drive and VGA graphics features (which were provided by the TCDEV) were lost.

The GCAT486DEV routed the GCAT486 signals to a number of connectors. These included PC/104 connectors, for the ISA bus, and connectors for most of the I/O, such as serial ports and LCD panel. It also contained active electronics: a DC-DC converter to provide 3.3V from 5V, buffers on the data bus, clock generation logic for the PC/104 bus, a battery for the RTC and a printer port.

A 50-way ribbon cable also connected many of the GCAT486 I/O signals to the TCDEV. It linked the COM1 and COM2 serial ports, parallel port, keyboard etc onto the TCDEV and in turn to the PC compatible connectors mounted on the edge of the TCDEV board. The TCDEV included an ISA bus connector allowing standard ISA bus boards to be used with the GCAT486.

H.2 CONNECTORS

There are many connectors on the GCAT486DEV. Users may derive the pin assignments of the connectors from the circuit diagram. Table H1 summarises the functions of each connector.

CONNECTOR	TYPE	FUNCTION / NOTES
J1	26-way (2x13)	Miscellaneous signals, incl. A/D.
J2	4-way Molex	Power input (if used stand-alone).
J3	14-way Flat Flex	Connects directly to mono LCD, DSP part no. LCDQVGA.
J4	Spade terminal	GND point
J5	14-way (2x7)	Connects to a mono LCD (alternative to J3)
J6	2-pin	LCD backlight inverter output (not fitted).
J7	64-way PC/104	8-bit PC/104 bus
J8	40-way PC/104	16-bit PC/104 bus
J9	100-way FX8	Connects to GCAT486 J4
J10	100-way FX8	Connects to GCAT486 J3
J11	14-way (2x7)	Connects to an alphanumeric LCD.
J12	12-way (2x6)	Designed for jumpers for power routing.
J13	Spade terminal	GND point
J14	5-way DIN	XT keyboard.
J15	10-way (2x5)	COM1 serial port. Pin assignments suit crimping to a 9-way D-type.
J16	10-way (2x5)	COM2 serial port. Pin assignments suit crimping to a 9-way D-type.
J17	26-way (2x13)	Printer port. Pin assignments suit crimping to a 25-way D-type.
J18	Spade terminal	GND point
J19	10-way (2x5)	COM3 serial port. Pin assignments suit crimping to a 9-way D-type.
J20	50-way (2x25)	Takes I/O signals to TCDEVPLUS I/O
J21	26-way (2x13)	Keypad. Configured to connect to Cherry Qwerty keypad, DSP part no. KBDXTAT.
J22	100-way FX8	Connects to a GCAT486P2 PC Card adapter.
J23	100-way FX8	Connects to a GCAT486P2 PC Card adapter.

TABLE H1 - GCAT486DEV CONNECTORS

H.3 CIRCUIT DESCRIPTION

This section should be read together with the circuit diagram below. Most of this circuitry appears on the TCDEVPLUS. As mentioned above, the main purpose of this appendix is to act as a guide for users intending to design their own motherboard. You should understand the circuits shown here, and implement them as appropriate on your own design.

IC13 and associated components form a DC-DC power supply, which generates a 3.3V supply for the GCAT486 from the 5V supply of the TCDEV. The 3.3V output is routed to the GCAT's 3V3 and VCC_CPU signals through jumpers on jumper are J12. Jumpers at J12 can be removed to allow power consumption to be measured, or alternative power supplies to be used.

IC9 monitors the current drawn by the GCAT486, through resistor R6. The signal VOUT is a voltage proportional to the current. VOUT in volts is twice the current in amperes. VOUT can be monitored either by a multimeter, or by a scope, to report on steady-state or dynamic current consumption respectively.

IC1 generates the two missing ISA bus clocks – BUSCLK at 8MHz and OSC at 14.318MHz.

The 16-bit CMOS switch IC5 operates as a transparent bi-directional path for the data bus. The D1, R3 and C3 circuit, together with internal characteristics of the chip, ensure that 5V logic signals on the PC/104 bus (D0-15) are converted to 3V signals to the GCAT486 on (SD0-15). This is a Pericom chip.

The gates around SW1 generate a debounced suspend/resume signal.

B1 is a battery and provides battery backup for the calendar clock.

The gates around the /MEMR signal disable the /MEMR signal from the EPROM on the TCDEV and the EPROM socket on the GCAT486DEV while the GCAT486's Flash chip is being accessed. In conjunction with the Flash programming program and the /ENFLASH signal from the GCAT486 Utility Register, this allows for an EPROM and the Flash chip to coexist. Should the BIOS in the GCAT486's Flash chip become corrupted, the GCAT486 LK8 can be set to the 2-3 position, and the GCAT486 can boot from a BIOS image in an EPROM plugged into the socket IC2. The GC4LV160 flash programming program can then be used to restore a BIOS image into the Flash chip. LK8 is then returned to the 1-2 position.

IC10, IC11 and the associated gates form the data port of a printer port, if the printer function is required. For unidirectional mode the HCT245 chip is removed. The HCT373 is replaced by an HCT374 with its output enable pin (pin 1) tied low. The /PPDWE pin from the Elan processor connects directly to the clock pin (pin 11) of the HCT374.

IC4 provides the site for an optional second Flash memory chip, connected to the Elan's second ROM chip select signal.

The board is laid out for a CCFL inverter for an LCD (IC3). This component is not fitted.

H.4 SOLDER LINKS

A number of functions can be configured with solder links on the GCAT486DEV board. The board layout is so dense we have implemented these configuration options with solder links which take less space than jumpers, as well as being more reliable.

Care must be taken when changing these link areas so that no accidental shorts are produced. Default settings are noted below.

LK1 VIRDA Source

This link is used to provide a power source to the IrDA transceiver module on the GCAT486. It should be used in conjunction with the GCAT486 LK5. See section 3.6.4 for more details.

VIRDA connects direct to 5V:	Install link (default setting)
VIRDA connects to 5V through a 10-ohm resistor:	Remove link

LK2 Flash Memory Pin 13

This pin may be used in the future to route the A22 address pin to an 8M byte Flash memory chip. At present it is not used and should not be connected.

LK3 SUS_RES Pin Function

The Elan's SUS_RES pin can be used as a fifteenth key matrix column pin, in some circumstances. At this stage there is no software support for this.

Pin used as a Key matrix pin:	Link 1 - 2
Pin used as a SUS_RES signal from the debouncing circuit:	Link 2 - 3 (default setting)

LK4 Printer Enable/Disable

This link is used to disable the printer buffers if the printer port multi-function pins are being used for other functions.

Printer buffers enabled:	Link 1 - 2 (default setting)
Printer buffers disabled:	Link 2 - 3

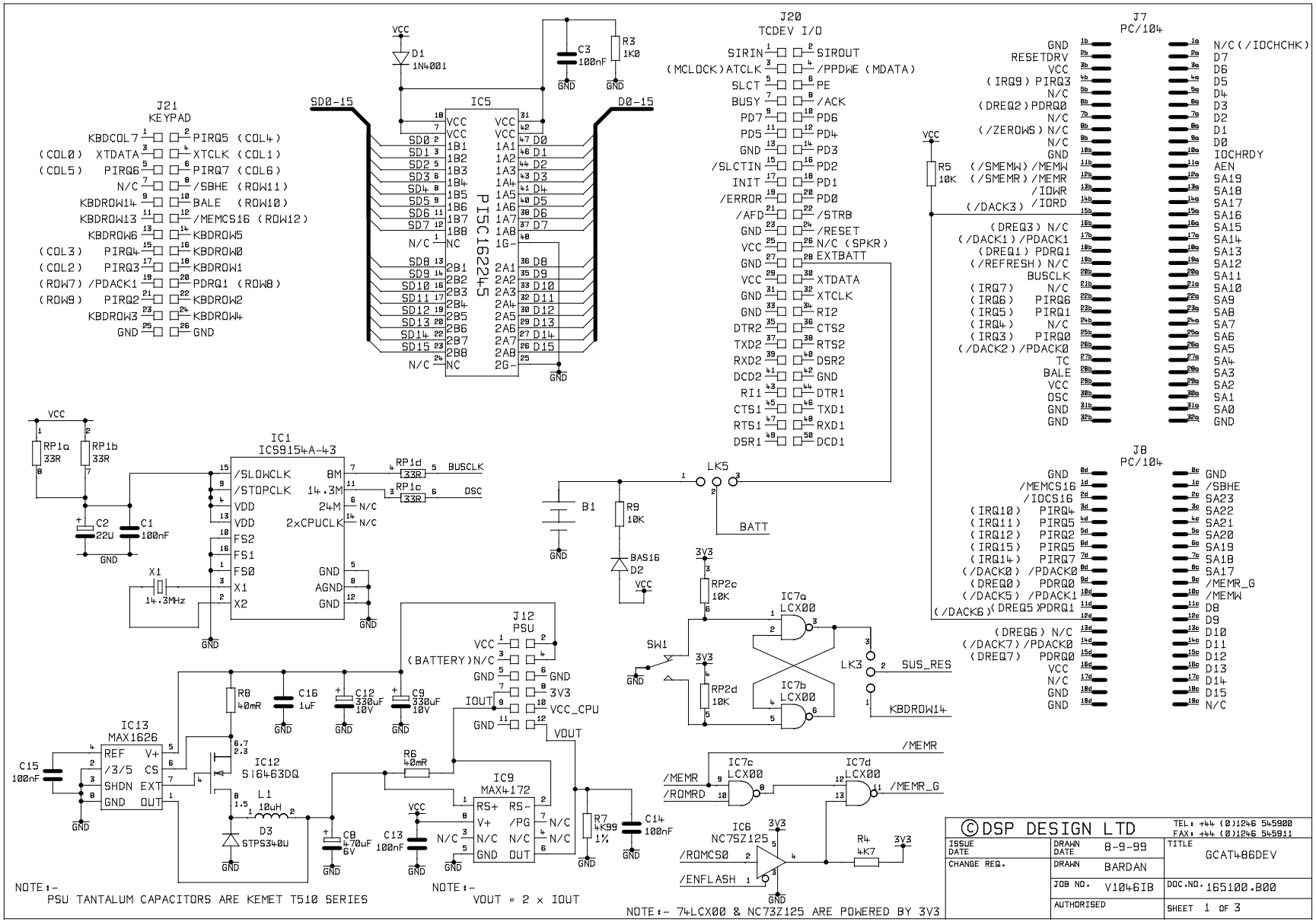
LK5 Battery Selection

The on-board battery or the TCDEV's battery can be used as the supply to the GCAT486.

GCAT486DEV battery:	Link 1 – 2 (Default setting)
TCDEVPLUS battery:	Link 2 – 3

H.5 CIRCUIT DIAGRAM

The following three pages are the circuit diagram of the GCAT486DEV. The circuit remains the copyright of DSP Design, but we grant permission for any or all of the circuit to be used by DSP Design customers who are using the circuit together with GCAT486 processor boards. The circuit diagrams are also included as Acrobat .PDF files on the GCAT486 Utilities Disks.


J21
KEYPAD
KBDCOL7 PIRQ5 (COL4)
(COL0) XTDATA XTCLK (COL1)
(COL5) PIRQ6 PIRQ7 (COL6)
N/C /SBHE (ROW11)
KBDROW14 BALE (ROW10)
KBDROW13 /MEMCS16 (ROW12)
KBDROW6 KBDROW5
(COL3) PIRQ4 KBDROW0
(COL2) PIRQ3 KBDROW1
(ROW7) /PDACK1 PDRQ1 (ROW8)
(ROW9) PIRQ2 KBDROW2
KBDROW3 KBDROW4
GND GND
VCC
D1
1N4001
C3
100nF
R3
1K0
SD0-15
D0-15
IC5
PI5C16245
J20
TCDEV I/O
SIRIN SIROUT
(MCLOCK) ATCLK /PPDWE (MDATA)
SLCT PE
BUSY /ACK
PD7 PD6
PD5 PD4
GND PD3
/SLCTIN PD2
INIT PD1
/ERROR PD0
/AFD /STRB
GND /RESET
VCC N/C (SPKR)
GND EXTBATT
VCC XTDATA
GND XTCLK
GND RI2
DTR2 CTS2
TXD2 RTS2
RXD2 DSR2
DCD2 GND
RI1 DTR1
CTS1 TXD1
RTS1 RXD1
DSR1 DCD1
J7
PC/104
GND N/C (/IOCHCHK)
RESETDRV D7
VCC D6
(IRQ9) PIRQ3 D5
N/C D4
(DREQ2) PDRQ0 D3
N/C D2
(/ZEROWS) N/C D1
N/C D0
GND IOCHRDY
(/SMEMW) /MEMW AEN
(/SMEMR) /MEMR SA19
/IOWR SA18
(/DACK3) /IORD SA17
SA16
(DREQ3) N/C SA15
(/DACK1) /PDACK1 SA14
(DREQ1) PDRQ1 SA13
(/REFRESH) N/C SA12
BUSCLK SA11
(IRQ7) N/C SA10
(IRQ6) PIRQ6 SA9
(IRQ5) PIRQ1 SA8
(IRQ4) N/C SA7
(IRQ3) PIRQ0 SA6
(/DACK2) /PDACK0 SA5
TC SA4
BALE SA3
VCC SA2
OSC SA1
GND SA0
GND GND
R5
10K
J8
PC/104
GND GND
/MEMCS16 /SBHE
/IOCS16 SA23
(IRQ10) PIRQ4 SA22
(IRQ11) PIRQ5 SA21
(IRQ12) PIRQ2 SA20
(IRQ15) PIRQ5 SA19
(IRQ14) PIRQ7 SA18
(/DACK0) /PDACK0 SA17
(DREQ0) PDRQ0 /MEMR_G
(/DACK5) /PDACK1 /MEMW
(/DACK6) (DREQ5) PDRQ1 D8
D9
(DREQ6) N/C D10
(/DACK7) /PDACK0 D11
(DREQ7) PDRQ0 D12
VCC D13
N/C D14
GND D15
GND N/C
IC1
ICS9154A-43
/SLOWCLK 8M
/STOPCLK 14.3M
VDD 24M
VDD 2xCPUCLK
FS2
FS1
FS0 GND
X1 AGND
X2 GND
RP1a 33R
RP1b 33R
RP1d 33R BUSCLK
RP1c 33R OSC
C2 22U
C1 100nF
X1 14.3MHz
LK5
B1
R9 10K
BAS16 D2
BATT
RP2c 10K
RP2d 10K
SW1
IC7a LCX00
IC7b LCX00
LK3 SUS_RES
KBDROW14
J12
PSU
VCC (BATTERY) N/C
GND GND
GND 3V3
IOUT VCC_CPU
GND VOUT
IC13
MAX1626
REF V+
/3/5 CS
SHDN EXT
GND OUT
C15 100nF
R8 40mR
C16 1uF
C12 330uF 10V
C9 330uF 10V
IC12
SI6463DQ
L1 10uH
D3
STPS340U
C8 470uF 6V
R6 40mR
IC9
MAX4172
RS+ RS-
V+ /PG
N/C N/C
GND OUT
C13 100nF
R7 4K99 1%
C14 100nF
/MEMR
/ROMRD
IC7c LCX00
IC7d LCX00
/MEMR_G
IC6
NC7SZ125
/ROMCS0
/ENFLASH
R4 4K7
3V3
NOTE:-
PSU TANTALUM CAPACITORS ARE KEMET T510 SERIES
NOTE:-
VOUT = 2 x IOUT
NOTE:- 74LCX00 & NC7SZ125 ARE POWERED BY 3V3
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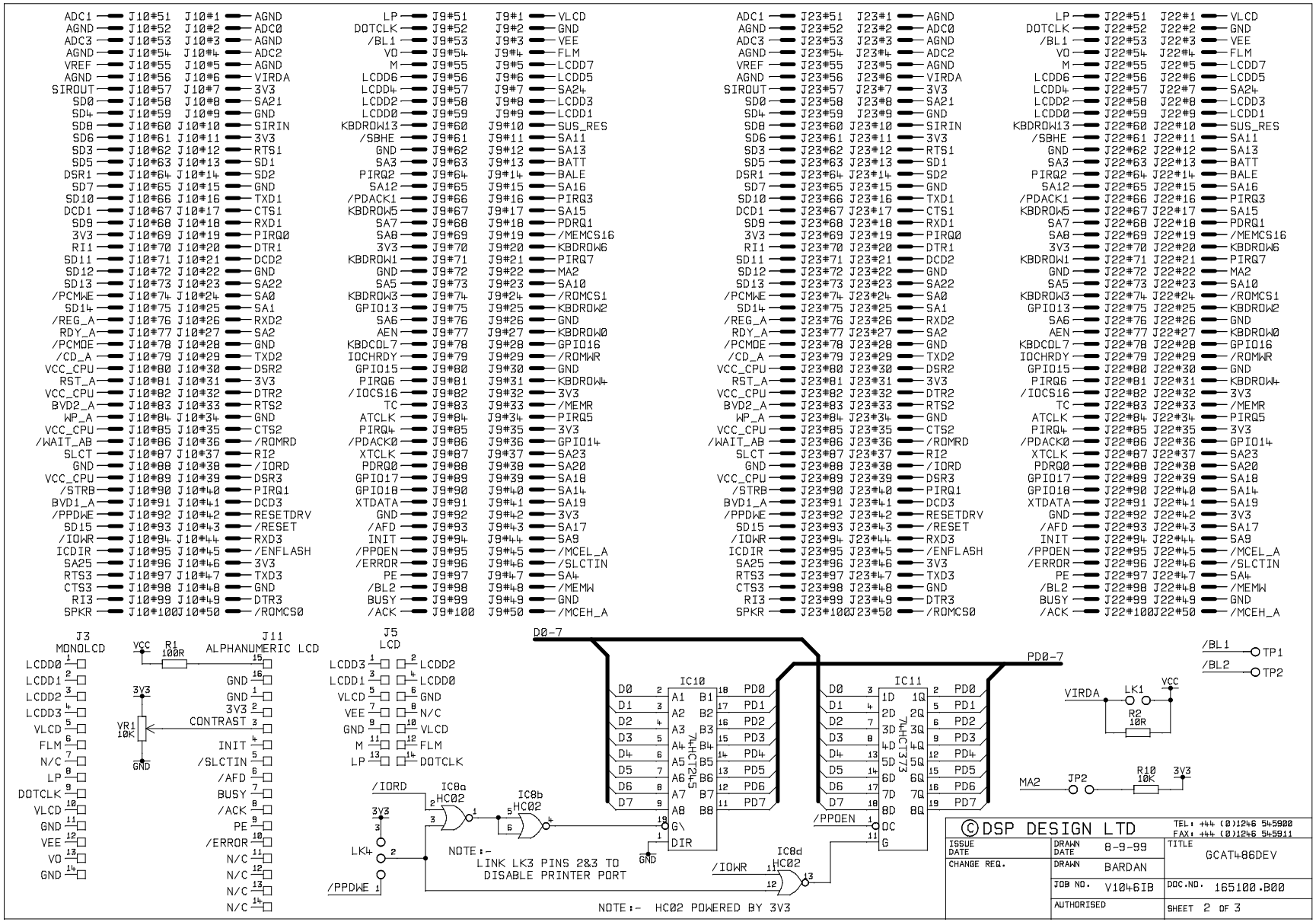
DOC.NO. 165100.B00
SHEET 1 OF 3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ADC3 J10#53 J10#3 AGND
AGND J10#54 J10#4 ADC2
VREF J10#55 J10#5 AGND
AGND J10#56 J10#6 VIRDA
SIROUT J10#57 J10#7 3V3
SD0 J10#58 J10#8 SA21
SD4 J10#59 J10#9 GND
SD8 J10#60 J10#10 SIRIN
SD6 J10#61 J10#11 3V3
SD3 J10#62 J10#12 RTS1
SD5 J10#63 J10#13 SD1
DSR1 J10#64 J10#14 SD2
SD7 J10#65 J10#15 GND
SD10 J10#66 J10#16 TXD1
DCD1 J10#67 J10#17 CTS1
SD9 J10#68 J10#18 RXD1
3V3 J10#69 J10#19 PIRQ0
RI1 J10#70 J10#20 DTR1
SD11 J10#71 J10#21 DCD2
SD12 J10#72 J10#22 GND
SD13 J10#73 J10#23 SA22
/PCMWE J10#74 J10#24 SA0
SD14 J10#75 J10#25 SA1
/REG_A J10#76 J10#26 RXD2
RDY_A J10#77 J10#27 SA2
/PCMOE J10#78 J10#28 GND
/CD_A J10#79 J10#29 TXD2
VCC_CPU J10#80 J10#30 DSR2
RST_A J10#81 J10#31 3V3
VCC_CPU J10#82 J10#32 DTR2
BVD2_A J10#83 J10#33 RTS2
WP_A J10#84 J10#34 GND
VCC_CPU J10#85 J10#35 CTS2
/WAIT_AB J10#86 J10#36 /ROMRD
SLCT J10#87 J10#37 RI2
GND J10#88 J10#38 /IORD
VCC_CPU J10#89 J10#39 DSR3
/STRB J10#90 J10#40 PIRQ1
BVD1_A J10#91 J10#41 DCD3
/PPDWE J10#92 J10#42 RESETDRV
SD15 J10#93 J10#43 /RESET
/IOWR J10#94 J10#44 RXD3
ICDIR J10#95 J10#45 /ENFLASH
SA25 J10#96 J10#46 3V3
RTS3 J10#97 J10#47 TXD3
CTS3 J10#98 J10#48 GND
RI3 J10#99 J10#49 DTR3
SPKR J10#100 J10#50 /ROMCS0
LP J9#51 J9#1 VLCD
DOTCLK J9#52 J9#2 GND
/BL1 J9#53 J9#3 VEE
VD J9#54 J9#4 FLM
M J9#55 J9#5 LCDD7
LCDD6 J9#56 J9#6 LCDD5
LCDD4 J9#57 J9#7 SA24
LCDD2 J9#58 J9#8 LCDD3
LCDD0 J9#59 J9#9 LCDD1
KBDROW13 J9#60 J9#10 SUS_RES
/SBHE J9#61 J9#11 SA11
GND J9#62 J9#12 SA13
SA3 J9#63 J9#13 BATT
PIRQ2 J9#64 J9#14 BALE
SA12 J9#65 J9#15 SA16
/PDACK1 J9#66 J9#16 PIRQ3
KBDROW5 J9#67 J9#17 SA15
SA7 J9#68 J9#18 PDRQ1
SA8 J9#69 J9#19 /MEMCS16
3V3 J9#70 J9#20 KBDROW6
KBDROW1 J9#71 J9#21 PIRQ7
GND J9#72 J9#22 MA2
SA5 J9#73 J9#23 SA10
KBDROW3 J9#74 J9#24 /ROMCS1
GPIO13 J9#75 J9#25 KBDROW2
SA6 J9#76 J9#26 GND
AEN J9#77 J9#27 KBDROW0
KBDCOL7 J9#78 J9#28 GPIO16
IOCHRDY J9#79 J9#29 /ROMWR
GPIO15 J9#80 J9#30 GND
PIRQ6 J9#81 J9#31 KBDROW4
/IOCS16 J9#82 J9#32 3V3
TC J9#83 J9#33 /MEMR
ATCLK J9#84 J9#34 PIRQ5
PIRQ4 J9#85 J9#35 3V3
/PDACK0 J9#86 J9#36 GPIO14
XTCLK J9#87 J9#37 SA23
PDRQ0 J9#88 J9#38 SA20
GPIO17 J9#89 J9#39 SA18
GPIO18 J9#90 J9#40 SA14
XTDATA J9#91 J9#41 SA19
GND J9#92 J9#42 3V3
/AFD J9#93 J9#43 SA17
INIT J9#94 J9#44 SA9
/PPOEN J9#95 J9#45 /MCEL_A
/ERROR J9#96 J9#46 /SLCTIN
PE J9#97 J9#47 SA4
/BL2 J9#98 J9#48 /MEMW
BUSY J9#99 J9#49 GND
/ACK J9#100 J9#50 /MCEH_A
ADC1 J23#51 J23#1 AGND
AGND J23#52 J23#2 ADC0
ADC3 J23#53 J23#3 AGND
AGND J23#54 J23#4 ADC2
VREF J23#55 J23#5 AGND
AGND J23#56 J23#6 VIRDA
SIROUT J23#57 J23#7 3V3
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SD4 J23#59 J23#9 GND
SD8 J23#60 J23#10 SIRIN
SD6 J23#61 J23#11 3V3
SD3 J23#62 J23#12 RTS1
SD5 J23#63 J23#13 SD1
DSR1 J23#64 J23#14 SD2
SD7 J23#65 J23#15 GND
SD10 J23#66 J23#16 TXD1
DCD1 J23#67 J23#17 CTS1
SD9 J23#68 J23#18 RXD1
3V3 J23#69 J23#19 PIRQ0
RI1 J23#70 J23#20 DTR1
SD11 J23#71 J23#21 DCD2
SD12 J23#72 J23#22 GND
SD13 J23#73 J23#23 SA22
/PCMWE J23#74 J23#24 SA0
SD14 J23#75 J23#25 SA1
/REG_A J23#76 J23#26 RXD2
RDY_A J23#77 J23#27 SA2
/PCMOE J23#78 J23#28 GND
/CD_A J23#79 J23#29 TXD2
VCC_CPU J23#80 J23#30 DSR2
RST_A J23#81 J23#31 3V3
VCC_CPU J23#82 J23#32 DTR2
BVD2_A J23#83 J23#33 RTS2
WP_A J23#84 J23#34 GND
VCC_CPU J23#85 J23#35 CTS2
/WAIT_AB J23#86 J23#36 /ROMRD
SLCT J23#87 J23#37 RI2
GND J23#88 J23#38 /IORD
VCC_CPU J23#89 J23#39 DSR3
/STRB J23#90 J23#40 PIRQ1
BVD1_A J23#91 J23#41 DCD3
/PPDWE J23#92 J23#42 RESETDRV
SD15 J23#93 J23#43 /RESET
/IOWR J23#94 J23#44 RXD3
ICDIR J23#95 J23#45 /ENFLASH
SA25 J23#96 J23#46 3V3
RTS3 J23#97 J23#47 TXD3
CTS3 J23#98 J23#48 GND
RI3 J23#99 J23#49 DTR3
SPKR J23#100 J23#50 /ROMCS0
LP J22#51 J22#1 VLCD
DOTCLK J22#52 J22#2 GND
/BL1 J22#53 J22#3 VEE
VD J22#54 J22#4 FLM
M J22#55 J22#5 LCDD7
LCDD6 J22#56 J22#6 LCDD5
LCDD4 J22#57 J22#7 SA24
LCDD2 J22#58 J22#8 LCDD3
LCDD0 J22#59 J22#9 LCDD1
KBDROW13 J22#60 J22#10 SUS_RES
/SBHE J22#61 J22#11 SA11
GND J22#62 J22#12 SA13
SA3 J22#63 J22#13 BATT
PIRQ2 J22#64 J22#14 BALE
SA12 J22#65 J22#15 SA16
/PDACK1 J22#66 J22#16 PIRQ3
KBDROW5 J22#67 J22#17 SA15
SA7 J22#68 J22#18 PDRQ1
SA8 J22#69 J22#19 /MEMCS16
3V3 J22#70 J22#20 KBDROW6
KBDROW1 J22#71 J22#21 PIRQ7
GND J22#72 J22#22 MA2
SA5 J22#73 J22#23 SA10
KBDROW3 J22#74 J22#24 /ROMCS1
GPIO13 J22#75 J22#25 KBDROW2
SA6 J22#76 J22#26 GND
AEN J22#77 J22#27 KBDROW0
KBDCOL7 J22#78 J22#28 GPIO16
IOCHRDY J22#79 J22#29 /ROMWR
GPIO15 J22#80 J22#30 GND
PIRQ6 J22#81 J22#31 KBDROW4
/IOCS16 J22#82 J22#32 3V3
TC J22#83 J22#33 /MEMR
ATCLK J22#84 J22#34 PIRQ5
PIRQ4 J22#85 J22#35 3V3
/PDACK0 J22#86 J22#36 GPIO14
XTCLK J22#87 J22#37 SA23
PDRQ0 J22#88 J22#38 SA20
GPIO17 J22#89 J22#39 SA18
GPIO18 J22#90 J22#40 SA14
XTDATA J22#91 J22#41 SA19
GND J22#92 J22#42 3V3
/AFD J22#93 J22#43 SA17
INIT J22#94 J22#44 SA9
/PPOEN J22#95 J22#45 /MCEL_A
/ERROR J22#96 J22#46 /SLCTIN
PE J22#97 J22#47 SA4
/BL2 J22#98 J22#48 /MEMW
BUSY J22#99 J22#49 GND
/ACK J22#100 J22#50 /MCEH_A
J3
MONOLCD
LCDD0 LCDD1 LCDD2 LCDD3 VLCD FLM N/C LP DOTCLK VLCD GND VEE VO GND
VCC R1 100R
3V3 VR1 10K GND
J11
ALPHANUMERIC LCD
GND GND 3V3 CONTRAST INIT /SLCTIN /AFD BUSY /ACK PE /ERROR N/C N/C N/C N/C
J5
LCD
LCDD3 LCDD2 LCDD1 LCDD0 VLCD GND VEE N/C GND VLCD M FLM LP DOTCLK
D0-7
PD0-7
IC10
74HC245
D0 D1 D2 D3 D4 D5 D6 D7
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
G\
DIR
GND
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
IC11
74HC373
1D 2D 3D 4D 5D 6D 7D 8D
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
OC
G
/PPOEN
/BL1 TP1
/BL2 TP2
VIRDA LK1 VCC R2 10R
MA2 JP2 R10 10K 3V3
/IORD IC8a HC02 IC8b HC02
3V3 LK4
/PPDWE
NOTE:- LINK LK3 PINS 2&3 TO DISABLE PRINTER PORT
/IOWR IC8d HC02
NOTE:- HC02 POWERED BY 3V3
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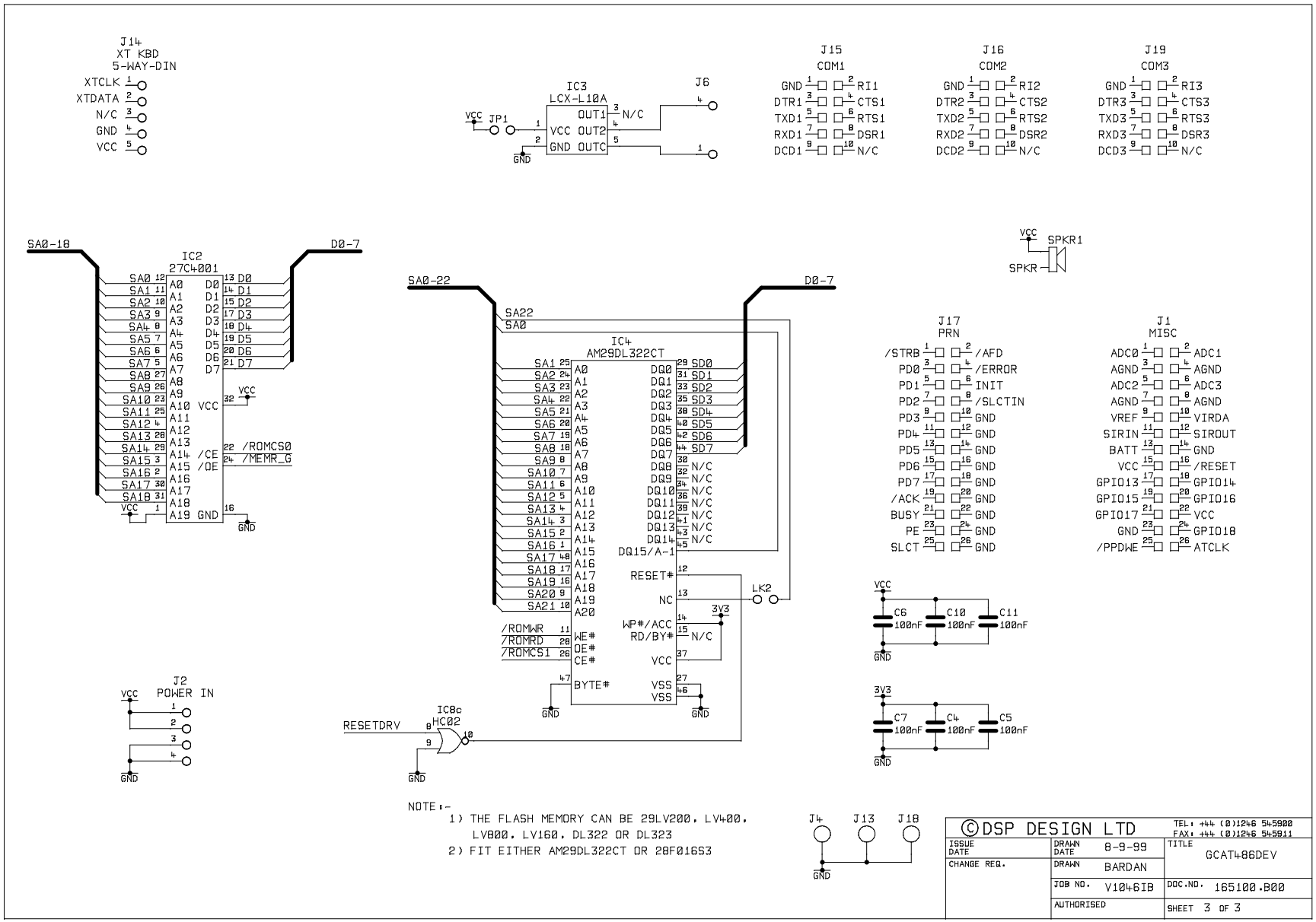

NOTE:-

1) THE FLASH MEMORY CAN BE 29LV200, LV400, LV800, LV160, DL322 OR DL323
2) FIT EITHER AM29DL322CT OR 28F016S3

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APPENDIX J: MOTHERBOARD DESIGN

This appendix contains some notes on the design of a “motherboard”, into which the GCAT486 can be plugged, as a PC-compatible component for a more complex system.

J.1 OVERVIEW

The GCAT486 can easily be integrated into larger systems, by plugging it onto another printed circuit board. In this manual we refer to this other user-designed board as a motherboard, which perhaps implies a large and complex PCB. However, a “motherboard” by this definition may also be a simple board, perhaps just adding a battery power supply circuit, or breakout connectors for an LCD and keypad.

J.2 CONNECTORS AND MECHANICAL CONSIDERATIONS

The GCAT486 plugs onto a motherboard through two 100-way connectors. These are Hirose FX8 family connectors. The connector on the GCAT486 is the FX8-100S-SV. The connector required on the motherboard is a Hirose FX8-100P-SV or FX8-100P-SV1. Using the FX8-100P-SV results in a 3mm distance between the faces of the two PCBs. The FX8-100P-SV1 results in a 4mm space. In the UK these connectors are available from Flint Distribution.

Figure C4 in Appendix C gives the dimensions of the GCAT486 and the positions and PCB footprint of the FX8 connectors. It is important to note that this drawing is looking down onto the processor side of the GCAT486, as though it has been positioned on top of the motherboard. The connector footprint details are of the connector which is to be used on the motherboard. Another way of considering the drawing is to imagine that it is the drawing of a motherboard of exactly the same size as the GCAT486.

Care should be taken with positioning any components between the two PCBs. Either 3mm or 4mm clearance is available, but of course some of that has already been taken up by components on the GCAT486.

The connectors will hold the GCAT486 onto the motherboard in laboratory conditions, but the two boards need to be secured with spacers and screws for production systems. Mounting hole positions are shown in Figure C4.

The positions of pins 1, 50, 51 and 100 are shown in Figure C4.

J.3 CIRCUIT DESIGN

Appendix H includes the circuit diagram of the GCAT486DEV development system. It also provides a description of this circuit. This should be studied carefully users who are designing their own motherboards, especially for connection with circuitry operating at 5V. Note that the GCAT486DEV is an old product which has been superceded by the TCDEVPLUS. However, most of the circuitry used on the GCAT486DEV is also present on the TCDEVPLUS, and the circuit of the

GCAT486DEV remains a good circuit for users to use as the basis of their own designs.

Section 4 in this manual discusses the GCAT486's ISA bus interface. This section should be read carefully by users who need to connect with circuitry on the ISA bus. This section describes aspects of mixing 3.3V and 5V systems, and the GCAT486DEV circuit diagram shows the data bus buffer required for this.

Design of ISA bus systems is beyond the scope of this manual. Users should obtain books describing ISA bus circuit design. Some aspects of ISA bus design are worth repeating:

- The signal AEN must be included in the design of I/O address decoders. This signal is used to distinguish between I/O transfers, when it is low, and DMA transfers, when it is high.
- If 16-bit memory or I/O transfers are required, the peripheral must signal to the processor that it is capable of performing a 16-bit transfer by pulling low the /MEMCS16 or /IOCS16 signal.
- If there is a possibility of more than one device asserting /MEMCS16 or /IOCS16 then these signals should be pulled low by open-drain transistors, and a low value pull-up resistor (say 330R to 1K) must be fitted to pull the signal back high.
- The address decoding for /MEMCS16 and /IOCS16 must NOT include the data strobes /MEMR, /MEMW, /IORD or /IOWR.
- Interrupts are active high, edge triggered. The interrupt request should normally be asserted by the peripheral and cleared by the interrupt service routine.
- If a second interrupt event occurs before the first interrupt is serviced then the IRQ pin will make only one low to high transition, and so the second interrupting event will not generate a second interrupt. Software must be written to cope with this eventuality.
- The RESETDRV signal should be used as a reset. It is active high and an output from the GCAT486. If you want to generate a reset to the GCAT486 then use the /RESET signal. This is active low and should be driven by an open drain driver.
- The GCAT486 does not implement pull-up resistors on SD0-15, in order to save power. In fact, the Elan chip has weak pull-down resistors on the data bus. Thus software will not see the data bus as containing 0FFh if reading from an unoccupied location. If this is an issue then pull-up resistors may be added, though possibly at the expense of power consumption.

In some designs it may be possible to fit only one of the two 100-way connectors. Appendix E gives the pin assignments of the connectors. The signals on the two connectors contain all of the signals on the ribbon cable connectors, plus signals required for PC Cards and ISA bus expansion. Since all of the signals on the ribbon cable connectors are also present on the 100-way connectors, if the GCAT486 is plugged into a motherboard there is no need to make use of the ribbon cable connectors.

For best noise and EMC performance the motherboard PCB should be multilayer, with internal power and ground planes. All power and ground pins of the connectors should be connected. Users should take due care with the layout of the circuit, by keeping tracks as short as possible, keeping clocks away from other signals, and keeping the data strobes away from other signals, as far as possible. DSP Design are pleased to advise on aspects of customers' motherboard designs.

All +3.3V and GND pins on the 100-way connectors should be connected to the +3.3V and GND power plane on your PCB. As mentioned in section 2.6, the VCC_CPU pins are also normally connected to the +3.3V plane. Unless you need to drive VCC_CORE from a different voltage you should also connect VCC_CORE pins to 3.3V on your motherboard.

Note that some pins are not 5V tolerant, so should not be driven above the +3.3V power supply rail. These include: PIRQ0, PIRQ1, GPIO_CS2, GPIO_CS3, GPIO13 to GPIO19, SIRIN, SIROUT, KBD_ROW0-6, /BL1, /BL2, SUS_RES and /RESET.

J.4 LOW-POWER DESIGN

Many users of the GCAT486 will have been attracted by its very low power consumption and will want to use it in battery operated equipment. While a tutorial in low power design is beyond the scope of this manual, a few points are worth making:

- Choose your components carefully, optimising each for low power.
- Remember that pull-up resistors attached to logic 0 signals will dissipate power.
- Power consumption in CMOS circuitry tends to rise in proportion with clock frequency, so choose the lowest clock speeds possible and consider shutting clocks off if appropriate.
- Power consumption tends to rise with the square of the supply voltage, so avoid 5V circuitry unless necessary.
- If mixing different supply rails then ensure that a device powered by a low power supply rail is not fed with a logic level of a higher voltage, unless the device is specifically capable of operating with high input voltages.
- Consider removing power altogether from circuitry which is not always required. However, this may result in a special case of the mixed power supply situation discussed above – in this case the lower supply voltage is 0V. In most cases this will result in the logic signal sourcing power to the powered-down device through its logic pins – something that must be avoided at all costs.
- The Elan places its pins in known states when it enters suspend. In many cases these are logic 0 levels, which makes it possible to then power off attached circuitry. AMD's documentation discusses the reset and suspend state of the Elan pins.
- Some of the Elan's GPIO pins can be programmed to make a transition from one state to another when it moves from one power state to another. This could be of use in powering off circuitry.

J.5 GPIO PINS

The Elan's GPIO pins may be of use in motherboard designs. The GPIO pins are described in section 8. Remember that most GPIO pins have alternative functions, so some GPIO pins may not be available in your configuration.

The GPIO pins can operate as digital inputs and outputs, but also in a number of other ways which are beyond the scope of this manual. Users should refer to AMD's Elan documentation for further details.

The GCAT486-specific BIOS interrupt calls, described in section 6.11, provide ways in which the GPIO pins may be set as inputs or outputs, and read or set to a logic level. These calls also provide a method of accessing all of the Elan's Chip Setup and

Control (CSC) Registers. This powerful mechanism must be used with considerable care, as it gives the user considerable control over the Elan processor, and therefore it is easy to crash the GCAT486 by inappropriate use.

The Elan has four programmable chip select address decoders – two for I/O space and two for memory space. The address decoder outputs can be routed to any of GPIO_CS0 to GPIO_CS14. This may be of use to some users. However, the two I/O space address decoders are already in use for the COM2 and COM3 UARTs, so are not normally available. If one or other of the UARTs are not used then the I/O space address decoders are available for users. The programming of the CSC registers for this use is beyond the scope of this manual.

APPENDIX K: FAULT REPORTING

DSP Design makes every effort to ship products and documentation which are completely free from faults, design errors and inconsistencies. Sometimes, however, problems do show up in the field. To help us put these right as quickly and efficiently as possible, we need as much information as possible from you, the user.

For this reason we have included here a “Product Fault Report” form. If you ever have cause to return a board for repair, or if you detect an error in the documentation, we would appreciate it if you could fill in the form on the next page, or a copy of it, and return the form to your supplier.

Prior to returning a faulty product, please check the following:

1. The board has been correctly configured for the intended application (see earlier appendix for board installation details).

2. The power supplies are providing correct voltage levels.

3. Cabling to the board is sound and connected correctly.

4. Other cards in the system are known to be correctly configured and functioning.

5. **PLEASE RETURN THE BOARD TO US IN EXACTLY THE SAME CONFIGURATION AS IT FAILED IN.**

Your help with this will enable us to sort out your problem more quickly. Thank you.

PRODUCT FAULT REPORT

CUSTOMER INFORMATION	PRODUCT INFORMATION
COMPANY NAME:	PRODUCT/DOCUMENT:
INDIVIDUAL CONTACT:	SERIAL NO:
PHONE NO:	DATE OF RETURN:

SYMPTOMS OBSERVED /DOCUMENTATION ERRORS (as applicable):

IN WHAT CONFIGURATION IS THE BOARD USUALLY USED? (WHAT OTHER BOARDS, WHAT SOFTWARE ETC.)?

FOR DSP DESIGN USE ONLY:

PRODUCT TEST REPORT:

DATE OF RECEIPT: REPAIRED BY:

CHARGES TO BE INVOICED: £

DATE OF RETURN: RETURNED BY: