Sprint 1 – power supply

## Task – “get the circuit plan” (“Schaltplan besorgen”)

To get the circuit plan we asked Mr. Strahnen if he could provide the files and data from the BumbleBee-Project (from the last Semester), what he then did of course.

These files contained an EAGLE ® formatted plan of the circuit.

**Task – “check the board” (“Board 1:1 prüfen”)**

We knew that the power supply circuit was generated with a web app by Texas Instruments ® called WEBENCH® System Power Architect. At first we created an account to use the tool and generated a new circuit plan with the following parameters:

* V\_in\_max : 25 V
* V\_in\_min : 13 V
* V\_out : 12 V
* I\_out : 5 A

These parameters are given by the maximum and minimum output of the accumulators (V\_in) we use and the SoC-Board restrictions which are 12V input voltage and 3.5A output current. We added another 1.5A for provision.

After that, we compared our new plan with the plan, the last project used. We figured out that they are the same so there cannot be the problem.

The next step was to compare all the components and the voltage control IC. There we saw that the last group, which designed and populate two circuit boards, used different ICs on each of them. So this cannot be correct.

Other big error sources are the SMD parts. The problem with them is that we cannot easily test them. There for we bought all the parts in DIP norm and built the circuit on a plugboard. The voltage control IC wasn’t available in DIP norm so we mounted it on an adapter to use it on the plug board.

Improvement suggestions for the last board