

Jan 27 (Wed), 2021 Harry LI
CMPE240 Welcome to 240
Section 2

Email: hua.li@sjsu.edu
Office Hours: M.W. 4:30-5:30 pm.
Zoom Based
Greensheet github/hualili/
CMPE240/2018F

References:

1. Greensheet on github
(650) 400-1116 Text message
Prereq Requirements 180D

Advanced Microprocessor Systems

Smart phones & RISC Architecture

5G, Edge AI → IoT, AI → GPU

Prototype System

Fully Functional Microprocessor
System

Action Items:

1. github/hualili/cmpe240
2. Prereq Requirements, 180D
3. LPC1769 CPU module
digi-key.com OR mouser.com

Handson: multiple projects, 3 mile
Stones

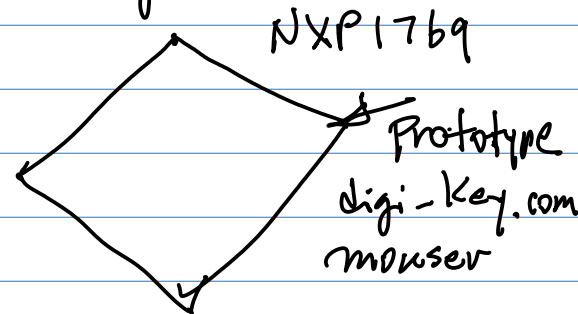
4. CPU Datasheet 5. MCU expresso

CMPE240 Feb 1 (Mon) 1/
Today's Topics: 1° System Level
Architecture — LPC1769
Ref: github/hualili/cmpe240/

2018F-102 2° CPU Data-
Sheet

Example:

1° CPU module @ center of the
System Layout Design



2° Wirewrapping Board
Dimension: 6" x 4"

with Through-Holes,
Architectural and one side of Board
Aspects whose through-Holes

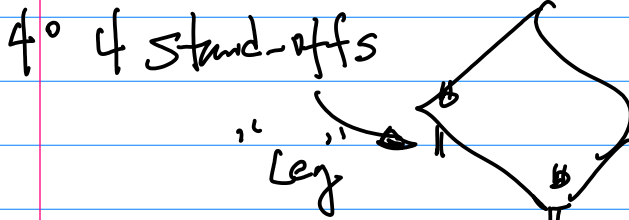
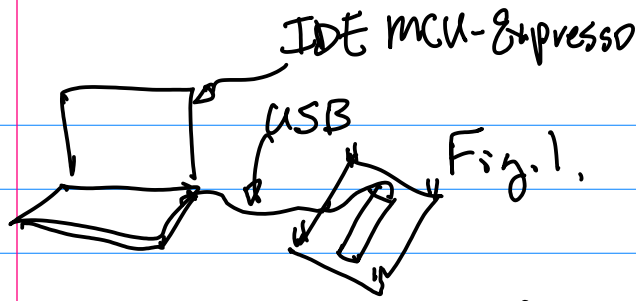
with metal plating; ~~But~~
not the entire Board (just
the through-Holes)

3° PWR CKT: J1 Connector

Right Angle Connector;
S/W Toggle Switch; IC
Regulator 7805, 1117

Red LED 4-10mA
Resistor, Cap. (LPF)

NXP.com Note: Debug/Development
No External PWR CKT



Ref: CPU module Design. pdf
github, Rev. D. OR higher
From the Datasheet, Two tables
on Each Side of the CPU module
First, Left Side, the outer table
is for mbed, Not interested.

Naming Convention:

- ① CPU pin is named identical
as the name appeared in the
CPU Datasheet;
- ② The physical connector Label(s)
are given on the SCH to match
up the physical Board

Question: Find the pin for GND

From SCH,

Connectivity Table

Functional Pin	Physical Pin	Note
GND	J2-1	
VIN	J2-2	4.5~5.5VDC

Enumeration of the pin(s)
CPU pin (1st pin) starts as
"0";

CPU Datasheet 2018S-3-
UM10360
CPU Architecture, PP.9

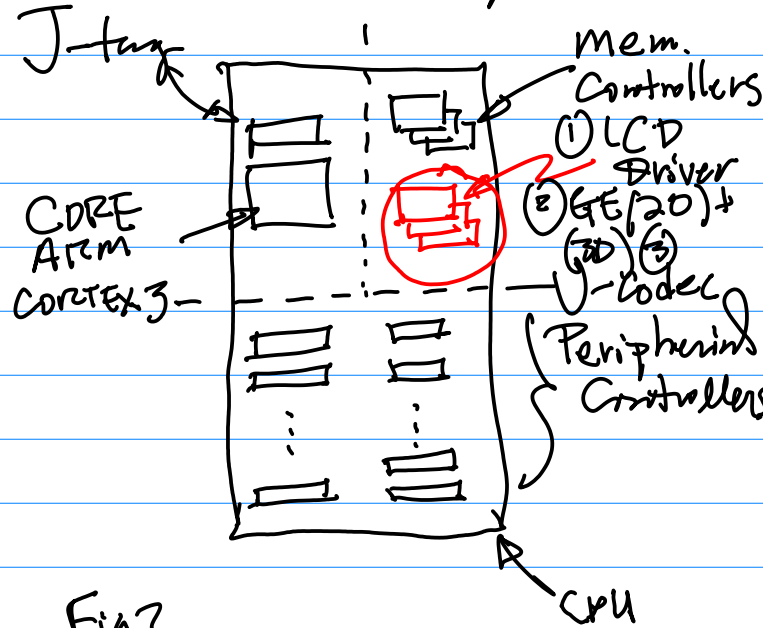


Fig 2.

Peripheral Controllers (SCH, ^{CPU} Datasheet)

Feb 3. CMPE240 HARRY LI

Note: 1° Have your Video when
Participating the Class; 2°
Honest Pledge Form/Sign
CANVAS submission By
Sat. 11:59 pm;

Today's Topics: 1° CPU
Architecture / CPU Datasheet
SCH; 2° Homework Design
of prototype Board

Peripheral Controller

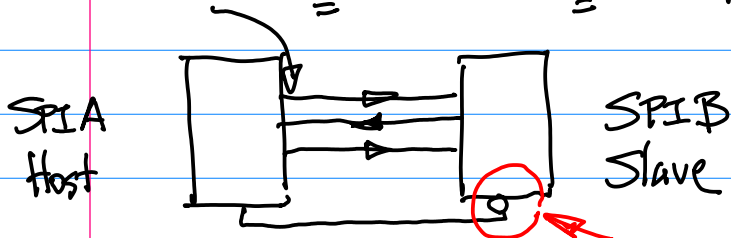
Ref: ① CPU Datasheet, pp.9.
② SCH

Example: From SCH.

1° SPI Serial Peripheral Interface

Note: RESET pin has to be Included in
Our Prototype Design

MOSI: Master Output Slave Interface



MISO: Master Input Slave Output

SCK: Serial Clock (0)

SSEL: Enable SPI Controller (on
the Slave Side, Active Low)

Note: MOSI_x, MISO_x, SCK_x,
SSEL_x, where x stands for the
xth of SPI Controller

Question: Find Number of SPI I/F
for this LPC1769 CPU?

Two SPI I/F SPI0, SPI1

2° UART (Serial I/F), Note RS232

TX (Transmitter)

Rx (Receiver)

3rd pin has to be a part of it: GND

Pd.0; Pd.1

Multiplexing, TX/SDA

Init & Config for Special
Purpose Registers will define
which function the pin will
I/O assume.

Action 1: Homework —
Read SCH, generate a
table for all peripheral
Controllers

Table: CPU Datasheet, pp.9

Table 2: SCH, to find subset
of the I/O Controller.

Advanced Feature:

G.E. Graphics Engine

Example: Broadcom
Pie3BT, 4 GE

NDA: GPU (Graphics
Processing Unit)

NAND 128 GPU.

TX2, 6 CPU +

256 GPU

"3+1"
pins

MOSI/MISO/SCK
SSEL (Enable)

Software Implementation


for G.E (2D, 3D)

Basic Concepts.

1° RISC (Reduced Instruction

Set Computer) { ARM
MIPS

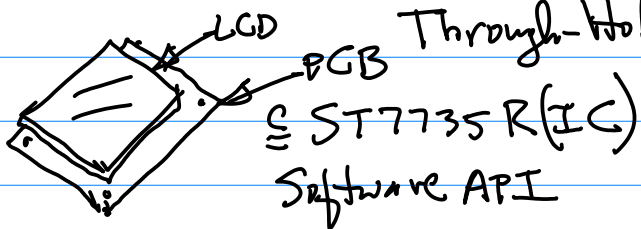
32 Bit

Datasheet for 7805, Cmps are those with Polarity "  "

Bill of the material to Build G.E.

SPI I/F Based Color LCD Device. a SPI (Not I2C)

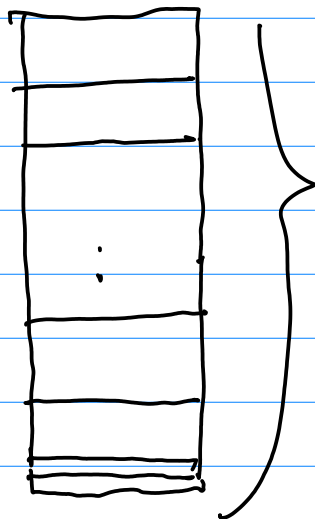
b Module - Connector



2-3 weeks

CPU Architecture Discussion

1^o memory map



$$2^{32} = 4 \text{ GB}$$

3^o memory Bank: 8

$$4 \text{ G}/8 = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2 / 2^3$$

$$= 2^9 \cdot 2^{10} \cdot 2^{10} = 512 \text{ M}$$

Question: How many Bits from the Addr. Bus do we need to uniquely define each memory Through-Hole Bank? 3 Bits

$$\begin{array}{ccccccc} a_{31} & a_{30} & a_{29} & a_{28} & \dots & a_1 & a_0 \\ \uparrow & & & & & & \uparrow \\ 0 & 0 & 0 & 1 & & & \text{LSBit} \end{array}$$

1st BANK

Starting Addr. of the 1st Bank,

Little Endian

0x0000_0000

What is the Starting Address of the 2nd Bank:

$$\begin{array}{cccc} a_{31} & a_{30} & a_{29} & a_{28} \\ 0 & 0 & 1 & 0 \end{array}$$

$$\underline{0010}$$

0x2000_0000 ; 2nd Bank

0x4000_0000 ; 3rd Bank

CMPE240 Feb10(Wed)

Ref: github/hualili/CMPE240

... 2018F-107-LEC6PP

Homework 1. Form 4-Person Team

First, Last Name, Last 4 Digits SID

E-mail Address → Submission

2^o Byte Addressable Machine
~ whose Smallest mem. cell
with unique address is a
Single Byte

Via Email & Canvas By Thursday

11:59 Subject Title → Team Coordinator

Document Name

E-mail Submission.

Homework 2: (1 pt)

Requirements (1) Build a prototype Board, (2) Write a first program

Turn on/off LED "Hello, the world"

Note: Use Prototype Board to Build GPP I/O to Drive LED on/off

(3) Build I/O Testing Circuit, the CKT input is from GPP (GPI/O)

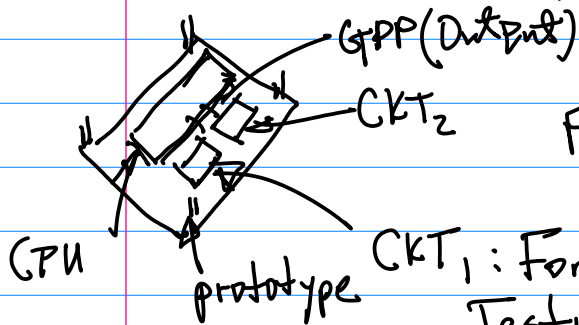


Fig. 1.

CKT₁: For Output Testing

"1" to Turn on LED

"0" to Turn off LED

CKT₂: For Input Testing

Input "1", Toggle Switch to connect GPP Input to V_{CC} (via a Resistor)

Input "0", Toggle the switch to GND (via Resistor)

(4) Write one page Report (IEEE paper format) white paper Due on CANVAS

Due 2 weeks from Today, Feb 24.

Submission:

1° Project Exported

Document Name First-Last-CMP240 in Zip format

2° White paper, Report

3° Video Clip (up to 5 ~ 7

Seconds) Short please.

Example: From PPT on GPP I/F.

Identify CPU GPP pin

P0.3 J2-22 Input

P0.21 J2-23 Output

Consider the Output Testing CKT,

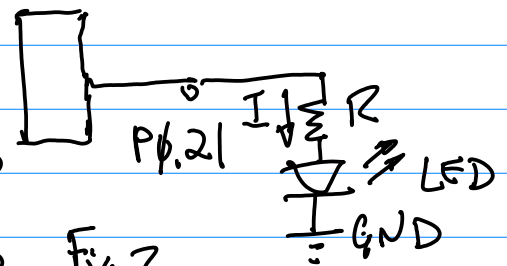


Fig. 2

$$V_{CC} = IR + V_{LED} \quad \dots (1)$$

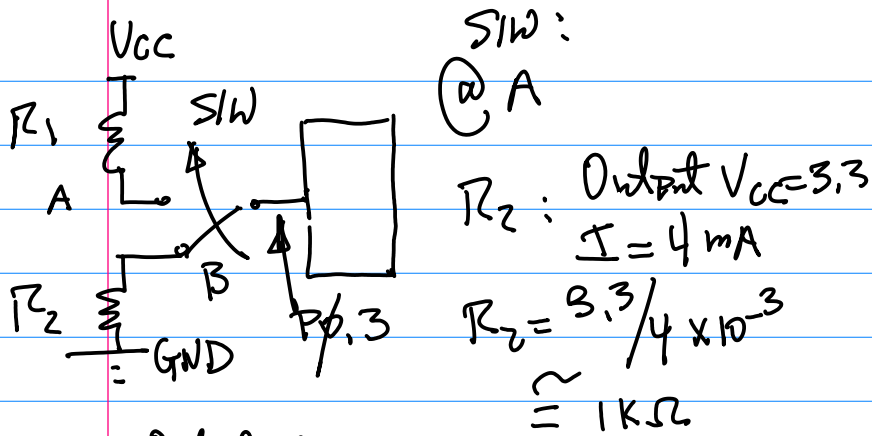
$$V_{CC} = 3.3 \text{ VDC}$$

$$I \cong 10 \text{ mA}, V_{LED} = 1.2 \text{ VDC}$$

$$3.3 = 10 \times 10^{-3} R + 1.2$$

$$R = (3.3 - 1.2) / 10^{-2} = 210 \Omega$$

Now, Let's Design CKT₂



\$R_1\$: Output, GND
 $V_{CC}/R_1 = 4\text{ mA}$, $\frac{3.3}{4\text{ mA}} \approx 1\text{ K}\Omega$

System Level & Software Design

1st GPU Architecture \rightarrow mem. map
 Peripheral Controllers BANK of
 GPP Controller a PWR-up Address
 1st Address

0X0000_0000 GPU when powered up

'It will fetch the 1st Executable Instruction' at this Location

