Jan 27 (Wed), 2021 | Harry Li

CMPE240 Welcome to 240 Section 2

Email: hua.li@sjsu.edu
Office Hours: M.W. 4:30-5:30 pm.
~~Zoom Based~~
Greensheet github/hualili
CMPE240/2018F

References:
1. Greensheet on github
(650) 400-1116 Text message
Prerequit Requirements 180D

Advanced Microprocessor Systems
Smart phones & RISC Architecture
5G, Edge AI → IoT, AI → GPU Architectural Aspects

Prototype System
Fully Functional Microprocessor System

Action Items:
1° github/hualili/cmpe240
2° Pre-requit Requirements, 180D
3° LPC1769 CPU module
digi-key.com OR mouser.com

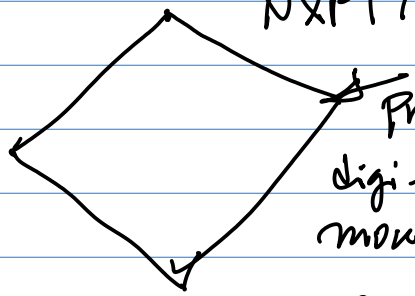
Handson: multiple projects, 3 mile stones

4° CPU Datasheet 5° MCU expresso

CMPE240 Feb1 (Mon) 1/

Todays Topics: 1° System Level Architecture — LPC1769
Ref: github/hualili/cmpe240/2018F-102 2° CPU Data-Sheet

Example:
1° CPU Module @ center of the System Layout Design
NXP1769



2° Wirewrapping Board
Dimension: 6"x4"
with Through-Holes, and one side of Board whose through-Holes with metal plating; But not the entire Board (just the throug-Holes)

3° PWR CKT: J1 Connector
Right Angle Connector; S/W Toggle Switch; IC Regulator 7805, 1117
Red LED & 10mA Resistor, Cap. (LPF)
Note: Debug/Development No External PWR CKT
NXP.com

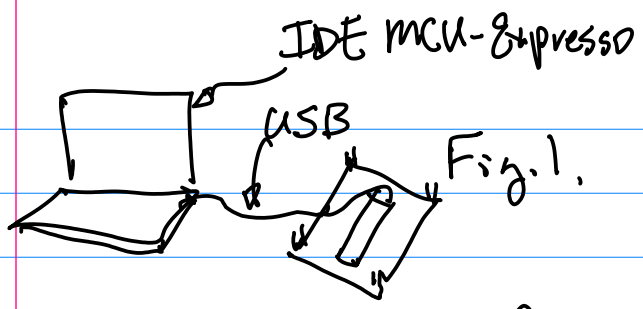
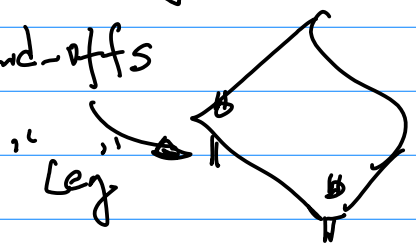


Fig. 1.



Ref: CPU module Design. pdf
github, Rev. D. or higher

From the Datasheet, Two tables on Each side of the CPU module
First, Left side, the outter table is for mbed, Not interested.

Naming Convention:

① CPU pin is named identical as the name appeared in the CPU Datasheet;

② The physical connector Label(s) are given on the SCH to match up the physical Board

Question: Find the pin for GND From SCH,

Connectivity Table

Connector J2 Position

Functional Pin	Physical Pin	Note
GND	J2-1	
VIN	J2-2	4.5~5.5VDC

Enumeration of the pin(s)
CPU pin (1st pin) starts as "0";

CPU Datasheet 2018S-3-UM10360
CPU Architecture, pp. 9

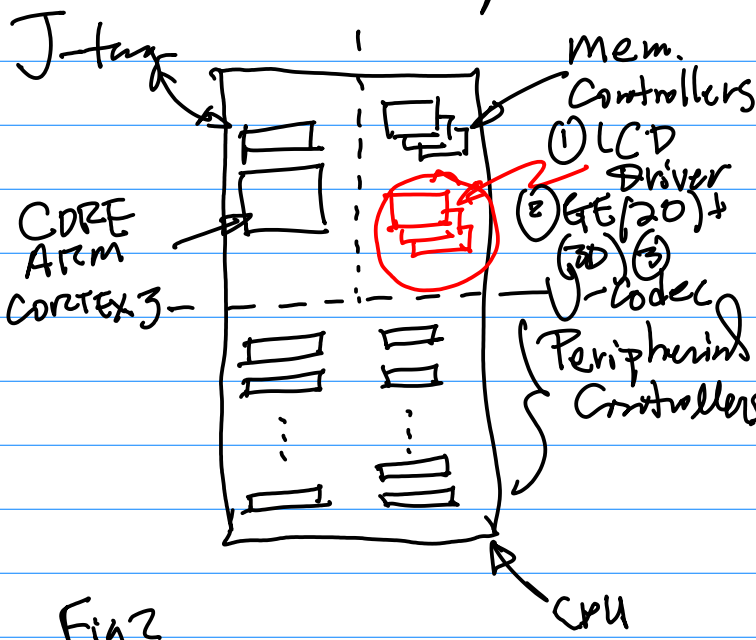


Fig 2.

Peripheral controllers (SCH, CPU Datasheet)

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Note: 1° Have your video when Participating the Class; 2° Honest Pledge Form/Sign CANVAS submission By Sat. 11:59 pm;

Today's Topics: 1° CPU Architecture/CPU Datasheet SCH; 2° Homework Design of prototype Board

Peripheral Controller

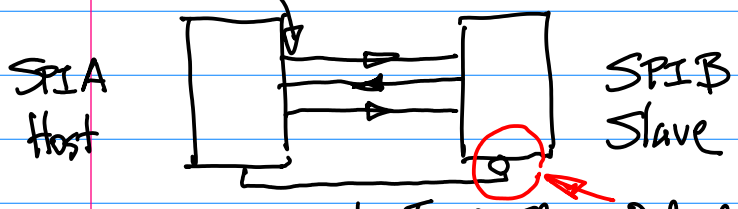
Ref: { ① CPU Datasheet, pp.9.
② SCH

Example: From SCH.

1° SPI Serial Peripheral Interface

Note: RESET pin has to Included in Our Prototype Design

MOSI: Master Output Slave Input



MISO: Master Input Slave Output

SCK: Serial Clock (O)

SSEL: Enable SPI Controller (ON the Slave Side, Active Low)

Note: $MOSI_x$, $MISO_x$, SCK_x, $SSEL_x$, where x stands for the xth of SPI Controller

Question: Find Number of SPI I/F for this LPC1769 CPU?

Two SPI I/F SPI0, SPI1

2° UART (Serial I/F), Note RS232

{ TX (Transmitter)
Rx (Receiver)

3rd pin has to Be a part of it: GND

P0.0; P0.1

multiplexing, TX/SDA

Init & Config for Special Purpose Registers will define which function the pin will I/O assume.

Action 1: Homework — Read SCH, generate a table for all Peripheral Controllers

{ Table: CPU Datasheet, pp.9
Table2: SCH, to find subset of the I/O Controller.

Advanced Feature:

G.E. Graphics Engine

Example: Broadcom

Pie3Bt, 4 → GE

NUDA: GPU (Graphics Processing Unit)

NAND 128 GPU, TX2, 64 GPU + 256 GPU

"3+1" Pins

{ MOSI/MISO/SCK
SSEL (Enable)

Software Implementation for G.E (2D, 3D)

Basic Concepts.

1° RISC (Reduced Instruction Set Computer) { ARM MIPS

32 Bit

Address Bus (Uni-direction) : 32 Bit
Data Bus (Bio-direction) : 32 Bit
Register Files { General Purpose Register
Special Purpose Reg.
SPRs

Memory : $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2} = 4$ GB

1K 1M 1G Byte

Note:
1° Byte Addressable
Smallest memory with an Unique Address is a Single Byte

CMPE240 Feb 8 (Mon), HARRY LI

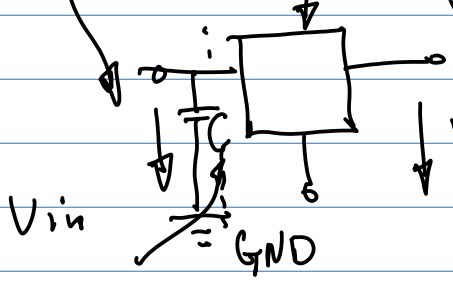
Today's Topics:
1° Bill of material (github)
2° CPU Architecture
3° Preparation to Bring up your CPU, MCU Expresso

Two Step Process to Prepare for Prototype Board,
Step1: CPU module LPC1769
Wire wrapping (Prototype Board)
"Glue" Logic Resistor, Caps, PWR Regulator IC (7805), Red LED, Stand-offs

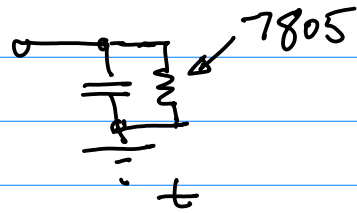
CMOS CPU ARM
Vout 3.3VDC, 10~30mA
Estimate 5.3V / 10mA, 3.3V / 30mA
3.3×10^{2} , 1.1×10^{2}
Ops.

Wall mount Adaptor
110ACV →
7.5VDC
1000~1500mA

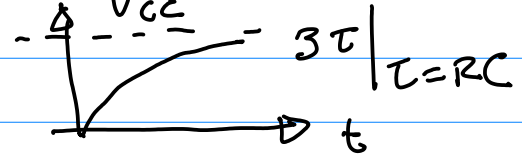
Note: PWR Regulator IC, 7805 (~2VDC Volt drop)



To Cap to Realize LPF.



$V_{cc}(1 - e^{-\frac{t}{RC}})$ ... (1)



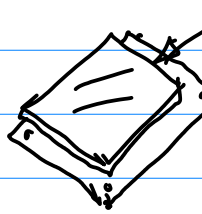
4.7 MF
2nd Part for Caps : 7805

Datasheet for 7805, Caps are those with Polarity "⊥" / "T"

Bill of the Material to Build G.E.

SPI I/F Based Color LCD Device. a SPI (Not I2C)

b Module — Connector Through-Hole

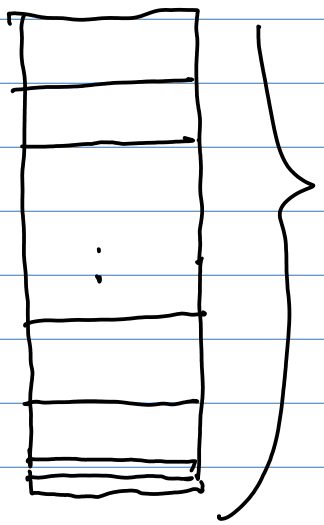


≅ ST7735R (IC) Software API

2-3 weeks

CPU Architecture Discussion

1° memory map



$2^{32} = 4\,GB$

2° Byte Addressable Machine ~ whose Smallest mem. cell With unique address is a Single Byte

3° memory Bank : 8

$4\,G/8 = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^{2} / 2^{3}$

$= 2^{9} \cdot 2^{10} \cdot 2^{10} = 512\,M$

Question: How many Bits from the Addr. Bus do we need to uniquely define Each memory Bank? 3 Bits

$a_{31}\ a_{30}\ a_{29}\ a_{28} \cdots a_1\ a_0$

0 0 0 ⋮

↑ 1st BANK Starting Addr. of the 1st Bank, 0X0000_0000

↑ LSBit Little Endian

What is the Starting Address of the 2nd BANK :

$a_{31}\ a_{30}\ a_{29}\ a_{28}$

0 0 1 ⋮ 0

0X2000_0000 ; — 2nd BANK

0X4000_0000 ; — 3rd BANK