Jan 27 (Wed), 2021   HARRY LI

CMPE240   Welcome to 240
                Section 2

Email: hua.li@sjsu.edu
Office Hours: M.W. 4:30-5:30 pm.
                Zoom Based
Greensheet   github/hualili
             CMPE240/2018F

References:
1. Greensheet on github
(650) 400-1116 Text Message
Prerequsit Requirements 180D

Advanced Microprocessor Systems

Smart phones ↑ RISC Architecture
5G, Edge AI → IoT, AI → GPU
                      Architectural
Prototype System   Aspects
    Fully Functional Microprocessor
                System

Action Items:
1° github/hualili/cmpe240
2° Pre-requsit Requirements, 180D
3° LPC1769 CPU module
      digi-key.com OR mouser.com
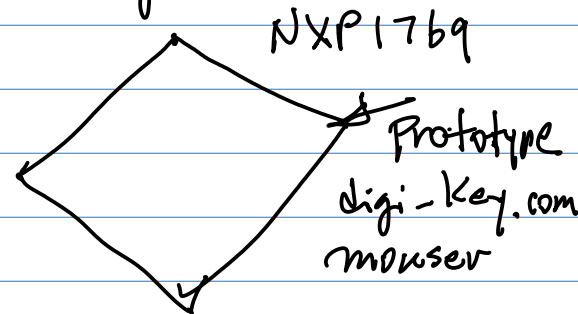Handson: multiple projects, 3 mile
        Stones
                   NXP.com
4° CPU Data sheet   5° MCU expresso

Todays Topics: 1° System Level
Architecture — LPC1769
Ref: github/hualili/cmpe240/
    2018F-102   2° CPU Data-
Sheet
Example:
1° CPU Module @ center of the
System Layout Design
                   NXP 1769

                   Prototype
                   digi-key.com
                   mouser

2° Wirewrapping Board
Dimension: 6" x 4"
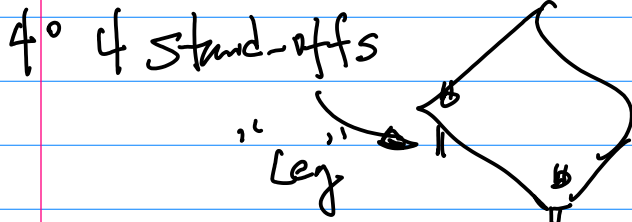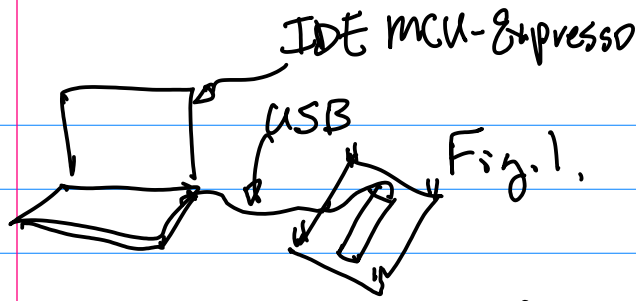with Through-Holes,
and one side of Board
whose through-Holes
with metal plating; But
not the entire Board (just
the through-Holes)

3° PWR CKT: J1 Connector
Right Angle Connector;
S/W Toggle Switch; IC
Regulator 7805, 1117
Red LED 4~10mA
Resistor, Cap.(LPF)
Note: Debug/Development
   No External PWR CKT

IDE MCU-Expresso

USB

Fig.1.

4° 4 Stand-offs

"Leg"

Ref: CPU module Design. pdf
github, Rev.D. or higher

From the Datasheet, Two tables
on Each side of the CPU module
First, Left side, the outter table
is for mbed, Not interested.

Naming Convention :
① CPU pin is named identical
as the name appeared in the
CPU Datasheet ;
② The physical connector Label(s)
are given on the SCH to match
up the physical Board

Question : Find the pin for GND

From SCH,
Connectivity Table

Functional Pin	Physical Pin	Note
GND	J2-1	
VIN	J2-2	4.5~5.5UDC

Connector J2
Position 1

Enumeration of the pin(s)
CPU Pin (1st pin) starts as
"∅";
CPU Datasheet 2018S-3-
UM10360
CPU Architecture, pp.9

J-tag

CORE
ARM
CORTEX 3-

mem.
Controllers
① LCD Driver
② GE/2D/ +
(3D) ③
V-Codec
Peripheral Controllers

CPU

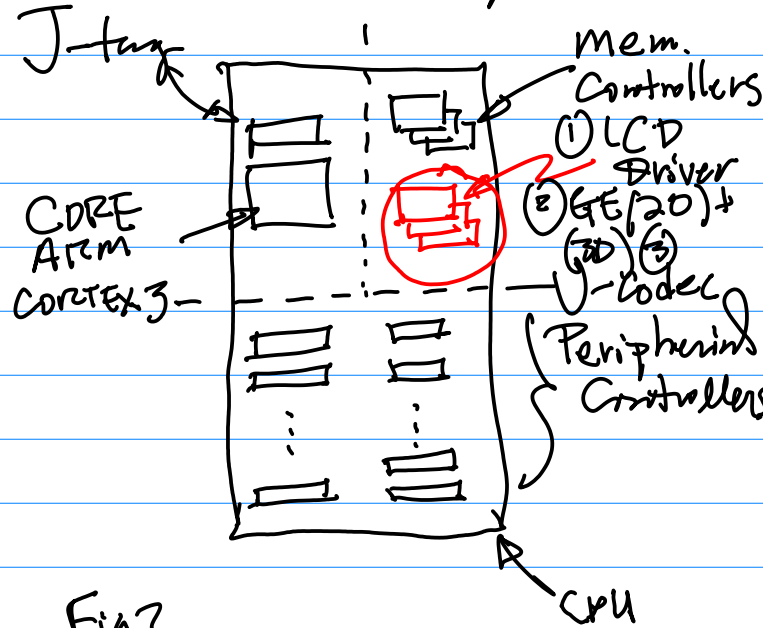Fig 2.
Peripheral Controllers (SCH, CPU Datasheet)

Feb 3. CMPE240 HARRY LI

Note : 1° Have your Video when
Participating the Class ; 2°
Honest Pledge Form / Sign
CANVAS submission By
Sat. 11:59 pm;

Today's Topics : 1° CPU
Architecture / CPU Datasheet
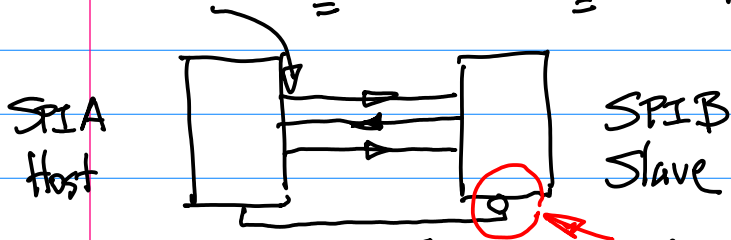SCH ; 2° Homework Design
of prototype Board

Peripheral Controller
Ref: ① CPU Datasheet, pp9.
     ② SCH

Example: From SCH.
1° SPI Serial Peripheral Interface
Note: RESET pin has to Included in
      Our Prototype Design

MOSI: Master Output Slave Input

SPIA Host   SPIB Slave

MISO: Master Input Slave Output
SCK: Serial Clock (O)
SSEL: Enable SPI Controller (ON
       the Slave Side, Active Low)

Note: MOSIx, MISOx, SCKx,
      SSELx, where x stands for the
      xth of SPI Controller   "3+1"
                                 Pins
Question: Find Number of SPI I/F   { MOSI/MISO/SCK
                                        { SSEL (Enable)
for this LPC1769 CPU?
   Two SPI I/F SPIo, SPI,
2° UART (Serial I/F), Note RS232
   { TX (Transmitter)
   { Rx (Receiver)
   3rd pin has to Be a part of it: GND
P0.0; P0.1
Multiplexing, TX/SDA

Init & Config for Special
Purpose Registers will define
which function the pin will
   I/O assume.

Action 1: Homework —
Read SCH, generate a
table for all Peripheral
Controllers
{ Table: CPU Datasheet, pp.9
{ Table 2: SCH, to find subset
   of the I/O Controller.

Advanced Feature:
G.E. Graphics Engine
Example: Broadcom
         Pie 3B+, 4 →GE
NUDA: GPU (Graphics
      Processing Unit)
      NAND 128 GPU.
      TX2, 6 CPU +
      256 GPU
        ↓
Software Implementation
for G.E (2D, 3D)
Basic Concepts.
1° RISC (Reduced Instruction
   Set Computer) { ARM
                  { MIPS
32 Bit

Address Bus (Uni-direction): 32 Bit
~~Data~~ Bus (Bio-direction) : 32 Bit
Register Files { General Purpose Register
{ Special Purpose Reg.

$$\underline{\underline{SPRS}}$$

Memory : $2^{32} = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2 = 4 GB$

Note:
1° Byte Addressable   1K   1M   Byte

Smallest memory   1 G
with an Unique Address is a Single Byte

CMPE240 Feb 8 (Mon), HARRY LI

Today's Topics :
1° Bill of material (github)

2° CPU Architecture

3° Preparation to Bring up your
    CPU, MCU Expresso

Two Step Process to Prepare for Prototype
Board,

Step1 : CPU module LPC1769
        Wire wrapping (Prototype Board)
      "Glue" Logic Resistor, Caps,
        PWR Regulator IC
        (7805), Red LED, Stand-offs

CMOS CPU ARM
Vout 3.3VDC, 10~30mA
Estimate 3.3V/10mA,   3.3V/30mA
3.3×10^2 1.1×10^2
Omps.

Wall mount
Adaptor
110 ACV →
7.5 VDC
1000 ~ 1500 mA

Note: PWR Regulator
IC, 7805 ($\sim$2VDC)
         Volt drop

Vin   GND
                V_out
                4.5~5.5
To Cap to Realize LPF.

7805

$$V_{cc}\left(1 - e^{-\frac{t}{RC}}\right) \quad \cdots (1)$$

V_{cc}
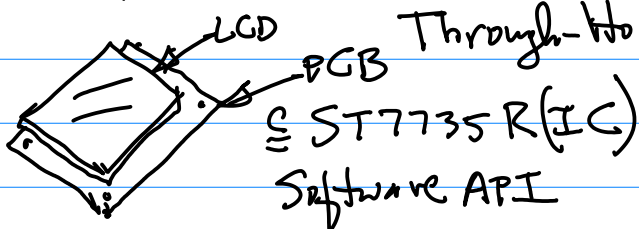$3\tau\Big|_{\tau=RC}$
t

4.7 uF
2nd Part for Caps : 7805

Datasheet for 7805, Caps are those with Polarity "⊥"

Bill of the Material to Build G.E.

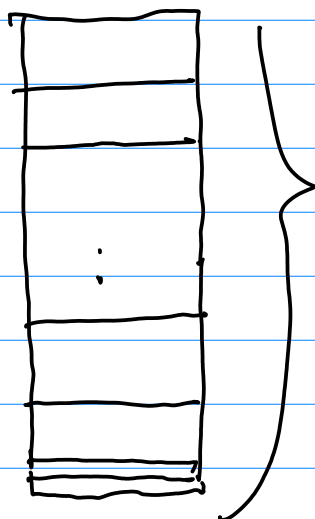SPI I/F Based Color LCD Device. $\underline{a}$ SPI (Not I2C)

$\underline{b}$ Module — Connector

LCD, RGB, Through-Hole

$\underline{c}$ ST7735 R(IC) Software API

2-3 weeks

CPU Architecture Discussion

$1°$ memory map

$$2^{32} = 4 \, GB$$

$2°$ Byte Addressable Machine

~ Whose Smallest mem. cell With unique address is a Single Byte

---

$3°$ memory Bank: 8

$$4 \, G/8 = \frac{2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2}{2^3}$$

$$= 2^9 \cdot 2^{10} \cdot 2^{10} = 512 \, M$$

Question: How many Bits from the Addr. Bus do we need to uniquely define Each memory Bank? 3 Bits

$a_{31} \, a_{30} \, a_{29} \, a_{28} \, \cdots \quad\quad a_1 \, a_0$

$\quad 0 \quad 0 \quad 0 \quad 0$ ↑ LSBit
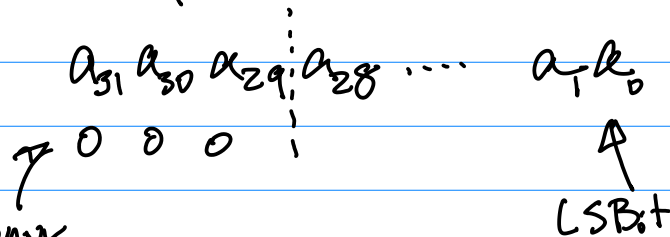
1st BANK

Little Endian

Starting Addr. of the 1st Bank,

0X 0000_0000

What is the Starting Address of the 2nd BANK:

$a_{31} \, a_{30} \, a_{29} \, a_{28}$

$\quad 0 \quad 0 \quad 1 \quad 0$
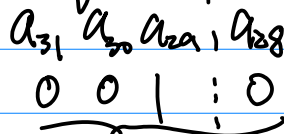
0X 2000_0000   ; — 2nd BANK
0X 4000_0000   ; — 3rd BANK

CmPE240 Feb10 (Wed)
Ref: github/hualili/cmpe240
    ... 2018F-107-LecGPP
Homework 1. Form 4-Person Team
First, Last Name, Last 4 Digits SID
E-mail Address ⟶ Submission

Via Email & Canvas By Thursday

11:59   Subject Title → Team Coordinator   1° Project Exported

Document Name   First_Last_CMPE240   in Zip format

E-mail Submission.

Homework 2: (1 pt)   2° White paper, Report

Requirements ① Build a prototype   3° Video Clip (up to 5~7

Board, ② Write a first program   Seconds) Short please.

Turn On/off LED "Hello, the world"   Example: From PPT ON GPP I/F.

Note: Use Prototype Board to Build   Identify CPU GPP pin

GPP I/O To Drive LED ON/OFF   P6.3 J2-22 Input

③ Build I/O Testing Circuit, the   P6.21 J2-23 Output

CKT input is from GPP (GPIO)   Consider the Output Testing CKT,

GPP (Output)

CKT₂   Fig 1.

CPU
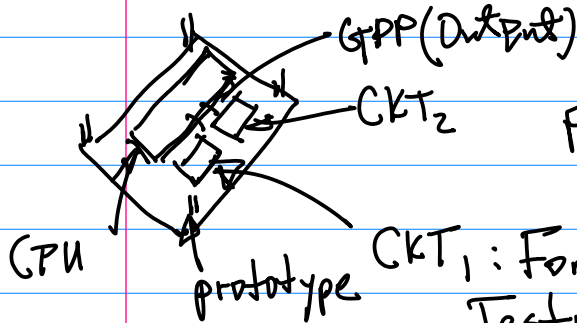
prototype   CKT₁ : For Output

Testing   "1" to Turn on LED

"0" to Turn off LED   Fig.2

$$V_{CC} = IR + V_{LED} \quad \cdots (!)$$

CKT₂ : For Input Testing

$$V_{CC} = 3.3 VDC$$

Input "1", Toggle Switch to connect GPP $I \cong 10 mA$, $V_{LED} = 1.2 VDC$

Input to Vcc (Via a Resistor)

Input "0", Toggle the switch to GND $$3.3 = 10 \times 10^{-3} R + 1.2$$

(Via Resistor) $$R = (3.3 - 1.2)/10^{-2} = 210$$

④ Write One page Report (IEEE paper Ω

format) White paper   Due ON CANVAS
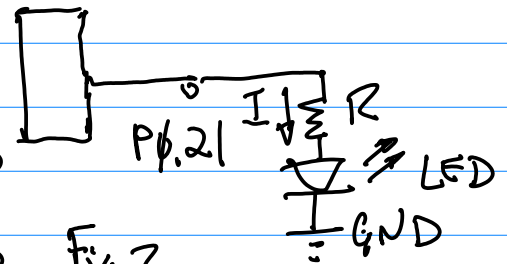
Now, Let's Design CKT₂

Due 2 weeks from Today, Feb 24.

Vcc

R_1 SW

A

R_2 B

GND

R_1 : Output, GND
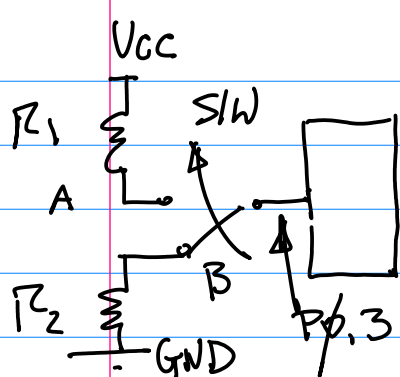
$V_{cc}/R_1 = 4mA$, $\frac{3.3}{4mA} \simeq 1K\Omega$

SW :
@ A

R_2 : Output $V_{cc} = 3.3$
$\underline{I = 4 mA}$

Pg.3 $R_2 = \frac{3.3}{4} \times 10^{-3}$

$\simeq 1K\Omega$

System Level & Software Design

1° CPU Architecture ──→ mem.
                          map
Peripheral Controllers   BANK 0

GPP Controller $\underline{a}$ PWR-up Address
                          1st Address

0X0000_0000   CPU when powered up

'it will fetch the 1st Executable Instruction
at this Location

Fig 1

Firmware

RoM/Flash BootLoader

Branch/Jump Instruction

0X0000_0000 power up Addr.

Feb 15 Monday

Today's Topic: GPP I/O Testing
        CPU Architecture & Special Purpose
Registers.

Power-up Addr : Addr.
when CPU is powered,
it will fetch the 1st
instruction to execute
at this memory location.

Firmware ── A program which
has been burn into RoM/Flash

Question: How do you write
C program to perform GPIO
init & config? So that I/O
I/F can be established?
Background:

{ Hardware : Peripheral
              Controllers
  Software
              ↓

GPP General
Purpose Port

(GPIO)
    ↓

GPP Controller

Special Purpose Registers
32 bits :
Their function :
$\underline{a}$ Control function : Init & Config
$\underline{b}$ Data Exchange Function :
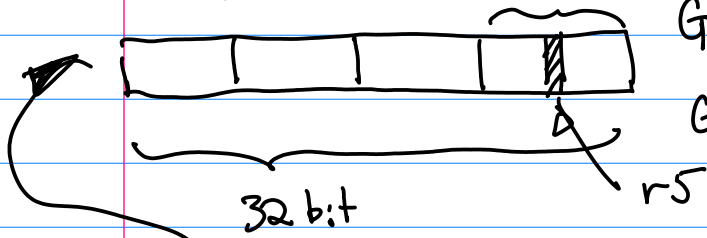$\underline{c}$ Pull up/Down

CMPE240

Naming convention:

Prefix + Root + Postscript
  3   3   (3)
 GPx   CON

General purpose   GPxCON

GPP — Port 1 — What is the
Size for GP1CON?

GPxCON [31:ϕ]
GPxCON [5] = 1
         = 0

32 bit   r5

Note: 1° 0X uuuu_uuuu
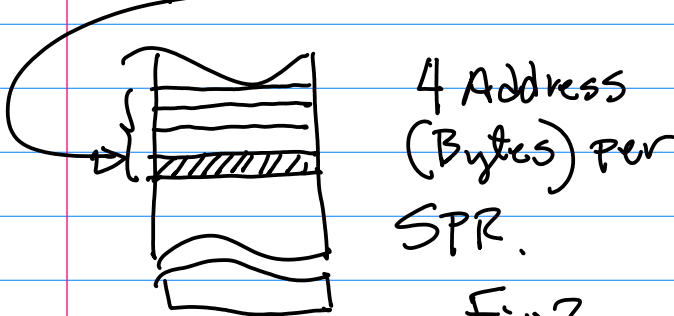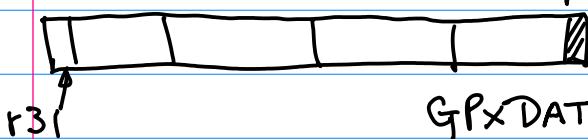   Suppose 0X4000_0200

4 Address
(Bytes) per
SPR.

Fig 2

Question: How many Control function
Can one Control Register define?

$2^{32} = 4G$

Now, GPxDAT, 0X4000_0204

r31   GPxDAT[0] Fig 3.

Fig 4.

CPU

8
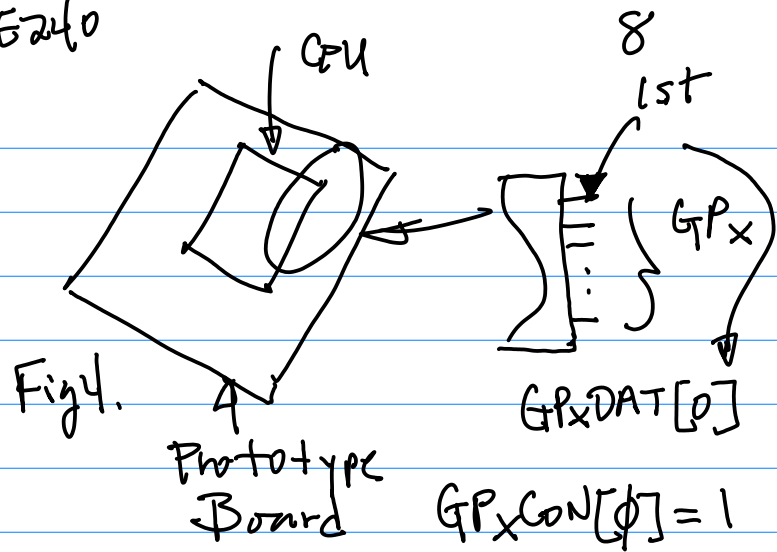1st
GPx

GPxDAT[0]

Photo type
Board   GPxCON[ϕ] = 1

Action 1: LPC1769 patch.zip
Import it as a project
into your IDE
Test run blenky Program
To modify the GPP
So Pϕ.2 & Pϕ.3
Can be employed for
I/O Testing

Note: 1° Project Panel on the
top left of your IDE GUI
→Select "Blenky" By
highlighting it.

CMPE240 Feb 17 (W)

Ref: 1° github/hwalili/
Cmpe240/2018S-11-
GPIO2015-1-30.zip

rϕ LSB(Little 2° ~/Cmpe240/
     Endian) 2018-10-LCD_
               DrawLine.zip

3° ~/2018F/2018F-107-~
(For GPP)

4° ~/2018F/2018F-109
(For SPI LCD)

5° ~/cmpe240/20185-10-~
DrawLine.zip
(For 2D GE-Line Plot;

Topics: 1° SPRs for SPI LCD
I/F; 2° SPRs for GPP.

Init & Config of Peripherial Controller(s)
{ GPP
{ SPI (Serial Peripheral Interface)
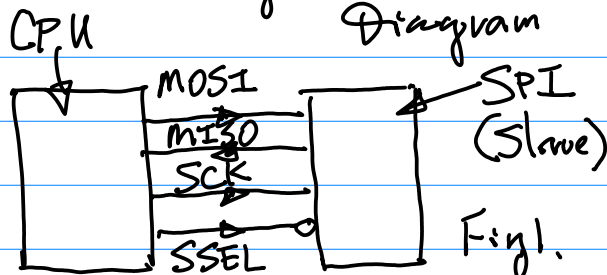
Note: External Connector → CPU GPP.
J2-X   Pø.2, etc.

Example: SPR↓
SPI Interface for color
LCD Display.

{ Hardware Design

{ Software Design

Consider Hardware Design Block
Step1   CPU   Diagram
SPI
Host

MOSI
MISO
SCK
SSEL

SPI
(Slave)

Fig1.

Pin Connectivity "3+1"

CPU	SPI(s)	Note
MOSI Pø.9/J2-5	SI	CPU (O)
MISO Pø.8/J2-6	SO	CPU (I)
SCK Pø.7/J2-7	CLK	CPU (O)
SSEL Pø.6/J2-8	$\overline{CS}$ (nCS)	CPU(O) Active Low

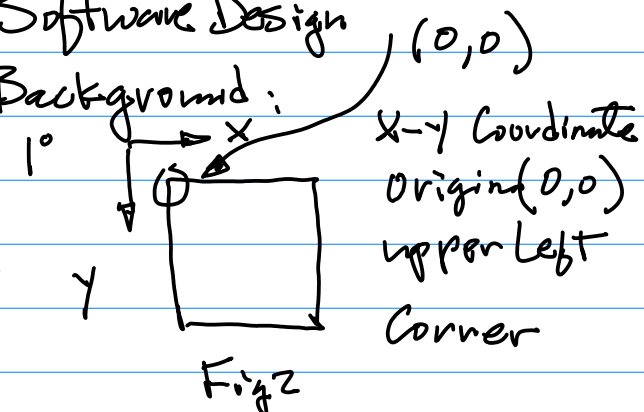Table1 : Connectivity Table

20185-8-SPI (photo Board)
2018F-108-LCD-Connector

Notes : Connectivity Table
for CPU to SPI LCD Display
Device.

Action 1 : Solder up the SPI
LCD Device ;

Software Design
Background :   (0,0)
1°   x
O
y   X-y Coordinate
Origin (0,0)
upper Left
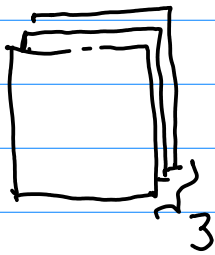Corner

Fig2

Resolution: M×N

M: No. of Pixels per row

N: No. of Rows per Frame

Example: 160×120

Width — No. of Pixels/Row

Height — No. of Rows

2° I(x,y) Image plane(s)

r: red ;
g: green;
b: blue.

Fig. 1   3

$$I(x,y)=(r(x,y), g(x,y), b(x,y)) \cdots (1)$$

Feb22 (monday)

A /////////   3D G.E. → B

Background Discussion   2D G.E.

GPP I/O Testing

① CPU Architecture   ② SPR — Init & Config.   ③ Implementation

CPU Block Diagram   Memory map   Peripheral Controller
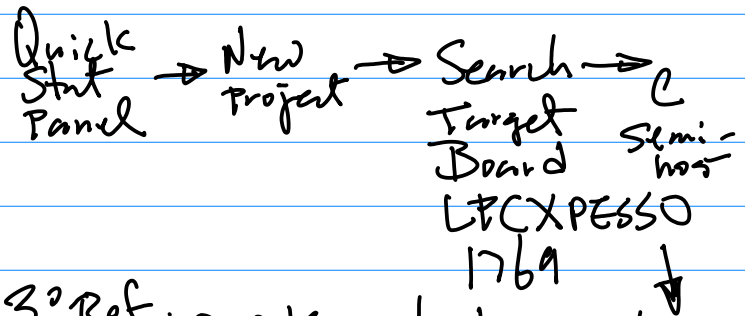
GPP + SPI

Development Environment
IDE & SDK

1° Ref: 2021S-106b-~
Note: IDE Not Backwards Compatible
Version 11.3.0 User Guide

2° Selection of Target CPU, Target → Board
LPC1769
(Picture of Board is Provided)

Quick Strt Panel → New Project → Search → C
                                    Target Semi-
                                    Board host
                              LPCXPESSO
                                1769 ↓
3° Ref: 2021S-106-homework
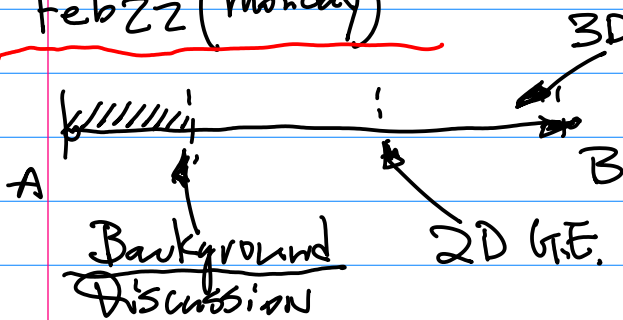
4° Report Template
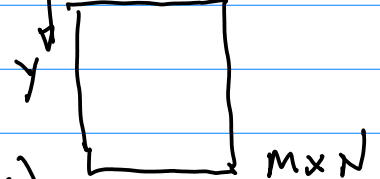2018-10~

Discussion On Graphics
1° Graphics { Pixel Graphics I(x,y)
              Vector Graphics }
                    2D & 3D G.E.
2° Display Device →x
                   ↓y

ⓐ Scanning
(Image Formation)

MxN

Stmt @ (0,0) → L2R one pixel at a time, → T2B one row at a time.

b Timing Calculation

b) Frame Rate FPS (Frame Per Second)

30 FPS

$f_F = 30 Hz;$ ... (1)

$T_F = 1/f_F = 33.3 \times 10^{-3} Sec.$