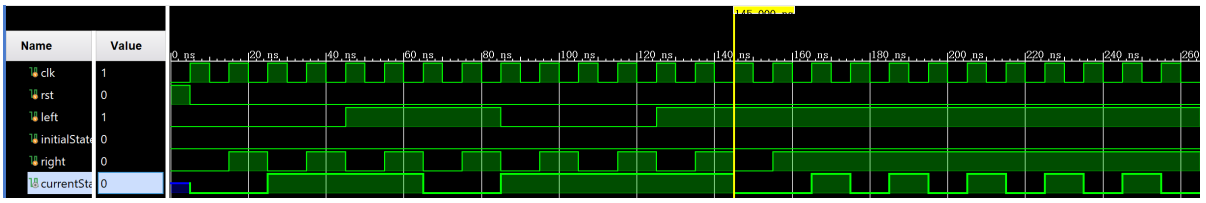
# Report Lab 4

## 1. Single cellular automatons

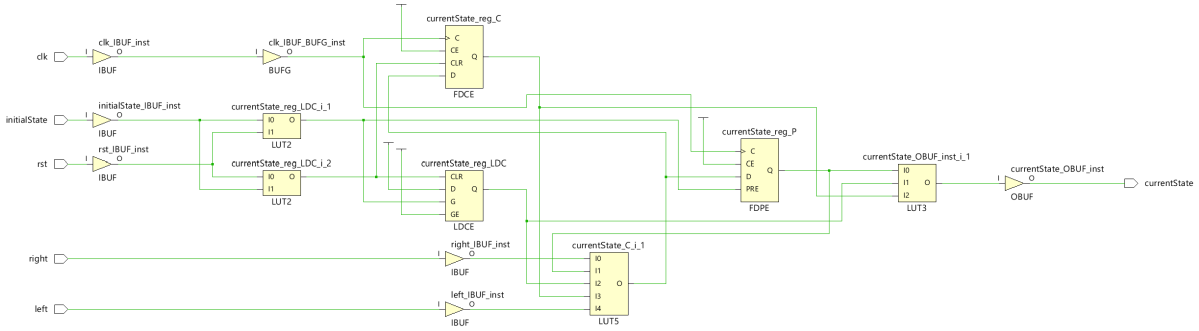
### 1. Behavior simulations:




After comparing with the truth table provided by the lab4.pdf, the result is correct.

### 2. Schematic and 3 reports:

2.1 Schematic:

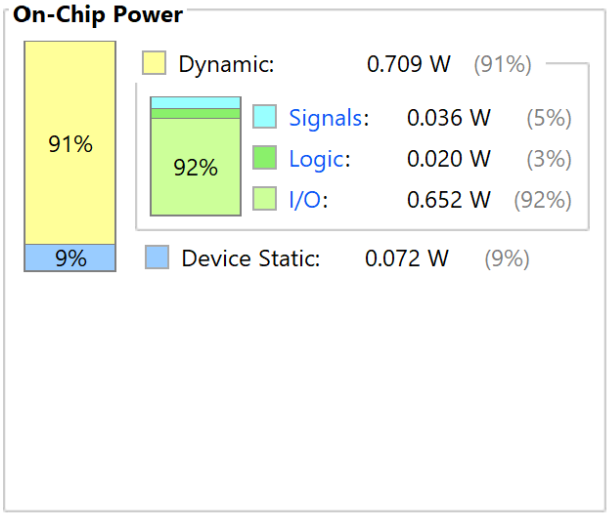



2.2 Power report:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

| | |
|---|---|
| **Total On-Chip Power:** | **0.78 W** |
| **Design Power Budget:** | **Not Specified** |
| **Power Budget Margin:** | **N/A** |
| **Junction Temperature:** | **28.9°C** |
| Thermal Margin: | 56.1°C (11.2 W) |
| Effective ϑJA: | 5.0°C/W |
| Power supplied to off-chip devices: | 0 W |
| Confidence level: | Low |

Launch Power Constraint Advisor to find and fix invalid switching activity




2.3 Area report:

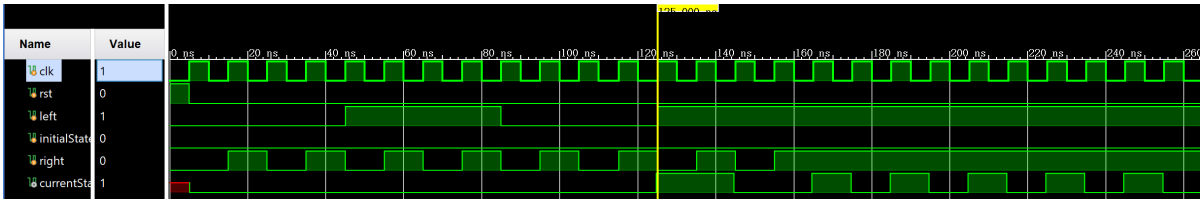
| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs | 3 | 0 | 20800 | 0.01 |
| LUT as Logic | 3 | 0 | 20800 | 0.01 |
| LUT as Memory | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 3 | 0 | 41600 | <0.01 |
| Register as Flip Flop | 2 | 0 | 41600 | <0.01 |
| Register as Latch | 1 | 0 | 41600 | <0.01 |
| F7 Muxes | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 8150 | 0.00 |

2.4 Timing report:

| Setup | | Hold | | Pulse Width | |
|---|---|---|---|---|---|
| Worst Negative Slack (WNS): | 2.149 ns | Worst Hold Slack (WHS): | 0.172 ns | Worst Pulse Width Slack (WPWS): | 1.500 ns |
| Total Negative Slack (TNS): | 0.000 ns | Total Hold Slack (THS): | 0.000 ns | Total Pulse Width Negative Slack (TPWS): | 0.000 ns |
| Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 | Number of Failing Endpoints: | 0 |
| Total Number of Endpoints: | 2 | Total Number of Endpoints: | 2 | Total Number of Endpoints: | 3 |

**All user specified timing constraints are met.**

### 3. Post-implementation simulation:




We can find that due to the P&R, the FSM does not work before 120ns...

## 2. 1-D cellular automatons

To have a better visualization of info in different reports, all info are put into the table below:

| Number of CAs | Total on-chip power (W) | WNS (ns) | Area utilization |
|---|---|---|---|
| 6 | 0.084 | 1.415 | 13.21% for IO<br>0.12% for LUT<br>0.04% for FF |
| 21 | 0.116 | 1.176 | 41.51% for IO<br>0.39% for LUT<br>0.15% for FF |
| 41 | 0.161 | 0.698 | 79.25% for IO<br>0.79% for LUT<br>0.30% for FF |

(The detailed screenshot can be seen in the folder)

From the table ,we can see that as the number of CAs increases, the total on-chip power is increasing, WNS gets worse and more area is consumed.

For the power, it increases since we need more LUT, FF and so on. For  the WNS, because the more the CAs, the longer the critical path will be according to the schematics, therefore the smaller the WNS. For the area, for sure the more CAs you designed in the circuit, the more area needs to be consumed.

The  interesting thing is that at first i reverse the output and internal state by mistake, when i run the top level simulation it gives me no errors, however the waveform goes to something like this and an error occurs during the running:


This is because i reverse the output state and internal state so there is no input at the beginning of the simulation. No input results in no output, no output again means no input... and the simulator will fall into some weird loop and cannot convergent. Hence the time cannot advance.