Lab01 – Modeling, synthesis, simulation and implementation of combinatorial logic circuits using FPGAs

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1 Objective

Learn how to model digital combinatorial logic circuits in Verilog. Learn (or refresh) how to use Xilinx EDA tool chain for synthesis, functional simulation and implementation (respectively Model/QuestaSim and ISE Xilinx/Vivado). Go through complete design flow for the examples below and learn how to qualitatively analyze results you get after different steps.

2 Exercises

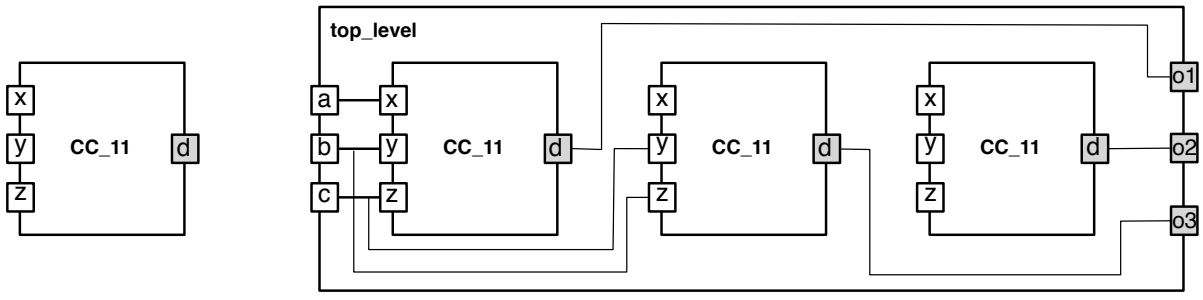
2.1 Simple combinatorial circuit

Write Verilog model of a combinatorial circuit (let's call it `CC_11`) that implements the following Boolean equation of 3 variables (inputs):

$$d(x, y, z) = x \cdot y + \overline{x} \cdot z + y \cdot z$$

2.2 Simple combinatorial circuit

Using the circuit described previously (`CC_11`), design a new circuit, called `top_level`, with three different instances of this module. You can chose freely the connectivity between different instances, however the following is imposed: 3 inputs of the top module `top_level` are connected to the first instance (on the left) as suggested in the Figure:



2.3 Gray code encoder

Write VHDL model of a circuit that will convert a 4-bit word input in BCD code into Gray code. The truth table of the Gray code is given below. Do not derive logic functions from the truth table. Rather, implement truth tables directly in VHDL (after all the synthesis tool should figure out the logic functions).

Decimal	Binary	Gray
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

3 To do

For the problems above:

1. Write Verilog model and verify gate-level description of the synthesized circuit.
2. For each module, design a test-bench to verify the functionality of the circuit.
3. Perform functional simulation using Model/QuestaSim & show correct behavior of the circuit.
4. For Gray code encoder to cover all possibilities of the inputs (if this has not been done yet).
5. Do the synthesis, Place & Route (P&R).
6. Analyze various reports to derive key Performance, Power, Area (PPA) design parameters and conclude. For example what happens with the critical path when we go from the circuit in Section 2.1 to circuit in Section 2.2.
7. Do simulation post P&R and show the impact of switching and propagation delays on timing.