ECE 385 Lab 2 Report Outline

- **Introduction**
  - Summarize what high-level function your circuit performs. How many words does your memory contain and what is the bit-width of each word? The introduction should be approximately 3 - 5 sentences.

- **Operation of the memory circuit**
  - Operation
    - Describe how the **addressing** is implemented. When does the circuit commit a read or write from/to the input switches and output register respectively.
    - Describe how a **write** operation is performed on the memory. Describe what switches you flip and in what order. Describe intuitively how the data flows through the circuit at each clock cycle.
    - Describe how a **read** operation is performed on the memory. Describe what switches you flip and in what order. Describe intuitively how the data flows through the circuit at each clock cycle.

- **Written description and block diagram of memory circuit implementation**
  - High-level description
    - Describe in words what components are necessary to perform the operations described in the written description of the memory circuit operation.
    - Include a high-level block diagram similar to figure 3 in the lab manual. This diagram should contain components on the granularity of registers, muxes, and blocks and include few/no individual gates.

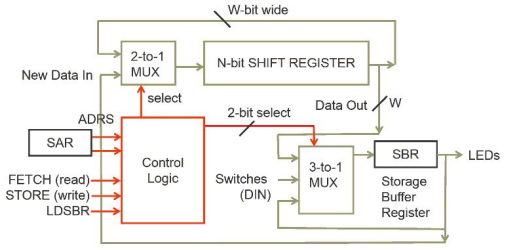
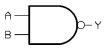
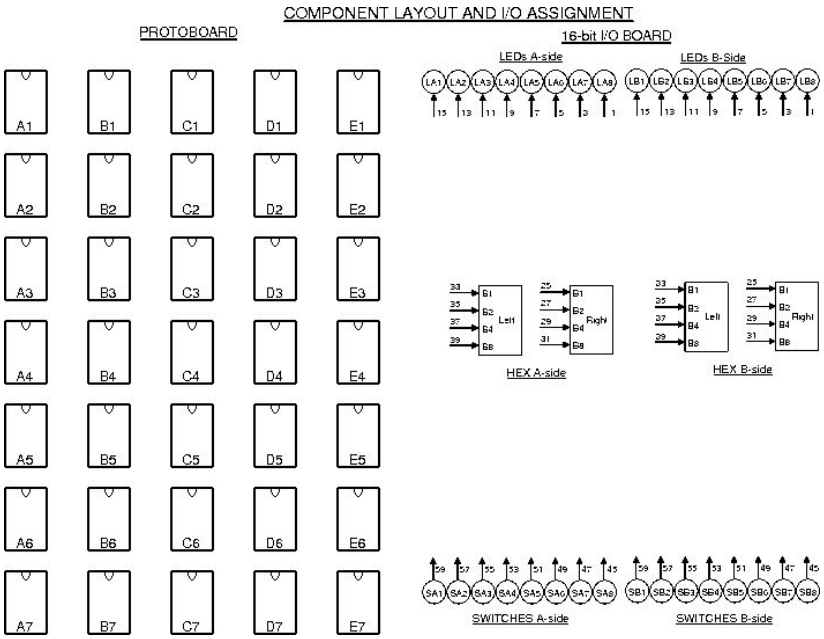


Figure 3: Block diagram of the shift-register storage unit.

  - Control Unit
    - Provide an intuitive written description of your control unit.
    - Include a block diagram of your control unit It is acceptable to turn in either:
      - A single high-level block diagram, which contains the sub-components inside the control unit.
      - Two block diagrams, one similar to figure 3 in the lab manual and one containing only the inside of the control unit.

- **Design steps taken and detailed circuit schematic**
  - Design Steps Taken
    - If you used k-maps or truth tables during design, include them here. (If you didn't need them, you don't need to include them).
    - You do not need a state diagram for this lab.
    - Written description of the design considerations taken (did you consider multiple implementations of the same circuit and the tradeoffs of each?)
  - Detailed Circuit Schematic
    - This diagram should show all components used and their interconnections down to the logic gate level. Gates should look like  and not like  . Large schematics can be broken down into a hierarchy (for example, in the main diagram, the control logic can be shown as a box with inputs and outputs and a separate detailed diagram of the control logic can be placed below the main diagram). You may omit gate level representations of complex chips which you used (counters, etc) and instead replace them with a block and all connections.

- **Component Layout Sheet**
  - Follow the guidelines on the Resources page on the course website. Blank layout sheets as well as a sample completed layout sheet can be found there. You may also use a computer tool for this portion.



- **Description of all bugs encountered and corrective measures taken**

- **Conclusion**
  - Summarize the lab in a few sentences