ECE 385

Fall 2021

Experiment 1

Introductory Experiment

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Introduction

The general goal of experiment #1 is to get familiar with ECE 385 experiment equipment and software and learn how to write a well-organized ECE 385 lab report. In this introductory lab, our group setup Quartus and build 2 different MUXs as well as performing the simulation on the designed circuit.

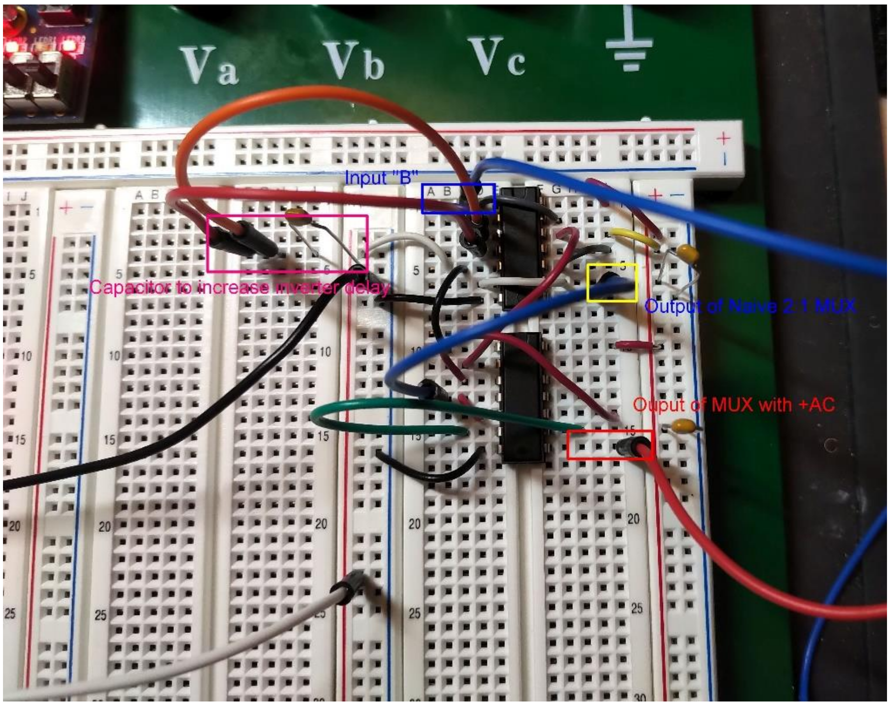
Circuit Description & Diagram

For this experiment is a simulation experiment, we did not design any real circuit. However, we still designed two circuit in simulation lab by means of logic diagram. The description is presented below.

For part A, we designed a circuit with three 7400 chips, which are used for the NAND gates, labeled by gate 1, 2, and 3. The circuit has three input A, B and C, as well as an output Z. For connection, firstly, A and C input connect to one of the pins of gate 1 and 3 respectively. Then connect the output of gate 1 and 3 with the output Z. Another pin of gate 1 along with two pins of 2 is connected to the input B. Finally, the output of gate 2 is attached to the another pin of gate 3.

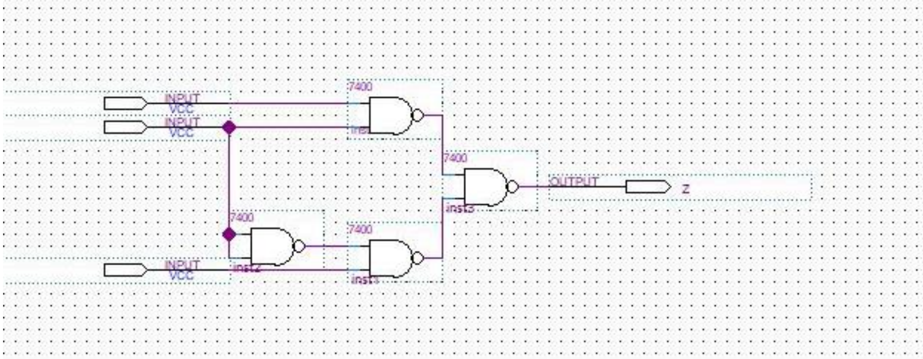
For part B, it is basically an improved version of part A circuit. The difference here is to connect the original output to the two pins of another 7400 chip. Then, connect input C and the output above to the last NAND gate. The output of the last gate, output Z, would be the output of the MUX.

The circuit diagram provided by Prof. Zoufu is presented below:

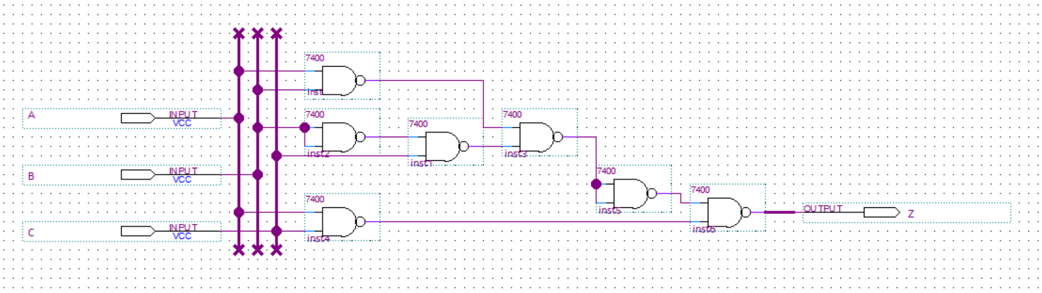


Circuit Diagram of MUX of pt.A & B

Logic Diagram



Pt. A



Pt. B

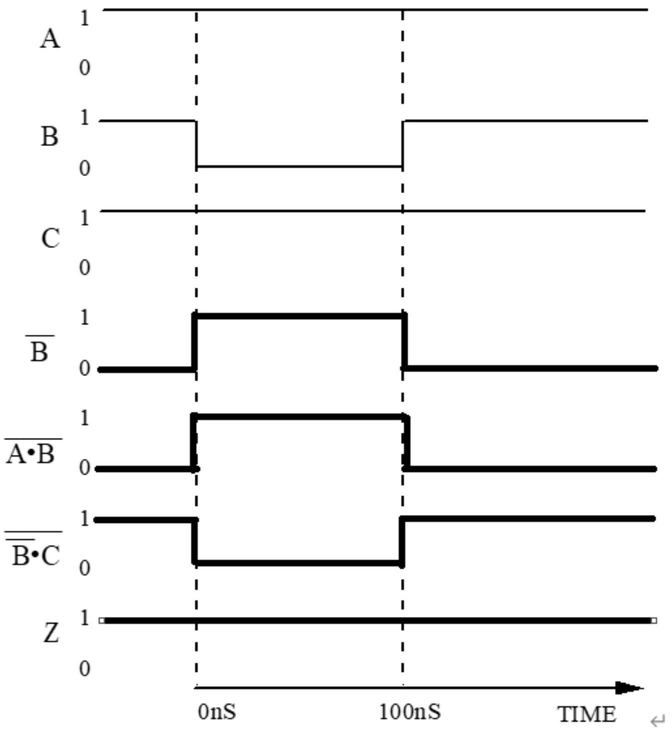
Lab Record & Discussion

We could write the truth table of MUX designed in part A and B.

B\AC	**00**	**10**	**11**	**01**
0	0	0	1	1
1	0	1	1	0

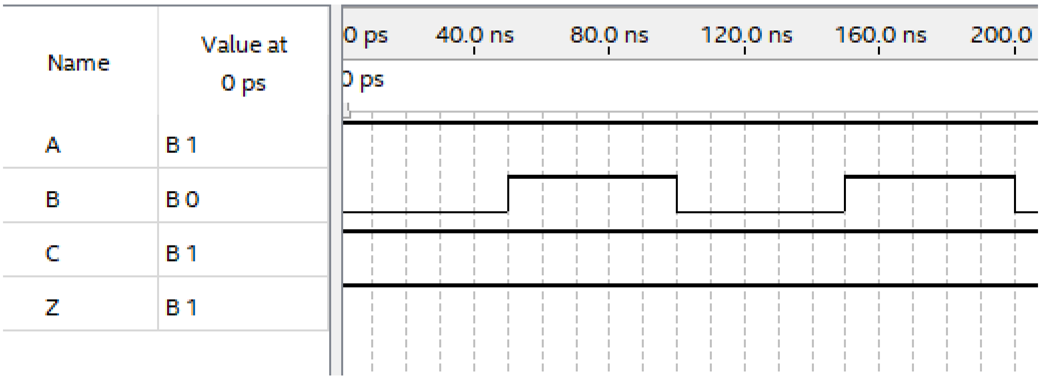
Truth Table of MUX

Then, we could plot the I/O diagram:



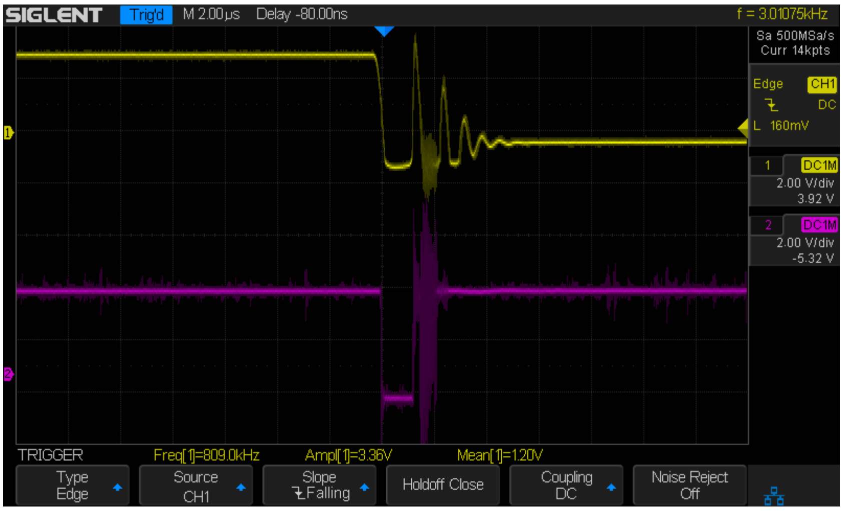
I/O diagram of MUX

We could easily find that glitch could occur in the MUX above, since there's continuous 1. However, in the pre-lab simulation, we did not observe any glitch. We guess it is because the component in simulation tools are ideal, or with incomparably small reaction time, which could not trigger the glitch.



Name	Value at 0 ps
A	B 1
B	B 0
C	B 1
Z	B 1

From the waveform provided by Prof. Zoufu, we could observe the static hazard clearly.



SIGLENT Trig'd M 2.00µs Delay -80.00ns f = 3.01075kHz

Sa 500MSa/s Curr 14kpts

Edge CH1 DC L 160mV

1 DC1M 2.00 V/div 3.92 V

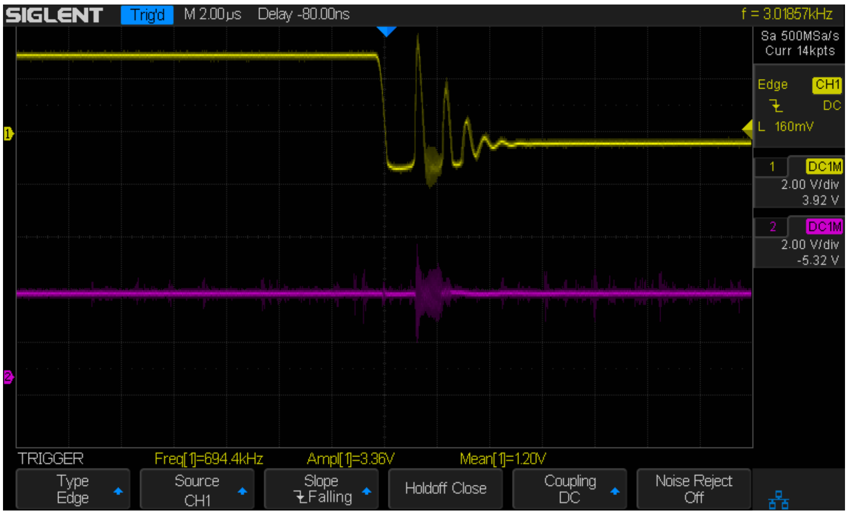
2 DC1M 2.00 V/div -5.32 V

TRIGGER Freq[1]=809.0kHz Ampl[1]=3.36V Mean[1]=1.20V

Type Edge | Source CH1 | Slope Falling | Holdoff Close | Coupling DC | Noise Reject Off

Waveform of original MUX

After reconnecting the circuit like part B, the static hazard disappears.



SIGLENT Trig'd M 2.00µs Delay -80.00ns f = 3.01857kHz

Sa 500MSa/s Curr 14kpts

Edge CH1 DC L 160mV

1 DC1M 2.00 V/div 3.92 V

2 DC1M 2.00 V/div -5.32 V

TRIGGER Freq[1]=694.4kHz Ampl[1]=3.36V Mean[1]=1.20V

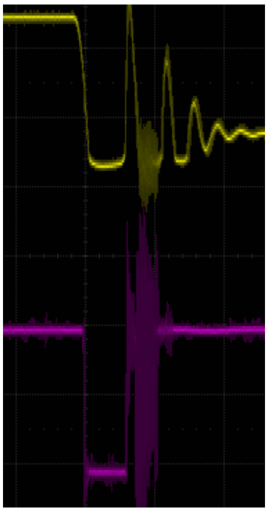
Type Edge | Source CH1 | Slope Falling | Holdoff Close | Coupling DC | Noise Reject Off

Waveform of Improved MUX

Post-lab Problem & Extra Problem

For the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?

The static zero hazard mostly occur at the falling edge of the input B



Glitch

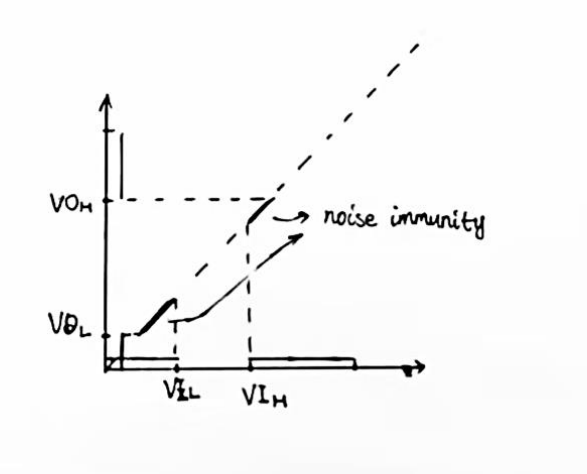
What is the advantage of a larger noise immunity? Why is the last inverter observed rather than simply the first? Given a graph of output voltage (VOUT) vs. input voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter?

Larger noise immunity means the logic gate could withstand larger interruption or noise but operate properly.

Using the last inverter rather than the first one is to eliminate the effect of noise and obtain a steady signal.

In order to calculate the noise immunity:

$$NM_H = NO_H - NI_H, \qquad NM_L = NI_L - NO_L$$



If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors?

It's a bad idea because we can't ensure that the LEDs will equally share current due to the variation in manufacturing; furthermore, it is possible that one LED will get much more current than the others leading to the damage of LEDs.

Conclusion

In this lab, we learnt how to set up a Quartus project and perform some simple simulation. The most important thing I learnt in this lab about the software is to use the same project name and diagram name. Furthermore, we also learnt how to build a MUX and how does the noise immunity work. Finally, we've gained knowledge of static hazard, which is a kind of glitch caused by the delay of components, representing as continuous 1 in truth table, and the methods to avoid static hazard by adding a constant source and a gate.