CNVLUTIN: Ineffectual-neuron-free DNN computing

J. Albericio, P. Judd, T. Hetherington*, T. Aamodt*, N. E. Jerger, A. Moshovos





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J. Albericio



P. Judd



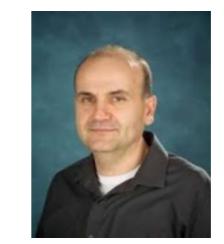
T. Hetherington*



T. Aamodt*

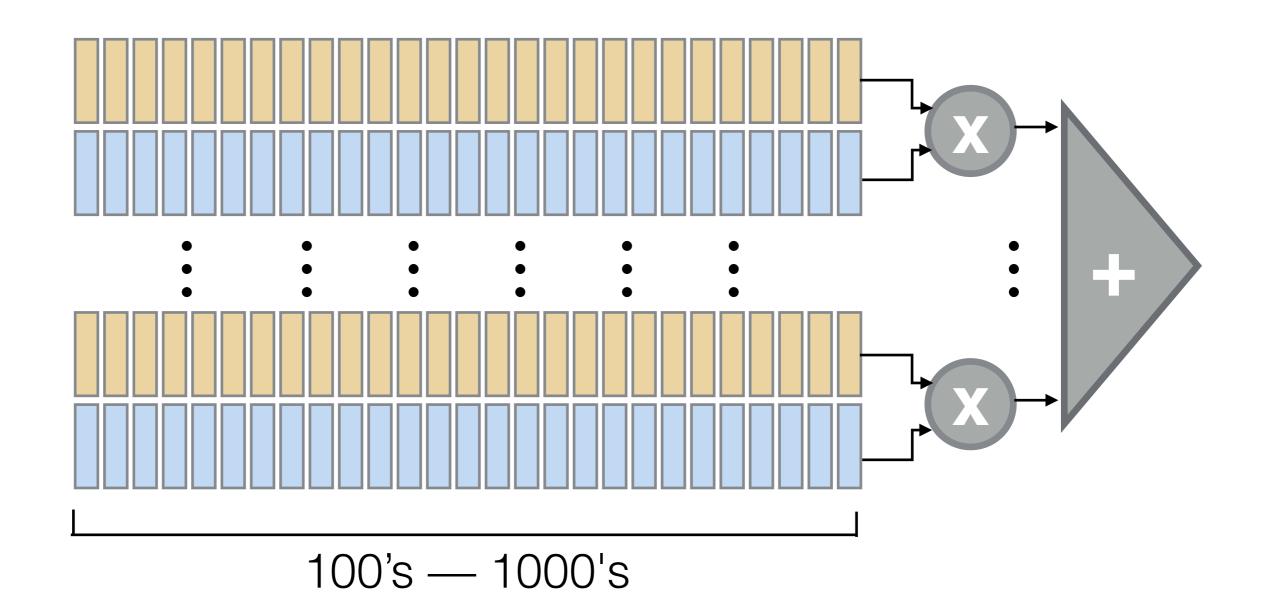


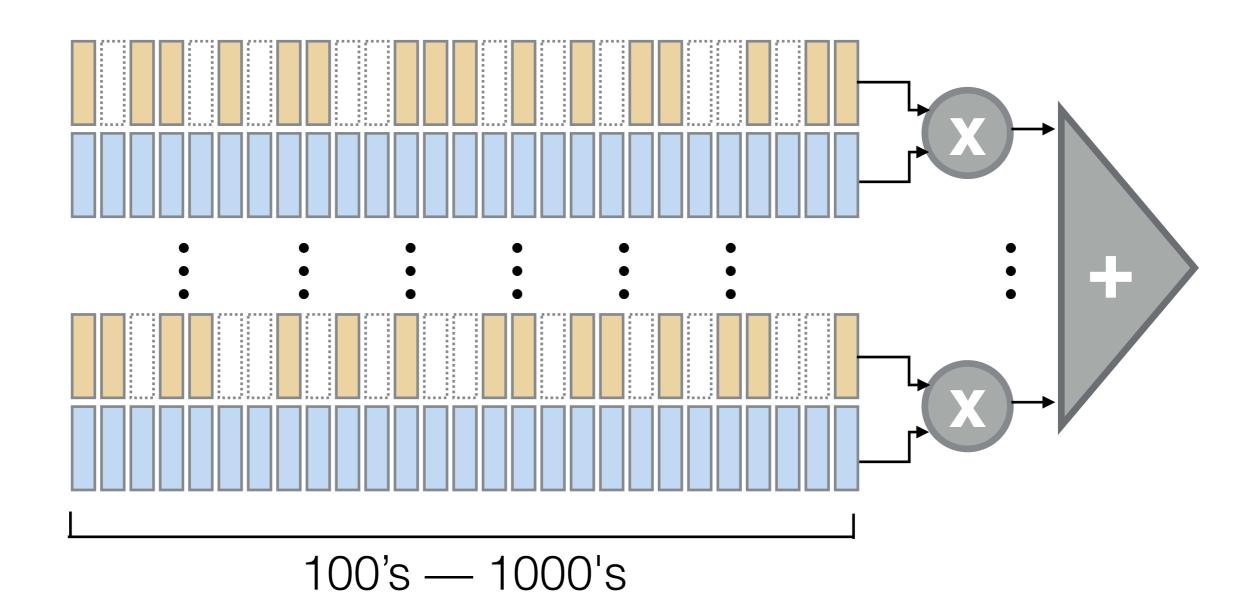
N. Enright Jerger A. Moshovos

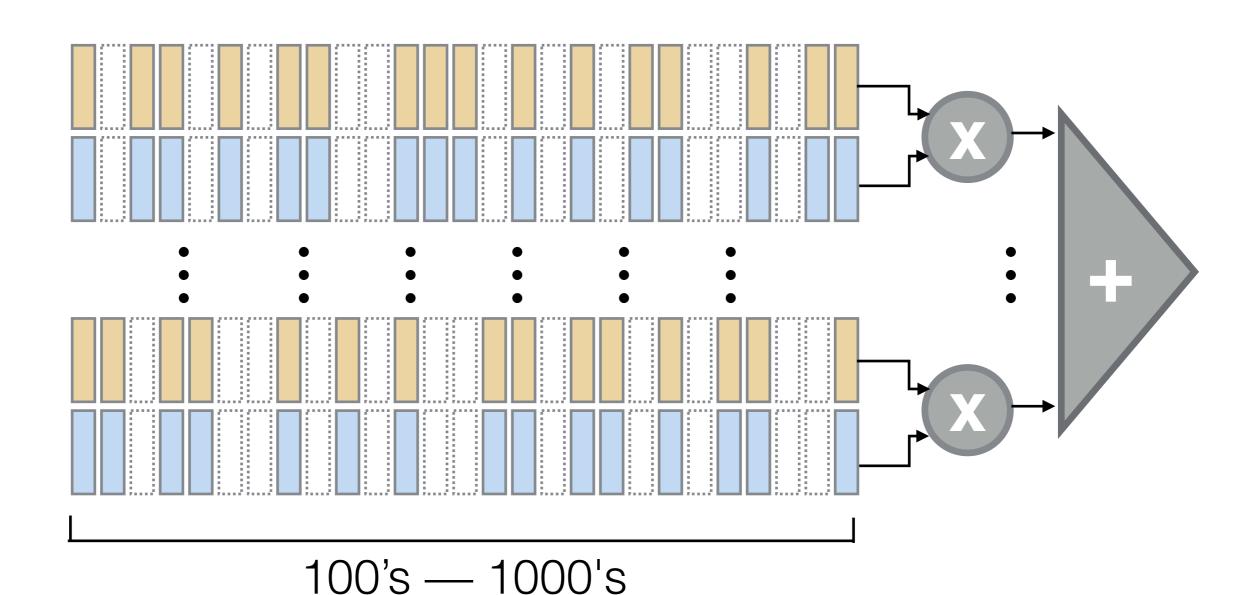


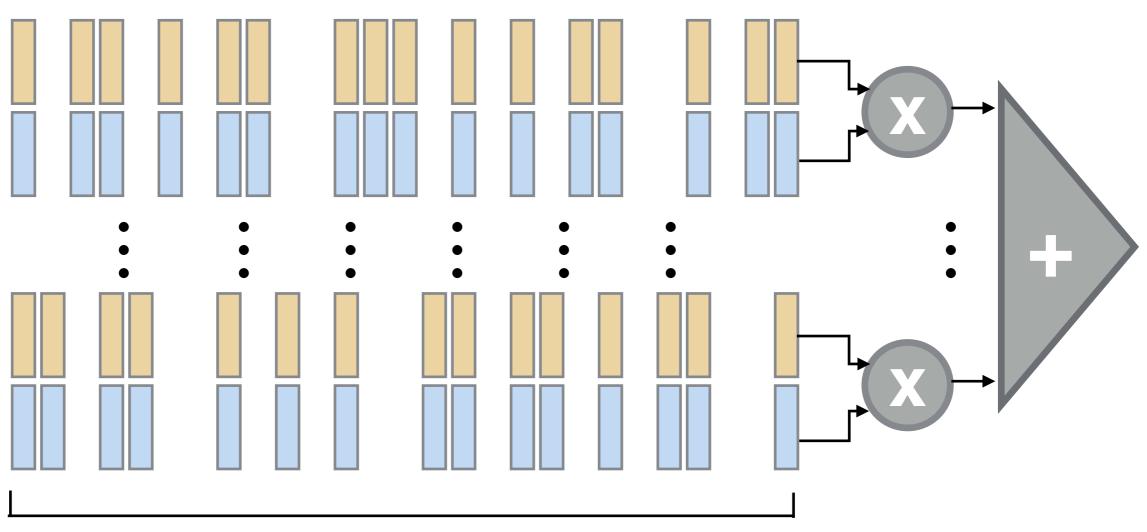


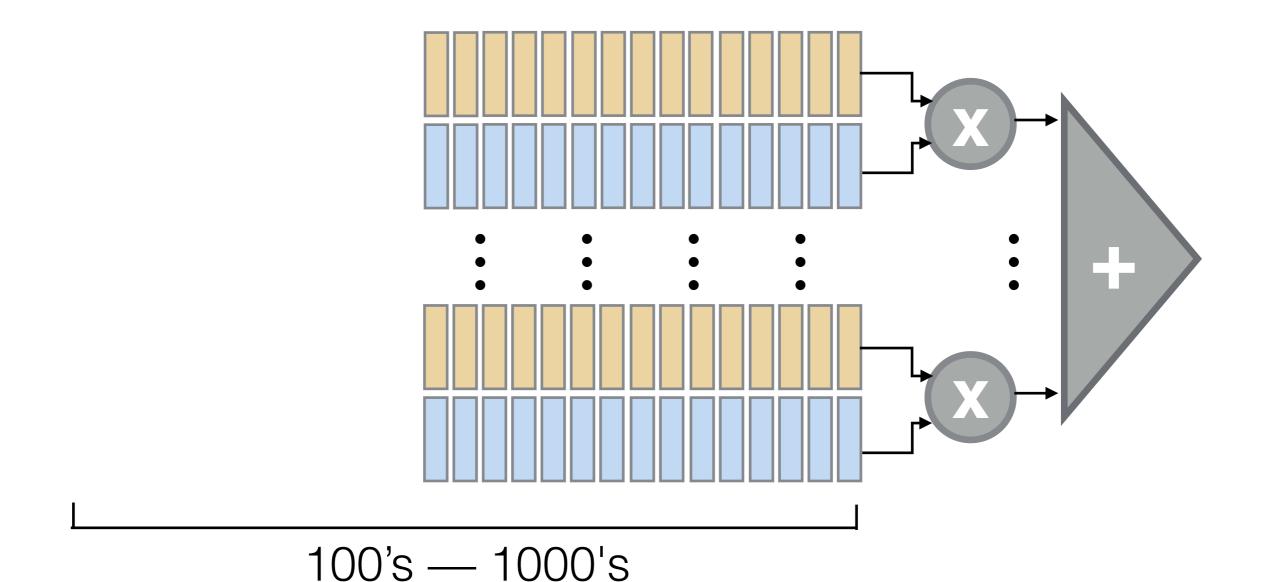












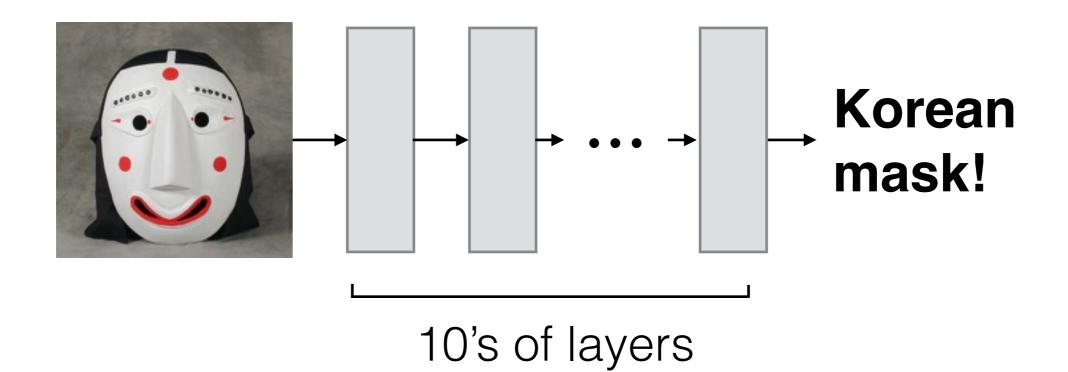
CNVLUTIN: Smarter SIMD

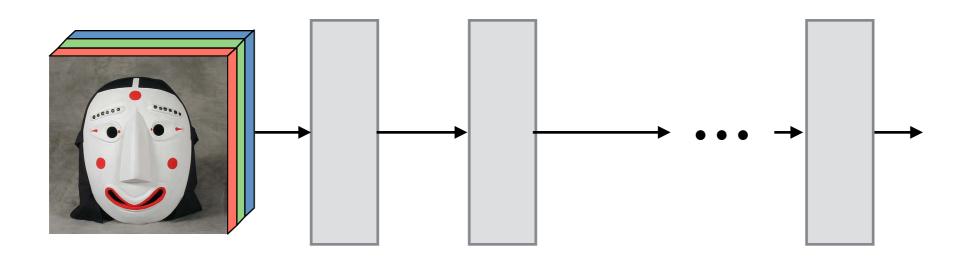
52% Performance — 2x ED²P

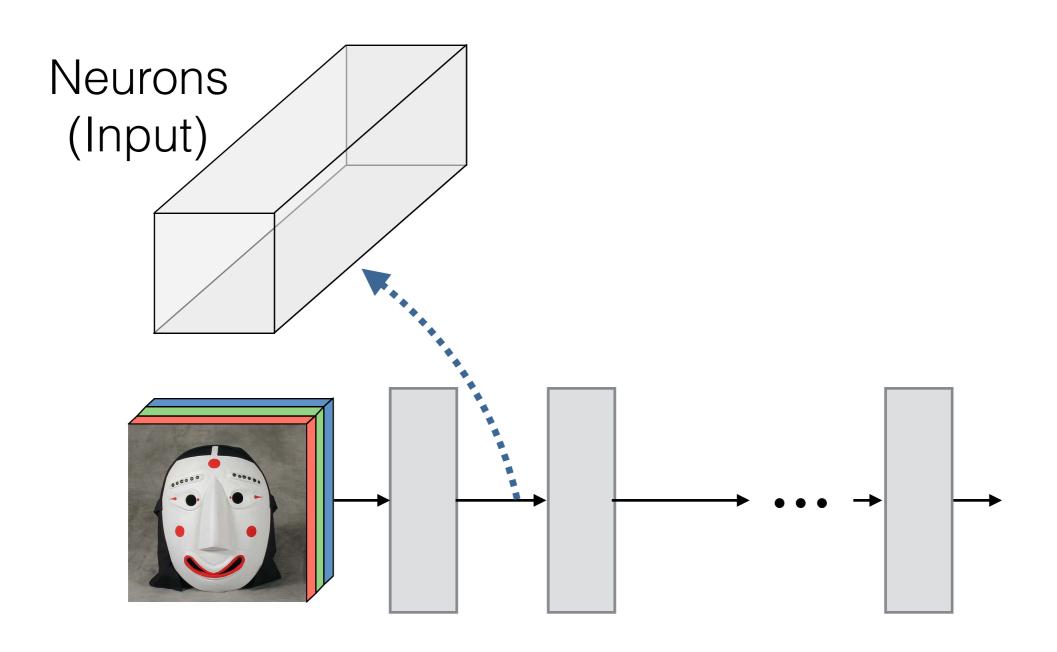
Out-of-the-box networks

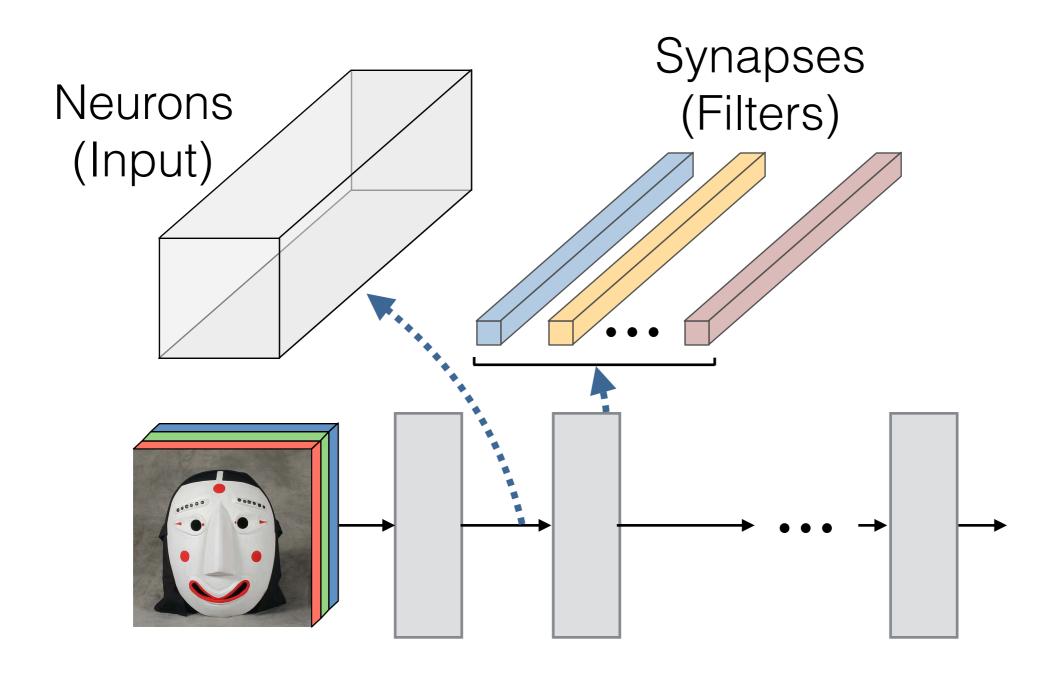
Outline

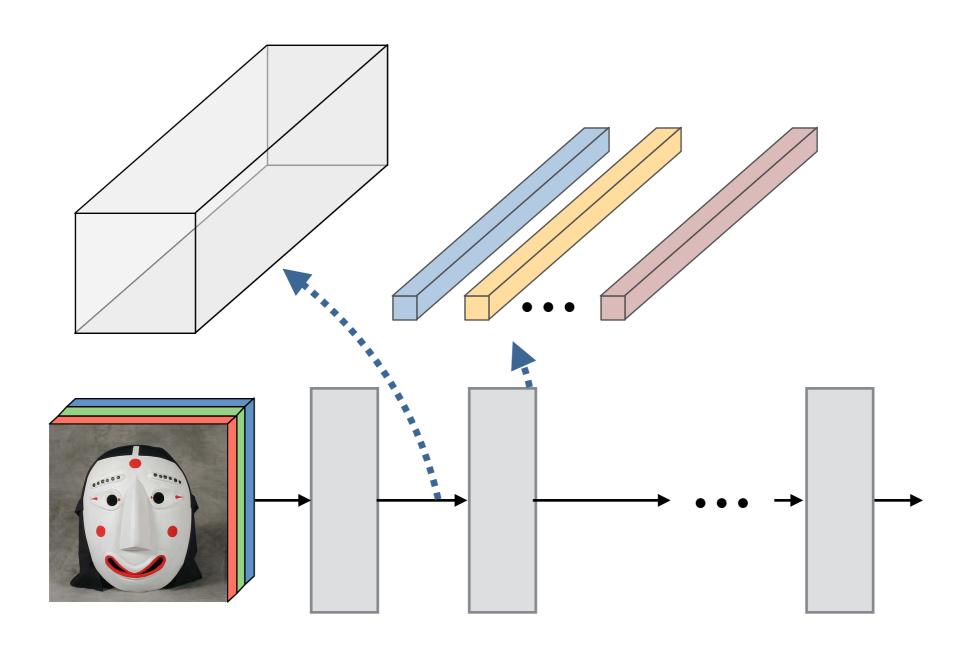
- 1. What's a CNN?
- 2. A wide SIMD design
- 3. CNVLUTIN: Skipping neurons in a wide SIMD design
- 4. Evaluation
- 5. Our approach

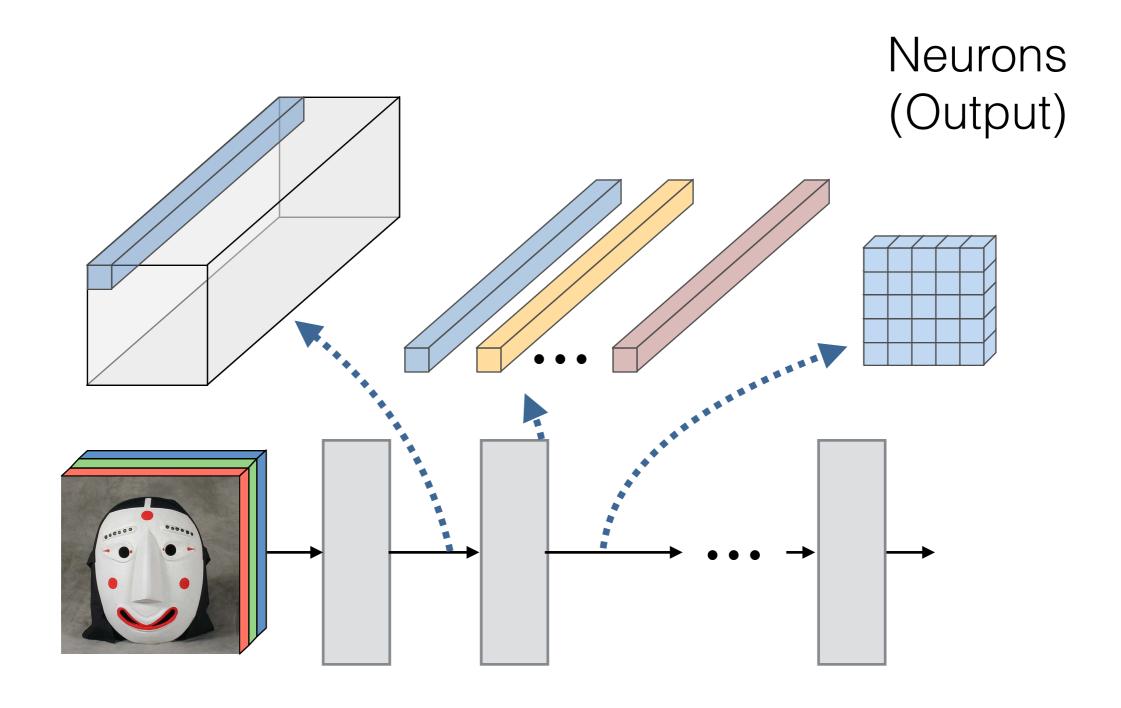


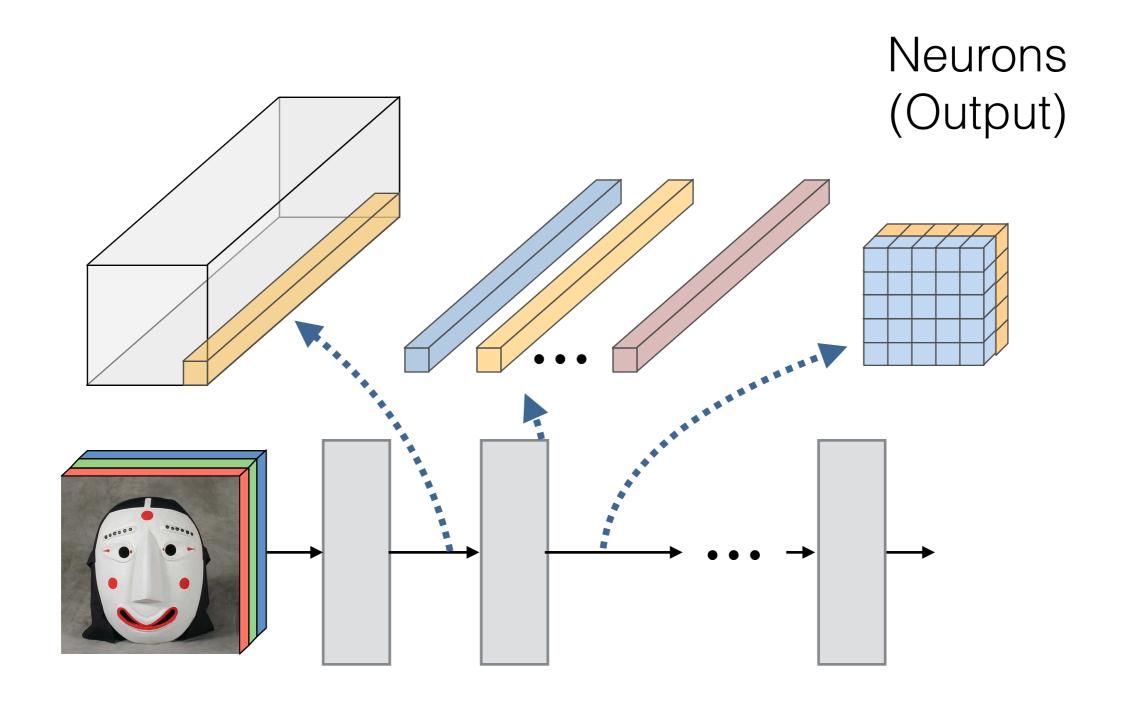


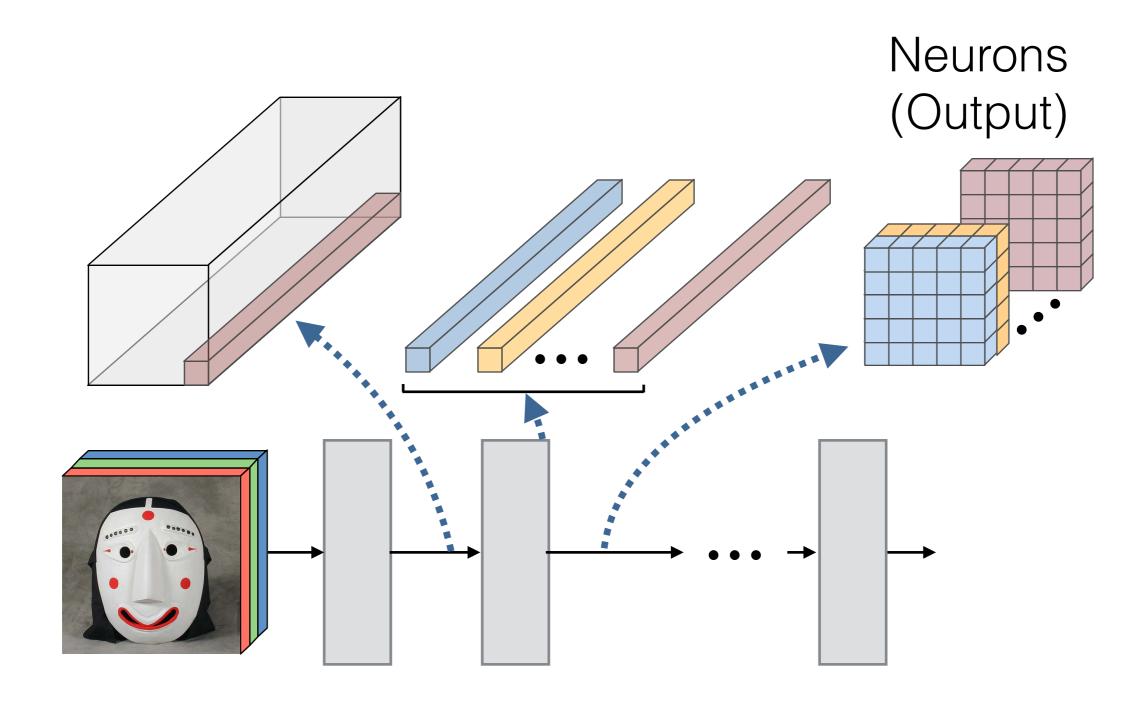


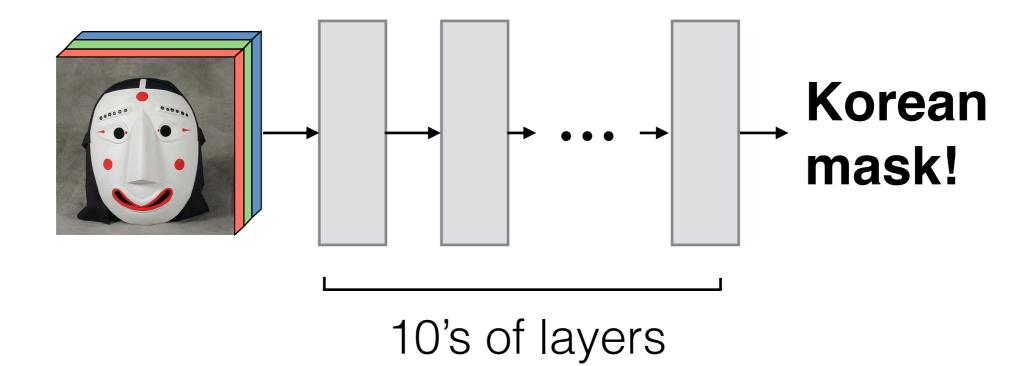


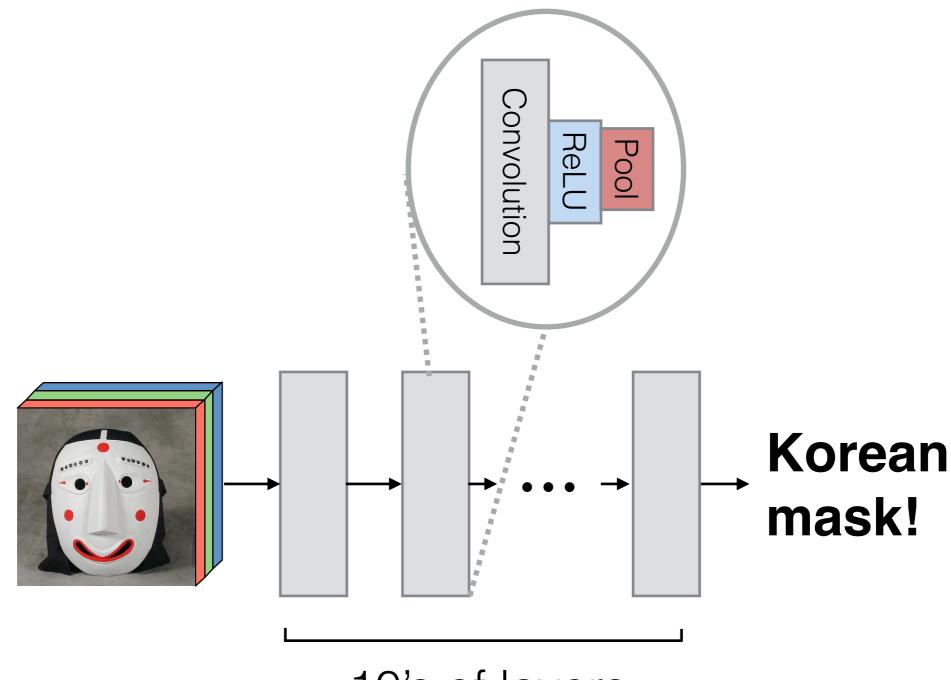




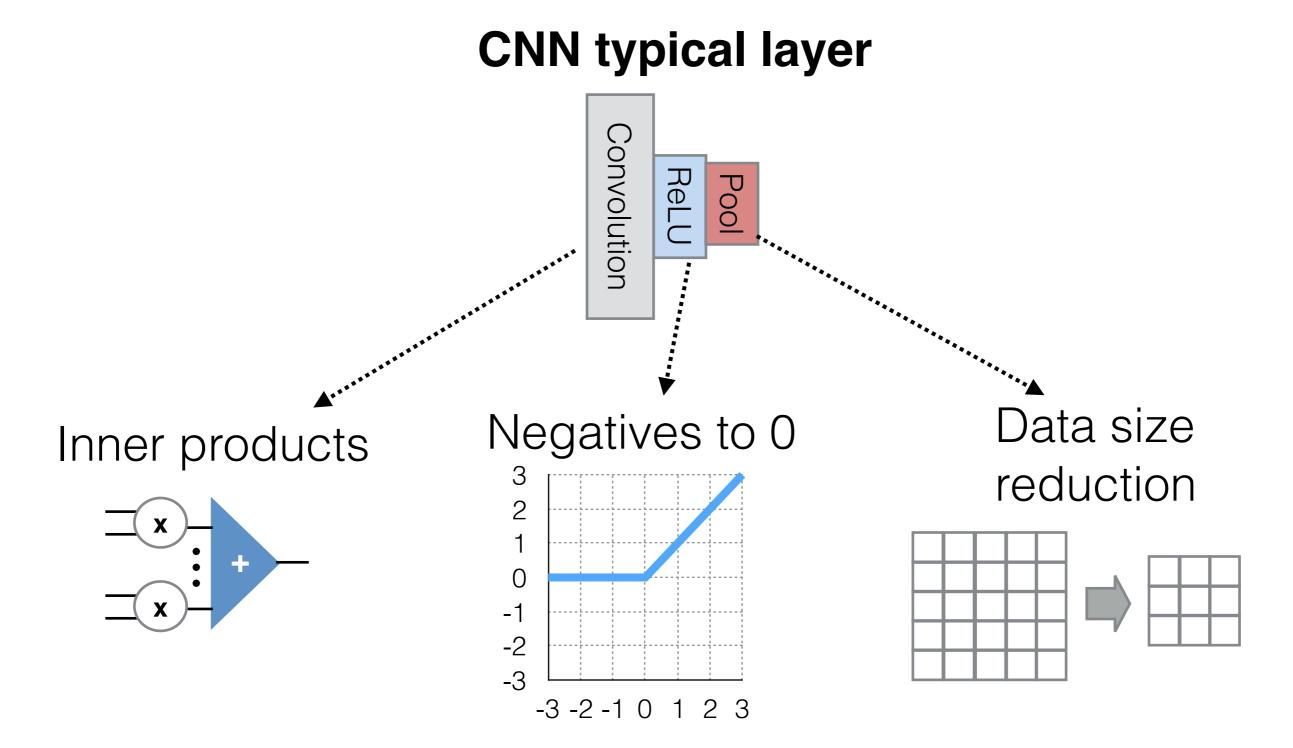








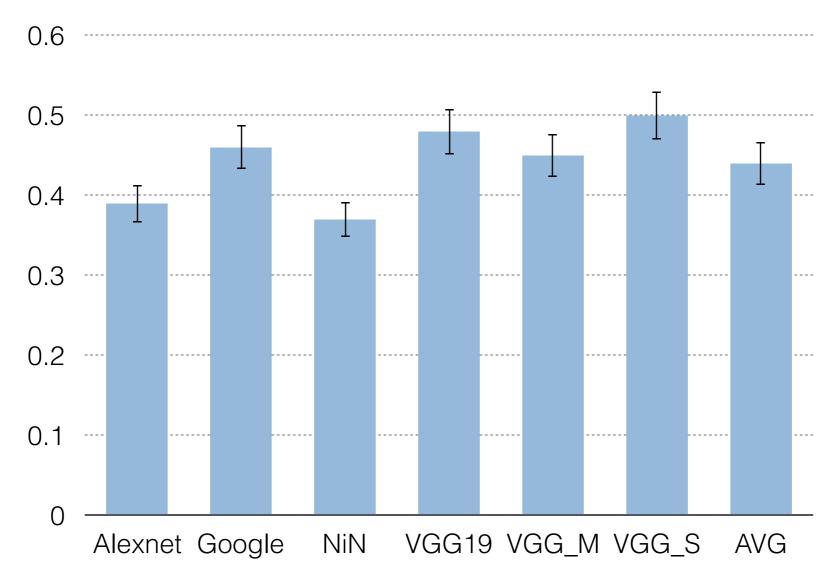
10's of layers



90%

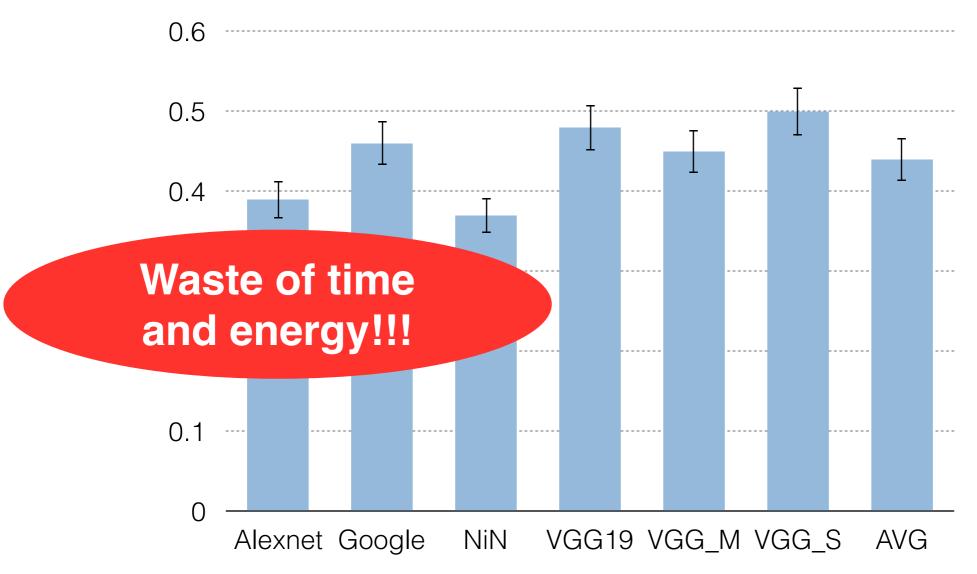
Time spent in convolutions

Lots of Runtime Zeroes



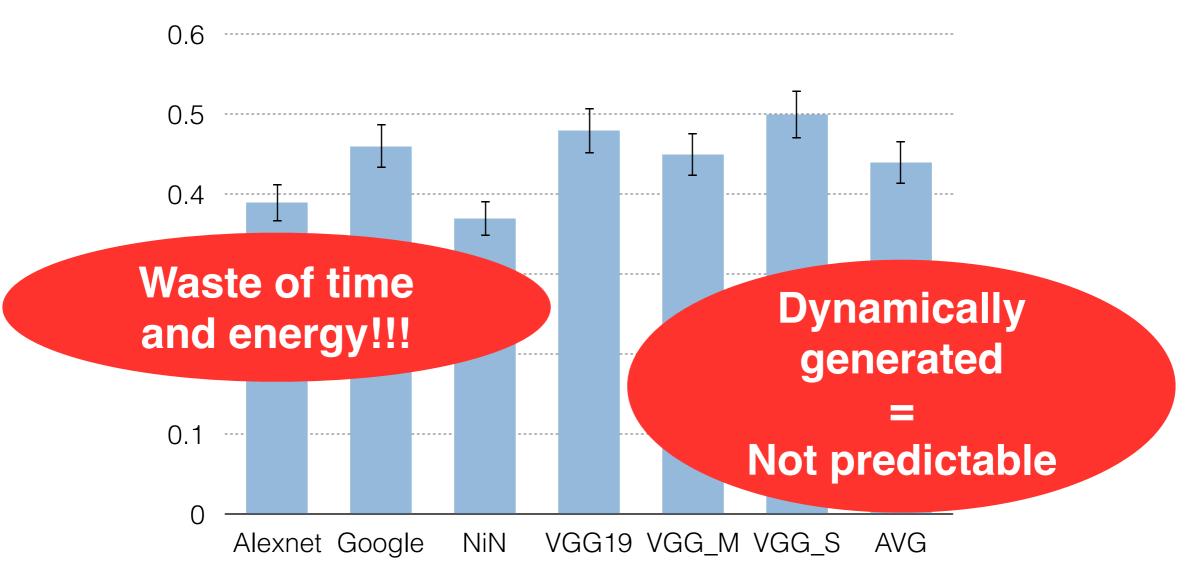
Fraction of zero neurons in multiplications

Lots of Runtime Zeroes



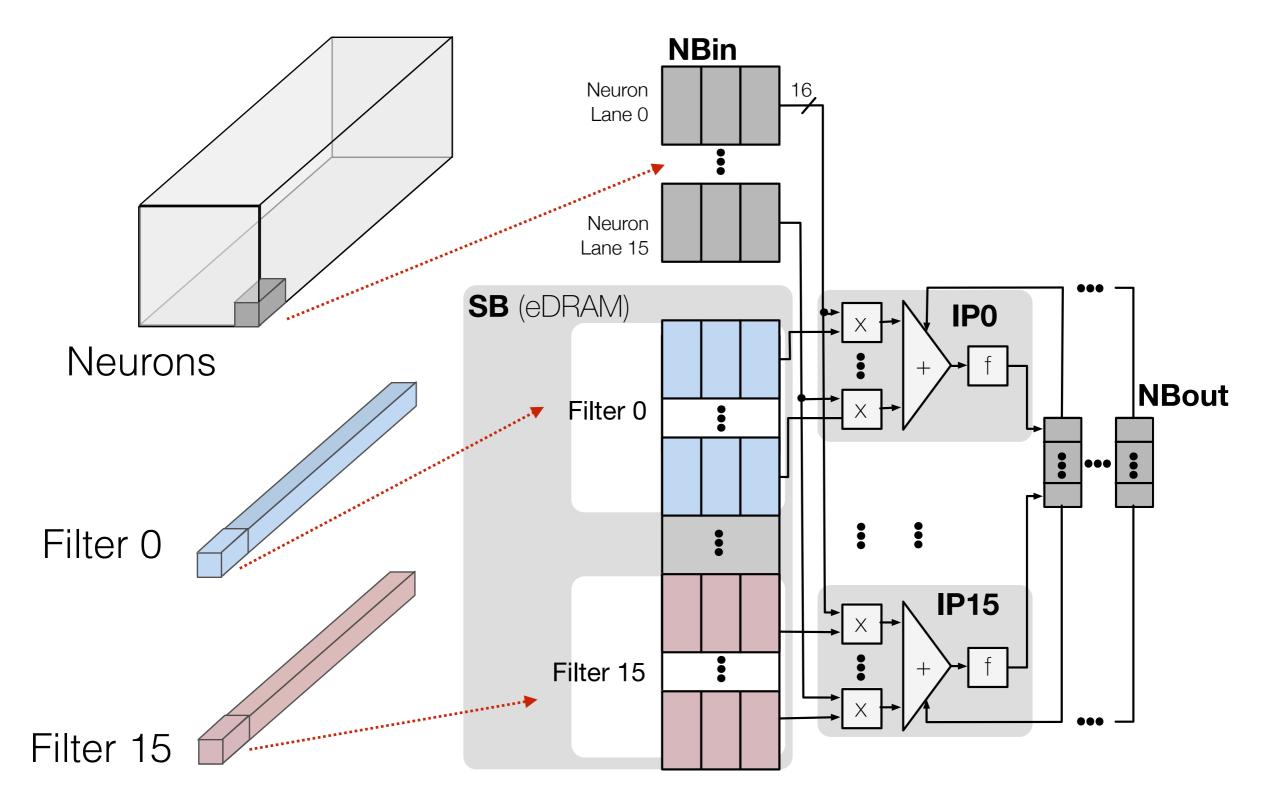
Fraction of zero neurons in multiplications

Lots of Runtime Zeroes



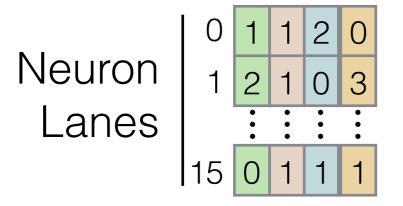
Fraction of zero neurons in multiplications

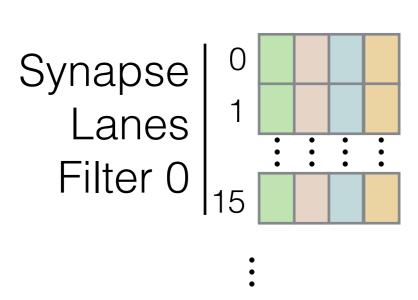
How to compute DNNs: DaDianNao*

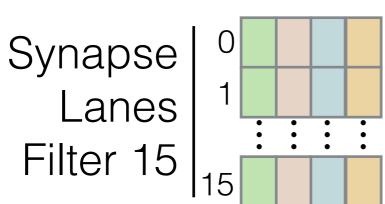


*Chen et al. MICRO 2014

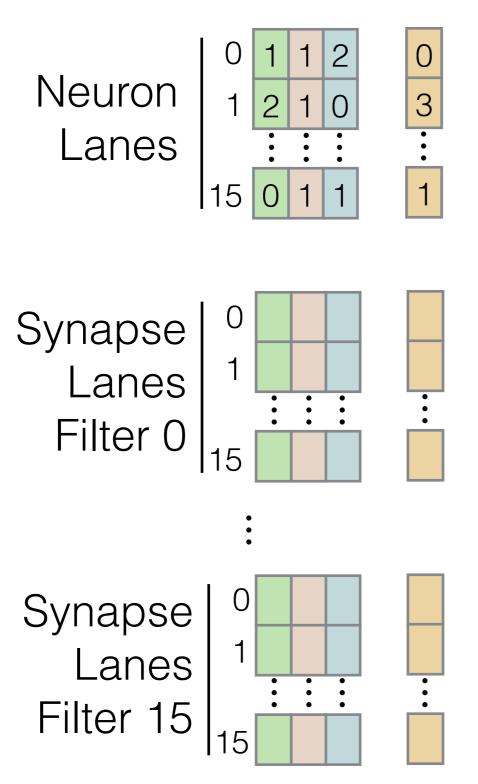
Processing in DaDianNao



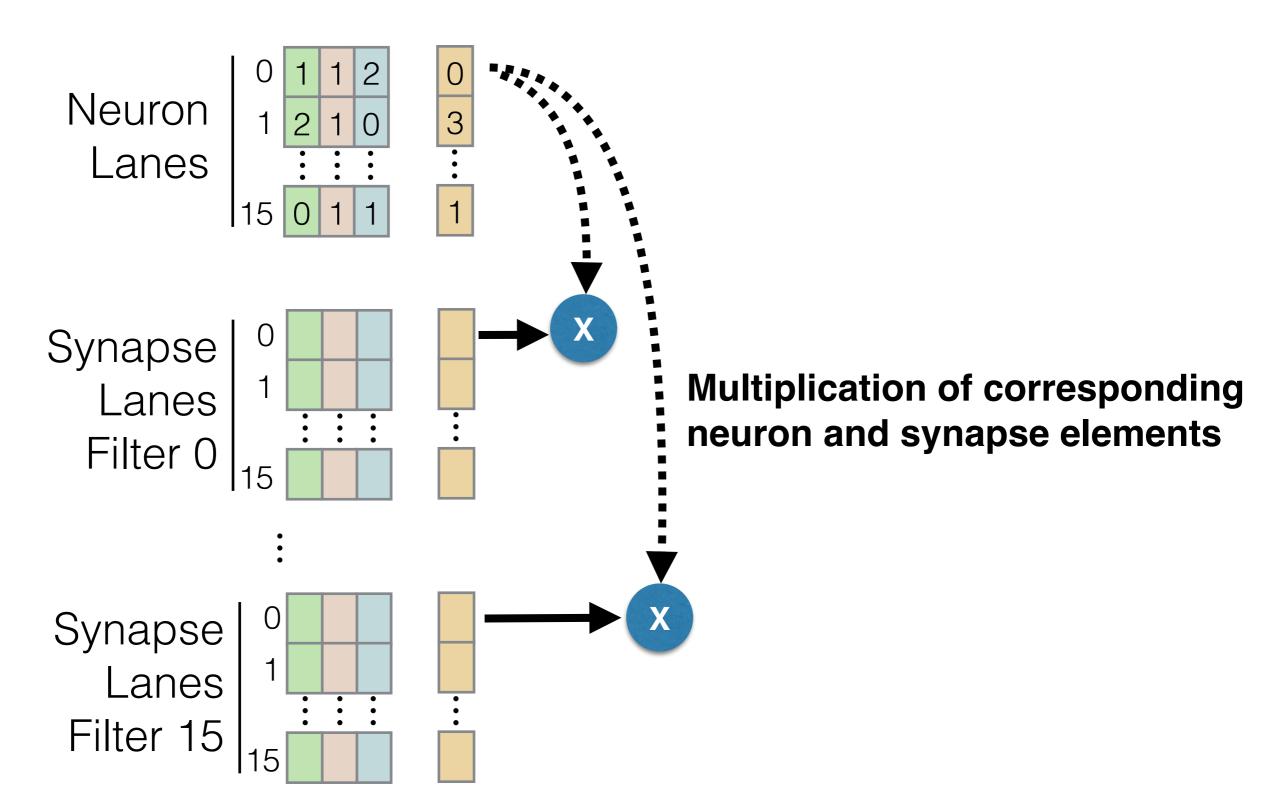


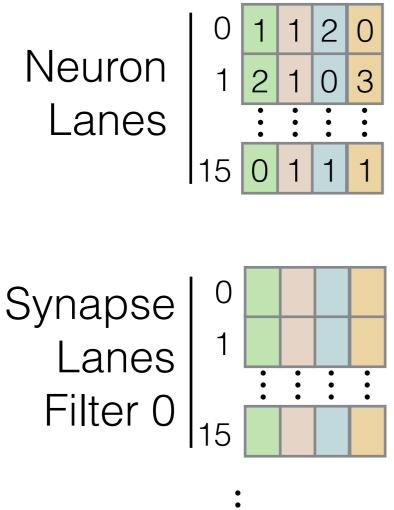


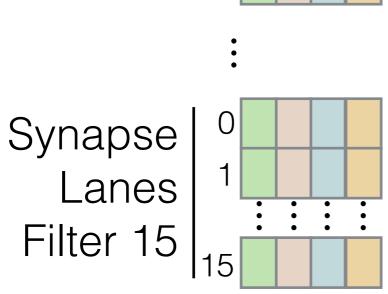
Processing in DaDianNao

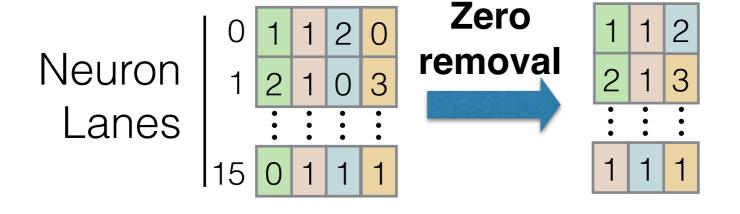


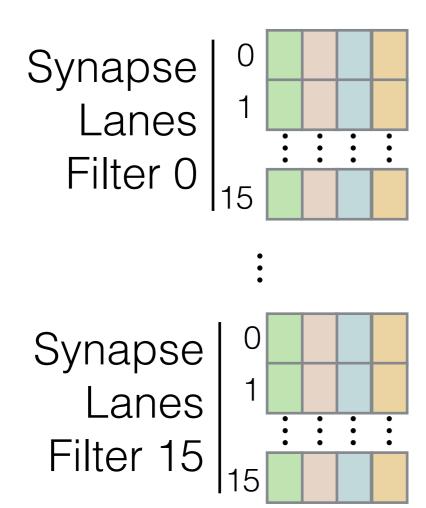
Processing in DaDianNao

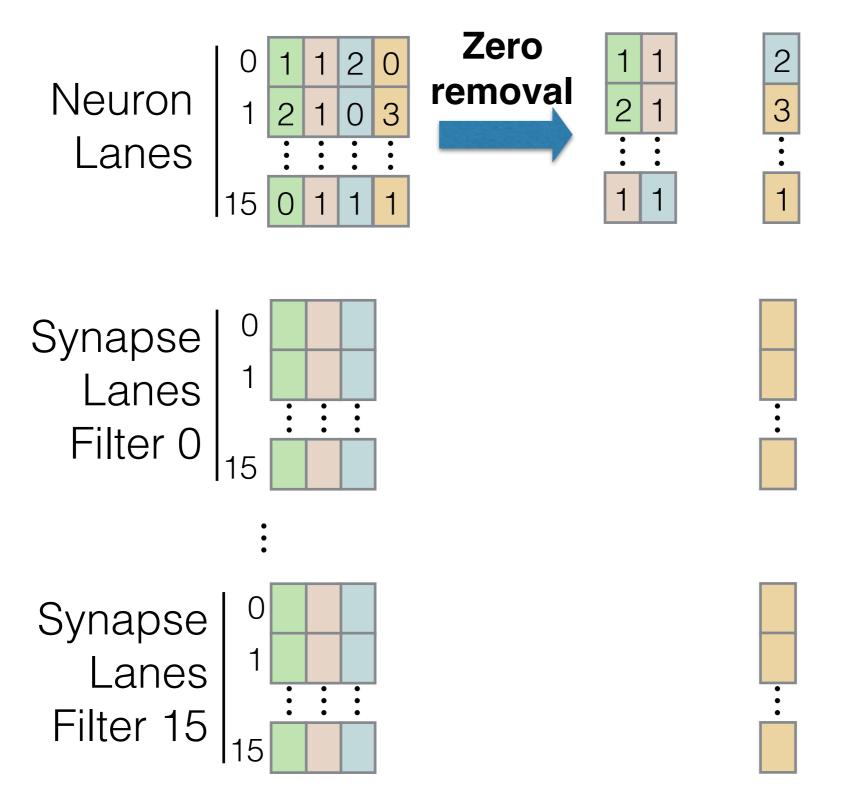


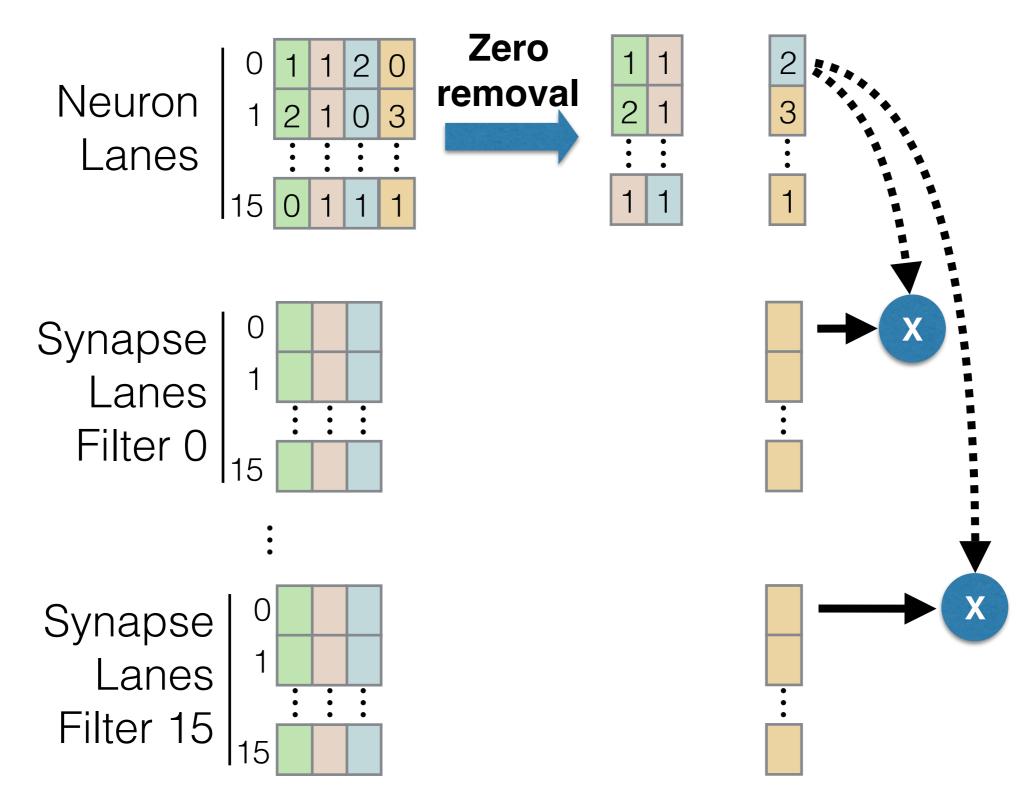


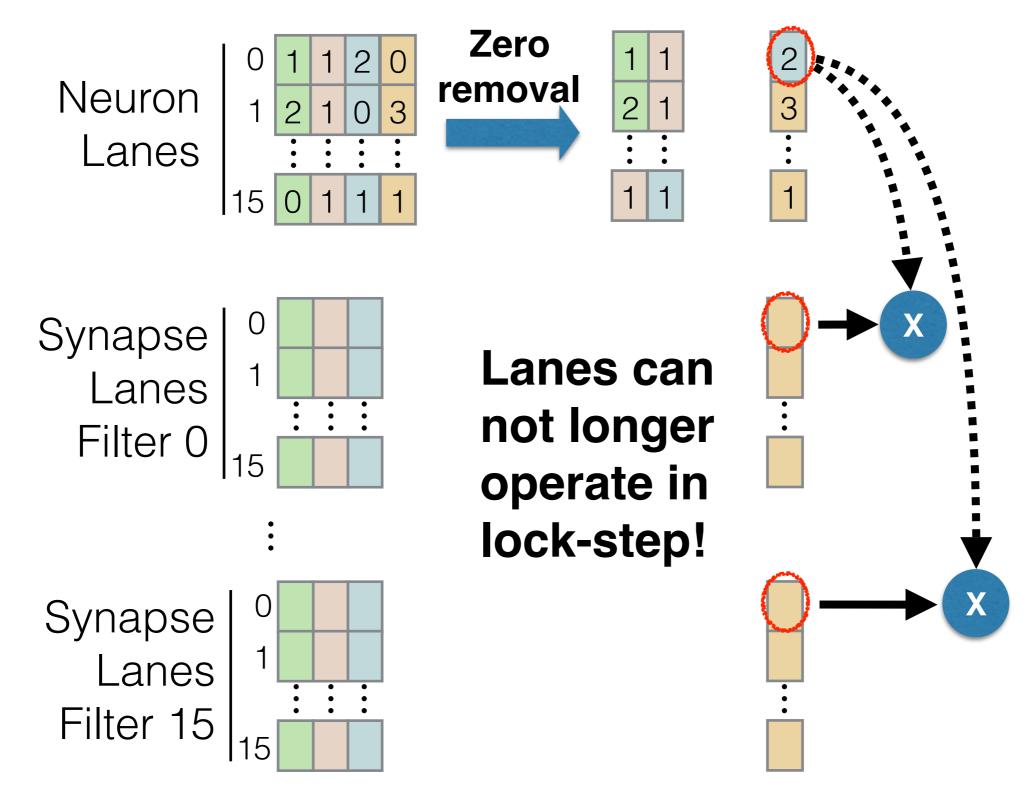




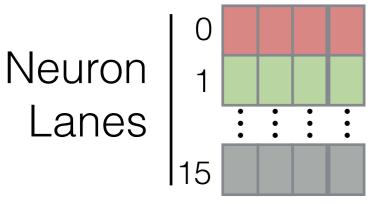


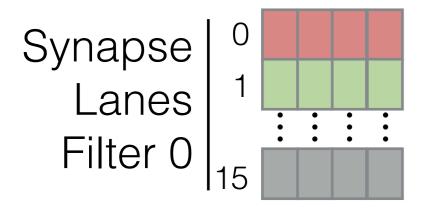


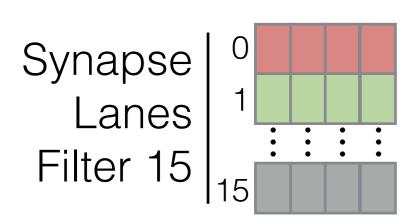


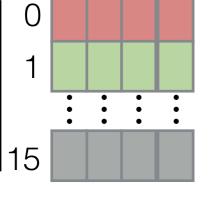


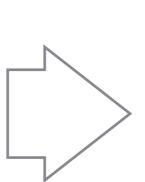
CNVLUTIN: Decoupling Lanes



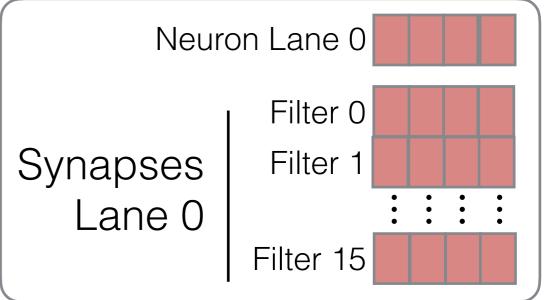




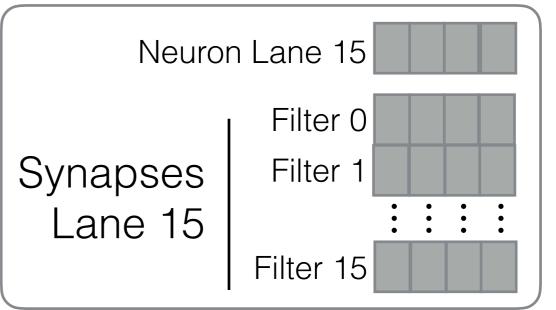




Subunit 0



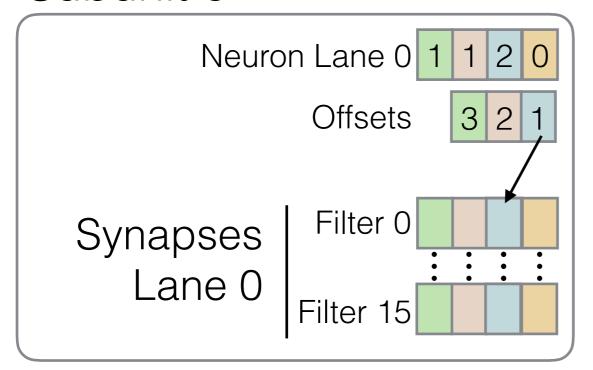
Subunit 15



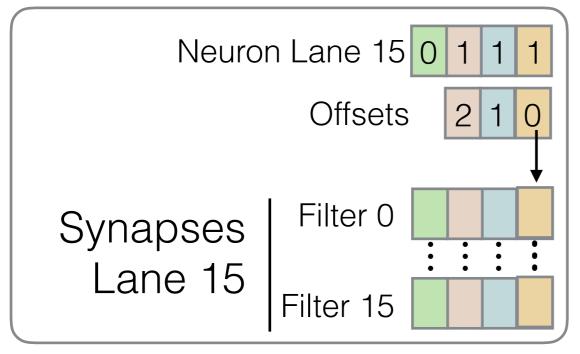
DaDianNao

CNVLUTIN: Decoupling Lanes

Subunit 0

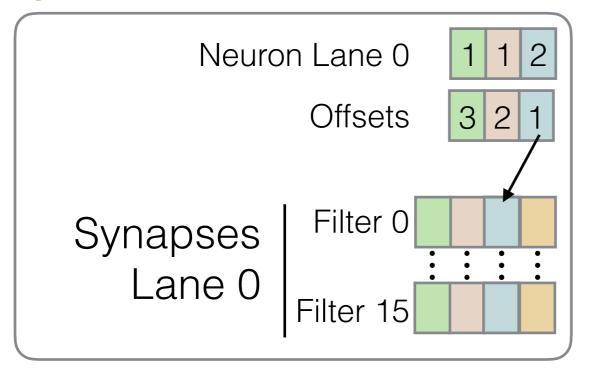


Subunit 15

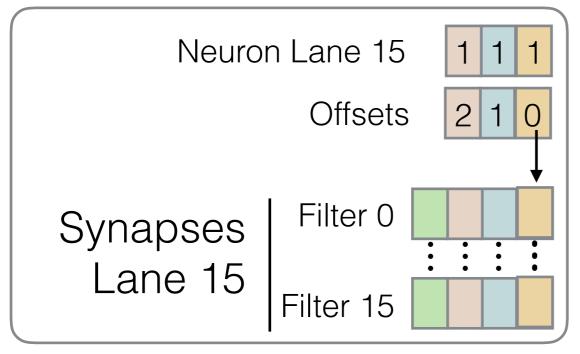


CNVLUTIN: Decoupling Lanes

Subunit 0

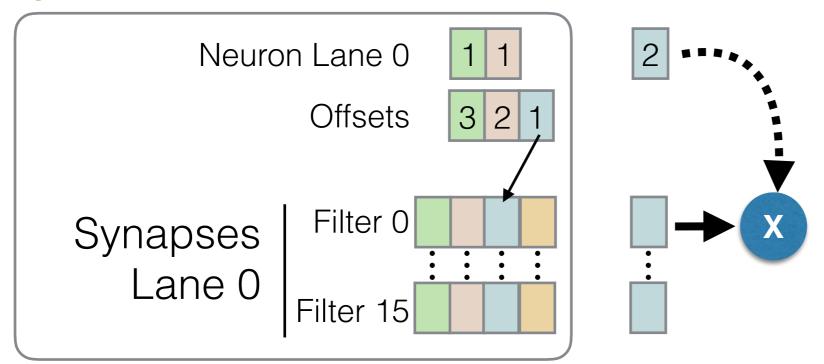


Subunit 15

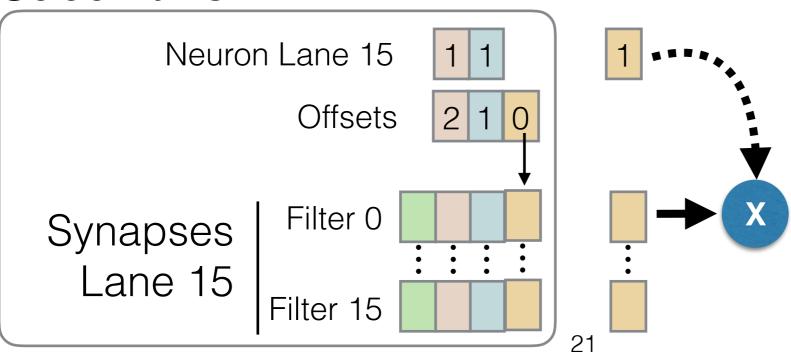


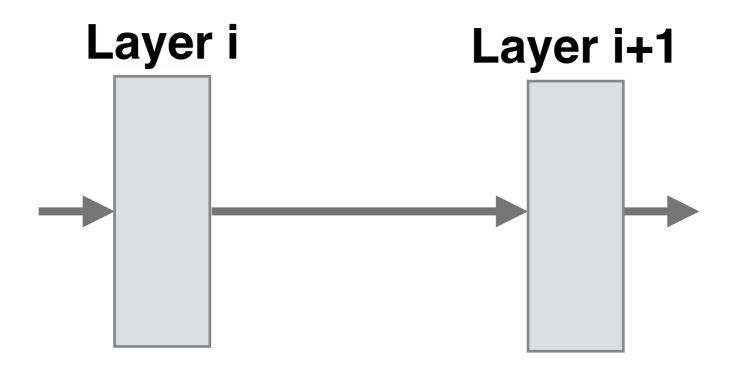
CNVLUTIN: Decoupling Lanes

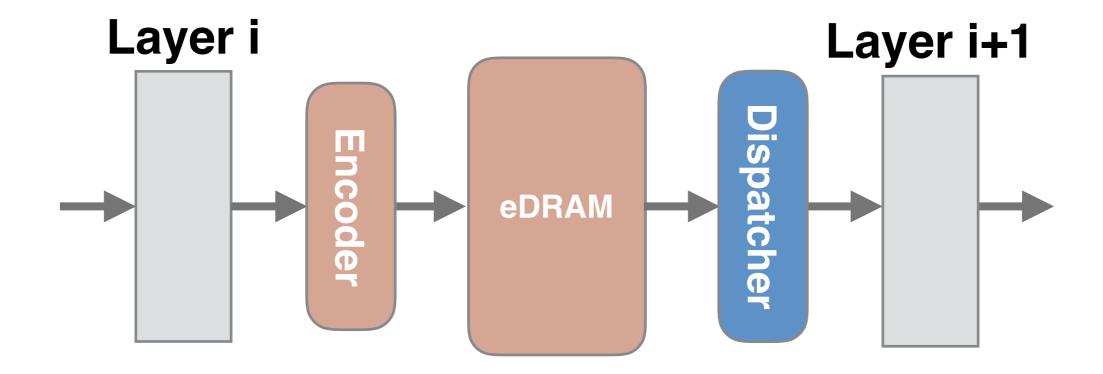
Subunit 0

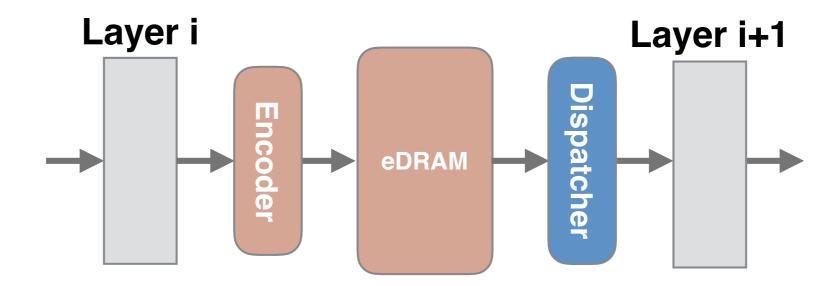


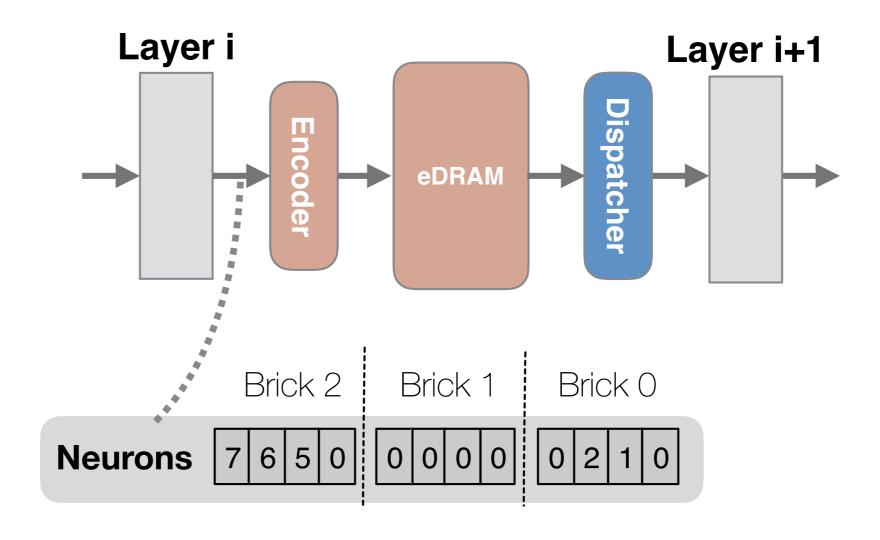
Subunit 15

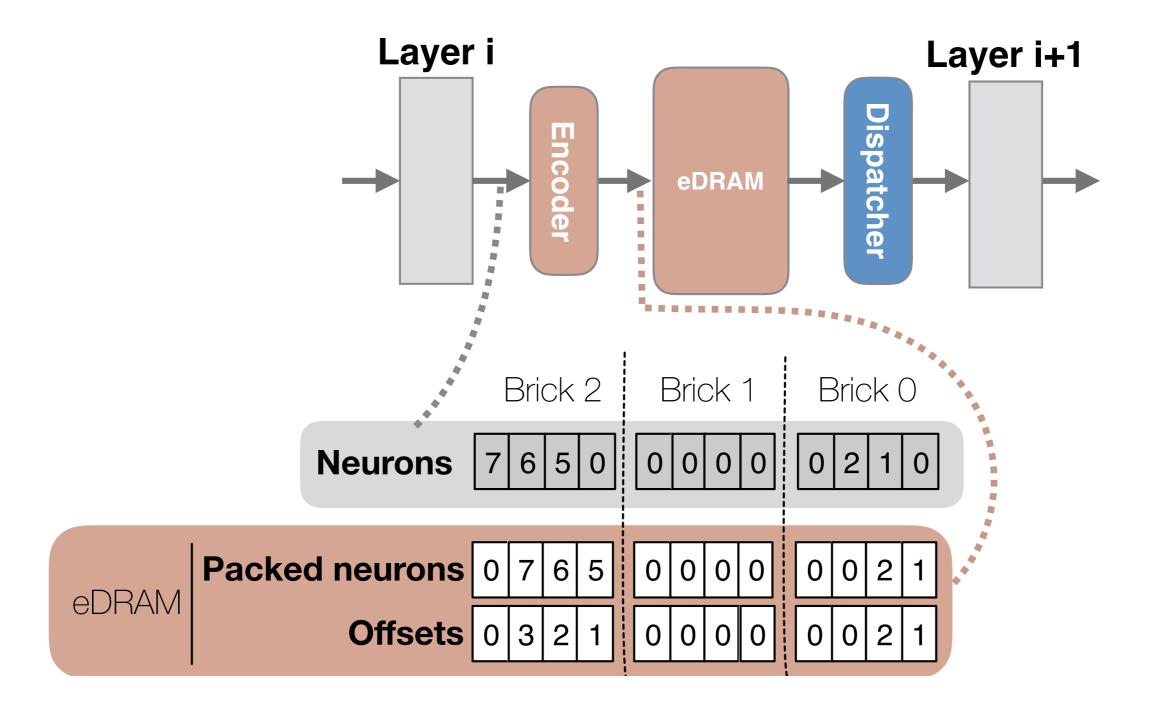


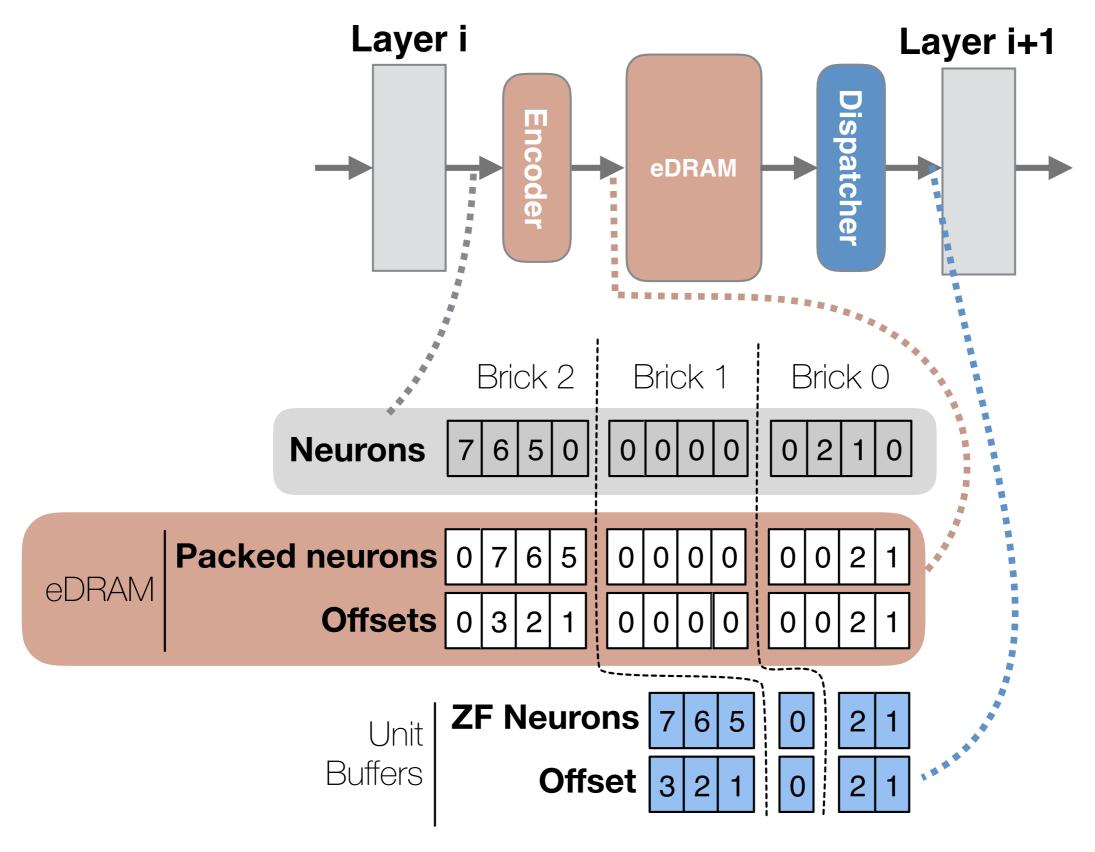




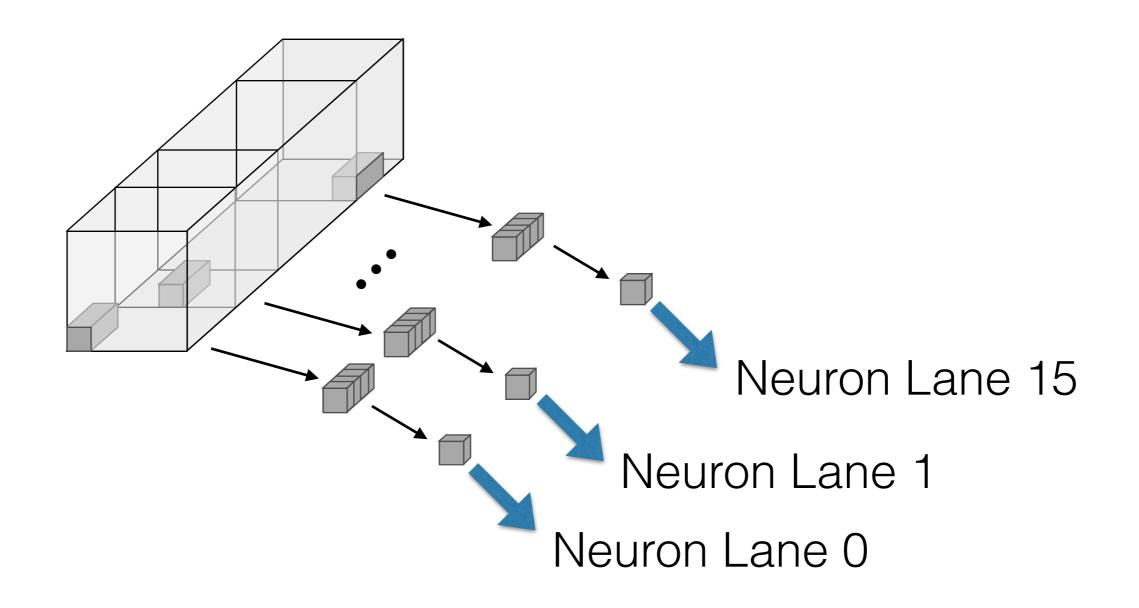








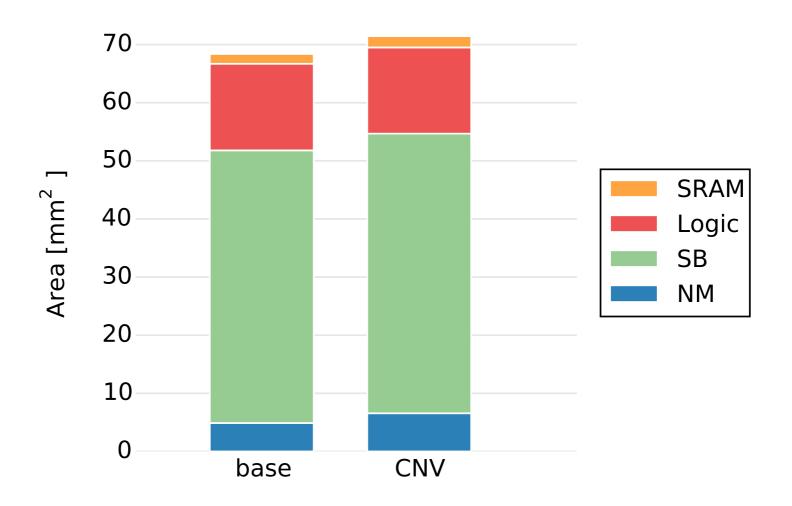
CNVLUTIN: Computation Slicing



Methodology

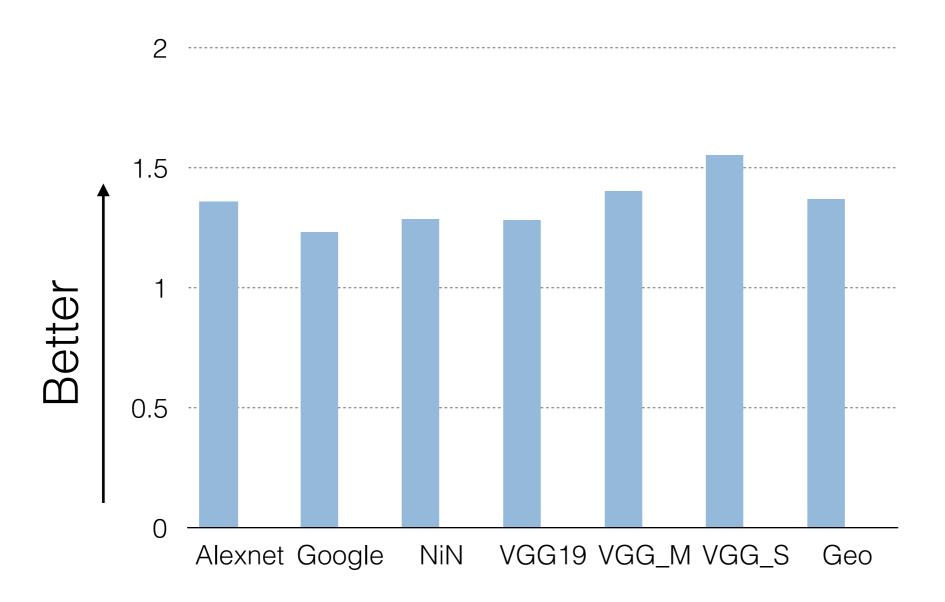
- In-house timing simulator: baseline + CNVLUTIN
- Logic + SRAM: Synthesis on 65nm TSMC
- eDRAM model: Destiny
- DNNs: Trained models from Caffe model zoo

Area

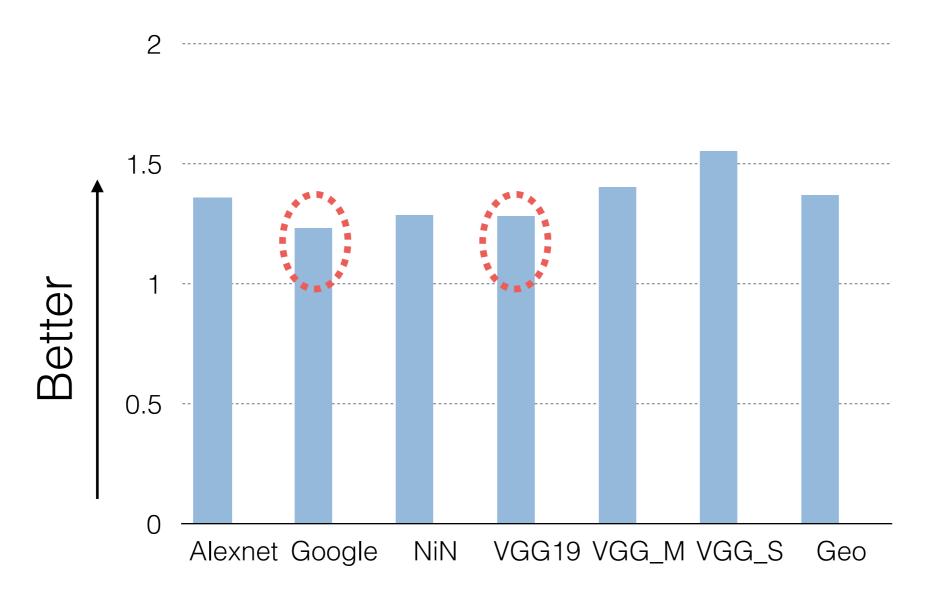


Only +4.5% in area overhead

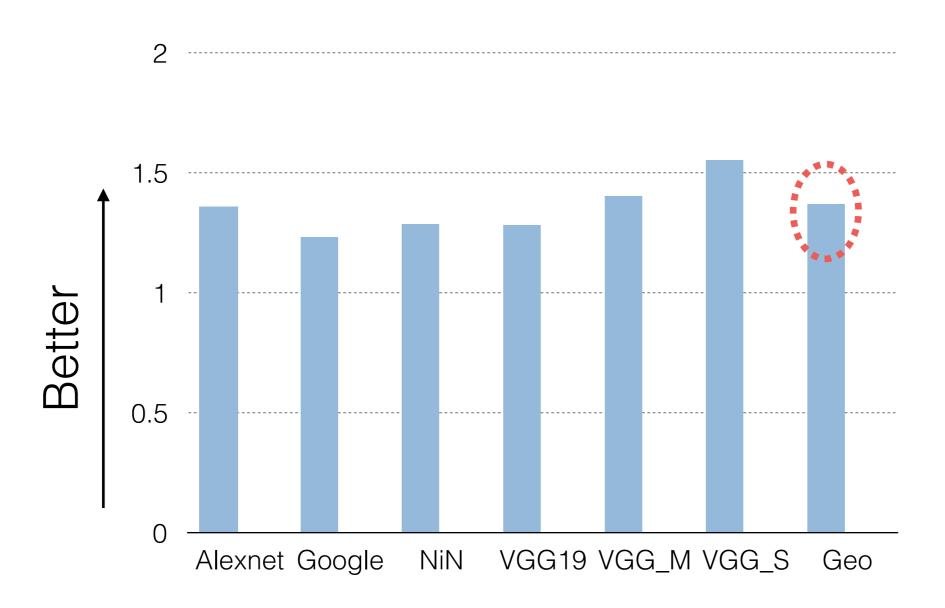
Speedup: ineffectual = 0



Speedup: ineffectual = 0



Speedup: ineffectual = 0



1.37x Performance on average

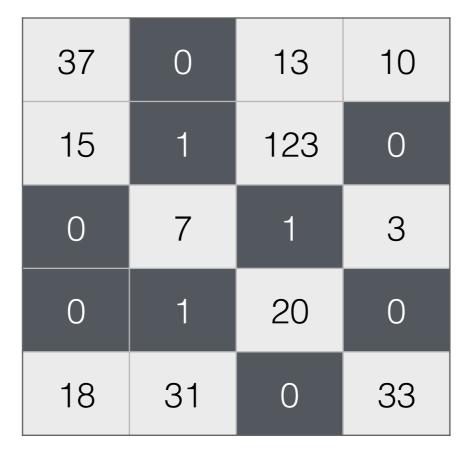
"If all you have is a hammer, everything looks like a nail"

(Maslow's hammer)

37	0	13	10
15	1	123	0
0	7	1	3
0	1	20	0
18	31	0	33

"If all you have is a hammer, everything looks like a nail"

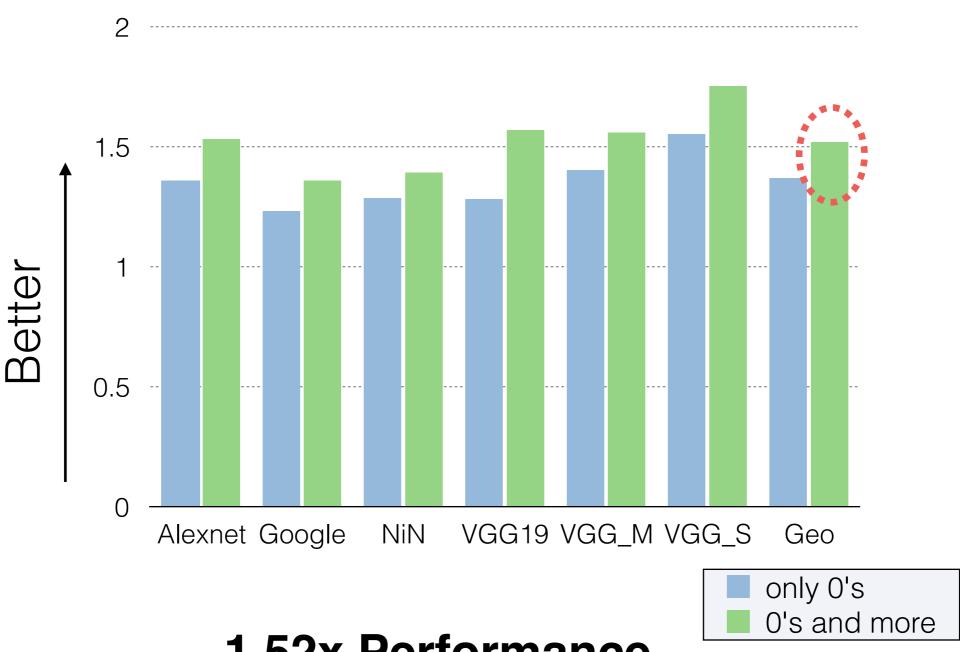
(Maslow's hammer)



Speedup: ineffectual >= 0



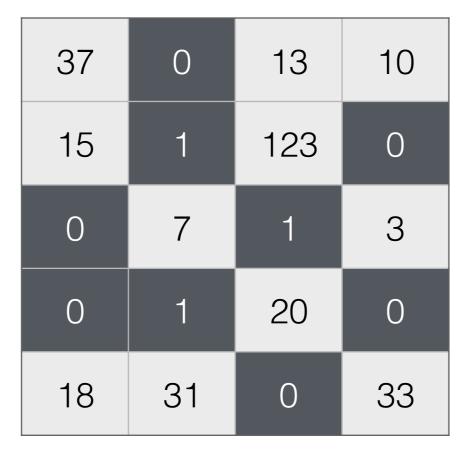
Speedup: ineffectual >= 0



1.52x Performance No accuracy lost

"If all you have is a hammer, everything looks like a nail"

(Maslow's hammer)



"If all you have is a hammer, everything looks like a nail"

(Maslow's hammer)

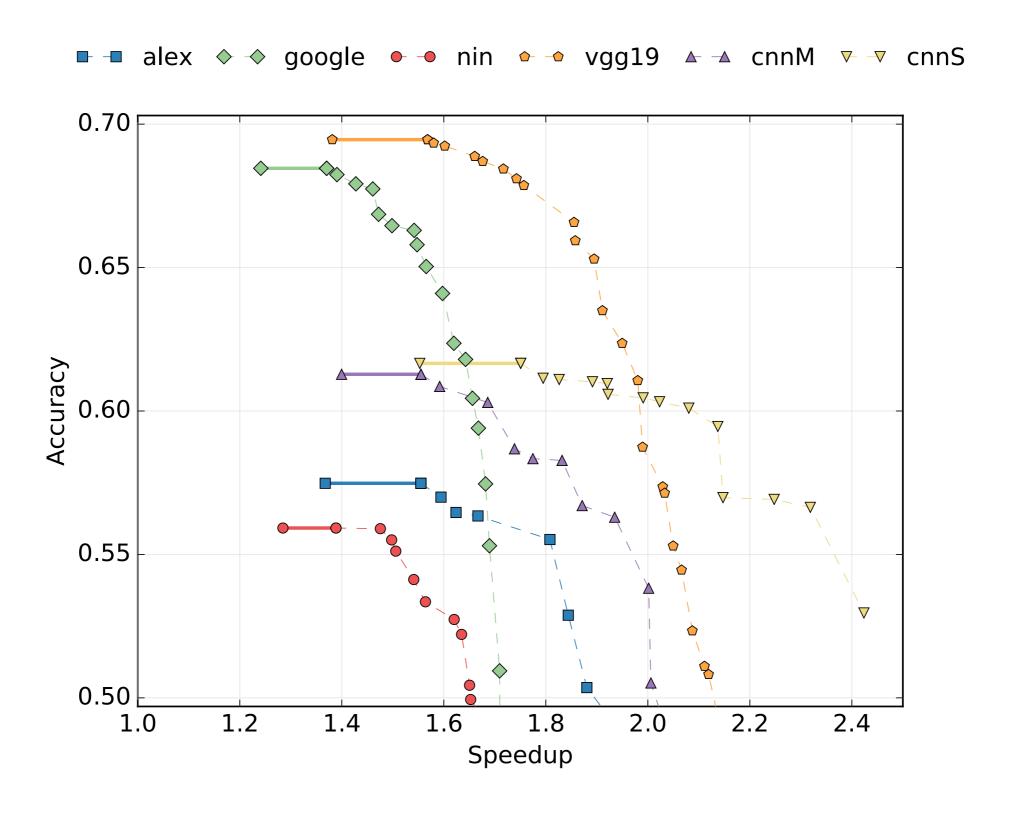
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"If all you have is a hammer, everything looks like a nail"

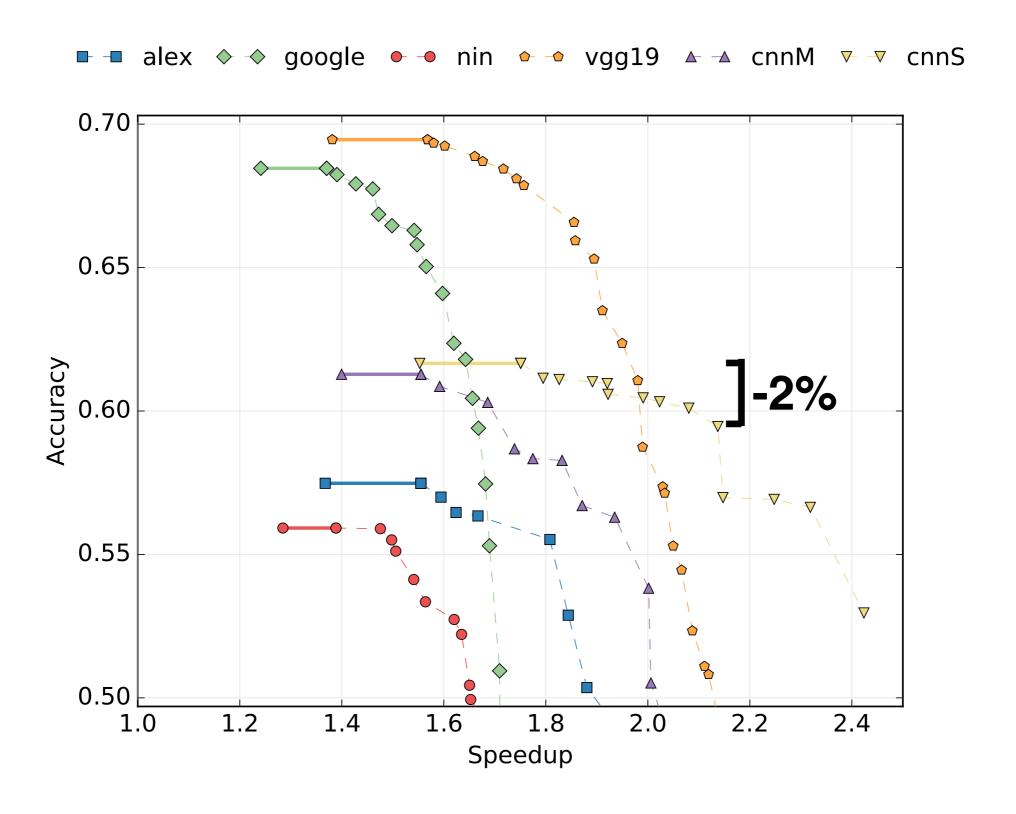
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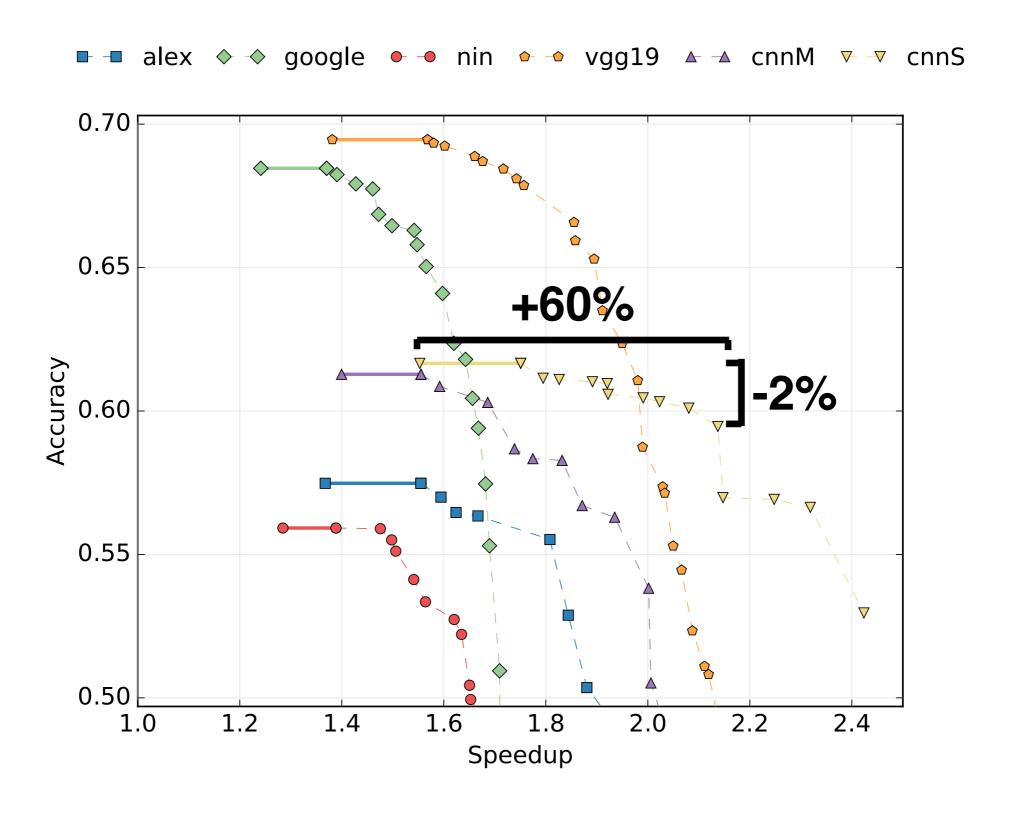
Trading accuracy for performance



Trading accuracy for performance



Trading accuracy for performance



CNVLUTIN: Smarter SIMD

52% Performance — 2x ED²P No accuracy lost

out-of-the-box networks

Our Approach

Value-Aware Deep Learning Acceleration

arXiv, a while ago:

Reduced-Precision Strategies for Bounded Memory in DNNs

ICS 2016

Proteus: Exploiting Numerical Precision Variability in DNNs

Today

CNVLUTIN: Ineffectual-Neuron-Free DNN Computing

CAL (to appear)

How to offer performance that scales linearly with required numerical precision

More things coming soon :-)

Additional Material

CNVLUTIN: Ineffectual-neuron-free DNN computing

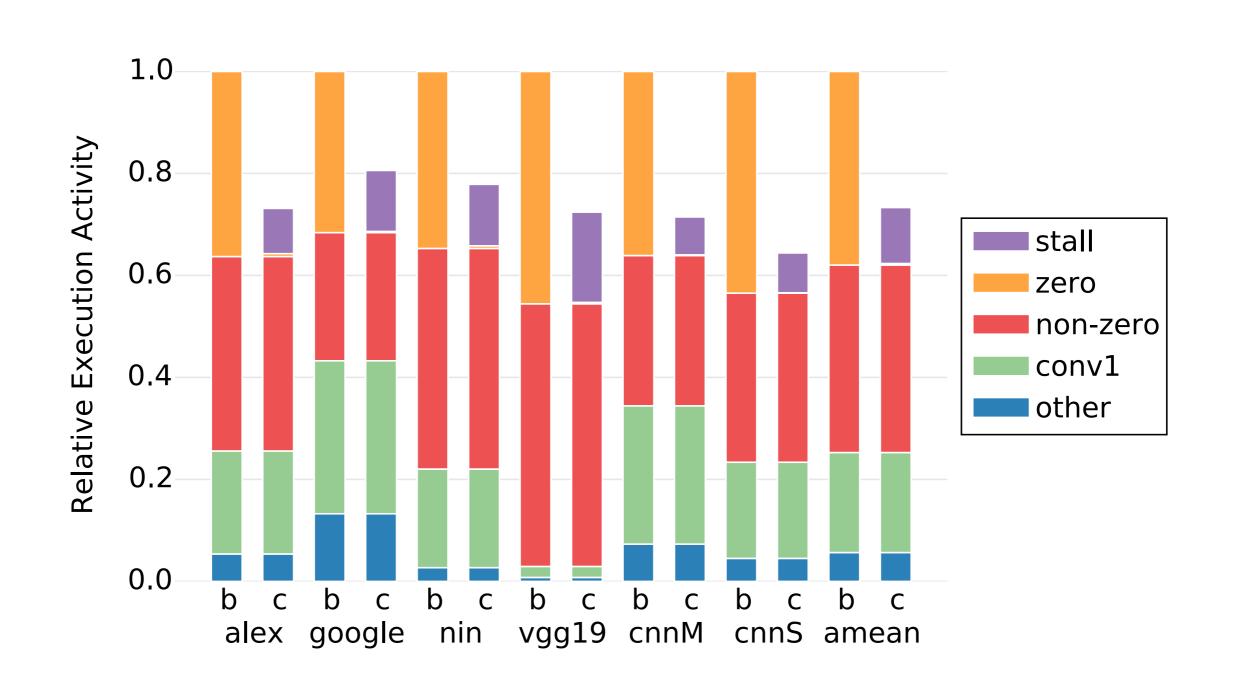
J. Albericio, P. Judd, T. Hetherington*, T. Aamodt*, N. E. Jerger, A. Moshovos





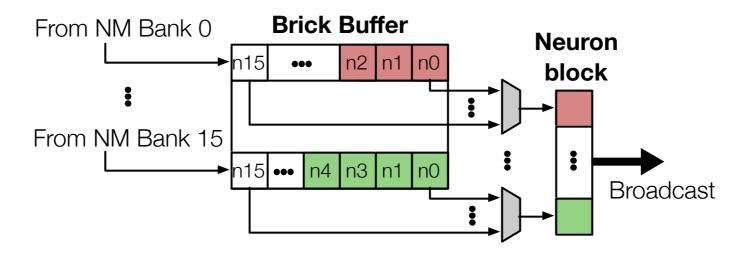
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Execution Activity Breakdown

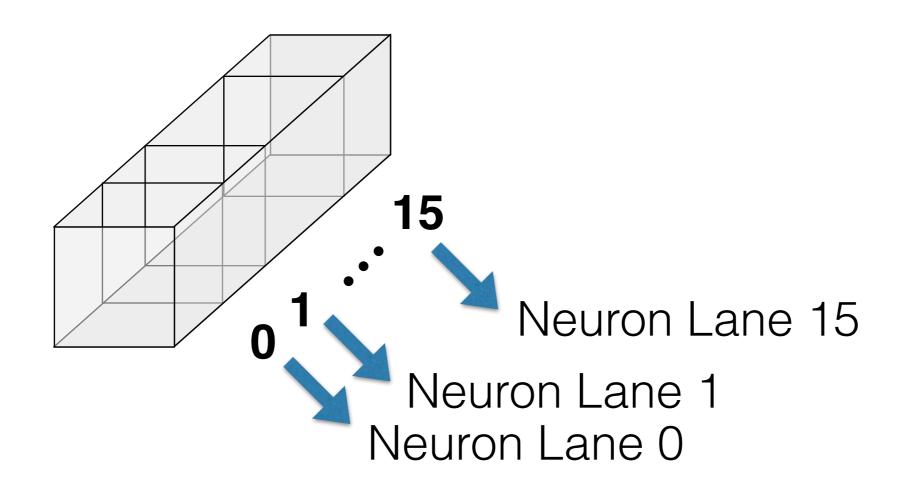


Dispatcher:

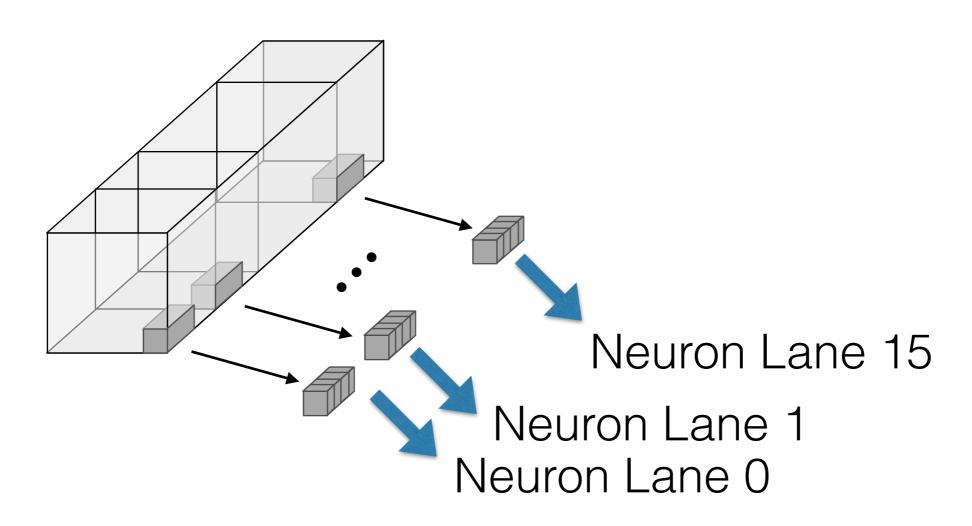
Reads Neuron Bricks - up to 16 neuron Maintain one per Neuron Lane



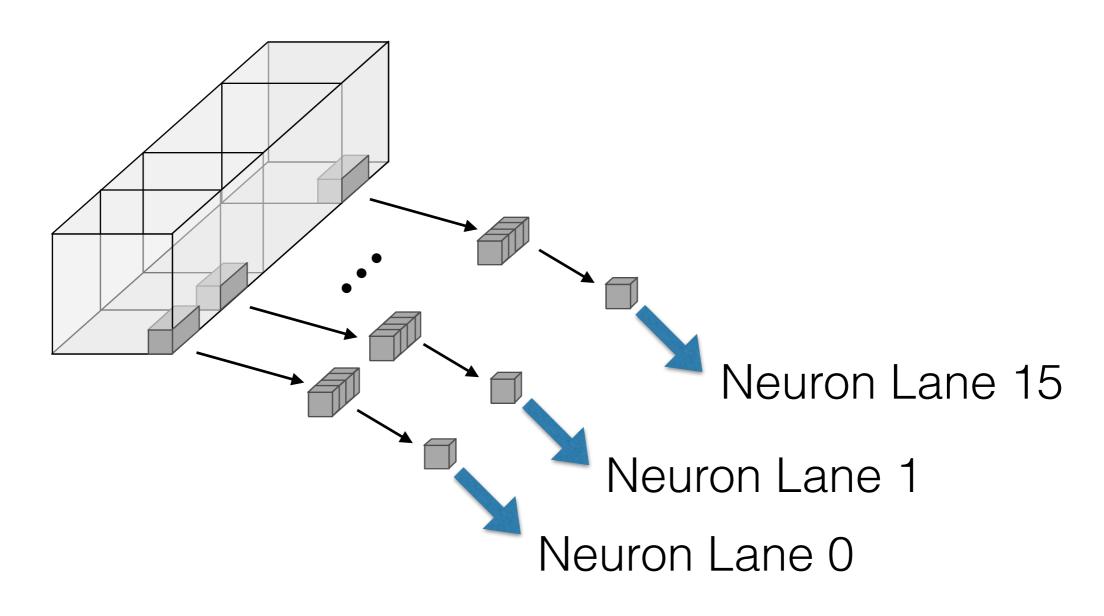
#1: Partition NM in 16 Slices over 16 banks



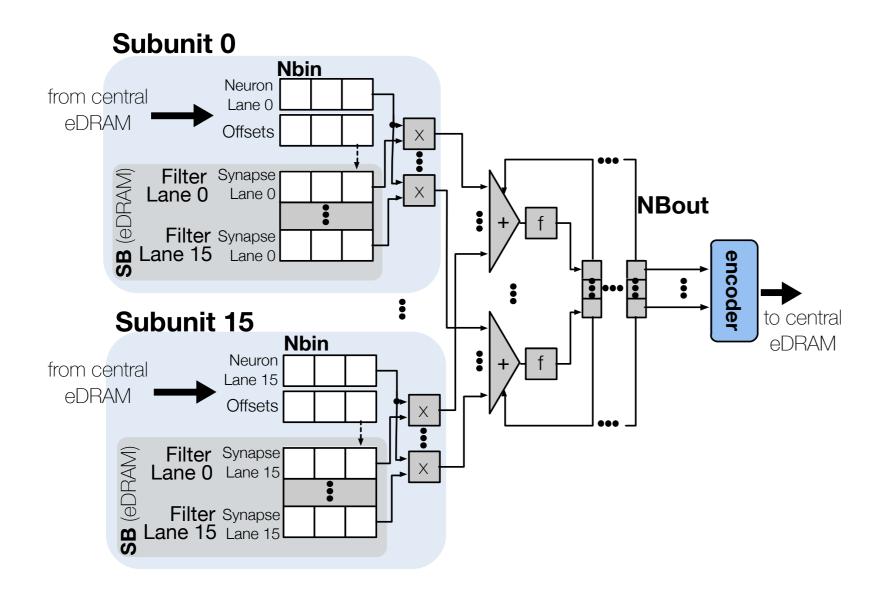
#2: Fetch and Maintain One Container per Slice Container: up to 16 non-zero neurons



#3: Keep neuron lanes supplied with one neuron per cycle



Cnvlutin: Summary



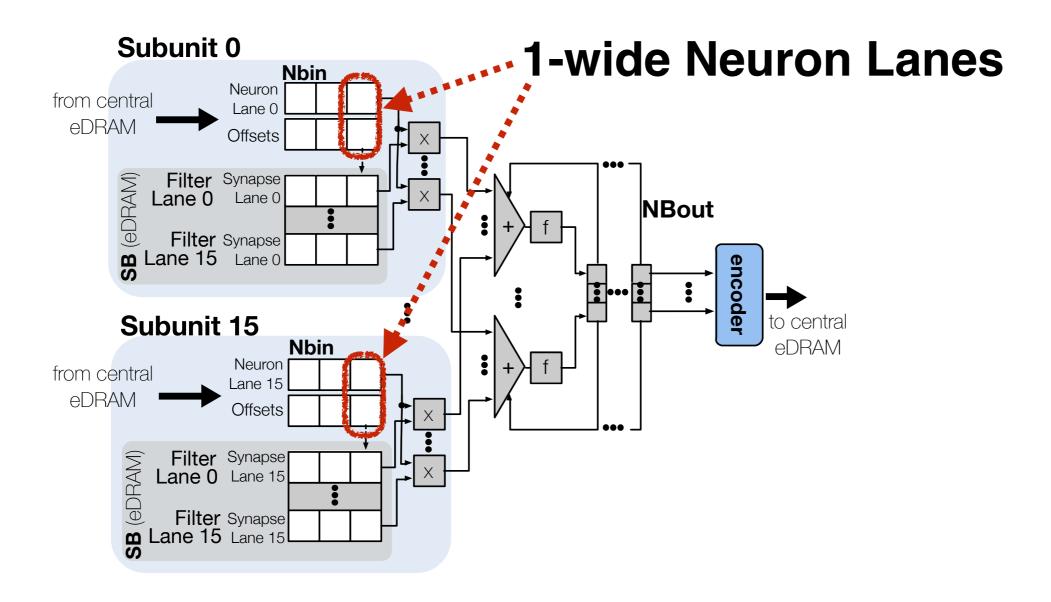
Decoupled Neuron Lanes:

Neuron + coordinate Proceed independently

Partitioned SB:

16-wide accesses1 synapse per filter

Cnvlutin: Summary



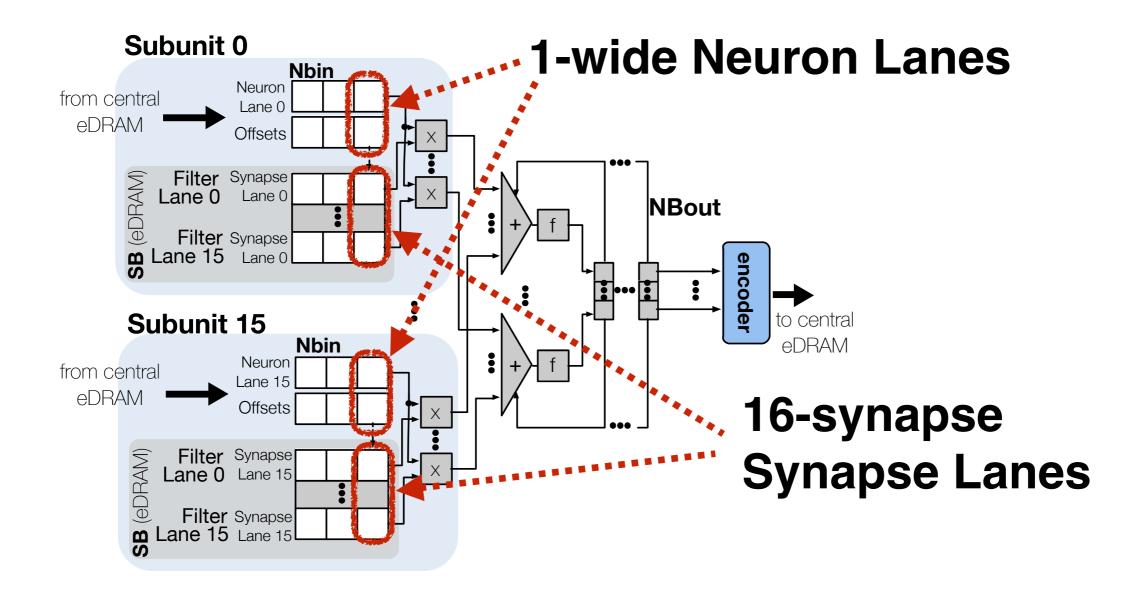
Decoupled Neuron Lanes:

Neuron + coordinate Proceed independently

Partitioned SB:

16-wide accesses1 synapse per filter

Cnvlutin: Summary



Decoupled Neuron Lanes:

Neuron + coordinate Proceed independently

Partitioned SB:

16-wide accesses1 synapse per filter