SR: Set/reset flip-flop

Description

Use the instruction "Set/reset flip-flop" to set or reset the bit of the specified operand, depending on the signal state of the inputs S and R1. If the signal state at input S is "1" and the input R1 is "0", the specified operand is set to "1". If the signal state is "0" at input S and "1" at input R1, the specified operand will be reset to "0".

Input R1 takes priority over input S. When the signal state is "1" on both inputs S and R1, the signal state of the specified operand is reset to "0".

The instruction is not executed if the signal state at the two inputs S and R1 is "0". The signal state of the operand then remains unchanged.

The current signal state of the operand is transferred to output Q and can be queried there.

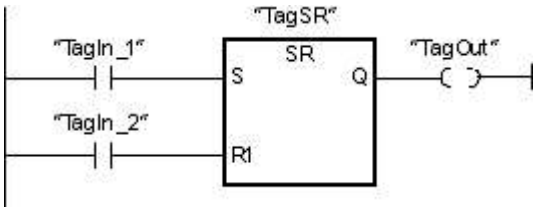
Parameters

The following table shows the parameters of the "Set/reset flip-flop" instruction:

Parameters	Declaration	Data type	Memory area	Description
S	Input	BOOL	I, Q, M, D, L	Enable setting
R1	Input	BOOL	I, Q, M, D, L, T, C	Enable resetting
<Operand>	InOut	BOOL	I, Q, M, D, L	Operand that is set or reset.
Q	Output	BOOL	I, Q, M, D, L	Signal state of the operand

Example

The following example shows how the instruction works:



The operands "TagSR" and "TagOut" are set when the following conditions are fulfilled:

- The operand "TagIn_1" has the signal state "1".
- The operand "TagIn_2" has the signal state "0".

The operands "TagSR" and "TagOut" are reset when one of the following conditions is fulfilled:

- The operand "TagIn_1" has signal state "0" and the operand "TagIn_2" has signal state "1".
- The operands "TagIn_1" and "TagIn_2" have signal state "1".

See also

Overview of the valid data types
Address areas of the CPUs

Master control relay
---(MCR<): Open MCR ranges
Basic information on LAD
Memory areas