FEATURES
300 MHz internal clock rate
FSK, BPSK, PSK, chirp, AM operation
Dual integrated 12-bit digital-to-analog converters (DACs)
Ultrahigh speed comparator, 3 ps rms jitter
Excellent dynamic performance
80 dB SFDR at 100 MHz (±1 MHz) AOUT
4× to 20× programmable reference clock multiplier
Dual 48-bit programmable frequency registers
Dual 14-bit programmable phase offset registers
12-bit programmable amplitude modulation and
on/off output shaped keying function
Single-pin FSK and BPSK data interfaces
PSK capability via input/output interface
Linear or nonlinear FM chirp functions with single-pin
frequency hold function
Frequency-ramped FSK
<25 ps rms total jitter in clock generator mode

特征
300 MHz 内部时钟速率
支持 FSK, BPSK, PSK, chirp, AM 调制
集成双路 12 位数/模转换器（DAC）
超高速比较器，3 个 PS RMS 抖动
出色的动态性能
80dB 的 SFDR 在 100 MHz（± 1 MHz）的 AOUT
4 ×20×可编程参考时钟倍频器
双 48 位可编程频率寄存器
双通道，14 位可编程相位偏移寄存器
12 位可编程振幅调制
ON / OFF 输出形键控功能
单引脚 FSK 和 BPSK 的数据接口
通过输入/输出接口实现 PSK 功能
单线实现线性或非线性的调频功能
频率暂停功能
频率 ramped 的 FSK
<25 ps 的均方根时钟发生器模式的总抖动

Automatic bidirectional frequency sweeping
Sin(x)/x correction
Simplified control interfaces
10 MHz serial 2- or 3-wire SPI compatible
100 MHz parallel 8-bit programming
3.3 V single supply
Multiple power-down functions
Single-ended or differential input reference clock

Small, 80-lead LQFP or TQFP with exposed pad
APPLICATIONS
Agile, quadrature LO frequency synthesis
Programmable clock generators
FM chirp source for radar and scanning systems
Test and measurement equipment
Commercial and amateur RF exciters
双向自动扫频
sin（x）/ x 修正
简化的控制接口
兼容 10 MHz 串行 2　或 3 线 SPI 总线
100 兆赫并行 8 位总线
3.3 V 单电源供电
多重省电功能
参考时钟可单端或差分输入
小型，80 引脚 LQFP 或带有散热焊盘的 TQFP 封装

应用
正交 LO 频率合成
可编程时钟发生器
调频雷达和扫描系统的线性调频源
测试与测量设备
商业及业余射频发射器

目录

GENERAL DESCRIPTION

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high speed, high performance quadrature DACs to form a digitally programmable I and Q synthesizer function. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase, amplitude-programmable sine and cosine outputs that can be used as an agile LO in communications, radar, and many other applications. The innovative high speed DDS core of the AD9854 provides 48-bit frequency resolution (1 μHz tuning resolution with 300 MHz SYSCLK). Maintaining 17 bits ensures excellent SFDR.

概述

在 AD9854 数字频率合成器是一种高度集成的器件，采用先进的 DDS 技术，具有两个内部耦合高速，高性能正交数模转换器以实现数字可编程的 I/Q 合成功能。使用精确的时钟参考源，AD9854 生成高度稳定，频率相位、幅度可编程的正弦和余弦信号，可作为通信，雷达以及许多其他应用中的可变本振输。新型的高速 AD9854 高速 DDS 内核可提供 48 位频率分辨率（300 MHz 的系统时钟 1 μ Hz 调谐分辨率）。保持 17 位，确保优秀的 SFDR。

The circuit architecture of the AD9854 allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The sine wave output (externally filtered) can be converted to a square wave by the internal comparator for agile clock generator applications.

The device provides two 14-bit phase registers and a single pin for BPSK operation.

AD9854 电路结构允许输出高达 150 兆赫的正交频率信号，同时可支持每秒 1 亿次品率更新。正弦波输出（外部过滤）可以经由片内比较器转换为方波信号，以用作时钟发生器。该器件提供两个 14 位相位寄存器和一个 BPSK 操作引脚。

For higher-order PSK operation, the I/O interface can be used for phase changes. The 12-bit I and Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrow-band output SFDR. The Q DAC can also be configured as a user-programmable control DAC if the quadrature function is not desired. When configured with the comparator, the 12-bit control DAC facilitates static duty cycle control in high speed clock generator applications.

对于高阶 PSK 应用，I / O 接口可用于相位控制。 12 位 I 和 Q 数模转换器，与新结构的 DDS 结合，提供良好的宽带或窄带输出的 SFDR。如果不需要正交树出，DAC 的 Q 路也可以配置为一个用户可编程控制 DAC。当与比较器配合用作高速时钟发生器时，12 位控制 DAC 有利于稳定占空比。

Two 12-bit digital multipliers permit programmable amplitude modulation, on/off output shaped keying, and precise amplitude control of the quadrature output. Chirp functionality is also included to facilitate wide bandwidth frequency sweeping applications. The programmable 4× to 20× REFCLK multiplier circuit of the AD9854 internally generates the 300 MHz system clock from an external lower frequency reference clock. This saves the user the expense and difficulty of implementing a 300 MHz system clock source.

两个 12 位可编程数字乘法器允许调幅，ON / OFF 输出形键控和正交输出的精确幅度控制。啁啾的功能还适用于宽带扫频应用。AD9854 内部的可编程 4 至 20 倍的 REFCLK 倍频电路可以从较低频率的外部参考时钟频率方便地产生 300 MHz 的系统时钟。这样可以节省用户的费用，降低采用 300 MHz 系统时钟源的困难。

Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of ramped FSK are supported. The AD9854 uses advanced 0.35 μm CMOS technology to provide a high level of functionality on a single 3.3 V supply.

The AD9854 is pin-for-pin compatible with the AD9852 single-tone synthesizer. It is specified to operate over the extended industrial temperature range of −40°C to +85°C.

单端或差分输入的 300 MHz 时钟也是允许的。支持常规单引脚 FSK 和增强谱 FSK。AD9854 采用先进的 0.35 微米 CMOS 技术，可在 3.3 V 单电源下提供高性能的功能。

AD9854 与 AD9852 引脚对引脚地兼容。它可以在-40 ° C 至+85 ° C 工业温度范围内工作。

第 8 页

To determine the junction temperature on the application PCB use the following equation:

TJ = Tcase + (ΨJT × PD)

where:

TJ is the junction temperature expressed in degrees Celsius.

Tcase is the case temperature expressed in degrees Celsius, as measured by the user at the top center of the package.

ΨJT = 0.3°C/W.

PD is the power dissipation (PD); see the Power Dissipation and Thermal Considerations section for the method to calculate PD.

要确定 PCB 上应用中的器件的结温使用下列公式：

TJ = Tcase + (ΨJT × PD)

其中：

TJ 是结温的摄氏度表示。

Tcase 是外壳温度的摄氏度表示，由用户在封装的顶部的中心位置测量。

ΨJT = 0.3°C/W.

PD 是散热焊盘;见功耗计算方法和 PD 的散热设计部分。

ESD 警告

ESD(静电放电)敏感器件

带电器件和电路板可能会在没有觉察的情况下放电。尽管本产品具有专利或专用的保护电路，但在遇到高能量的 ESD 时，器件可能会损坏。因此，应当采用适当的 ESD 防范措施，以避免器件性能下降或功能丧失。

THEORY OF OPERATION

The AD9854 quadrature output digital synthesizer is a highly flexible device that addresses a wide range of applications. The

device consists of an NCO with a 48-bit phase accumulator, a programmable reference clock multiplier, inverse sinc filters, digital multipliers, two 12-bit/300 MHz DACs, a high speed analog comparator, and interface logic. This highly integrated device can be configured to serve as a synthesized LO, an agile clock generator, or an FSK/BPSK modulator.

Analog Devices, Inc., provides a technical tutorial about the operational theory of the functional blocks of the device. The tutorial includes a technical description of the signal flow through a DDS device and provides basic applications information for a variety of digital synthesis implementations. The document, A Technical Tutorial on Digital Signal Synthesis, is available from the DDS Technical Library, on the Analog Devices DDS website at www.analog.com/dds.

操作原理

正交输出的 AD9854 数字频率合成器是一个高度灵活的设备，应用广泛。该装置由一个 48 位相位累加器，一个可编程参考时钟倍频器，反 SINC 滤波器，数字乘法器，两个 12-bit/300 MHz 的 DAC，1 个高速模拟比较器和接口逻辑构成。这种高度集成的器件可以配置集成本地震荡器，捷变频的时钟发生器或者 FSK/ BPSK 的调制器。

ADI 公司提供了有关该设备的功能说明和使用教程。本教程包括对 DDS 的设备信号流程的技术说明，并提供了数字频率合成器实现各种基本应用的信息。该数字信号合成技术指导，可从 DDS 的技术资料库，在 ADI 公司的的网站 www.analog.com/dds.下载

MODES OF OPERATION

The AD9854 has five programmable operational modes. To select a mode, three bits in the control register (parallel Address 1F hex) must be programmed, as described in Table 5.

操作模式

AD9854 有五个可编程的运作模式。要选择某一模式，三个控制寄存器（并行地址为十六进制 1F）位必须进行编程，如表 5 所示。

Table 5. Mode Selection Table

Mode 2	Mode 1	Mode 0	Result
0	0	0	Single tone
0	0	1	FSK
0	1	0	Ramped FSK
0	1	1	Chirp
1	0	0	BPSK

In each mode, some functions may be prohibited. Table 6 lists the functions and their availability for each mode.

每种模式，某些功能可能被禁止。表 6 列出了每种模式下可用的功能。

Table 6. Functions Available for Modes

	Mode				
Function	Single Tone	FSK	Ramped FSK	Chirp	BPSK
Phase Adjust 1	•	•	•	•	•
Phase Adjust 2					•
Single-Pin FSK/BPSK or HOLD		•	•	•	•
Single-Pin Shaped Keying	•	•	•	•	•
Phase Offset or Modulation	•	•	•	•	
Amplitude Control or Modulation	•	•	•	•	•
Inverse Sinc Filter	•	•	•	•	•
Frequency Tuning Word 1	•	•	•	•	•
Frequency Tuning Word 2		•	•		
Automatic Frequency Sweep			•	•	

Single Tone (Mode 000)

This is the default mode when the MASTER RESET pin is asserted. It can also be accessed if the user programs this mode into the control register. The phase accumulator, responsible for generating an output frequency, is presented with a 48-bit value from the Frequency Tuning Word 1 registers that have default values of 0. Default values from the remaining applicable registers further define the single-tone output signal qualities.

The default values after a master reset configure the device with an output signal of 0 Hz and zero phase. At power-up and reset, the output from the I and Q DACs is a dc value equal to the midscale output current. This is the default mode amplitude setting of 0. See the On/Off Output Shaped Keying (OSK) section for more details about the output amplitude control. All or some of the 28 program registers must be programmed to produce a user-defined output signal.

Figure 35 shows the transition from the default condition (0 Hz) to a user-defined output frequency (F1).

单音（模式 000）

这是主复位引脚有效后的默认模式。它也可由用户程序通过控制寄存器来设置。相位累加器所产生输出频率，由频率控制字 1 寄存器中默认值为 0 的 48 位设置。剩余的频率控制字 1 寄存器进一步明确单音输出信号质量，这些位默认值是 0。

主复位后的默认信号输出值设定为 0 赫兹和零相位。在上电和复位，从 I 和 Q 路 DAC 的输出是直流，其值等于量程输出电流。这是默认模式幅度设置为 0。请参阅振荡键控调制关于输出幅度控制更详细的部分。为了产生用户所需的信号频率，需要对全部或部分的 28 个寄存器进行编程。

图 35 显示了从默认设置（0 Hz）到用户定义的输出频率（F1）的过渡。

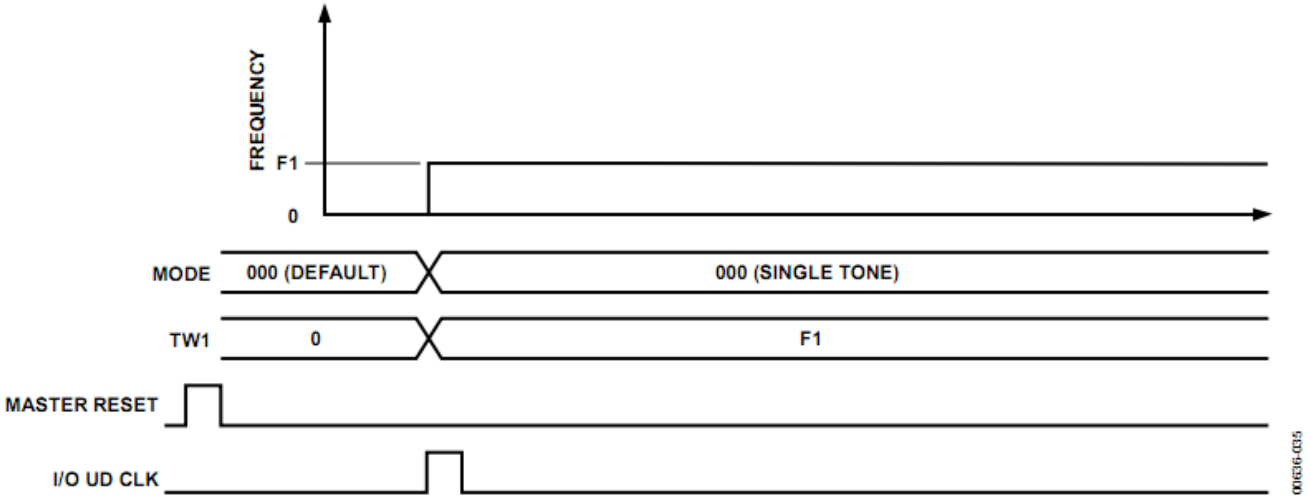


Figure 35. Default State to User-Defined Output Transition

As with all Analog Devices DDS devices, the value of the frequency tuning word is determined by

和 ADI 公司所有 DDS 器件一样，频率控制字值由下式决定:

$$FTW = (Desired\ Output\ Frequency \times 2^N)/SYSCLK$$

where:

N is the phase accumulator resolution (48 bits in this instance).

Desired Output Frequency is expressed in hertz.

FTW (frequency tuning word) is a decimal number.

其中：

N 为相位累加器的分辨率（在此处为 48 位）。

所需的输出频率单位为赫兹。

FTW（频率调谐字）是一个小数。

After a decimal number has been calculated, it must be rounded to an integer and then converted to binary format, that is, a series of 48 binary-weighted 1s and 0s. The fundamental sine wave DAC output frequency range is from dc to one-half SYSCLK.

Changes in frequency are phase continuous, meaning that the first sampled phase value of the new frequency is referenced from the time of the last sampled phase value of the previous frequency.

The I and Q DACs of the AD9854 are always 90° out of phase. The 14-bit phase registers do not independently adjust the phase of each DAC output. Instead, both DACs are affected equally by a change in phase offset.

经过一个十进制数进行了计算，必须四舍五入为整数，然后转换为二进制格式，也就是 48 个二进制加权的 1 和 0。基

本的正弦波 DAC 输出频率范围从 DC 到二分之一的系统时钟 SYSCLK。

在频率变化是相位连续的，既是说新的频率相位值参考从先前的最后一次采样频率的相位值。

I 和 Q 的 AD9854 DAC 的总是 90 ° 的相位差。 14 位相位寄存器不独立调节每个 DAC 输出相位。相反，两个 DAC 是同样受到了相同偏置的影响。

The single-tone mode allows the user to control the following signal qualities:

- Output frequency to 48-bit accuracy
- Output amplitude to 12-bit accuracy
- Fixed, user-defined amplitude control
- Variable, programmable amplitude control
- Automatic, programmable, single-pin-controlled on/off output shaped keying
- Output phase to 14-bit accuracy

These qualities can be changed or modulated via the 8-bit parallel programming port at a 100 MHz parallel byte rate or at a 10 MHz serial rate. Incorporating this attribute permits FM, AM, PM, FSK, PSK, and ASK operation in single-tone mode.

单音频模式允许用户控制以下信号特征：

•输出频率为 48 位精度

•输出幅度为 12 位精度

•固定，用户定义的幅度控制

•可变，可编程振幅控制

•自动，可编程，单引脚控制开/关输出形键控

•输出相位，以 14 位精度

这些参数可以通过 100 MHz 并行字节率 的 8 位并行总线或在 10 MHz 串行速率的串行总线设置。此外,这一特性使单频模式支持 FM, AM, PM, FSK, PSK 和 ASK 等多种调制方式.

Unramped FSK (Mode 001)

When the unramped FSK mode is selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word Register 1 and Frequency Tuning Word Register 2 and the logic level of Pin 29 (FSK/BPSK/HOLD). A logic low on Pin 29 chooses F1 (Frequency Tuning Word 1, Parallel Address 4 hex to Parallel Address 9 hex), and a logic high chooses F2 (Frequency Tuning Word 2, Parallel Register Address A hex to Parallel Register Address F hex). Changes in frequency are phase continuous and are internally coincident with the FSK data pin (Pin 29); however, there is deterministic pipeline delay between the FSK data signal and the DAC output. (Refer to the pipeline delays in Table 1.)

The unramped FSK mode, shown in Figure 36, represents traditional FSK, radio teletype (RTTY), or teletype (TTY) transmission of digital data. FSK is a very reliable means of digital communication; however, it makes inefficient use of the bandwidth in the RF spectrum. Ramped FSK, shown in Figure 37, is a method of conserving bandwidth.

unramped FSK（模式 001）

当 unramped FSK 模式时，DDS 的输出频率是频率调谐字寄存器 1、频率调谐字寄存器 2 和引脚 29（FSK/BPSK/HOLD）逻辑电平的函数。引脚 29 的逻辑低电平选择频率 F1（频率调谐字 1，十六进制并行地址 4 到 9），逻辑高电平选择频率 F2（频率调谐字 2，十六进制并行地址 A 到 F）。输出频率变化时相位是连续的，并在内部与 FSK 数据引脚（引脚 29）一致，但是， FSK 数据信号与 DAC 输出之间存在确定性的流水线延迟。（请参考表 1 中的流水线延迟。）

该 unramped FSK 模式，如图 36 所示，代表传统的 FSK，无线电电传印字机（RTTY）或电传（TTY 的）的数字数据传输。数字通信的 FSK 是一个非常可靠的手段，但是，它的频带利用率不高。 Ramped 的 FSK，如图 37 所示，是一个节约带宽的方法。

Ramped FSK (Mode 010)

This mode is a method of FSK whereby changes from F1 to F2 are not instantaneous, but are accomplished in a frequency sweep or ramped fashion (the ramped notation implies that the sweep is linear). Although linear sweeping, or frequency ramping, is easily and automatically accomplished, it is only one of many schemes. Other frequency transition schemes can be implemented by changing the ramp rate and ramp step size on the fly in a piecewise fashion.

Ramped 的 FSK（模式 010）

此模式是一种 FSK 的方法，即从 F1 到 F2 变化不是瞬间，而是在频率扫描或 ramped 方式完成（即 ramped 符号意味着扫描是线性的）。虽然线性扫频，或频率斜坡，很容易和自动完成，它只是众多方案之一。其他频率的扫频，可以通过改变扫频速率和扫频步长实现。

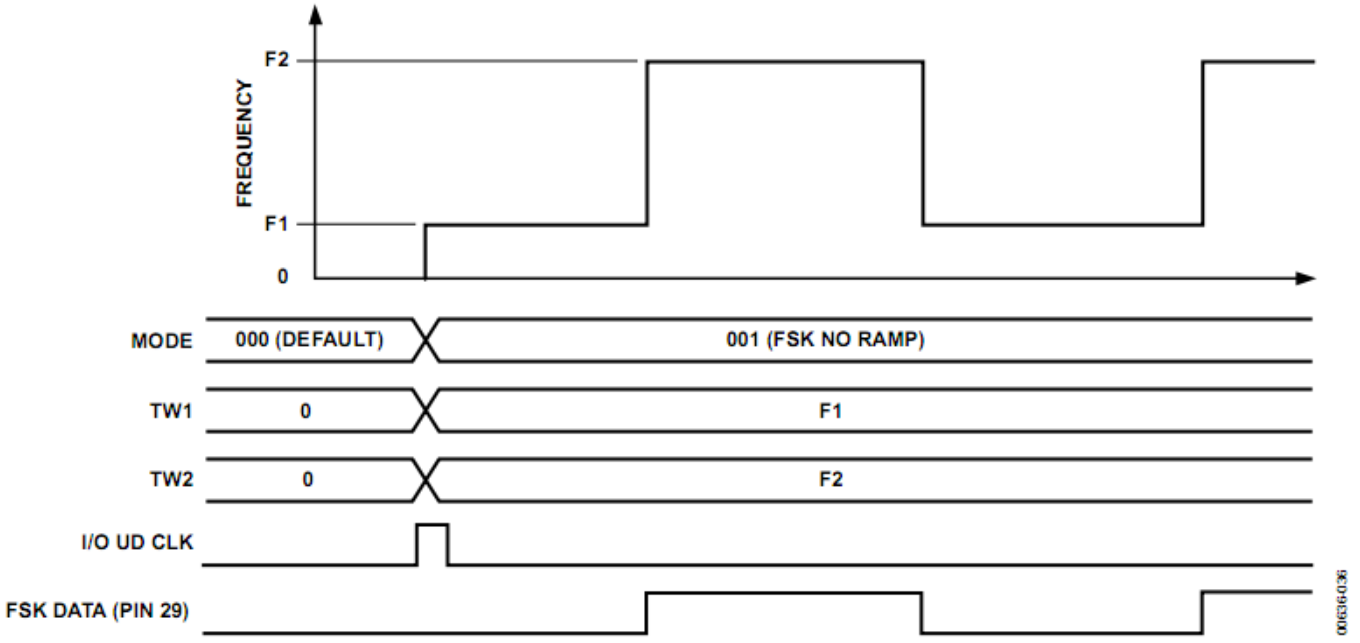


Figure 36. Unramped (Traditional) FSK Mode

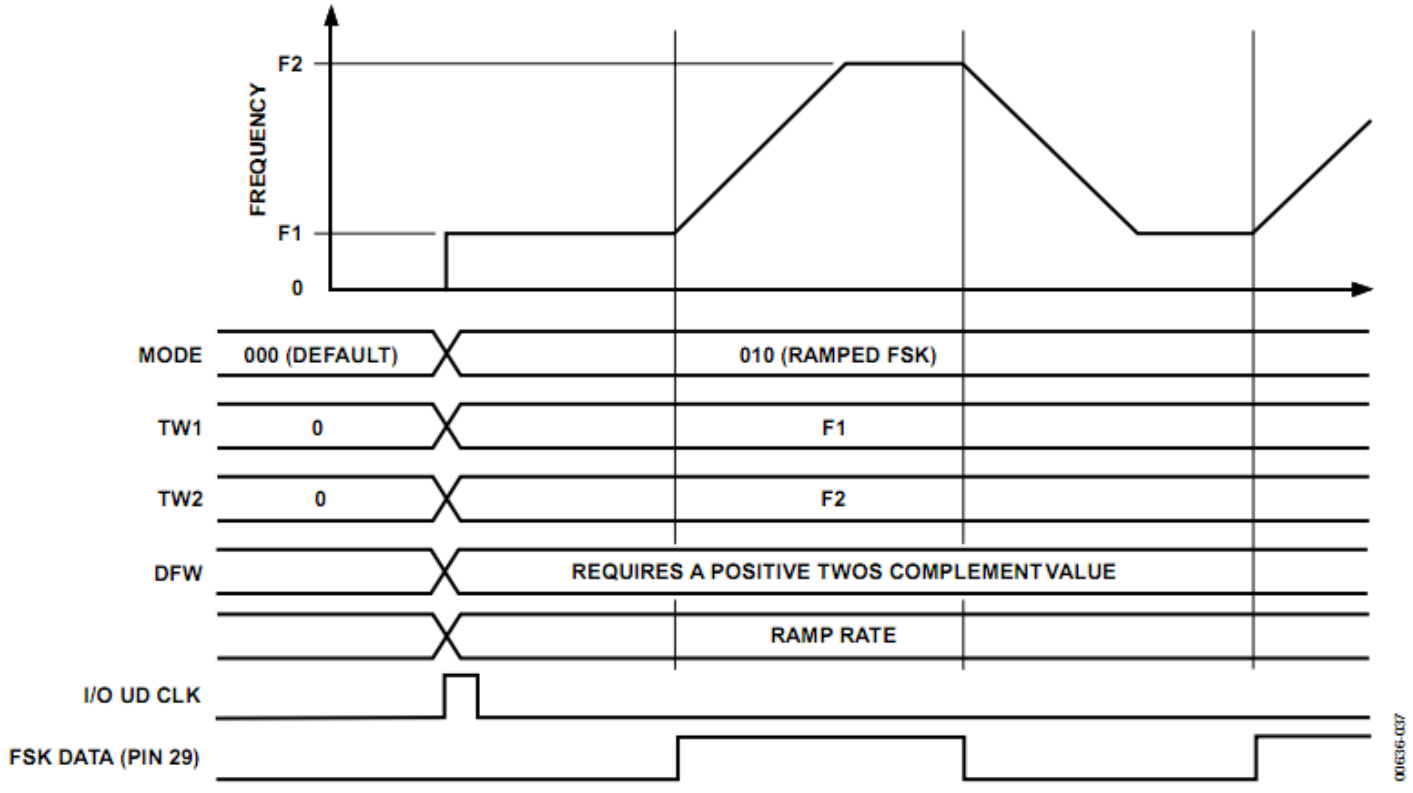


Figure 37. Ramped FSK Mode (Start at F1)

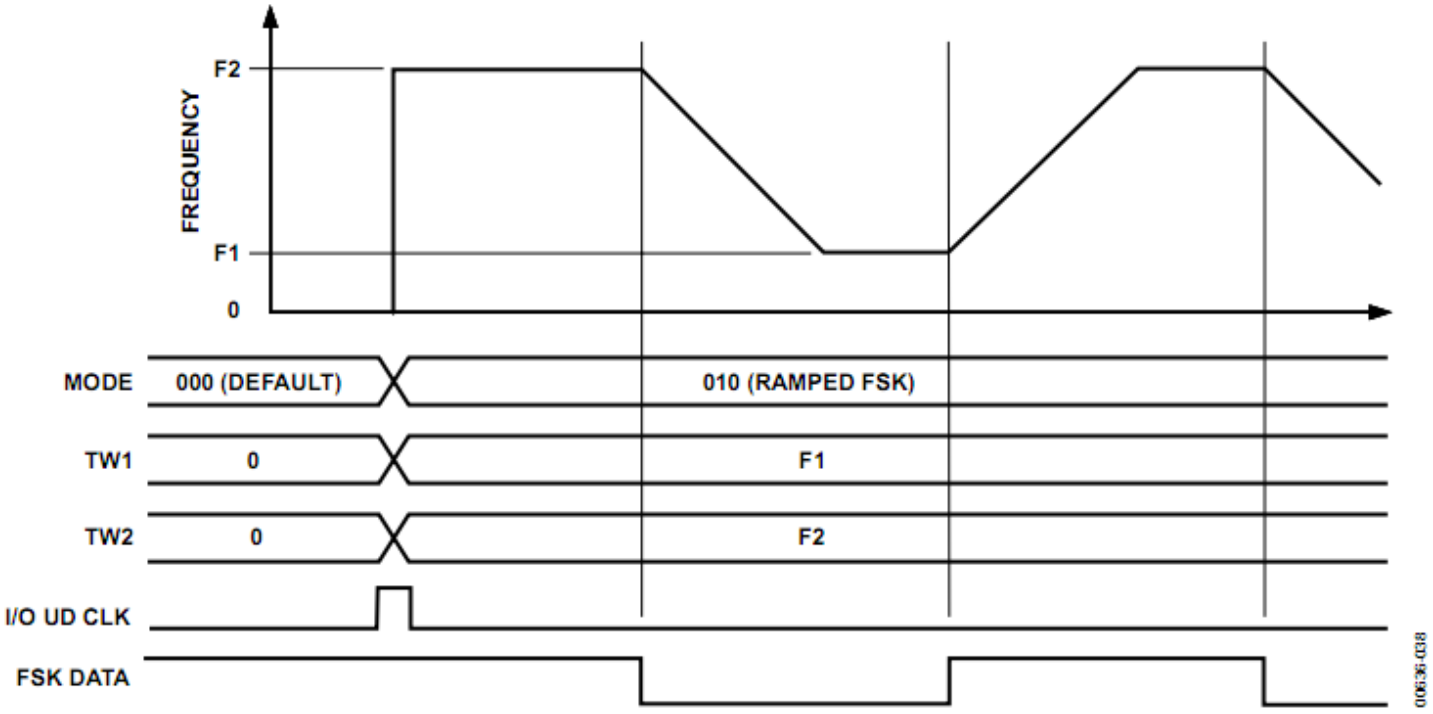


Figure 38. Ramped FSK Mode (Start at F2)

Frequency ramping, whether linear or nonlinear, necessitates that many intermediate frequencies between F1 and F2 are output in addition to the primary F1 and F2 frequencies. Figure 37 and Figure 38 depict the frequency vs. time characteristics of a linear ramped FSK signal.

频率扫描，无论是线性或非线性，必须是从 F1 到 F2 除了 F1 和 F2 的中间频率主频率输出。图 37 和图 38 描述了线性 ramped FSK 信号的频率随时间变化的特点。

Note that in ramped FSK mode, the delta frequency word (DFW) is required to be programmed as a positive twos complement value. Another requirement is that the lowest frequency (F1) be programmed in the Frequency Tuning Word 1 register.

请注意，在 ramped FSK 模式，频率变化字（DFW 的）必须被编程为一个正的补码值。另一个要求是最低的频率（F1）写入到频率调谐字 1 寄存器。

The purpose of ramped FSK is to provide better bandwidth containment than traditional FSK by replacing the instantaneous frequency changes with more gradual, user-defined frequency changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of inter-mediate frequencies, and the time spent at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency to be loaded into F2 registers.

该 ramped FSK 的目的是利用逐步取代、用户定义的频率变化替代瞬时频率变化，以提供更好的带宽控制。在 F1 和 F2 的停留时间可等于或远大于在每个中间频率所花费的时间。用户控制在 F1 和 F2 的驻留时间，中间频率数量，并在每个中间频率上的驻留时间。不像 unramped FSK，ramped FSK 要求最低频率加载到 F1 寄存器，最高频率加载到 F2 寄存器。

Several registers must be programmed to instruct the DDS on the resolution of intermediate frequency steps (48 bits) and the time spent at each step (20 bits). Furthermore, the CLR ACC1 bit in the control register should be toggled (low-high-low) prior to operation to ensure that the frequency accumulator is starting from an all 0s output condition. For piecewise, nonlinear frequency transitions, it is necessary to reprogram the registers while the frequency transition is in progress to affect the desired response.

为了确定 DDS 中间频率步进值（48 位）的分辨率和每一步驻留时间（20 位），必须对几个寄存器进行编程。此外，在控制寄存器中的 CLR ACC1 位应在操作前切换（低-高-低），以确保频率累加器是从全 0 输出状态开始。对于分段，非线性频率转换，当频率切换有可能影响到相位时，需要重新编程寄存器的频率转移。

Parallel Register Address 1A hex to Parallel Register Address 1C hex comprise the 20-bit ramp rate clock registers. This is a countdown counter that outputs a single pulse whenever the count reaches 0. The counter is activated when a logic level change

occurs on the FSK input, Pin 29. This counter is run at the system clock rate, 300 MHz maximum. The time period between each output pulse is given as

(N + 1) × System Clock Period

where N is the 20-bit ramp rate clock value programmed by the user.

并行寄存器地址 1A 到 1C 构成了 20 位的上升的速度时钟寄存器。这是一个倒数计数器，每当计数达到 0 输出一个脉冲。当 FSK 输入，引脚 29 逻辑电平变化时，计数器被激活。这个计数器运行在系统时钟频率，最大 300 MHz。每个输出脉冲之间的时间可表示为

（N +1）×系统时钟周期

其中，N 为由用户编程的 20 位上升速度时钟值。

The allowable range of N is from 1 to (2^20 − 1). The output of this counter clocks the 48-bit frequency accumulator shown in Figure 39. The ramp rate clock determines the amount of time spent at each intermediate frequency between F1 and F2. The counter stops automatically when the destination frequency is achieved. The dwell time spent at F1 and F2 is determined by the duration that the FSK input, Pin 29, is held high or low after the destination frequency has been reached.

N 的允许范围是从 1 到（2^{20}- 1）。此计数器的输出时钟的 48 位累加器的频率如图 39 所示。扫频速率时钟决定了在 F1 和 F2 之间的每个中间频率的驻留时间。频率达到目的值后计数器自动停止。花费在 F1 或 F2 的驻留时间，决定于 29 脚的 FSK 输入信号，在频率达到目的值后保持高或者低电平的时间。

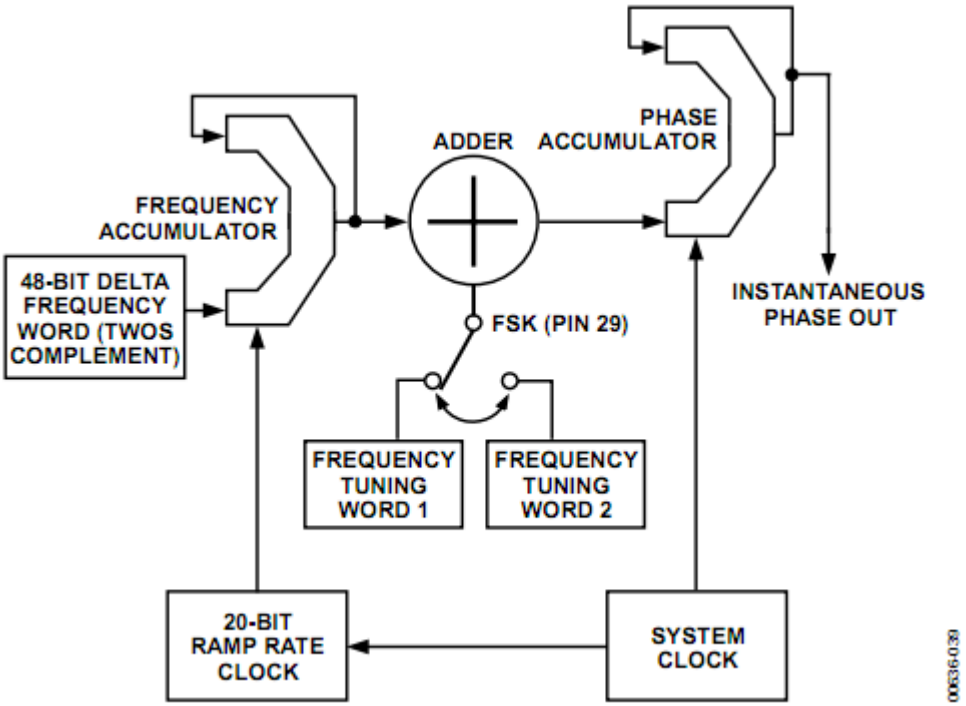


Figure 39. Block Diagram of Ramped FSK Function

Parallel Register Address 10 hex to Parallel Register Address 15 hex comprise the 48-bit, twos complement, delta frequency word registers. This 48-bit word is accumulated (added to the accumulator's output) every time it receives a clock pulse from the ramp rate counter. The output of this accumulator is added to or subtracted from the F1 or F2 frequency word, which is then fed into the input of the 48-bit phase accumulator that forms the numerical phase steps for the sine and cosine wave outputs. In this fashion, the output frequency is ramped up and down in frequency according to the logic state of Pin 29. This ramping rate is a function of the 20-bit ramp rate clock. When the destination frequency is achieved, the ramp rate clock is stopped, halting the frequency accumulation process.

Generally speaking, the delta frequency word is a much smaller value compared with the value of the F1 or F2 tuning word. For example, if F1 and F2 are 1 kHz apart at 13 MHz, the delta frequency word might be only 25 Hz.

并行寄存器地址 10 到 15 包括 48 位二进制补码，频率变化字寄存器。这 48 位字每收到一个从速率计数器输出的时钟脉冲自动累加（添加到累加器的输出）。这个累加器输出被加（或无进位地加）到从 F1 或 F2 频率字，然后将进入构成正弦或余弦数字相位的 48 位相位累加器。在这种方式下，输出频率根据引脚 29 的逻辑状态递增或递减。扫频速率是

20 位扫频速度时钟的函数。当达到目的频率时，扫频速率时钟停止，停止频率积累的过程。

一般来说，频率变化字与 F1 或 F2 调谐字值比较而言是一个较小的值。例如，如果 F1 和 F2 是 13 兆赫上下偏 1 kHz，频率变化字可能只有 25 赫兹。

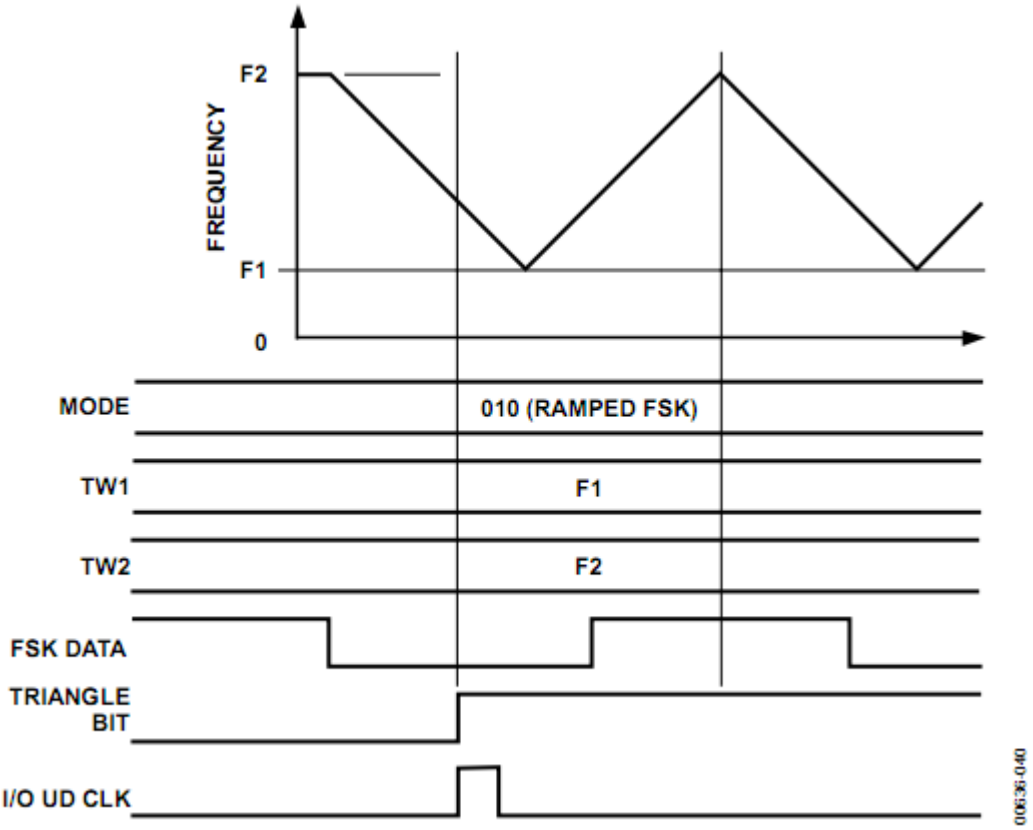


Figure 40. Effect of Triangle Bit in Ramped FSK Mode

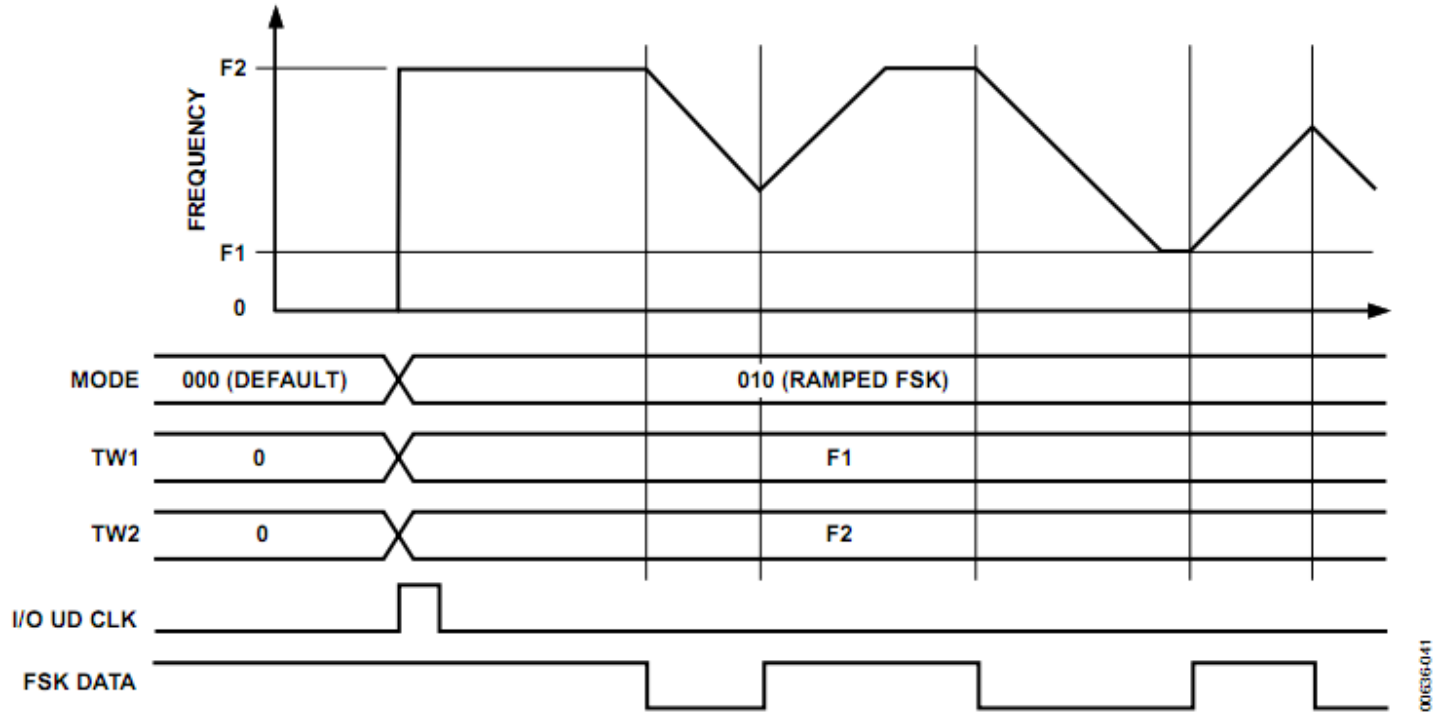


Figure 41. Effect of Premature Ramped FSK Data

Figure 41 shows that premature toggling causes the ramp to immediately reverse itself and proceed at the same rate and resolution until the original frequency is reached.

The control register contains a triangle bit at Parallel Register Address 1F hex. Setting this bit high in Mode 010 causes an automatic ramp-up and ramp-down between F1 and F2 to occur without toggling Pin 29, as shown in Figure 40. The logic state

of Pin 29 has no effect once the triangle bit is set high. This function uses the ramp rate clock time period and the step size of the delta frequency word to form a continuously sweeping linear ramp from F1 to F2 and back to F1 with equal dwell times at every frequency. Use this function to automatically sweep between any two frequencies from dc to Nyquist.

In the ramped FSK mode with the triangle bit set high, an automatic frequency sweep begins at either F1 or F2, according to the logic level on Pin 29 (FSK input pin) when the triangle bit's rising edge occurs (Figure 42). If the FSK data bit is high instead of low, F2, rather than F1, is chosen as the start frequency.

图 41 显示了过早的切换导致扫频方向改变，并以同一扫频速率和分辨率继续，直到返回原始频率。

控制寄存器包含一个并行地址为 1F 的三角形位。在模式 010 中设置此位为高将导致频率自动地在 F1 和 F2 之间上升和下降而不受切换引脚 29 的控制，如图 40 所示。一旦三角位被设置为高，引脚 29 的逻辑状态就不再起作用。这一功能根据扫频速率时钟周期与频率步进值形成一个从 F1 到 F2 再回到 F1 的连续的线性扫频，在这一扫频过程中，在每个中间频率驻留同样的时间。使用此功能可以在从直流到奈奎斯特频率的任何两个频率之间自动扫频。

在 ramped FSK 模式与三角形位设置为高时，当三角形位逻辑电平出现上升沿（图 42），根据引脚 29（FSK 的输入脚）确定自动扫频从 F1 或 F2 开始，。如果 FSK 数据位为高则 F2 为扫频起始频率。

Additional flexibility in the ramped FSK mode is provided by the AD9854's ability to respond to changes in the 48-bit delta frequency word and/or the 20-bit ramp rate counter at any time during the ramping from F1 to F2 or vice versa. To create these nonlinear frequency changes, it is necessary to combine several linear ramps with different slopes in a piecewise fashion. This is done by programming and executing a linear ramp at a rate or slope and then altering the slope (by changing the ramp rate clock or delta frequency word, or both). Changes in slope can be made as often as needed before the destination frequency has been reached to form the desired nonlinear frequency sweep response. These piecewise changes can be precisely timed using the 32-bit internal update clock (see the Internal and External Update Clock section).

ramped FSK 模式中，AD9854 从 F1 到 F2 的扫频过程中可以在任何时间响应 48 位频率步进字的变化和/或 20 位的扫频速度控制字的改变，这提供了更多的灵活性，反之亦然。要产生这些非线性的频率变化，需要分段地结合多个线性的扫频。这可以通过执行线性扫频，然后改变斜率（通过改变扫频时钟速率或步进值，或两者）。在目标频率达到前，可以任意频繁地改变频率上升的斜率，以产生所需的非线性扫频。在坡度变化可为经常目的地之前需要的频率已达到预期的形成非线性扫频响应。这些变化可以使用 32 位内部更新时钟精确地分段（见内部和外部更新时钟部分）。

Nonlinear ramped FSK has the appearance of the chirp function shown in Figure 43. The difference between a ramped FSK function and a chirp function is that FSK is limited to operation between F1 and F2, whereas chirp operation has no F2 limit frequency.

Two additional control bits (CLR ACC1 and CLR ACC2) are available in the ramped FSK mode that allow more options. If CLR ACC1 (Register Address 1F hex) is set high, it clears the 48-bit frequency accumulator (ACC1) output with a retriggerable one-shot pulse of one system clock duration. If the CLR ACC1 bit is left high, a one-shot pulse is delivered on the rising edge of every update clock. The effect is to interrupt the current ramp, reset the frequency to the start point (F1 or F2), and then continue to ramp up (or down) at the previous rate. This occurs even when a static F1 or F2 destination frequency has been achieved.

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to previous DDS operation, CLR ACC2 must be set to logic low.

非线性 ramped FSK 信号频率变化如图 43 所示。 Ramped FSK 与 chirp 功能的不同的是，FSK 的频率变化仅限于 F1 和 F2 之间，而 chirp 功能没有 F2 的频率限制。

在 ramped FSK 模式下有两个额外的控制位（CLR ACC1 和 CLR ACC2）提供更多的选择。如果 CLR ACC1（寄存器地址为 1F）设置为高，在下一个系统时钟的脉冲期间清除 48 位频率累加器（ACC1）的输出。如果 CLR ACC1 位被保持高电平，在每一个更新时钟的上升沿输出一个单脉冲。它的作用是停止当前的扫频，将频率重置到起始频率点（F1 或 F2），然后不断以往的斜率向上扫频（或向下）。这种情况发生在当频率已经达到目的频率并静止即达到 F1 或 F2 频率时。

另外，在 CLR ACC2 控制位（寄存器地址 1F ），可清除频率累加器（ACC1）和相位累加器（ACC2）。当此位被设置为高， DDS 的相位累加器的输出结果保持在 0 赫兹。只要此位设置为高，频率和相位累加器就清零，使输出一直为 0 Hz。要返回到以前的 DDS 操作时，CLR ACC2 必须设置为逻辑低电平。

Chirp (Mode 011)

This mode is also known as pulsed FM. Most chirp systems use a linear FM sweep pattern, but the AD9854 can also support nonlinear patterns. In radar applications, use of chirp or pulsed FM allows operators to significantly reduce the output power needed to achieve the result that a single-frequency radar system would produce. Figure 43 shows a very low resolution nonlinear chirp, demonstrating the different slopes that are created by varying the time steps (ramp rate) and frequency steps (delta frequency word).

线性调频（模式 011）

这种模式也称为脉冲调频。大多数线性调频系统使用线性调频扫描模式，但 AD9854 也可以支持非线性模式。在雷达应用中，使用调频脉冲线性调频或允许使用者大幅降低输出功率，却能达到单频雷达系统产生的效果。图 43 显示了一个非常低的分辨率非线性调频，显示了这是由不同的时间步进（斜率）和频率步进（频率步进字）造成了不同的频率上升斜率。

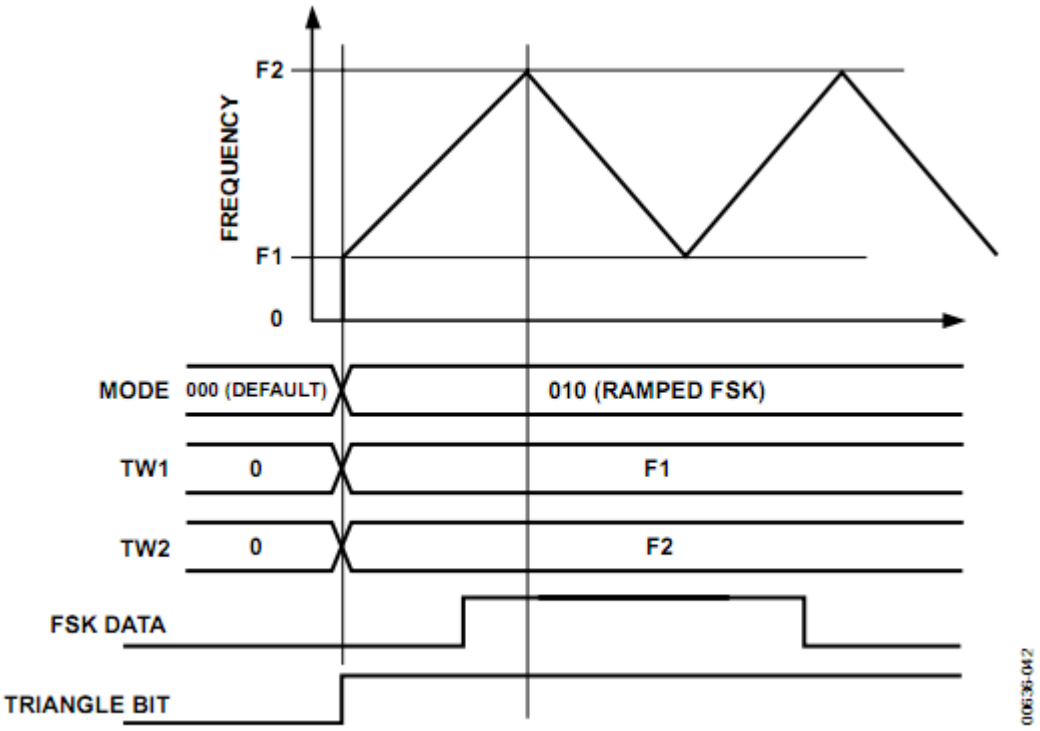


Figure 42. Automatic Linear Ramping Using the Triangle Bit

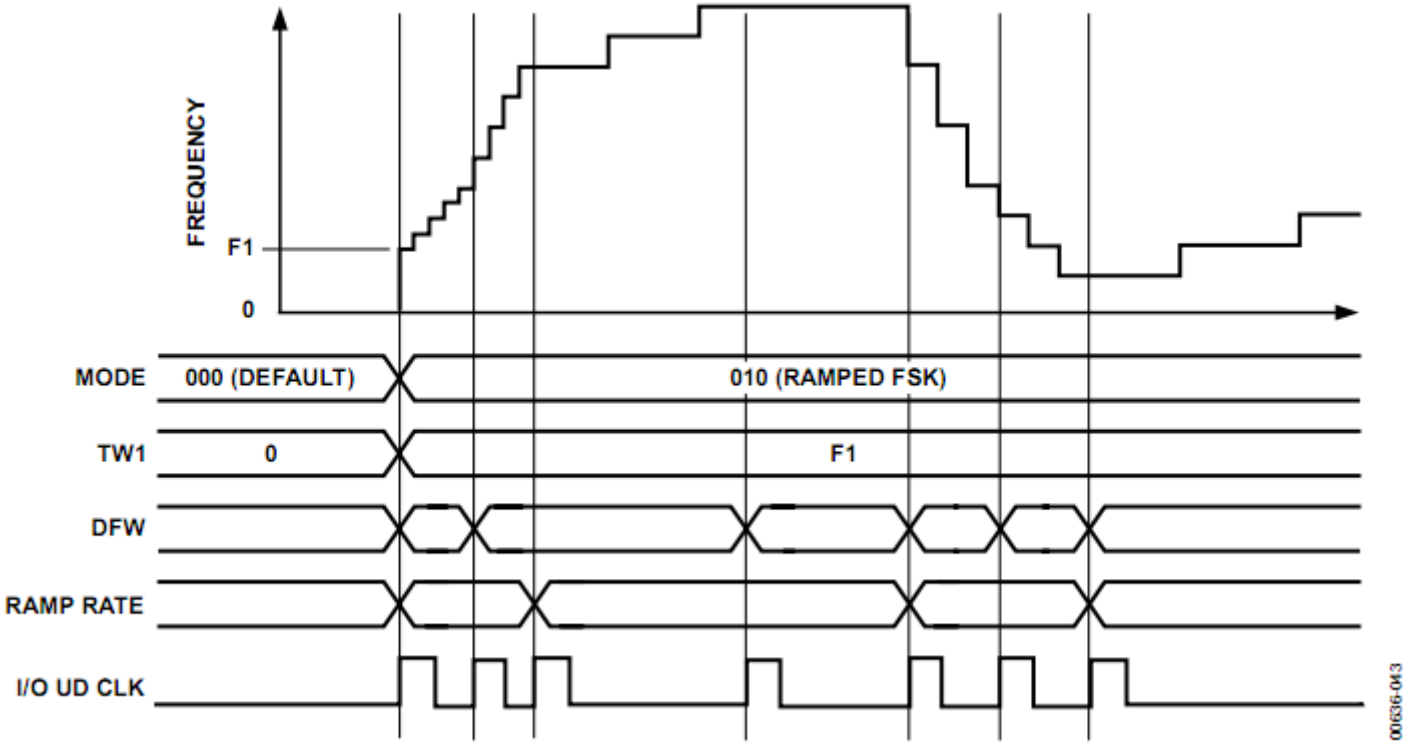


Figure 43. Example of a Nonlinear Chirp

The AD9854 permits precise, internally generated linear, or externally programmed nonlinear, pulsed or continuous FM over the complete frequency range, duration, frequency resolution, and sweep direction(s). All of these are user programmable. Figure 44 shows a block diagram of the FM chirp components.

AD9854 允许在完整的频率范围，内部产生或外部编程产生精确的，线性或非线性的，持续时间、频率分辨率和扫描方向（s）可控得，脉冲或连续调频。所有这些都是用户可编程的。图 44 显示了线性调频组件框图。

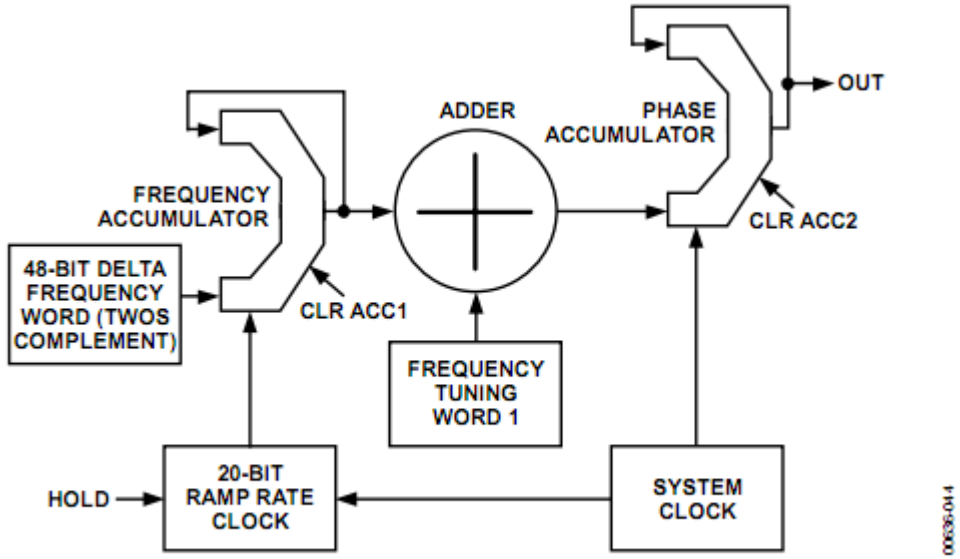


Figure 44. FM Chirp Components

Basic FM Chirp Programming Steps

1. Program a start frequency into Frequency Tuning Word 1 (FTW1) at Parallel Register Address 4 hex to Parallel Register Address 9 hex.
2. Program the frequency step resolution into the 48-bit, twos complement delta frequency word (Parallel Register Address 10 hex to Parallel Register Address 15 hex).
3. Program the rate of change (time at each frequency) into the 20-bit ramp rate clock (Parallel Register Address 1A hex to Parallel Register Address 1C hex).

When programming is complete, an I/O update pulse at Pin 20 engages the program commands.

The necessity for a twos complement delta frequency word is to define the direction in which the FM chirp moves. If the 48-bit delta frequency word is negative (MSB is high), the incremental frequency changes are in a negative direction from FTW1. If the 48-bit word is positive (MSB is low), the incremental frequency changes are in a positive direction from FTW1.

It is important to note that FTW1 is only a starting point for FM chirp. There is no built-in restraint requiring a return to FTW1. Once the FM chirp begins, it is free to move (under program control) within the Nyquist bandwidth (dc to one-half the system clock). However, instant return to FTW1 can be easily achieved.

基本线性调频编程步骤

1。编程将起始频率写入并行寄存器地址为 4 到 9 的频率调谐字 1（FTW1）。

2。编程将频率步进分辨率进写入 48 位二进制补码形式的频率步进字节，（并行寄存器地址 10 到 15）。

3。编程将频率变化率(每个频率的驻留时间)写入 20 位的扫频速率时钟（并行寄存器地址 1A 到 1C）。

当编程完成后，引脚 20 输入一个 I/ O 更新脉冲在使能编程命令。

频率步进字采用有符号补码形式来区分 FM 频率偏移的方向。如果 48 位频率步进字为负（最高位为高），频率的变化是从 FTW1 向负方向增加。如果 48 位字为正（最高位为低），频率增量的变化是从 FTW1 向正的方向。

请注意，FTW1 只是一个线性调频的起点。有没有内置的功能使频率回到 FTW1。一旦开始了 FM 调频，频率可以在（程序的控制下）在奈奎斯特频带范围（DC 到系统时钟的一半）内任意移动。然而，瞬间回 FTW1 也可以轻松实现。

Two control bits (CLR ACC1 and CLR ACC2) are available in the FM chirp mode that allow the return to the beginning frequency, FTW1, or to 0 Hz. When the CLR ACC1 bit (Register Address 1F hex) is set high, the 48-bit frequency accumulator (ACC1) output is cleared with a retriggerable one-shot pulse of one system clock duration. The 48-bit delta frequency word input to the accumulator is unaffected by the CLR ACC1 bit. If the CLR ACC1 bit is held high, a one-shot pulse is delivered to the frequency accumulator (ACC1) on every rising edge of the I/O update clock. The effect is to interrupt the current chirp, reset the frequency to that programmed into FTW1, and continue the chirp at the previously programmed rate and direction. Clearing the output of the frequency accumulator in the chirp mode is illustrated in Figure 45. Shown in the diagram is the I/O update clock, which is either user supplied or internally generated.

两个控制位（CLR ACC1 和 CLR ACC2）可在 FM 调频模式，使频率返回到起始频率，FTW1 或 0 赫兹。当 CLR ACC1 位（寄存器地址 1F）被设置为高，48 位频率累加器（ACC1）输出随着一个持续时间为一个系统时钟周期的重置信号清除。 48 位频率步进字输入到累加器的过程不受 CLR ACC1 位的影响。如果 CLR ACC1 位持续为高，在每一个 I/ O 更新时钟的上升沿，一个单脉冲传递到频率累加器（ACC1）。其效果是中断当前的扫频，复位频率进入编程写入 FTW1 的频率，继续以先前编程的速度和方向扫频。线性调频模式中清除累加器的输出过程如图 45 所示。如图所示是 I/O 更新时钟，这个信号可以由用户提供或由芯片内部产生。

Alternatively, the CLR ACC2 control bit (Register Address 1F hex) is available to clear both the frequency accumulator (ACC1) and the phase accumulator (ACC2). When this bit is set high, the output of the phase accumulator results in 0 Hz output from the DDS. As long as this bit is set high, the frequency and phase accumulators are cleared, resulting in 0 Hz output. To return to the previous DDS operation, CLR ACC2 must be set to logic low. This bit is useful in generating pulsed FM.

Figure 46 illustrates the effect of the CLR ACC2 bit on the DDS output frequency. Note that reprogramming the registers while the CLR ACC2 bit is high allows a new FTW1 frequency and slope to be loaded.

Another function that is available only in chirp mode is the HOLD pin (Pin 29). This function stops the clock signal to the ramp rate counter, halting any further clocking pulses to the frequency accumulator, ACC1. The effect is to halt the chirp at the frequency existing just before the HOLD pin is pulled high. When Pin 29 is returned low, the clock and chirp resumes. During a hold condition, the user can change the programming registers; however, the ramp rate counter must resume operation at its previous rate until a count of 0 is obtained before a new ramp rate count can be loaded. Figure 47 shows the effect of the hold function on the DDS output frequency.

另外，CLR ACC2 控制位（寄存器地址 1F），可清除的频率累加器（ACC1）和相位累加器（ACC2）。当此位被设置为高，则 DDS 相位累加器的输出结果为 0 赫兹。只要此位长期设置为高，频率和相位累加器就一直清零，输出持续为 0 Hz。要返回到以前的 DDS 模式时，CLR ACC2 必须设置为逻辑低电平。该位在产生脉冲调频时相当有用。

图 46 显示了 CLR ACC2 位对 DDS 输出频率影响。请注意，在 CLR ACC2 位为高时重新编程的寄存器，而使得新 FTW1

频率和扫频斜率被加载。

另一个仅在线性调频模式可用的功能是 HOLD 引脚（引脚 29）。此功能停止输入到扫频斜率计数器的时钟信号，停止任何输入到频率累加器 ACC1 的时钟脉冲。其作用是在保持引脚被拉高前,将现有的线性调频暂停在当前频率。当引脚 29 返回低，时钟和线性调频重新开始。在暂停模式下，用户可以更改寄存器值，但是，扫频斜率必须复位到它先前的值,直到计数器计数为 0,新的扫频斜率才可以加载。图 47 显示了暂停功能对 DDS 输出频率的影响。

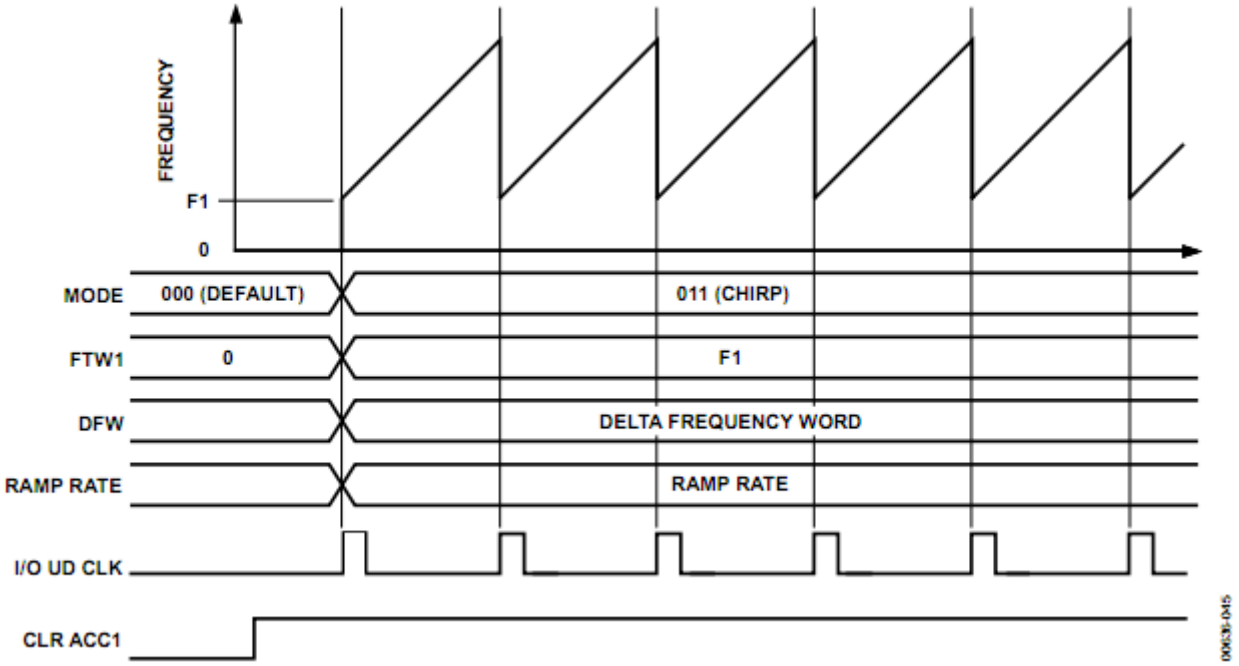


Figure 45. Effect of CLR ACC1 in FM Chirp Mode

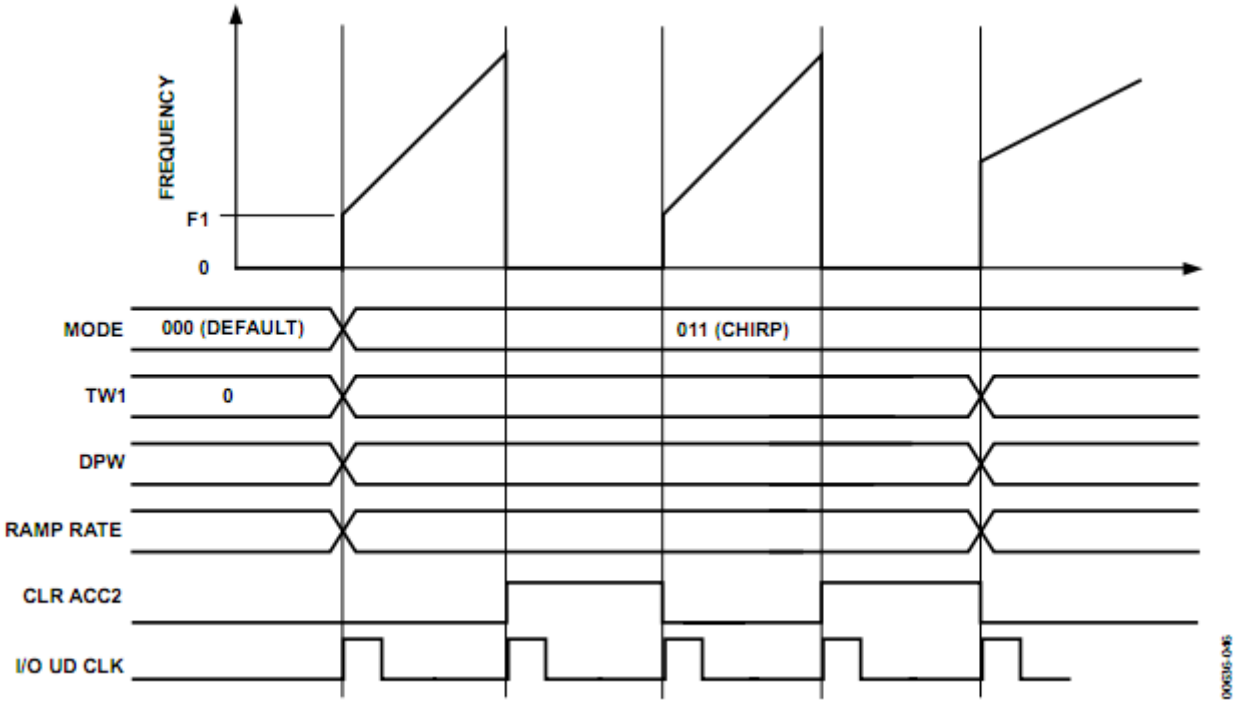


Figure 46. Effect of CLR ACC2 in Chirp Mode

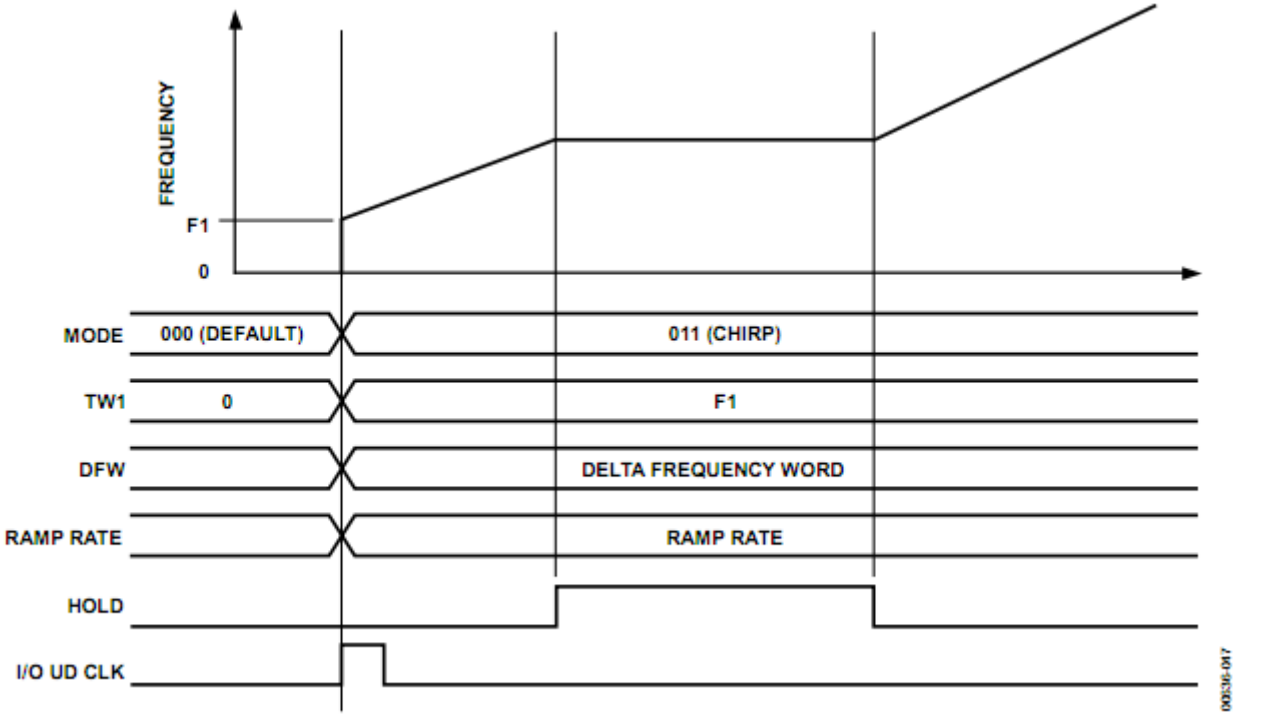


Figure 47. Example of Hold Function

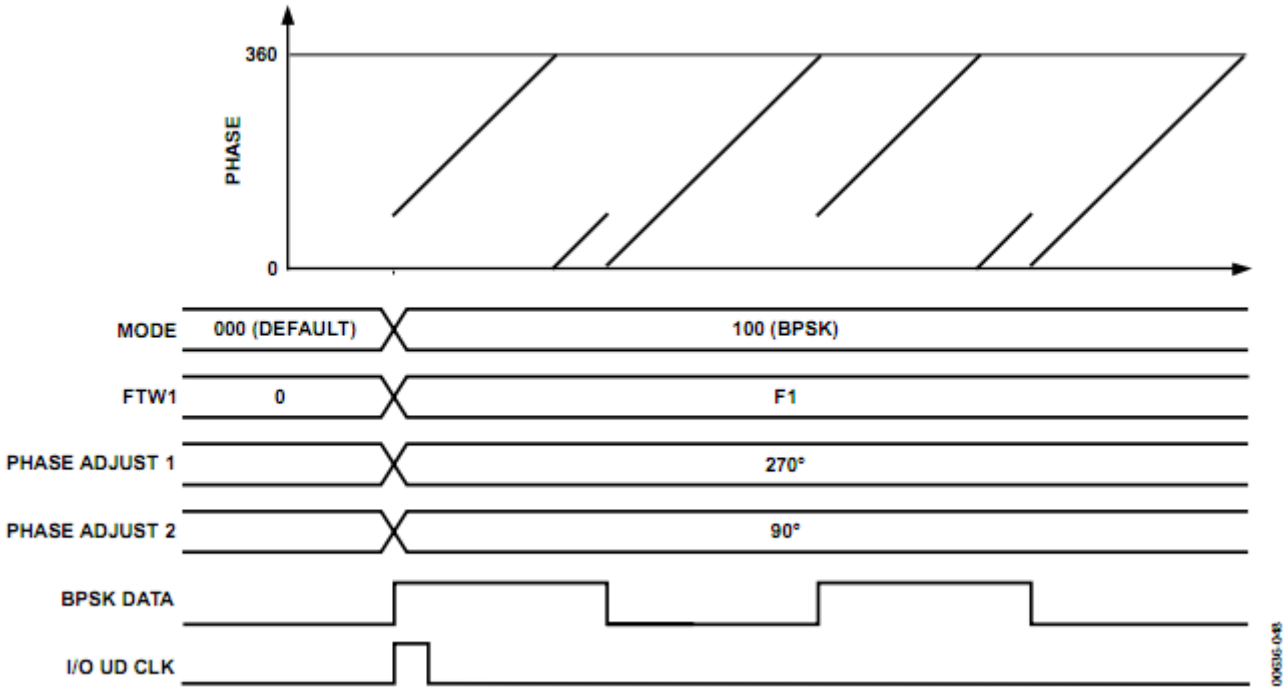


Figure 48. BPSK Mode

The 32-bit automatic I/O update counter can be used to construct complex chirp or ramped FSK sequences. Because this internal counter is synchronized with the AD9854 system clock, precisely timed program changes are possible. For such changes, the user need only reprogram the desired registers before the automatic I/O update clock is generated.

In chirp mode, the destination frequency is not directly specified. If the user fails to control the chirp, the DDS automatically confines itself to the frequency range between dc and Nyquist. Unless terminated by the user, the chirp continues until power is removed.

When the chirp destination frequency is reached, the user can choose any of the following actions:

- Stop at the destination frequency by using the HOLD pin or by loading all 0s into the delta frequency word registers of the frequency accumulator (ACC1).
- Use the HOLD pin function to stop the chirp, and then ramp down the output amplitude by using the digital multiplier stages and the output shaped keying pin (Pin 30), or by using the program register control (Address 21 to Address 24 hex).

- Abruptly end the transmission with the CLR ACC2 bit.
- Continue chirp by reversing direction and returning to the previous or another destination frequency in a linear or user-directed manner. If this involves reducing the frequency, a negative 48-bit delta frequency word (the MSB is set to 1) must be loaded into Register 10 hex to Register 15 hex. Any decreasing frequency step of the delta frequency word requires the MSB to be set to logic high.
- Continue chirp by immediately returning to the beginning frequency (F1) in a sawtooth fashion, and then repeating the previous chirp process using the CLR ACC1 control bit. An automatic, repeating chirp can be set up by using the 32-bit update clock to issue the CLR ACC1 command at precise time intervals. Adjusting the timing intervals or changing the delta frequency word changes the chirp range. It is incumbent upon the user to balance the chirp duration and frequency resolution to achieve the proper frequency range.

32 位自动 I/O 更新计数器可以用来构建复杂的线性调频或 ramped FSK 的序列。由于这种内部计数器是与 AD9854 的系统时钟同步，可以准确地定时改变频率。对于这样的变化，用户只需要在自动 I/ O 更新时钟脉冲产生之前重新编程所需的寄存器即可。

在 Chirp 模式，目标频率不是直接指定。如果用户无法控制线性调频，DDS 自动配置为直流到奈奎斯特频率之间的范围。除非被用户终止，线性调频继续进行，直到电源被切断。

当频率线性调频到达目的频率，用户可以选择以下操作之一：

•使用 HOLD 引脚或加载全 0 到频率累加器（ACC1）寄存器中的频率步进字,使频率停止在目标频率。

•使用保留引脚功能停止线性调频，然后通过数字乘法器和输出键控引脚（引脚 30）减小输出功率，或使用程序寄存器控制输出幅度（地址 21 至 24） 。

•利用 CLR ACC2 位立即结束传输。

•以线性或用户自定的方式向反方向继续扫频,直到回到原始的频率或者另一目的频率。如果这一过程涉及减小频率，一个 48 位补码形式的扫频步进字必须加载到寄存器地址 10 到 15。任何频率步进字降低频率要求 MSB 被设置为逻辑高电平。

•使用 CLR ACC1 控制位，以锯齿方式立即返回到开始频率（F1）继续线性调频，然后重复前面的过程中的线性调频。通过设置 32 位更新时钟，在精确的时间间隔发出 CLR ACC1 命令，可以实现自动，可重复的线性调频。调整的时间间隔或改变频率步进字改变线性调频变化范围。在使用中，用户应该根据需要，平衡频率分辨率及频率驻留时间，以获得合适的频率范围。

BPSK (Mode 100)

Binary, biphase, or bipolar phase shift keying is a means to rapidly select between two preprogrammed 14-bit output phase offsets that equally affect both the I and Q outputs of the AD9854. The logic state of Pin 29, the BPSK pin, controls the selection of Phase Adjust Register 1 or Phase Adjust Register 2. When low, Pin 29 selects Phase Adjust Register 1; when high, it selects Phase Adjust Register 2. Figure 48 illustrates phase changes made to four cycles of an output carrier

Basic BPSK Programming Steps

1. Program a carrier frequency into Frequency Tuning Word 1.
2. Program the appropriate 14-bit phase words into phase Adjust Register 1 and Phase Adjust Register 2.
3. Attach the BPSK data source to Pin 29.
4. Activate the I/O update clock when ready.

Note that for higher-order PSK modulation, the user can select the single-tone mode and program Phase Adjust Register 1 using the serial or high speed parallel programming bus.

BPSK（模式 100）

二进制，两相或双相相移键控是一种手段，迅速选择两种预编程的 14 位相位偏移,输出结果同样的影响 AD9854 的 I 路和 Q 路输出。BPSK 的管脚第 29 针的逻辑状态，控制选择相位调整寄存器 1 相或相位调整寄存器 2。当低，引脚 29 选择相位调整寄存器 1，当高，它会选择相位调整寄存器 2。图 48 说明了四个周期的载波的相位变化。

基本 BPSK 的编程步骤

1。将载波频率编程写入频率控制字 1。

2。将合适的 14 位的相位控制字写入相位调整寄存器 1 及相位调整寄存器 2。

3。将 BPSK 的数据源连接到引脚 29。

4。准备就绪后激活 I/ O 更新时钟。

请注意，对于高阶 PSK 调制，用户可以选择单频模式，利用串行或并行的高速总线编程相位调整寄存器 1 实现。

USING THE AD9854

INTERNAL AND EXTERNAL UPDATE CLOCK

This update clock function is comprised of a bidirectional I/O pin (Pin 20) and a programmable 32-bit down-counter. To program changes that are to be transferred from the I/O buffer registers to the active core of the DDS, a clock signal (low-to-high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit update clock.

When the user provides an external update clock, it is internally synchronized with the system clock to prevent a partial transfer of program register information due to a violation of data setup or hold time. This mode allows the user to completely control when updated program information becomes effective. The default mode for the update clock is internal (the internal update clock control register bit is logic high). To switch to external update clock mode, the internal update clock control register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses at intervals set by the user.

使用本 AD9854

内部和外部更新时钟

此更新时钟功能是由一个双向 I/ O 引脚（引脚 20）和一个可编程的 32 位递减计数器构成。为了将设置从 I / O 缓冲寄存器传送到 DDS 内核，必须从外部引脚 20 输入或由内部 32 位更新生时钟成一个时钟信号（低到高的上升沿）。

当用户提供了一个外部更新时钟，它在内部与系统时钟同步，以防止由于数据建立时间或数据保持时间冲突而造成寄存器部分装载。此模式允许用户完全控制写入信息何时生效。复位后默认的更新时钟设置是内部时钟（内部更新时钟控制寄存器位为逻辑高）。要切换到外部更新时钟模式下，内部更新时钟控制寄存器位必须设置为逻辑低电平。内部更新模式用于以用户设定的时间间隔自动产生周期性的更新脉冲。

An internally generated update clock can be established by programming the 32-bit update clock registers (Address 16 hex to Address 19 hex) and setting the internal update clock control register bit (Address 1F hex) to logic high. The update clock down-counter function operates at half the rate of the system clock (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O update of the DDS output or functions is generated. The update clock is internally and externally routed to Pin 20 to allow users to synchronize the programming of update information with the update clock rate. The time between update pulses is given as

(N + 1)(System Clock Period × 2)

where N is the 32-bit value programmed by the user, and the allowable range of N is from 1 to (232 − 1).

The internally generated update pulse that is output from Pin 20 has a fixed high time of eight system clock cycles.

Programming the update clock register to a value less than five causes the I/O UD CLK pin to remain high. Although the update clock can function in this state, it cannot be used to indicate when data is transferring. This is an effect of the minimum high pulse time when I/O UD CLK functions as an output.

使用内部产生的更新时钟需要编程 32 位更新时钟寄存器（地址 16 到 19）设定，并设置内部更新时钟控制寄存器（地址 1F）为逻辑高。更新时钟可在系统时钟速度的一半（最大值 150 MHz）从 32 位二进制值（由用户编程）向下计数，器和计数下来。当计数达到 0 时，产生一个使 DDS 输出或功能改变的自动的 I/O 更新脉冲。更新时钟是内部连接到 20 针输出，让用户能够同步数据与更新时钟。更新脉冲之间的时间可表示为

（N + 1）（系统时钟周期× 2）

其中，N 为由用户编程的 32 位值，允许的范围是从 1 到（2^{32-1}）。

从引脚 20 输出的内部产生的更新脉冲，固定为 8 个系统时钟周期的高电平。

编程更新时钟寄存器的值小于 5 将导致 I / O 引脚 UD CLK 持续为高电平。虽然更新时钟在这种状态下也能工作，但它不能被用来指示数据传输。这是 UD CLK 功能作为输出时的最小高脉冲时间造成的影响。

ON/OFF OUTPUT SHAPED KEYING (OSK)

The on/off OSK feature allows the user to control the amplitude vs. time slope of the I and Q DAC output signals. This function is used in burst transmissions of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the OSK EN bit (Control Register Address 20 hex) to logic high in the control register. Otherwise, if the OSK EN bit is set low, the digital multipliers responsible for amplitude control are bypassed and the I and Q DAC outputs are set to full-scale amplitude.

In addition to setting the OSK EN bit, a second control bit, OSK INT (also at Address 20 hex), must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multipliers to user-programmable 12-bit registers, allowing users to dynamically shape the amplitude transition in practically any fashion. These 12-bit registers, labeled Output Shape Key I and Output Shape Key Q, are located at Address 21 hex through Address 24 hex, as listed in Table 8. The maximum output amplitude is a function of the RSET resistor and is not programmable when OSK INT is enabled.

ON / OFF 输出形键控（OSK）

开/关振荡键控调制功能允许用户控制 I 和 Q 信号斜率进而控制 DAC 输出幅度。此功能是用于数字数据的猝发式传输，以减少猝发的宽带的数据的影响。用户必须首先将控制寄存器中的 OSK EN 位（控制寄存器地址 20）置为逻辑高，启用数字乘法器。否则，如果 OSK EN 位为低，I 路和 Q 路 DAC 输出绕过用作幅度控制的数字乘法器，设置为满幅度。除了设置 OSK EN 位，第二个控制位，OSK INT 位（也在地址 20），必须设置为逻辑高电平。逻辑高电平选择输出频率上升或频率下降的线性内部控制。OSK INT 位的一个逻辑低的允许用户能够以任何方式动态地控制输出幅度。如表 8 所示，这些 12 位的寄存器，I 路输出波形控制字和 Q 路输出波形控制字，分别位于地址 21 到地址 24。OSK INT 为允许时，最大输出幅度是 RSET 电阻器的函数，而无法编程改变。

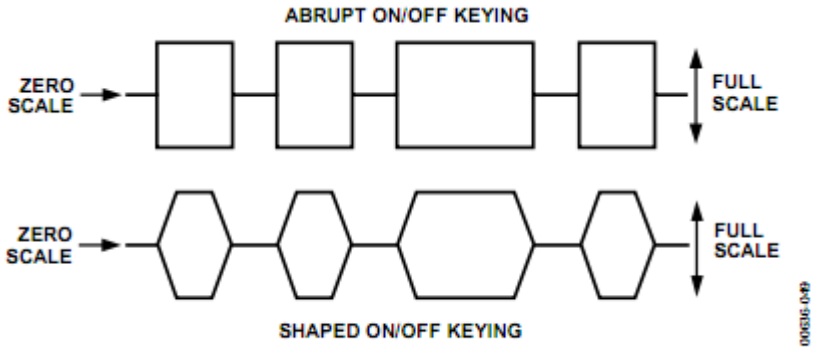


Figure 49. On/Off Output Shaped Keying

The transition time from zero scale to full scale must also be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the program-mable 8-bit ramp rate counter. This is a down-counter that is clocked at the system clock rate (300 MHz maximum) and that generates one pulse whenever the counter reaches 0. This pulse is routed to a 12-bit counter that increments with each pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all 0s at its inputs, the input signal is multiplied by 0, producing zero scale. When the multiplier has a value of all 1s, the input signal is multiplied by a value of 4095 or 4096, producing nearly full scale. There are 4094 remaining fractional multiplier values that produce output amplitudes scaled according to their binary values.

从零到满刻度的的过渡时间也必须进行编程设置。过渡时间是两个固定的元素和一个变量的函数。变量元素是可编程的 8 位斜率计数器。这是一个系统时钟频率（300 MHz 的最大）驱动的减法计数器，当计数器到达 0 时产生一个脉冲。这个脉冲被送入一个 12 位计数器，每个脉冲增加 1。在 12 位计数器的输出连接到 12 位数字乘法器。当数字乘法器输入值为全 0，输入信号乘以 0，产生零输出。当数字乘法器输入值为全 1，输入信号乘以 4095 或 4096 的价值，生产几乎满偏的输出。还有其它 4094 个乘数值，根据自己的二进制值产生相应的输出振幅。

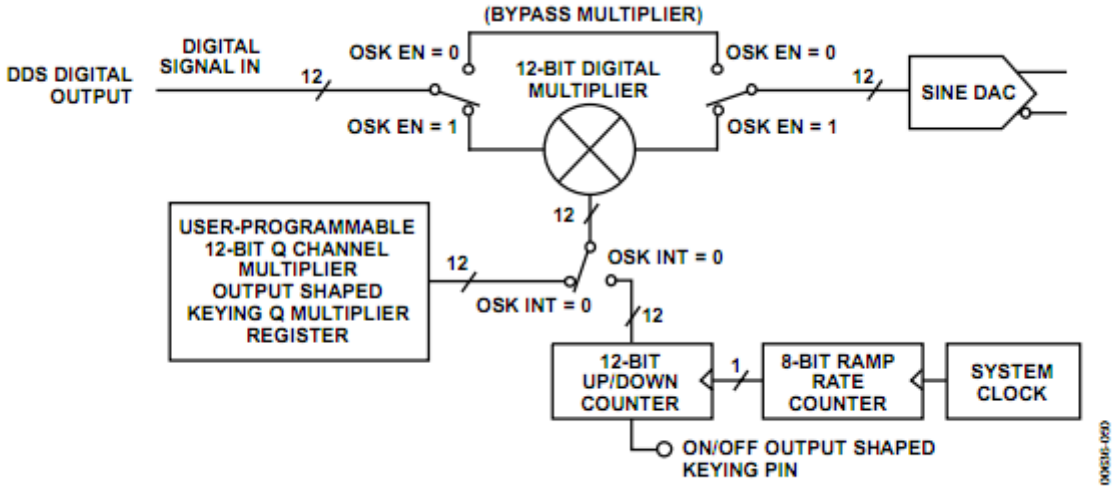


Figure 50. Block Diagram of Q DAC Pathway of the Digital Multiplier Section Responsible for the Output Shaped Keying Function

The two fixed elements of the transition time are the period of the system clock (which drives the ramp rate counter) and the number of amplitude steps (4096). For example, if the system clock of the AD9854 is 100 MHz (10 ns period) and the ramp rate counter is programmed for a minimum count of 3, the transition takes two system clock periods (one rising edge loads the countdown value, and the next edge decrements the counter from 3 to 2). If the countdown value is less than 3, the ramp rate counter stalls and therefore produces a constant scaling value to the digital multipliers. This stall condition may have an application for the user.

The relationship of the 8-bit countdown value to the time between output pulses is given as

(N + 1) × System Clock Period

where N is the 8-bit countdown value.

It takes 4096 of these pulses to advance the 12-bit up-counter from zero scale to full scale. Therefore, the minimum output shaped keying ramp time for a 100 MHz system clock is

4096 × 4 × 10 ns ≈ 164 μs

The maximum ramp time is

4096 × 256 × 10 ns ≈ 10.5 ms

Finally, changing the logic state of Pin 30, output shaped keying automatically performs the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp up to full-scale amplitude and to hold until the logic level is changed to low, causing the outputs to ramp down to zero scale.

过渡时间的两个固定的要素是系统时钟周期（驱动扫频速率计数器）和振幅步数（4096）。例如，如果 AD9854 系统时钟为 100 MHz（10 ns 的周期），扫频斜率计数器设置为最小值 3，过渡需要两个系统时钟周期（一个上升沿载入倒计时值，而下一个边缘将计数器从 3 递减至 2）。倒计时值小于 3 时，扫频速率时钟停止，因此产生一个恒定的缩放倍数输入数字乘法器。这种停滞的情况可能会对用户有用。

8 位倒计时值与输出脉冲时间之间关系的计算公式为

（N +1）×系统时钟周期

其中 N 是 8 位倒计时的值。

4096 个这样的脉冲促使 12 位加法计数器值从零增加到满刻度。因此，100 MHz 系统时钟下的最小输出键控过渡时间为

4096× 4×10≈164 微秒纳秒

最大过渡时间

4096×256×10 纳秒≈10.5 毫秒

最后，改变引脚 30 的逻辑状态，OSK INT 为高时，输出键控自动执行设定的功能。引脚 30 的一个逻辑高会导致输出线性上升到满幅度，并持续到逻辑电平变低，导致输出幅度下降至零。

I AND Q DACS

The sine and cosine outputs of the DDS drive the Q and I DACs, respectively (300 MSPS maximum). The maximum

amplitudes of these output are set by the DAC RSET resistor at Pin 56. These are current-output DACs with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides the best spurious-free dynamic range (SFDR) performance. The value of RSET is 39.93/IOUT, where IOUT is expressed in amps. DAC output compliance specifications limit the maximum voltage developed at the outputs to −0.5 V to +1 V. Voltages developed beyond this limitation cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to the compliance limits. Both DAC outputs should be terminated equally for best SFDR, especially at higher output frequencies, where harmonic distortion errors are more prominent.

Both DACs are preceded by inverse sin(x)/x filters (also called inverse sinc filters) that precompensate for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. Both DACs can be powered down when not needed by setting the DAC PD bit high (Address 1D hex of the control register). I DAC outputs are designated as IOUT1 and IOUT1, Pin 48 and Pin 49, respectively. Q DAC outputs are designated as IOUT2 and IOUT2, Pin 52 and Pin 51, respectively.

I 路和 Q 路 DAC

DDS 的正弦和余弦输出驱动 Q 路和 I 路的 DAC 是相互独立的（300 MSPS 的最大值）。这些输出的最大振幅设置由 56 引脚电阻的 DAC RSET 设定。这些都是最大输出电流为 20 mA 的电流输出型 DAC，但标称输出电流 10 毫安提供最好的无杂散动态范围（SFDR）性能。RSET 设定值为 39.93/IOUT，其中输出电流单位为安培。 设计 DAC 输出端的最大电压输出范围限制在−0.5V 到+1V，电压超过这个范围将造成较大的 DAC 的失真，并可能造成永久性损坏。用户必须选择一个适当的负载阻抗，以将输出电压摆幅限制在允许范围内。为了获得最佳的 SFDR，特别是在谐波失真严重的较高的输出频率，两路 DAC 输出应当同样有同样的终端阻抗。

两路 DAC 都先经过了反 sin（x）/x 的过滤器（也称为逆 SINC 滤波器）以预补偿 DAC 输出频率不同造成的振幅变化，实现了从直流到奈奎斯特频率平坦的幅度响应。两个 DAC 在不需要时可通过设置 DAC 的 PD 位为高（控制寄存器地址 1D）关闭。I 路 DAC 输出被命名为 IOUT1 和 IOUT1 反，引脚分别为 48 和 49。 Q 路 DAC 输出被命名为 IOUT2 和 IOUT2 引脚分别为 52 和 51。

CONTROL DAC

The 12-bit Q DAC can be reconfigured to perform as a control or auxiliary DAC. The control DAC output can provide dc control levels to external circuitry, generate ac signals, or enable duty cycle control of the on-board comparator. When the SRC Q DAC bit in the control register (Parallel Address 1F hex) is set high, the Q DAC inputs are switched from internal 12-bit Q data source (default setting) to external 12-bit, twos complement data supplied by the user. Data is channeled through the serial or parallel interface to the 12-bit Q DAC register (Address 26 hex and Address 27 hex) at a maximum data rate of 100 MHz. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the I DAC. The single RSET resistor on the AD9854 sets the full-scale output current for both DACs. When not needed, the control DAC can be separately powered down to conserve power by setting the Q DAC power-down bit high (Address 1D hex). Control DAC outputs are designated as IOUT2 and IOUT2, Pin 52 and Pin 51, respectively.

控制 DAC

这 12 位 Q 路 DAC 可以进行重新配置作为控制或辅助数模转换器。控制 DAC 输出可为外部电路提供直流控制电平，产生交流信号，或用来控制板上比较器的占空比。当控制位寄存器中的 SRC Q DAC 位（并行地址 1F）设置为高，Q 路 DAC 的输入从来自内部的 12 位 Q 路数据源（默认设置）切换到用户提供的外部 12 位，有符号补码形式的数据。数据通过串行或并行接口输入 12 位 Q DAC 寄存器（地址 26 和 27）最大数据传输速率 100 MHz。该 DAC 的时钟频率为系统时钟，最大 300 MSPS，并具与 I 路 DAC 具有相同的最大电流输出能力。AD9854 的 RSET 电阻设置的最大 DAC 输出电流对两路 DAC 起同样的作用。不需要时，控制 DAC 可以通过设置 Q DAC 电源关闭位高（地址 1D）单独断电以节能。控制 DAC 的输出指定为 IOUT2 和 IOUT2，分别为 52 脚和 51 脚。

INVERSE SINC FUNCTION

The inverse sinc function precompensates input data to both DACs for the sin(x)/x roll-off characteristic inherent in the DAC's output spectrum. This allows wide bandwidth signals (such as QPSK) to be output from the DACs without appreciable

amplitude variations as a function of frequency. The inverse sinc function can be bypassed to reduce power consumption significantly, especially at higher clock speeds. When the Q DAC is configured as a control DAC, the inverse sinc function does not apply to the Q path. Inverse sinc is engaged by default and is bypassed by bringing the bypass inverse sinc bit high in Control Register 20 hex, as noted in Table 8.

逆 Sinc 函数

sinc 函数根据 DAC 输出频谱所固有的 sin(x)/ X 的滚降特性预压缩输入到两个 DAC 的数据。这使得宽带信号（例如 QPSK）输出时幅度不会明显的随频率变化。逆 sinc 函数可以被绕过，以显著降低功耗，尤其是在较高的时钟速度。当 Q 路 DAC 配置作为控制 DAC 时，逆 sinc 函数无法应用到 Q 路。如表 8 中所示，逆 Sinc 在默认情况下是开启的，通过设置控制寄存器地址为 20 的 bypass inverse sinc 位为高禁用。

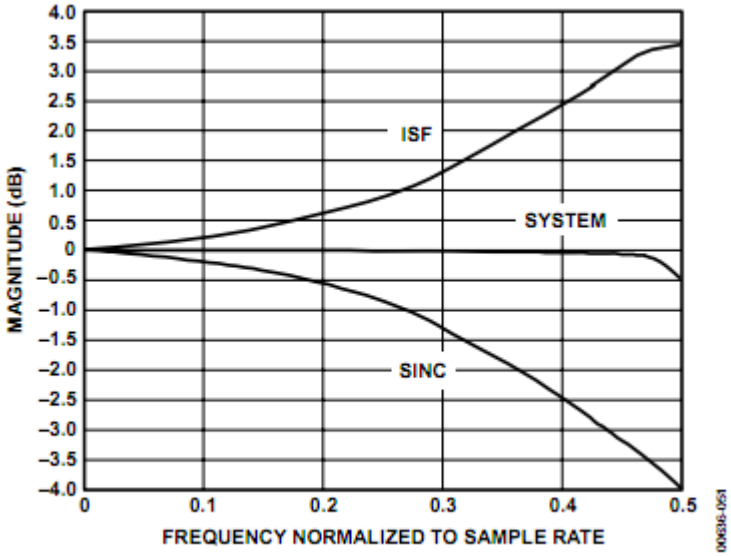


Figure 51. Inverse Sinc Filter Response

REFCLK MULTIPLIER

The REFCLK multiplier is a programmable PLL-based reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20×. With this function, users can input as little as 15 MHz at the REFCLK input to produce a 300 MHz internal system clock. Five bits in Control Register 1E hex set the multiplier value, as detailed in Table 7. The REFCLK multiplier function can be bypassed to allow direct clocking of the AD9854 from an external clock source. The system clock for the AD9854 is either the output of the REFCLK multiplier (if it is engaged) or the REFCLK inputs. REFCLK can be either a single-ended or differential input by setting Pin 64, DIFF CLK ENABLE, low or high, respectively.

参考时钟倍频

该乘数是一个可编程的基于 PLL 的参考时钟倍频器，它允许用户选择对时钟进行 4 ×20×范围的整数倍倍频。有了这个功能，用户可以输入在 REFCLK 输入 15 MHz 的低频时钟而生产出高达 300 MHz 的内部系统时钟。如表 7 所示，控制寄存器地址 1E 的 5 个控制位设置参考时钟倍频值。

该时钟倍频功能可以被禁止以允许 AD9854 从外部时钟源直接计时。AD9854 的系统时钟可以选择参考时钟倍频器的输出（如果它被启用）或参考时钟输入。通过设置 64 脚 DIFF CLK ENABLE 低或者高，可以对应地选择参考时钟单端输入或差分输入。

PLL Range Bit

The PLL range bit selects the frequency range of the REFCLK multiplier PLL. For operation from 200 MHz to 300 MHz (internal system clock rate), the PLL range bit should be set to Logic 1. For operation below 200 MHz, the PLL range bit should be set to Logic 0. The PLL range bit adjusts the PLL loop parameters for best phase noise performance within each range.

PLL Filter

The PLL FILTER pin (Pin 61) provides the connection for the external zero-compensation network of the PLL loop filter. The zero-compensation network consists of a 1.3 kΩ resistor in series with a 0.01 µF capacitor. The other side of the network should

be connected as close as possible to Pin 60, AVDD. For optimum phase noise performance, the clock multiplier can be bypassed by setting the bypass PLL bit in Control Register Address 1E hex.

Differential REFCLK Enable

A high level on the DIFF CLK ENABLE pin enables the differ-ential clock inputs, REFCLK and REFCLK (Pin 69 and Pin 68, respectively). The minimum differential signal amplitude required is 400 mV p-p at the REFCLK input pins. The center point or common-mode range of the differential signal can range from

1.6 V to 1.9 V.

When Pin 64 (DIFF CLK ENABLE) is tied low, REFCLK (Pin 69) is the only active clock input. This is referred to as single-ended mode. In this mode, Pin 68 (REFCLK) should be tied low or high.

PLL 频率范围位

PLL 的频率范围位选择了参考频率乘法器 PLL 频率范围。为了工作在 200 兆赫到 300 兆赫（内部系统时钟频率），锁相环范围位应设置为逻辑 1。对于低于 200 MHz 运行，PLL 的频率范围位应被设置为逻辑 0。 PLL 的频率范围位将每个频率范围内的锁相环路参数调整为最佳相位噪声性能。

PLL 滤波器

PLL 滤波器引脚（引脚 61）提供了 PLL 环路滤波器的外部零补偿网络连接。该零补偿网络由一个 0.01μF 的电容与一个 1.3kΩ的电阻串联实现。该网络的另一端，应尽可能靠近连接到引脚 60 的 AVDD。为了达到最佳的相位噪声性能，可以通过设置控制寄存器地址为 1E 的 bypass PLL 位禁用时钟乘法器。

启用差分时钟输入

DIFF CLK ENABLE 引脚的一个高电平允许参考时钟以差分形式输入，输入端口为 REFCLK 和 REFCLK（分别为引脚 69 和引脚 68）。REFCLK 输入引脚最小差分信号幅度为 400 mV 峰峰值。中心点或差分信号的共模范围可以从

1.6 V 至 1.9V。

当引脚 64（DIFF CLK ENABLE）被置低，REFCLK（引脚 69）是唯一有效时钟输入。这被称为单端模式。在这种模式下，引脚 68（的 REFCLK）置高或低。

High Speed Comparator

The comparator is optimized for high speed and has a toggle rate greater than 300 MHz, low jitter, sensitive input, and built-in hysteresis. It also has an output level of 1 V p-p minimum into 50 Ω or CMOS logic levels into high impedance loads. The comparator can be powered down separately to conserve power. This com-parator is used in clock-generator applications to square up the filtered sine wave generated by the DDS.

Power-Down

The programming registers allow several individual stages to be powered down to reduce power consumption while maintaining the functionality of the desired stages. These stages are identified in Table 8, Address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered up.

Furthermore, and perhaps most significantly, the inverse sinc filters and the digital multiplier stages can be bypassed to achieve significant power reduction by programming the control registers in Address 20 hex. Again, logic high causes the stage to be bypassed. Of particular importance is the inverse sinc filter; this stage consumes a significant amount of power.

A full power-down occurs when all four PD bits in Control Register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 mA).

高速比较器

比较器适合用于高速，具有切换速度大于 300 MHz 的低抖动，敏感的输入，并内置迟滞。它也有 1 V 最小输出电平匹到 50Ω或 CMOS 逻辑电平高阻抗负。该比较器可单独断电以节省电力。这个比较器用于时钟发生器应用正视过滤正弦波的 DDS 产生。

编程寄存器允许关闭一些个别功能以降低功耗，同时维持所需的功能。这些状态列于表 8，地址 1D。通过设置指定位

为逻辑高关闭。逻辑低表明功能启用。

此外，也许是最重要的是，反正弦过滤器和数字乘法器模块可以通过编程控制寄存器地址 20 中的某一位为高关闭，以明显降低功耗。再次，逻辑高电平使功能被关闭。尤其重要的是逆 SINC 滤波器，这一功能会消耗较多的功率。

当控制寄存器 1D 中所有的 PD 控制位都置为逻辑高时，芯片完全关闭。这样可以将电源消耗减少到约 10 毫瓦（3 毫安）。

PROGRAMMING THE AD9854

The AD9854 register layout table (Table 8) contains information for programming the chip for the desired functionality. Although many applications require very little programming to configure the AD9854, some use all 12 accessible register banks. The AD9854 supports an 8-bit parallel I/O operation or an SPI®-compatible serial I/O operation. All accessible registers can be written and read back in either I/O operating mode.

S/P SELECT (Pin 70) is used to configure the I/O mode. Systems that use the parallel I/O mode must connect the S/P SELECT pin to VDD. Systems that operate in the serial I/O mode must tie the S/P SELECT pin to GND.

Regardless of the mode, the I/O port data is written to a buffer memory and only affects operation of the part after the contents of the buffer memory are transferred to the register banks. This transfer of information occurs synchronously to the system clock in one of two ways:

- Internally, at a rate programmable by the user.
- Externally, by the user. I/O operations can occur in the absence of REFCLK, but the data cannot be moved from the buffer memory to the register bank without REFCLK. (See the Internal and External Update Clock section for more details.)

MASTER RESET

The MASTER RESET pin must be held at logic high active for a minimum of 10 system clock cycles. This initializes the communications bus and loads the default values listed in the Table 8 section.

AD9854 的编程

在 AD9854 寄存器布局表（表 8）包含编程芯片实现所需功能的信息。尽管许多应用需要很少的编程配置 AD9854，一些使用所有 12 个可访问的寄存器组。 AD9854 支持的一个 8 位并行 I/ O 操作或一个 SPI®兼容的串行 I/ O 操作。所有可访问的寄存器都可以在两种 I / O 工作模式下被写入并读取。

S/P SELECT（引脚 70）用于配置 I/ O 模式。系统使用并行 I/ O 模式，必须连接 S/P SELECT 引脚到 VDD。系统使用串行 I/ O 模式必须相应的将 S/P SELECT 引脚接地。

无论在何种模式中，I/O 端口数据写入缓冲存储器中，只有缓冲存储器中的内容转移到寄存器组后，才影响器件的操作。这种信息传递用以下两种方法中的一种与系统时钟同步：

•内部，以用户编程的速率。

•从外部由用户提供。 I/O 操作可以不需要系统时钟的参与，但没有系统时钟的作用，数据不能从缓冲存储器移动到寄存器组。 （详情请参阅内部和外部更新时钟部分。）

主复位

为了复位，MASTER RESET 引脚必须保持在逻辑高电平最少 10 个系统时钟周期。这将初始化通信总线，寄存器装载表 8 中列出的默认值。

Table 8. Register Layout 略

PARALLEL I/O OPERATION

With the S/P SELECT pin tied high, the parallel I/O mode is active. The I/O port is compatible with industry-standard DSPs and microcontrollers. Six address bits, eight bidirectional data bits, and separate write/read control inputs comprise the I/O port pins. Parallel I/O operation allows write access to each byte of any register in a single I/O operation of up to one per 10.5 ns. Readback capability for each register is included to ease designing with the AD9854. (Reads are not guaranteed at 100 MHz because they are intended for software debugging only.)

Parallel I/O operation timing diagrams are shown in Figure 52 and Figure 53.

SERIAL PORT I/O OPERATION

With the S/P SELECT pin tied low, the serial I/O mode is active. The serial port is a flexible, synchronous, serial communication port, allowing easy interface to many industry-standard micro-controllers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola® 6905/11 SPI and Intel® 8051 SSR protocols. The interface allows read/write access to all 12 registers that configure the AD9854 and can be configured as a single-pin I/O (SDIO) or two unidirectional pins for input and output (SDIO/SDO). Data transfers are supported in MSB-or the LSB-first format for up to 10 MHz.

When configured for serial I/O operation, most AD9854 parallel port pins are inactive; only some pins are used for the serial I/O operation. Table 9 describes pin requirements for serial I/O operation.

Note that when operating the device in serial I/O mode, it is best to use the external I/O update clock mode to avoid an update occurring during a serial communication cycle. Such an occurrence may cause incorrect programming due to a partial data transfer. To exit the default internal update mode, program the device for external update operation at power-up before starting the REFCLK signal but after a master reset. Starting the REFCLK causes this information to transfer to the register bank, forcing the device to switch to external update mode.

并行 I/O 操作

随着 S/P 值的 SELECT 置高，并行 I/O 模式被激活。该 I/O 端口与行业标准的 DSP 和微控制器兼容。六位地址，八位双向数据，以及独立的读/写控制输入构成了 I/O 端口引脚。并行 I/O 操作允许在一个写操作访问任何寄存器字节，I/O 操作可达 10.5 纳秒每次。为了方便 AD9854 设计，每个寄存器都可以读回。（读不能保证在 100 兆赫，因为它们唯一目的是软件调试。）

并行 I / O 操作时序图如图 52 和图 53。

串行端口 I / O 操作

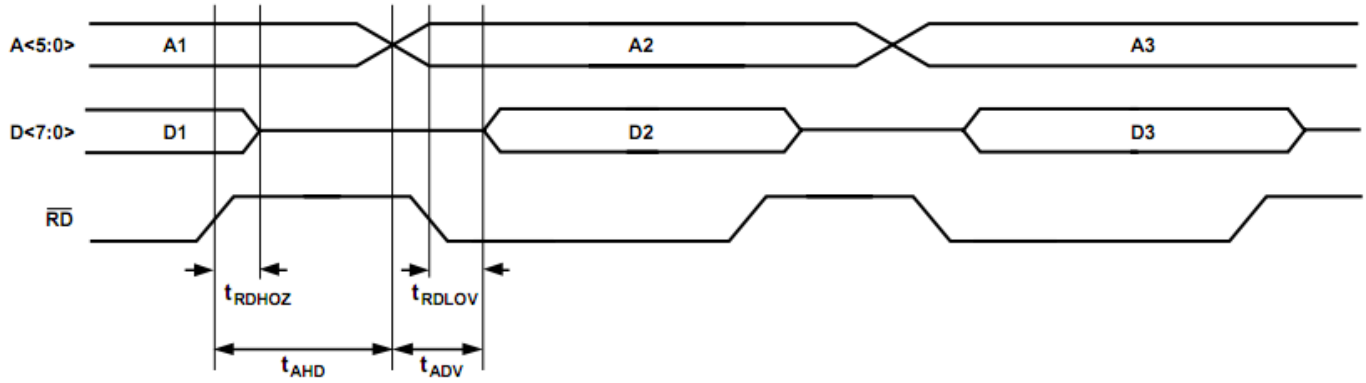
随着 S/P SELECT 引脚连接到低电平时，串行 I/O 模式被激活。串行端口是一个灵活的同步串行通信端口，便于连接众多行业标准的微控制器和微处理器。串行 I/O 兼容大多数同步传输格式，包括摩托罗拉®6905/11 SPI 和英特尔® 8051 SSR 协议。该接口允许读/写访问配置 AD9854 的所有 12 项寄存器，可配置为单线 I/O（SDIO）接口或双线输入和输出（SDIO / SDO）的单向引脚。数据传输支持 MSB 或 LSB 格式，速率高达 10 MHz。

当配置为串行 I/O 总线时，大多数 AD9854 并行端口引脚处于非活动状态，只有一些引脚用于串行 I/O 操作。表 9 给出了串行 I/O 操作要求的引脚。

请注意，当设备工作在串行 I/O 模式时，最好使用外部 I/O 更新时钟模式，以避免在串行通信时发生更新。发生这种情况可能导致由于只有部分数据传输而不能正确的编程。要退出默认的内部更新模式设置为外部更新模式，需要在设备上电主复位后操作，然后再启动 REFCLK 信号。启动 REFCLK 使此信息传输到寄存器组，迫使切换到外部设备更新模式。

Table 9. Serial I/O Pin Requirements

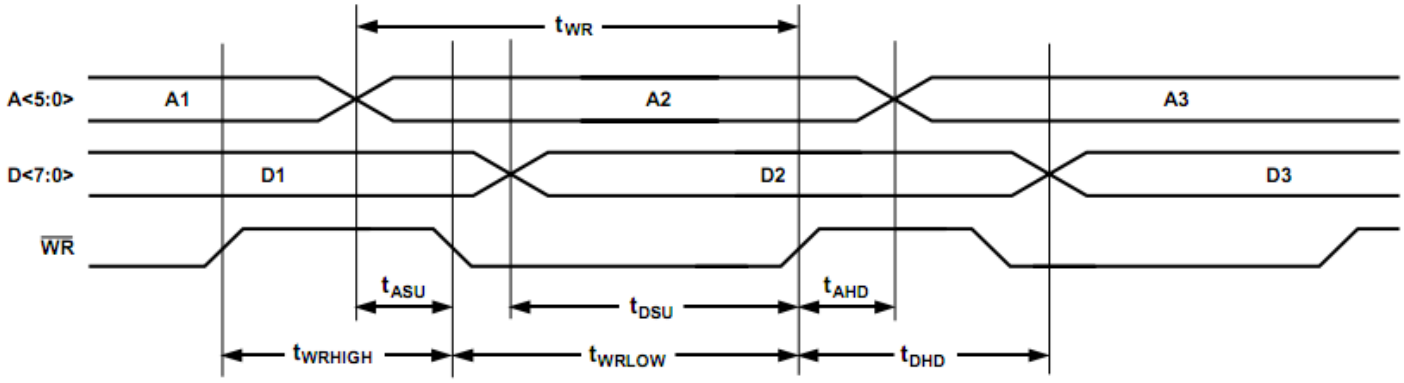
Pin Number	Mnemonic	Serial I/O Description
1 to 8	D [7:0]	The parallel data pins are not active; tie to VDD or GND.
14 to 16	A [5:3]	The A5, A4, and A3 parallel address pins are not active; tie these pins to VDD or GND.
17	A2/IO RESET	IO RESET.
18	A1/SDO	SDO.
19	A0/SDIO	SDIO.
20	I/O UD CLK	Update Clock. Same functionality for serial mode as parallel mode.
21	$\overline{WR}$/SCLK	SCLK.
22	$\overline{RD}$/$\overline{CS}$	$\overline{CS}$—Chip Select.



SPECIFICATION	VALUE	DESCRIPTION
t_{ADV}	15ns	ADDRESS TO DATA VALID TIME (MAXIMUM)
t_{AHD}	5ns	ADDRESS HOLD TIME TO RD SIGNAL INACTIVE (MINIMUM)
t_{RDLOV}	15ns	$\overline{RD}$ LOW TO OUTPUT VALID (MAXIMUM)
t_{RDHOZ}	10ns	$\overline{RD}$ HIGH TO DATA THREE-STATE (MAXIMUM)

00636-052

Figure 52. Parallel Port Read Timing Diagram



SPECIFICATION	VALUE	DESCRIPTION
t_{ASU}	8.0ns	ADDRESS SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
t_{DSU}	3.0ns	DATA SETUP TIME TO $\overline{WR}$ SIGNAL ACTIVE
t_{ADH}	0ns	ADDRESS HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
t_{DHD}	0ns	DATA HOLD TIME TO $\overline{WR}$ SIGNAL INACTIVE
t_{WRLOW}	2.5ns	$\overline{WR}$ SIGNAL MINIMUM LOW TIME
t_{WRHIGH}	7ns	$\overline{WR}$ SIGNAL MINIMUM HIGH TIME
t_{WR}	10.5ns	MINIMUM WRITE TIME

00636-053

Figure 53. Parallel Port Write Timing Diagram

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases of a serial communication cycle with the AD9854. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9854 coincident with the first eight SCLK rising edges. The instruction byte provides the AD9854 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write and the register address to be acted upon.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9854. The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9854 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. (Table 10 describes how many bytes must be transferred.) The AD9854 internal serial I/O controller expects every byte of the register being accessed to be transferred. Therefore, the user should write between I/O update clocks.

At the completion of a communication cycle, the AD9854 serial port controller expects the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IO RESET pin immediately

terminates the current communication cycle. After IO RESET returns low, the AD9854 serial port controller requires the subsequent eight rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9854 is registered on the rising edge of SCLK, and all data is driven out of the AD9854 on the falling edge of SCLK.

Figure 54 and Figure 55 show the general operation of the AD9854 serial port.

主要的串行接口操作

AD9854 有两种串行通信周期。第 1 阶段是指令周期，这是 8 个 SCLK 上升沿同步写一个指令字节到 AD9854。指令字节给 AD9854 的串口控制器提供了有关数据传输周期既第二阶段的通信周期 2 信息。第一阶段的指令字节定义了下一个数据传输是读还是写,以及要操作的寄存器地址。

每一个通信周期的前 8 个 SCLK 的上升边缘用来写入 AD9854 的指令字节。其余的 SCLK 边缘，都是第二通信周期。第 2 阶段是 AD9854 和系统控制器之间实际的数据传输。在通信周期 2 中实际传输的数据位数是寄存器地址的函数。（表 10 描述了多少字节必须被转移。）在 AD9854 内部串行 I/O 控制器期待每个字节的寄存器被访问读写。因此，用户应该在 I / O 更新时钟之间读写。

在一个通信周期完成后，AD9854 的串口控制器认为随后 8 个 SCLK 的上升沿是下一个通信周期的指令字节。此外，IO RESET 引脚有效的高电平将立即终止当前的通信周期。在 IO RESET 引脚返回低电平侯，AD9854 串口控制器要求随后的 8 个 SCLK 的上升沿输入的是下一个通信周期的指令字节。

所有数据输入到 AD9854 是发生在 SCLK 的上升沿，所有输出数据的在 SCLK 的下降沿输出。

图 54 和图 55 显示了 AD9854 的主要串口操作。

Table 10. Register Address vs. Data Bytes Transferred

Serial Register Address	Register Name	Number of Bytes Transferred
0	Phase Offset Tuning Word Register 1	2
1	Phase Offset Tuning Word Register 2	2
2	Frequency Tuning Word 1	6
3	Frequency Tuning Word 2	6
4	Delta frequency register	6
5	Update clock rate register	4
6	Ramp rate clock register	3
7	Control register	4
8	I path digital multiplier register	2
9	Q path digital multiplier register	2
A	Shaped on/off keying ramp rate register	1
B	Q DAC register	2

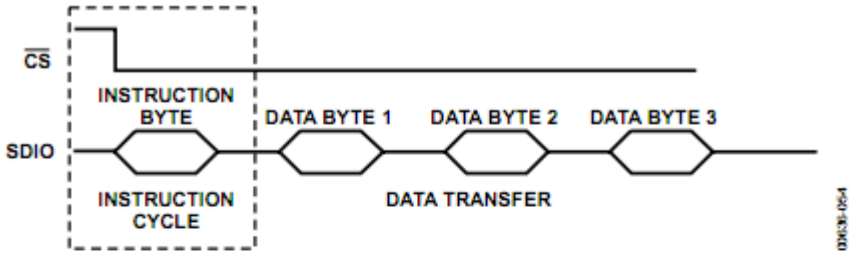


Figure 54. Using SDIO as a Read/Write Transfer

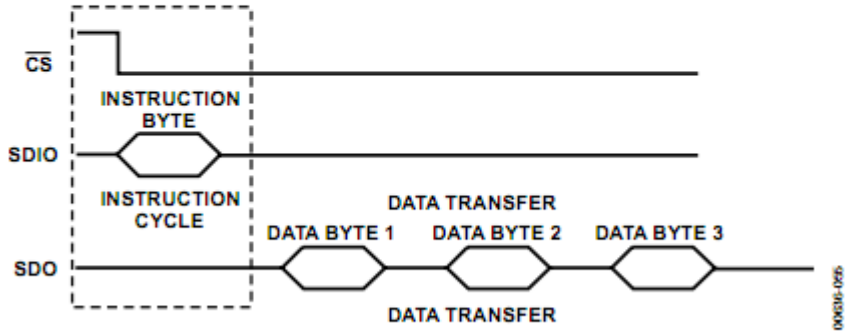


Figure 55. Using SDIO as an Input and SDO as an Output

INSTRUCTION BYTE

The instruction byte contains the following information:

指令字节

指令字节包含以下信息：

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
R/$\overline{W}$	X	X	X	A3	A2	A1	A0

R/W—Bit 7 determines whether a read or write data transfer occurs following the instruction byte. Logic high indicates read operation. Logic 0 indicates a write operation.

Bit 6, Bit 5, and Bit 4 are dummy bits (don’t care).

A3, A2, A1, A0—Bit 3, Bit 2, Bit 1, and Bit 0 determine which register is accessed during the data transfer portion of the communication cycle (see Table 8 for register address details). SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK

Serial Clock (Pin 21). The serial clock pin is used to synchronize data to and from the AD9854 and to run the internal state machines. The SCLK maximum frequency is 10 MHz.

CS

Chip Select (Pin 22). Active low input that allows more than one device on the same serial communication line. The SDO and SDIO pins go to a high impedance state when this input is high. If this pin is driven high during a communication cycle, the cycle is suspended until CS is reactivated low. The chip select pin can be tied low in systems that maintain control of SCLK.

读/写位 7 确定控制字节后发生的数据传输读还是写。逻辑高电平表示读取操作。逻辑 0 表示写操作。

第 6 位，第 5 位和第 4 位是虚位（不需要关心）。

A3，A2，A1 和 A0--第 3 位，第 2 位，第 1 位和第 0 位确定传输通信周期中访问哪个寄存器的数据（见表 8 寄存器地址详情）。

串行接口引脚说明

SCLK

串行时钟（引脚 21）。串行时钟引脚用于同步 AD9854 输入输出数据以及驱动内部运行状态机。SCLK 的最高频率为 10 兆赫。

CS

片选（引脚 22）。低电平有效，允许同一串行通信线路上接一个以上的设备。当此输入为高电平时，SDO 和 SDIO 为高阻状态。如果此引脚在一个通信周期被置高，通信周期被挂起，直到 CS 值低被重新激活。在系统中片选引脚可连接到低电平，保留 SCLK 控制。

SDIO

Serial Data I/O (Pin 19). Data is always written to the AD9854 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 0 of Register Address 20 hex. The default is Logic 0, which configures the SDIO pin as bidirectional.

SDO

Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9854 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

IO RESET

Synchronize I/O Port (Pin 17). Synchronizes the I/O port state machines without affecting the contents of the addressable registers. An active high input on the IO RESET pin causes the current communication cycle to terminate. After the IO RESET pin returns low (Logic 0), another communication cycle can begin, starting with the instruction byte.

SDIO

串行数据 I/O（引脚 19）。数据总是从该引脚写入 AD9854。然而，该引脚也可被用来作为一个双向数据线。这个引脚的配置位在控制寄存器地址位 20 的 0 位。默认为逻辑 0，配置为双向的 SDIO 引脚。

SDO

串行数据输出（引脚 18）。从该引脚读取数据，用于单独行脚传输和接收数据的协议。在 AD9854 工作在单个双向 I/O 模式情况下在，该引脚不输出数据，并设置为高阻抗状态。

IO RESET

同步 I / O 端口（引脚 17）。同步 I/ O 端口的状态机，而不影响寻址寄存器内容。IO RESET 引脚上一个有效的高电平将导致当前通信周期终止。IO RESET 引脚回到低（逻辑 0），另一个通信周期开始，首先传输指令字节。

NOTES ON SERIAL PORT OPERATION

The AD9854 serial port configuration bits reside in Bit 1 and Bit 0 of Register Address 20 hex. It is important to note that the configuration changes immediately upon a valid I/O update. For multibyte transfers, writing to this register can occur during the middle of a communication cycle. The user must compensate for this new configuration for the remainder of the current com-munication cycle.

The system must maintain synchronization with the AD9854; otherwise, the internal control logic is not able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register and then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle properly write the first two data bytes into the AD9854, but the subsequent eight rising SCLK edges are interpreted as the next instruction byte, not the final byte of the previous communication cycle.

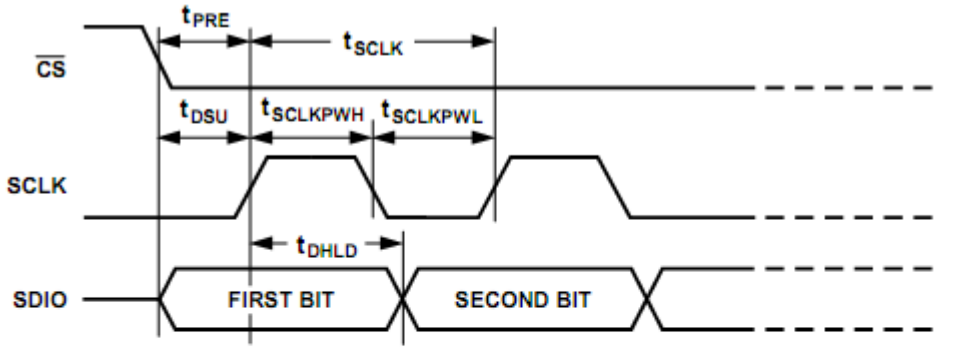
In the case where synchronization is lost between the system and the AD9854, the IO RESET pin provides a means to re-establish synchronization without reinitializing the entire chip. Asserting the IO RESET pin (active high) resets the AD9854 serial port state machine, terminating the current I/O operation and forcing the device into a state in which the next eight SCLK rising edges are understood to be an instruction byte. The IO RESET pin must be deasserted (low) before the next instruction byte write can begin. Any information written to the AD9854 registers during a valid communication cycle prior to loss of synchroni-zation remains intact.

串口操作的注意事项

AD9854 的串行端口配置位位于寄存器地址 20 的第 1 位和 20 位。重要的是要注意，一有有效的 I / O 更新配置立即更改。多字节传输，写这个寄存器可以发生在一个通信周期的中。用户必须弥补目前通信周期其余的新配置。

该系统必须保持与 AD9854 同步，否则，内部控制逻辑无法识别进一步的指令。例如，如果系统发送指令写一个 2 字节的寄存器，然后输出 3 字节的寄存器 SCLK 脉冲（24 个 SCLK 的上升沿），通讯同步丢失。在这种情况下，第 16 个 SCLK 周期的上升边缘后，指令正确地写入到 AD9854 的前两个数据字节，但随后的八边 SCLK 的上升作为下一个指令字节，而不是以前的通信周期的最后一个字节解释。

在这种系统和 AD9854 之间丢失同步的情况下，IO RESET 引脚提供一种手段，重新建立同步而不用重新初始化整个芯片。置高 IO RESET 管脚（高电平有效）复位 AD9854 串行端口状态机，结束当前的 I/O 操作，并使接器件准备好接收接下来 8 个 SCLK 上升沿的指令字节。IO RESET 引脚必须置为无效（低），然后下一个指令字节写就可以开始。任何通讯周期同步丢失之前的有效期间的写入到 AD9854 的寄存器的信息保持不变。



SYMBOL	MIN	DEFINITION
t_{PRE}	30ns	$\overline{CS}$ SETUP TIME
t_{SCLK}	100ns	PERIOD OF SERIAL DATA CLOCK
t_{DSU}	30ns	SERIAL DATA SETUP TIME
$t_{SCLKPWH}$	40ns	SERIAL DATA CLOCK PULSE WIDTH HIGH
$t_{SCLKPWL}$	40ns	SERIAL DATA CLOCK PULSE WIDTH LOW
t_{DHLD}	0ns	SERIAL DATA HOLD TIME

Figure 56. Timing Diagram for Data Write to AD9854

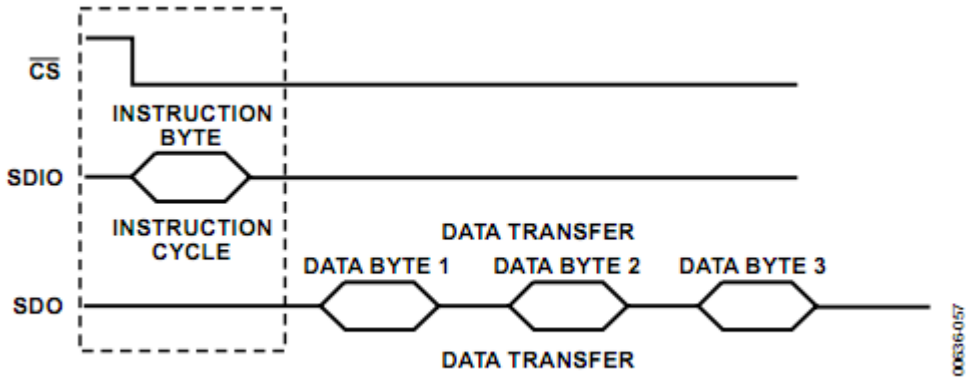


Figure 57. Timing Diagram for Read from AD9854

MSB/LSB TRANSFERS

The AD9854 serial port can support MSB- and LSB-first data formats. This functionality is controlled by Bit 1 of Serial Register Bank 20 hex. When this bit is set active high, the AD9854 serial port is in LSB-first format. This bit defaults low, to the MSB-first format. The instruction byte must be written in the format indicated by Bit 1 of Serial Register Bank 20 hex. Therefore, if the AD9854 is in LSB-first mode, the instruction byte must be written from least significant bit to most significant bit.

CONTROL REGISTER DESCRIPTION

The control register is located in the shaded portion of Table 8 at Address 1D to Address 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position, and Bit 0 is located in the lower right position of the shaded portion. In the text that follows, the register descriptions have been subdivided to make it easier to locate the text associated with specific control categories.

MSB/ LSB 传输方式

AD9854 的串行接口可以支持的 MSB 及 LSB 优先数据格式。此功能是由串行寄存器地址 20 的 1 位控制。当此位被设置为有效的高电平时，AD9854 串行端口处于 LSB 优先格式。该位默认低，MSB 优先格式。指令字节必须按串行寄存器地址 20 第 1 位所指示的格式输入。因此，如果 AD9854 在 LSB 优先模式时，指令字节必须是最低位到最高位传输。

控制寄存器的说明

如表 8 中的阴影部分所示，控制寄存器位于地址 1D 到地址 20。它有 32 位。 31 位位于左上角的位置，位 0 位于阴影部分右下角中的的位置。在后面的文本已详细说明寄存器功能，使其更容易找到与特定的位相关的文字。

CR [31:29] are open.

CR [28] is the comparator power-down bit. When this bit is set (Logic 1), its signal indicates to the comparator that a power-down mode is active. This bit is an output of the digital section and is an input to the analog section.

CR [27] must always be written to Logic 0. Writing this bit to Logic 1 causes the AD9854 to stop functioning until a master reset is applied.

CR [26] is the Q DAC power-down bit. When this bit is set (Logic 1), it indicates to the Q DAC that a power-down mode is active.

CR [25] is the full DAC power-down bit. When this bit is set (Logic 1), it indicates to both the I and Q DACs, as well as the reference, that a power-down mode is active.

CR [24] is the digital power-down bit. When this bit is set

(Logic 1), its signal indicates to the digital section that a power-down mode is active. Within the digital section, the clocks are forced to dc, effectively powering down the digital section. In this state, the PLL still accepts the REFCLK signal and continues to output the higher frequency.

CR [23] is reserved. Write to 0.

控制寄存器位[31:29]是闲置的。

控制寄存器位[28]这是掉电比较标志位。当此位被置位（逻辑 1），其信号指示的比较器，掉电模式已启动。该位是数字部分输出，是对模拟部分的输入。

控制寄存器位[27]必须始终写入逻辑 0。此位写为逻辑 1 时，AD9854 停止工作，直到主复位。

控制寄存器位[26]是 Q DAC 的电源关闭位。当此位被置位（逻辑 1），它表示 Q DAC 掉电模式已启动。

控制寄存器位[25]是完全 DAC 的电源关闭位。当此位被置位（逻辑 1），它表明 I 和 Q 路数模转换器以及参考电源的掉电模式已启动。

控制寄存器位[24]是数字电源下位。当此位被置位（逻辑 1），其信号指示的数字部分的掉电模式已启动。在数字部分，时钟被迫直流，数字部分有效断电。在这种状态下，PLL 仍然接受 REFCLK 的信号，并继续输出较高频率。

控制寄存器位[23]是保留的。写为 0。

CR [22] is the PLL range bit, which controls the VCO gain. The power-up state of the PLL range bit is Logic 1; a higher gain is required for frequencies greater than 200 MHz.

CR [21] is the bypass PLL bit, active high. When this bit is active, the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power-up state of the bypass PLL bit is Logic 1 with PLL bypassed.

CR [20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

CR [15] is the Clear Accumulator 1 bit. This bit has a one-shot type of function. When this bit is written active (Logic 1), a Clear Accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to 0. The bit is then automatically reset, but the buffer memory is not reset. This bit allows the user to easily create a sawtooth frequency sweep pattern with minimal intervention. This bit is intended for chirp mode only, but its function is still retained in other modes.

CR [14] is the clear accumulator bit. When this bit is active high, it holds both the Accumulator 1 and Accumulator 2 values at 0 for as long as the bit is active. This allows the DDS phase to be initialized via the I/O port.

CR [13] is the triangle bit. When this bit is set, the AD9854 automatically performs a continuous frequency sweep from F1 to F2 frequencies and back. This results in a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped FSK.

CR [12] is the source Q DAC bit. When this bit is set high, the Q path DAC accepts data from the Q DAC register.

CR [11:9] are the three bits that describe the five operating modes of the AD9854:

0x0 = single-tone mode

0x1 = FSK mode

0x2 = ramped FSK mode

0x3 = chirp mode

0x4 = BPSK mode

控制寄存器位[22] 是 PLL 范围位，控制 VCO 增益。 复位后 PLL 范围位的状态为逻辑 1。频率大于 200 MHz 时要求更高的增益。

控制寄存器位[21]是绕过锁相环位，高有效。当该位有效时，PLL 被断电同时 REFCLK 输入用来驱动系统时钟信号。旁路锁相环位在复位后状态为逻辑 1，默认锁相环被绕过。

控制寄存器位[20:16]位是 PLL 倍频数。这两位是 REFCLK 的乘法因子除非旁路锁相环位。该 PLL 倍频的有效范围是从 4 到 20，包括 4 和 20。

控制寄存器位[15]清除累加器 1 位。该位有一个一次性的功能。当该位被写入有效（逻辑 1），清除累加器 1 信号传送到 DDS 的逻辑电路，累加器值重置为 0。该位被自动复位，但缓冲存储器不被复位。该位允许用户轻松地最少干预地创建一个锯齿扫频模式。此位只用于 chirp 模式，但其功能在其他模式下仍然保留。

控制寄存器位[14]是清除累加器位。当该位为高电平有效，只要当他是有效的高电平时,就将两个累加器--累加器 1、2 都置零。这使得 DDS 相位通过 I / O 端口初始化。

控制寄存器位[13]是三角位。当此位被设置，AD9854 自动执行从 F1 到 F2 的连续频率扫描频率和返回。这样生成一个三角形的频率扫描。当此位被设置，运行模式必须设置为 ramped FSK。

控制寄存器位[12]是 Q 数模数据源转换器位。当此位被设置为高， Q 路 DAC 从 Q 数模转换器数据寄存器接受数据。

控制寄存器位[11:9]3 个位来描述的 AD9854 的五个工作模式：

0x0 =单音频模式

0x1 = FSK 模式

0x2 = ramped FSK 模式

0x3 =线性调频模式

0x4 = BPSK 调制模式

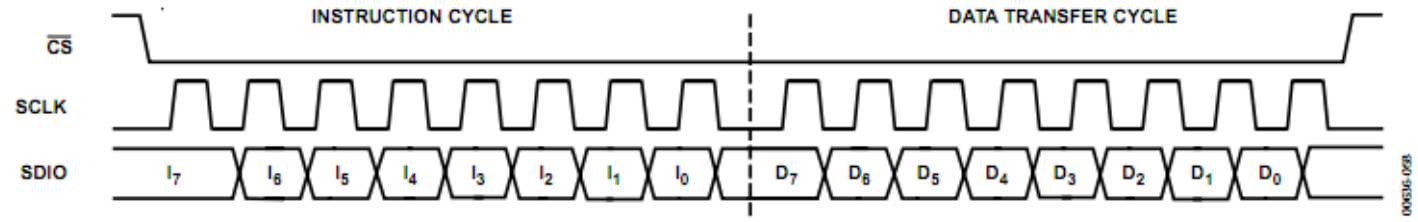


Figure 58. Serial Port Write Timing Clock Stall Low

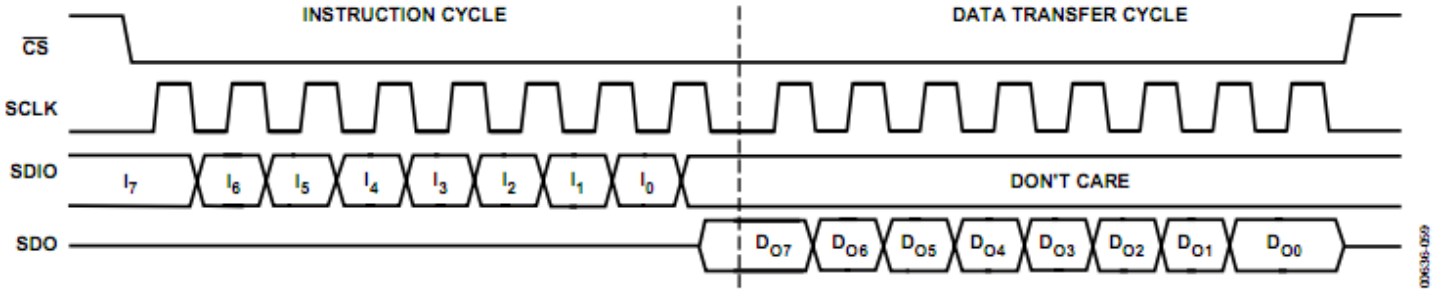


Figure 59. 3-Wire Serial Port Read Timing Clock Stall Low

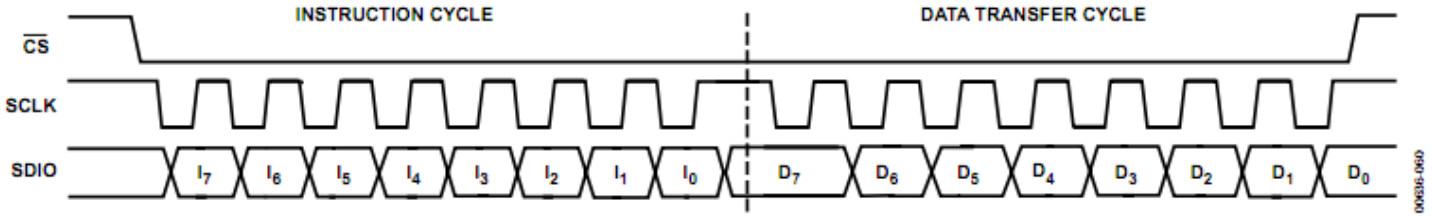


Figure 60. Serial Port Write Timing Clock Stall High

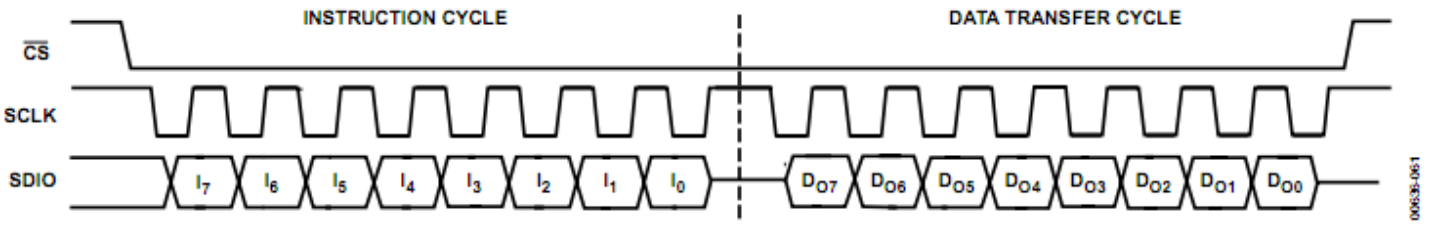


Figure 61. 2-Wire Serial Port Read Timing Clock Stall High

控制寄存器位[8] is the internal update active bit. When this bit is set to Logic 1, the I/O UD CLK pin is an output and the AD9854 generates the I/O UD CLK signal. When this bit is set to Logic 0, external I/O UD CLK functionality is performed and the I/O UD CLK pin is configured as an input.

控制寄存器位[7] is reserved. Write to 0.

控制寄存器位[6] is the inverse sinc filter bypass bit. When this bit is set, the data from the DDS block goes directly to the output shaped keying logic, and the clock to the inverse sinc filter is stopped. Default is clear with the filter enabled.

控制寄存器位[5] is the shaped keying enable bit. When this bit is set, the output ramping function is enabled and is performed in accordance with the CR [4] bit requirements.

控制寄存器位[4] is the internal/external output shaped keying control bit. When this bit is set to Logic 1, the output shaped keying factor is internally generated and applied to both the I and Q paths. When this bit is cleared (default), the output shaped keying function is externally controlled by the user, and the ouput shaped keying factor is the value of the I and Q output shaped keying factor register. The two registers that are the output shaped keying factors also default low such that the output is off at power-up until the device is programmed by the user.

CR [3:2] are reserved. Write to 0.

CR [1] is the serial port MSB-/LSB-first bit. Default is low, MSB first.

CR [0] is the serial port SDO active bit. Default is low, inactive.

控制寄存器位[8]是内部更新有效位。当此位被设置为逻辑 1， I/O UD CLK 引脚为输出，由 AD9854 产生 I/O UD 的时钟信号。当此位被设置为逻辑 0 时，执行外部 I/O UD 的时钟功能，I/O UD CLK 引脚配置为输入。

控制寄存器位[7]是保留的。写为 0。

控制寄存器位[6]是逆 SINC 滤波器旁路位。当此位被设置，从 DDS 的块中输出的数据将直接进入输出波形键控逻辑电路，反 SINC 滤波器的时钟停止。默认是清除即启用了过滤器。

控制寄存器位[5]是波形键控使能位。当此位被设置，输出斜坡功能处于开启状态，并按 CR[4]位设置运行。

控制寄存器位[4]是内部/外部输出波形键控控制位。当此位被设置为逻辑 1，输出波形键控因素是内部产生并应用于 I 和 Q 路。当该位清零（默认），输出波形键控功能是由用户外部控制，将输出的波形键控因素是 I 和 Q 输出波形键控因数寄存器的值。这两个寄存器，输出形键控等因素默认为低，复位后输出为零，直到该设备由用户编程。

控制寄存器位[3:2]被保留。写为 0。

控制寄存器位[1]是串口 MSB/LSB-first 位。默认为低，MSB 在前。

控制寄存器位[0]是串口 SDO 的有效位。默认为低，无效。

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9854 is a multifunctional, high speed device that targets a wide variety of synthesizer and agile clock applications. The

numerous innovative features contained in the device each consume incremental power. If enabled in combination, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management is a critical element in the successful application of the AD9854. However, in most cases, disabling the inverse sinc filter prevents exceeding the maximum die temperature, because the inverse sinc filter consumes approximately 30% of the total power.

The AD9854 is specified to operate within the industrial temperature range of −40°C to +85°C. This specification is conditional, however, such that the absolute maximum junction temperature of 150°C is not exceeded. At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

Many variables contribute to the operating junction temperature within the device, including

- Package style
- Selected mode of operation
- Internal system clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9854 for a given set of operating conditions.

The AD9854 is available in two package styles: a thermally enhanced surface-mount package with an exposed heat sink and a standard (nonthermally enhanced) surface-mount package. The thermal impedance of these packages is 16.2°C/W and 38°C/W, respectively, measured under still air conditions.

功耗和散热注意事项

AD9854 是一种多功能、为多种频率合成器和时钟应用开发的高速设备。在设备中所包含众多创新功能，每种功能消耗额外的电源。如果组合启用多种功能，可能会超过设备的安全热工况。认真分析和考虑功耗和热措施是成功应用 AD9854 的关键因素。然而，在大多数情况下，禁用反 sinc 滤波器可以防止超过最大温度，因为反 sinc 滤波器消耗大约 30％的总功率。

被 AD9854 指定的在-40° C 至+85° C 工业温度范围内工作。这个规范是有条件的，绝对最高结温为不超过 150° C。在高工作温度时必须极其小心操作装置，以避免超过结温损坏设备。

许多因素有助于设备工作于结温范围内，包括

•封装形式

•选择的操作模式

•内部系统时钟速度

•电源电压

•环境温度

这些因素的组合决定了一个给定的操作条件内 AD9854 的结温。

在 AD9854 有两种封装方式可供选择：一热增强型表面贴装裸露散热片和一个标准（nonthermally 增强）表面贴装封装。这些封装的热阻抗分别为 16.2℃/ W 和 38 ° C / W 的，分别在静止空气条件下测得。

THERMAL IMPEDANCE

The thermal impedance of a package can be thought of as a thermal resistor that exists between the semiconductor surface and the ambient air. The thermal impedance is determined by the package material and the physical dimensions of the package. The dissipation of the heat from the package is directly dependent on the ambient air conditions and the physical connection made between the IC package and the PCB.

Adequate dissipation of heat from the AD9854 relies on all power and ground pins of the device being soldered directly to a copper plane on a PCB. In addition, the thermally enhanced package of the AD9854ASVZ has an exposed paddle on the bottom of the package that must be soldered to a large copper plane, which, for convenience, can be the ground plane. Sockets for either package style of the device are not recommended.

JUNCTION TEMPERATURE CONSIDERATIONS

The power dissipation (PDISS) of the AD9854 in a given application is determined by many operating conditions. Some of the conditions have a direct relationship with PDISS, such as supply voltage and clock speed, but others are less deterministic. The total power dissipation within the device and its effect on the junction temperature must be considered when using the device. The junction temperature of the device is given by

(Thermal Impedance × Power Consumption) +

Ambient Temperature

The maximum ambient temperature combined with the maximum junction temperature establishes the following power consumption limits for each package: 4.06 W for ASVZ models and 1.71 W for ASTZ models.

热阻抗

一个封装的热阻抗可以被看作是一种半导体表面与周围空气间存在的热电阻。热阻抗是由包装材料和包装的物理尺寸决定的。从封装上直接散掉的热量直接取决于环境空气状况以及 IC 封装和 PCB 之间的物理连接。

足够的散热依赖于 AD9854 器件的所有电源和接地引脚被直接焊接到 PCB 上的铜平面。此外，该 AD9854ASVZ 热增强型封装底部有一裸露焊盘，该焊盘必须被焊接到一个大的铜箔面，为了方便可焊接到地平面。无论哪种型号的器件封装不推荐使用芯片插座。

结温因素

AD9854 在给定的应用中的功率耗散（PDISS）由许多工作条件决定。一些条件与 PDISS 有直接关系，如电源电压和时钟速度，但其他的因素关系较小。使用该设备时必须考虑该装置内的总功耗及其对结温的影响。该器件的结温可由下列公式计算：

（热阻抗×功耗）+ 环境温度

最高环境温度与最高结温联合决定了每种封装的最大电源消耗： ASVZ 型封装为 4.06 W 和 ASTZ 型封装为 1.71W。

Supply Voltage

The supply voltage affects power dissipation and junction temperature because PDISS = V × I. Users should design for 3.3 V nominal; however, the device is guaranteed to meet specifications over the full temperature range and over the supply voltage range of 3.135 V to 3.465 V.

Clock Speed

Clock speed directly and linearly influences the total power dissipation of the device and therefore the junction temperature. As a rule, to minimize power dissipation, the user should select the lowest possible internal clock speed to support a given application. Typically, the usable frequency output bandwidth from a DDS is limited to 40% of the clock rate to ensure that the requirements of the output low-pass filter are reasonable. For a typical DDS application, the system clock frequency should be 2.5 times the highest desired output frequency.

Mode of Operation

The selected mode of operation of the AD9854 significantly influences the total power consumption. Although the AD9854 offers many features targeting a wide variety of applications, the device is designed to operate with only a few features enabled at once for a given application. If multiple features are enabled at higher clock speeds, the maximum junction temperature of the die may be exceeded, severely limiting the long-term reliability of the device. Figure 62 and Figure 63 show the power requirements associated with each feature of the AD9854. These graphs should be used as a guide in determining power consumption for specific feature sets.

Figure 62 shows the supply current consumed by the AD9854 over a range of frequencies for two possible configurations. All circuits enabled means that the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are enabled. Basic configuration means that the output scaling multipliers, the inverse sinc filter, the Q DAC, and the on-board comparator are disabled.

电源电压

电源电压影响功耗和结温因为 PDISS= V×I。用户应设计为 3.3 V 标称电压，但是，该设备是保证符合在整个温度范围规格和电源电压范围 3.135V 至 3.465 V 。

时钟速度

时钟速度和总功耗以及结温直接线性相关。因此，以减少功率损耗，用户应选择尽可能最低的内部时钟速度，以支持特定的应用。通常情况下，从 DDS 输出的可用频率带宽限制为 40％的时钟速度，以保证输出的低通滤波器要求是合理的。对于一个典型的 DDS 的应用，系统时钟频率应该是 2.5 倍的最高期望的输出频率。

操作模式

AD9854 操作模式的选择显著影响着总功耗。虽然 AD9854 为广泛的应用提供了多种特点，该设备被设计为在某一特定应用中只启用只有少数特定的应用功能。如果有多个功能于更高的时钟速度启用，芯片温度可能会超过最大结温度，严重地影响设备的长期可靠性。图 62 和图 63 显示了与每个 AD9854 功能相关的电源消耗要求。这些图表应该被用来作为确定具体的功能配置电源消耗的指南。

图 62 显示了 AD9854 的两个可能配置在一系列频率范围的供电电流消耗。所有电路启用意味着输出比例乘法器，逆 SINC 滤波器的 Q 路 DAC 和板上比较器均被启用。基本配置意味着输出比例乘法器、逆 SINC 滤波器、Q DAC 和板上比较器被禁用。

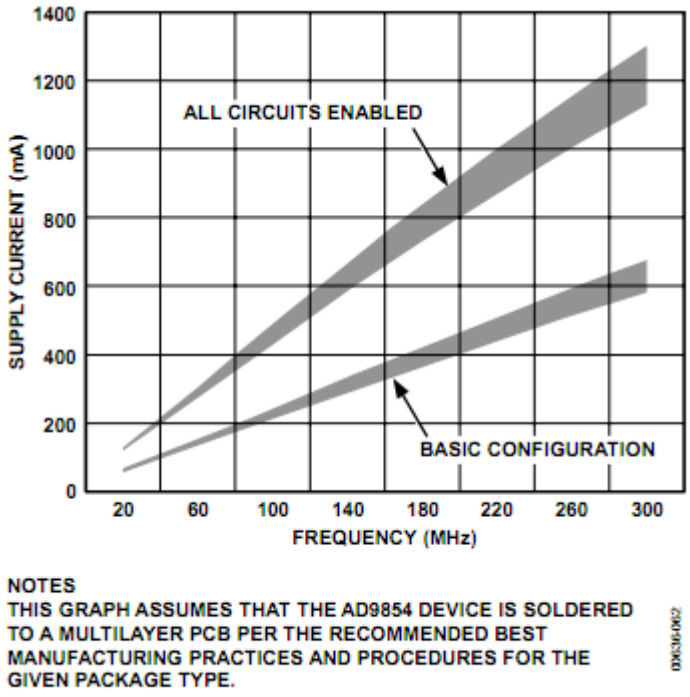


Figure 62. Current Consumption vs. Clock Frequency

Figure 63 shows the approximate current consumed by each of four functions.

图 63 显示了四个功能近似的电流消耗。

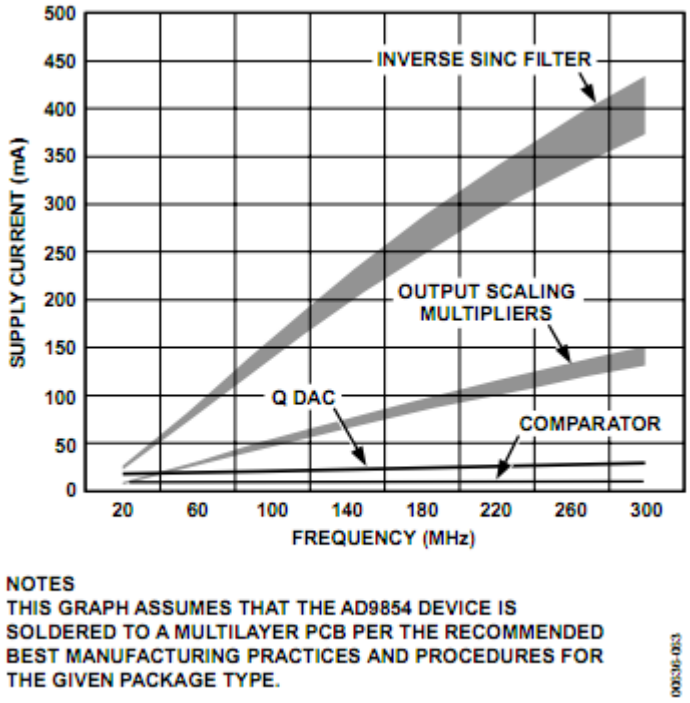


Figure 63. Current Consumption by Function vs. Clock Frequency

EVALUATION OF OPERATING CONDITIONS

The first step in applying the AD9854 is to select the internal clock frequency. Clock frequency selections greater than 200 MHz require the use of the thermally enhanced package (AD9854ASVZ); other clock frequencies may allow the use of the standard plastic surface-mount package, but more information is needed to make that determination.

The second evaluation step is to determine the maximum required operating temperature for the AD9854 in a given application. Subtract this value from 150°C, which is the maximum junction temperature allowed for the AD9854. For the extended industrial temperature range, the maximum operating temperature is 85°C, which results in a difference of 65°C. This is the maximum temperature gradient that the device can experience due to power dissipation.

The third evaluation step is to divide the maximum temperature gradient by the thermal impedance to determine the maximum power dissipation allowed for the application. For example, 65°C divided by the thermal impedance of the package being used yields the total power dissipation limit (4.06 W for the ASVZ models and 1.71 W for the ASTZ models). Therefore, for a 3.3 V nominal power supply voltage, the current consumed by the device with full operating conditions must not exceed 515 mA for the standard plastic package and 1242 mA for the thermally enhanced package. The total set of enabled functions and operating conditions of the AD9854 application must support these current consumption limits.

To determine the suitability of a given AD9854 application in terms of the power dissipation requirements use Figure 62 and Figure 63. These graphs assume that the AD9854 device is soldered to a multilayer PCB per the recommended best manufacturing practices and procedures for the given package type. This ensures that the specified thermal impedance specifications are achieved.

THERMALLY ENHANCED PACKAGE

MOUNTING GUIDELINES

Refer to the AN-772 Application Note for details on mounting devices with an exposed paddle.

使用条件评价

应用 AD9854 的第一步是选择内部时钟频率。时钟频率超过 200 兆赫的需要选择使用增强散热型封装（AD9854ASVZ），其他的时钟频率可能允许使用标准的塑料表面贴装封装，但需要更多的信息以作出决定。

第二个步骤是评估，以确定 AD9854 在一个给定应用的最大工作温度。这从温度减去 150℃，这是 AD9854 允许的最高结温的值。工作在扩展工业温度范围内，最高工作温度为 85°C，最大温度差异 65°C。考虑到功率耗散，这是该装置能达到的最大温度。

第三步是评估热阻抗造成的最高温度梯度，以确定应用中允许的最大功耗。例如，65°C 除以使用封装的热阻抗得到总功率消耗限额（ASVZ 型封装为 4.06 W 和 ASTZ 型封装为 1.71 W）。因此，对于一个 3.3 V 标称电源电压，以全功能设置下器件消耗电流为标准塑料封装不得超过 515 毫安，增强散热型封装不得超过 1242 毫安。AD9854 启用的功能和应用的工作条件必须满足这些电流消耗限额。

要确定给定 AD9854 应用是否满足功耗方面的要求，可以参考图 62 和图 63。这些图表假设 AD9854 被焊接到多层印刷电路板，根据给定的封装类型按照设备制造业的最佳建议做法和程序。这可以确保指定的热阻抗规格得以实现。

热增强型封装安装指南

参考 AN-772 应用手册上安装带有裸露焊盘芯片的详细信息。

EVALUATION BOARD

An evaluation board package is available for the AD9854 DDS device. This package consists of a PCB, software, and documentation to facilitate bench analysis of the device's performance. To ensure optimum dynamic performance from the device, users should familiarize themselves with the operation and performance capabilities of the AD9854 with the evaluation board and use the evaluation board as a PCB reference design.

EVALUATION BOARD INSTRUCTIONS

The AD9852/AD9854 Revision E evaluation board includes either an AD9852ASVZ or AD9854ASVZ IC.

The ASVZ package permits 300 MHz operation by virtue of its thermally enhanced design. This package has a bottom-side heat slug that must be soldered to the ground plane of the PCB directly beneath the IC. In this manner, the evaluation board PCB ground plane layer extracts heat from the AD9852 or AD9854 IC package. If device operation is limited to 200 MHz or less, the ASTZ package can be used without a heat slug in customer installations over the full temperature range.

Evaluation boards for both the AD9852 and AD9854 are identical except for the installed IC.

评估板

评估板套件可用于 AD9854 DDS 芯片。这个套件包包括一个印刷电路板，软件和文件，以方便对芯片性能进行分析。为了确保最佳的器件的动态性能，用户应熟悉 AD9854 评估板的原理及性能，并以此作为自己电路板的设计参考。

评估板说明

版本 E 的 AD9852/AD9854 评估板包括 AD9852ASVZ 或 AD9854ASVZ 集成电路。

ASVZ 封装通过其增强散热型设计允许 300MHz 工作频率。芯片封装的底部有散热片，必须直接焊接到 IC 下方的 PCB 的接地平面。在这种方式下，评估板 PCB 地平面层可以从 AD9854 或 AD9852 的 IC 封装底部吸收热量。如果设备的操作仅限于 200 MHz 或更少，ASTZ 封装可用于整个温度范围，也不需要客户安装散热片。

AD9852 和 AD9854 的评估板除了安装的芯片不同外是完全相同的（两者 PIN TO PIN，可相直接替换）。

To assist in proper placement of the pin header shorting jumpers, the instructions refer to direction (left, right, top, bottom) as well as header pins to be shorted. Pin 1 for each 3-pin header is marked on the PCB corresponding with the schematic diagram. When following these instructions, position the PCB so that the PCB text can be read from left to right. The board is shipped with the pin headers configuring the board as follows:

- REFCLK for the AD9852 or AD9854 is configured as differential. The differential clock signals are provided by the MC100LVEL16D differential receiver.
- The input clock for the MC100LVEL16D is single ended via J25. This signal may be 3.3 V CMOS or a 2 V p-p sine wave capable of driving 50 Ω (R13).
- Both DAC outputs from the AD9852 or AD9854 are routed through the two 120 MHz elliptical LP filters, and their outputs are connected to J7 (Q, or control DAC) and J6 (I, or cosine DAC).
- The board is set up for software control via the printer port connector.

- The output currents of the DAC are configured for 10 mA.

GENERAL OPERATING INSTRUCTIONS

Load the CD software onto your PC's hard disk. The current software (Version 1.72) supports Windows® 95, Windows 98, Windows 2000, Windows NT®, and Windows XP. Connect a printer cable from the PC to the AD9854 evaluation board printer port connector labeled J11.

为了协助妥善安置引脚短路跳线帽，指示方向（左，右，上，下），以及被短路针脚。PCB 上每个 3 针接头的引脚 1 标有相应的原理图。当按照这些指示时，印刷电路板的放置应使 PCB 的文字可以左到右读出。电路板附带的排针配置如下：

•AD9852 或 AD9854 的 REFCLK 配置为差分输入。差分时钟信号提供由 MC100LVEL16D 差分接收机。

•MC100LVEL16D 输入时钟可以通过 J25 设置为单端。这个信号可以是 3.3 V CMOS 或 2 V 峰峰值的正弦波具有驱动 50Ω负载（R 13）的能力。

• AD9852 或者是 AD9854 的 DAC 输出接到两个 120 MHz 的椭圆 LP 滤波器，其输出连接到 J7（Q，或控制 DAC）及 J6（I，或余弦 DAC）。

•电路板通过打印机端口连接到电脑以接受设置或控制。

•DAC 的输出电流配置为 10 毫安。

一般操作说明

读取 CD 软件到您的电脑的硬盘上。目前的软件（版本 1.72）支持 Windows®95，视窗 98，视窗 2000，Windows NT ® 的，和 Windows XP。从 PC 连接打印机电缆连接到 AD9854 的评估板打印机端口连接标记 J11。

Hardware Preparation

Use the schematics (see Figure 64 and Figure 65) in conjunction with these instructions to become acquainted with the electrical functioning of the evaluation board.

Attach power wires to the connector labeled TB1 using the screw-down terminals. This connector is plastic and press-fits over a 4-pin header soldered to the board. Table 11 lists the connections to each pin.

硬件准备

使用原理图（见图 64 和图 65）结合这些指令的，来熟悉评估板的功能。

将电源线连接到标有 TB1 的接线端使用螺丝式终端。此连接器是塑料的，与焊接到电路板上的 4 针接头匹配。表 11 列出了每个引脚的连接。

Table 11. Power Requirements for DUT Pins[1]

AVDD 3.3 V	DVDD 3.3 V	VCC 3.3 V	Ground
For all DUT analog pins	For all DUT digital pins	For all other devices	For all devices

[1] DUT = device under test.

Clock Input, J25

Attach REFCLK to the clock input, J25. This is a single-ended input that is routed to the MC100LVEL16D for conversion to differential PECL output. This is accomplished by attaching a 2 V p-p clock or sine wave source to J25. Note that this is a 50 Ω impedance point set by R13. The input signal is ac-coupled and then biased to the center-switching threshold of the MC100LVEL16D. To engage the differential clocking mode of the AD9854, Pin 2 and Pin 3 (the bottom two pins) of W3 must be connected with a shorting jumper.

The signal arriving at the AD9854 is called the reference clock. When engaging the on-chip PLL clock multiplier, this signal is the reference clock for the PLL and the multiplied PLL output becomes the system clock. If the PLL clock multiplier is to be bypassed, the reference clock supplied by the user directly operates the AD9854 and is therefore the system clock.

Three-State Control

The W9, W11, W12, W13, W14, and W15 switch headers must be shorted to allow the provided software to control the AD9854 evaluation board via the printer port connector, J11.

Programming

If programming of the AD9854 is not to be provided by the user's PC and Analog Devices software, the W9, W11, W12, W13, W14, and W15 headers should be opened (shorting jumpers removed). This effectively detaches the PC interface and allows J10 (the 40-pin header) and J1 to assume control without bus contention. Input signals on J10 and J1 going to the AD9854 should be 3.3 V CMOS logic levels.

时钟输入，J25

附加的 REFCLK 时钟输入，J25。这是一个连接到 MC100LVEL16D 转换为到差分 PECL 输出的单端输入。这是通过附加 2 V 峰峰时钟或正弦波源到 J25。请注意，这是一个由 R13 设置的 50Ω阻抗点。输入信号为交流耦合，然后偏置到 MC100LVEL16D 中心开关阈值。为了产生差分的 AD9854 时钟，W3 的引脚 2 和引脚 3（底部的两个引脚）必须用跳线帽短路。

到达 AD9854 的信号被称为参考时钟。当启用片上 PLL 时钟乘法器，此信号为 PLL 和倍频器 PLL 参考时钟，倍频器 PLL 输出成为系统时钟。如果 PLL 时钟倍频器被关闭，参考时钟由用户提供直接提供给 AD9854，因此是系统时钟。

三态控制

W9、W11、W12、W13、W14 及 W15 的跳线帽短路以允许所提供的软件通过打印机端口连接器，J11 来控制 AD9854 评估板。

编程

如果 AD9854 编程不是由用户的电脑和 ADI 软件，W9、W11、W12、W13、W14 及 W15 的跳线帽应该是和打开（拔掉跳线帽）。这可以有效地分离 PC 接口，并允许的 J10（40 针接头）和 J1 起控制作用而不产生总线竞争。从 J10 和 J1 输入到 AD9854 的信号应为 3.3 V CMOS 逻辑电平。

Low-Pass Filter Testing

The purpose of the 2-pin W7 and W10 headers (associated with J4 and J5) is to allow the two 50 Ω, 120 MHz filters to be tested during PCB assembly without interference from other circuitry attached to the filter inputs. Typically, a shorting jumper is attached to each header to allow the DAC signals to be routed to the filters. If the user wishes to test the filters, the shorting jumpers at W7 and W10 should be removed and 50 Ω test signals should be applied at the J4 and J5 inputs to the 50 Ω elliptic filters. Users should refer to the schematic provided and to the following sections to properly position the remaining shorting jumpers.

Observing the Unfiltered IOUT1 and the Unfiltered IOUT2 DAC Signals

The unfiltered DAC outputs can be observed at J5 (the I, or cosine DAC, signal) and J4 (the Q, or control DAC, signal). Use the following procedure to route the two 50 Ω terminated analog DAC outputs to the SMB connectors and to disconnect any other circuitry:

1. Install shorting jumpers at W7 and W10.
2. Remove the shorting jumper at W16.
3. Remove the shorting jumper from the 3-pin W1 header.
4. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W4 header.

The raw DAC outputs may appear as a series of quantized (stepped) output levels that may not resemble a sine wave until they are filtered. The default 10 mA output current develops a 0.5 V p-p signal across the on-board 50 Ω termination. If the observation equipment offers 50 Ω inputs, the DAC develops only 0.25 V p-p due to the double termination.

If using the AD9852 evaluation board, the user can control IOUT2 (the control DAC output) by using the serial or parallel ports. The 12-bit, twos complement value(s) is/are written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum), with all 0s being midscale. Rapidly changing the contents of the control DAC register (up to 100 MSPS) allows IOUT2 to assume any waveform that can be programmed.

低通滤波器的测试

2 针的 W7 和 W10 头（与 J4 和 J5 的相连）的目的是为了在印刷电路板组装期间测试两个 50Ω，120 MHz 的过滤器，并阻止其他电路的干扰连接到滤器输入。通常使用时,用跳线帽，让每个 DAC 的信号路输入到过滤器。如果用户希望测试滤波器,在 W7 和 W10 的跳线帽应该被移除，50Ω测试信号应在 J4 和 J5 输入到 50Ω椭圆滤波器。用户应参照电路

图，并妥善收藏多余的跳线帽。

观测未过滤 IOUT1 和未过滤 IOUT2 DAC 的信号

未过滤的 DAC 输出可在 J5 观察到（I 路，或余弦 DAC 的信号）和 J4（即 Q 或控制 DAC，信号）。使用下列程序，以便将两个 50Ω终端的模拟 DAC 输出到 SMB 连接器，并断开所有其他电路：

1。在 W10 W7 安装跳线帽。

2。取掉 W16 的跳线帽。

3。取掉 3 针跳线 W1 短路跳线帽。

4。在 3 针跳线 W4 的引脚 1 和引脚 2（下面的两针）安装跳线帽。

原始 DAC 输出可能显示为量化（步进）的输出电平，而不会像一个正弦波，直到它们被过滤。默认为 10 mA 输出电流，在开发板 50Ω终端电阻上产生 0.5 Vp - p 的电压信号。如果观察设备提供 50Ω输入，由于终端电阻并联的结果，DAC 的输出只有 0.25 V 峰峰值。

如果使用的是 AD9852 的评估板，用户可以通过串行或并行端口控制 IOUT2（控制 DAC 输出）。12 位，二进制补码值（S）被写入控制 DAC 寄存器，设置 IOUT2 输出静态直流电平。允许十六进制值 7FF（最大）到 800（最低），中间值为全 0。迅速更新控制 DAC 寄存器（高达 100 MSPS）的内容允许 IOUT2 输出任何可以被编程的波形。

Observing the Filtered IOUT1 and the Filtered IOUT2

The filtered I (cosine DAC) and Q (control DAC) outputs can be observed at J6 (for the I signal) and J7 (for the Q signal). Use the following procedure to route the 50 Ω (input and output Z) low-pass filters into the pathways of the I and Q signals to remove images, aliased harmonics, and other spurious signals that are greater than approximately 120 MHz:

1. Install shorting jumpers at W7 and W10.
2. Install a shorting jumper at W16.
3. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W1 header.
4. Install a shorting jumper on Pin 1 and Pin 2 (bottom two pins) of the 3-pin W4 header.
5. Install a shorting jumper on Pin 2 and Pin 3 (bottom two pins) of the 3-pin W2 and W8 headers.

The resulting I and Q signals appear as nearly pure sine waves and 90° out of phase with each other. These filters are designed with the assumption that the system clock speed is at or near its maximum speed (300 MHz). If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible, or inevitable, that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters. If the AD9852 evaluation board is used, any reference to the Q signal should be interpreted as meaning the control DAC.

观察滤波后的 IOUT2 和滤波后的 IOUT1

过滤后的 I（余弦 DAC）和 Q（控制 DAC）的输出可在 J6（I 路信号）和 J7（Q 路信号）观察。使用下列程序，以便将 50Ω（输入和输出阻抗）低通接入 I 和 Q 路信号的通路，消除除镜像，谐波失真，以及其他大于约 120 兆赫杂散信号：

1。安装 W10 W7 短路跳线帽。

2。安装 W16 的跳线帽。

3。在三针跳线头 W1 的引脚 1 和引脚 2（底部的两针）安装短路跳线帽。

4。在三针跳线头 W4 的引脚 1 和引脚 2（底部的两针）安装短路跳线帽。

5。在三针跳线头 W2 和 W8 的引脚 2 和引脚 3（底部的两针）安装短路跳线帽。

由此产生的 I 和 Q 信号显示为纯正弦波，彼此的相位相差 90 °。这些过滤器是基于系统时钟速度达到或接近其最高速度（300 MHz）的假设设计的。如果系统时钟速度远低于 300 兆赫，例如 200 兆赫，可能或不可避免的，有害的 DAC 输出以及基频信号将通过低通滤波器。如果使用 AD9852 的评估板，Q 路信号应被理解为控制 DAC（AD9852 没有正交的 Q 路）。

Observing the Filtered IOUT1 and the Filtered IOUT1

The filtered I DAC outputs can be observed at J6 (the true signal) and J7 (the complementary signal). Use the following procedure to route the 120 MHz low-pass filters in the true and complementary output paths of the I DAC to remove images, aliased harmonics, and other spurious signals that are greater than approximately 120 MHz:

1. Install shorting jumpers at W7 and W10.
2. Install a shorting jumper at W16.
3. Install a shorting jumper on Pin 2 and Pin 3 (top two pins) of the 3-pin W1 header.
4. Install a shorting jumper on Pin 2 and Pin 3 (top two pins) of the 3-pin W4 header.
5. Install a shorting jumper on Pin 2 and Pin 3 (bottom two pins) of the 3-pin W2 and W8 headers.

The resulting signals appear as nearly pure sine waves and 180° out of phase with each other. If the system clock speed is much less than 300 MHz, for example 200 MHz, it is possible, or inevitable, that unwanted DAC products other than the fundamental signal will be passed by the low-pass filters.

观察滤波后的 IOUT1 和滤波后的 IOUT1 反

过滤后的我 DAC 输出可在 J6 的（真正的信号）和 J7（互补信号）观察。使用下列程序，以便用 120 MHz 低通滤波器在真实和互补输出 DAC 路径滤除镜频，谐波失真，以及其他大于 120 MHz 的杂散信号：

1。安装 W10 W7 短路跳线帽。

2。安装 W16 的跳线帽。

3。在三针跳线头 W1 的引脚 2 和引脚 3（底部的两针）安装短路跳线帽。

4。在三针跳线头 W4 的引脚 2 和引脚 3（底部的两针）安装短路跳线帽。

5。在三针跳线头 W2 和 W8 的引脚 2 和引脚 3（底部的两针）安装短路跳线帽。

由此产生的信号显示为纯正弦波，两信号相位差近 180 ° 。如果系统时钟速度远低于 300 兆赫，例如 200 兆赫，可能或不可避免的，有害的 DAC 输出以及基频信号将通过低通滤波器。

Connecting the High Speed Comparator

To connect the high speed comparator to the DAC output signals use either the quadrature filtered output configuration (for AD9854 only) or the complementary filtered output configuration outlined in the previous section (for both the AD9854 and the AD9852). Follow Step 1 through Step 4 in either the Observing the Filtered IOUT1 and the Filtered IOUT2 section or the Observing the Filtered IOUT1 and the Filtered IOUT1 section. Then install a shorting jumper on Pin 1 and Pin 2 (top two pins) of the 3-pin W2 and W8 headers. This reroutes the filtered signals away from the output connectors (J6 and J7) and to the 100 Ω configured comparator inputs. This sets up the comparator for differential input without affecting the comparator output duty cycle, which should be approximately 50% in this configuration.

The user can change the value of RSET Resistor R2 from 3.9 kΩ to 1.95 kΩ to receive more robust signals at the comparator inputs. This decreases jitter and extends the operating range of the comparator. To implement this change install a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with that provided by R2. This boosts the DAC output current from 10 mA to 20 mA and doubles the peak-to-peak output voltage developed across the loads, thus resulting in more robust signals at the comparator inputs.

连接高速比较器

要连接 DAC 的输出信号到高速比较器可以使用正交滤波的输出配置（只对于 AD9854）或互补滤波的输出配置上一节所概述（AD9854 和 AD9852 均可采用）。按照步骤，执行观察滤波后的 IOUT2、IOUT1 部分或观测滤波后的 IOUT1、IOUT1 反中的步骤 1 到 4。然后在 3 针跳线头 W2 和 W8 的引脚 1 和引脚 2（上两脚）安装跳线帽。这样将滤波的信号从输出接口（J6 的和 J7）转移到了 100Ω 阻抗匹配的比较器输入的。这个差分输入比较设置不影响比较器输出的约为 50％的占空比。

用户可以将 RSET 设定电阻 R2 的值从 3.9kΩ改为 1.95kΩ，以使比较器的输入接收更强的信号。这减少抖动和扩展了比较器的工作范围。要实现这个转变在 W6 安装跳线帽，以提供除 R2 外的第二个 3.9kΩ的片式电阻（R20 的）。这将 DAC 的输出电流从 10 mA 提升到 20 mA，同时加到负载上的输出电压峰峰值翻倍，从而向比较器输入更大的信号强度。

Single-Ended Configuration

To connect the high speed comparator in a single-ended configuration so that the duty cycle or pulse width can be controlled, a dc threshold voltage must be present at one of the comparator inputs. The user can supply this voltage using the control DAC. A 12-bit, twos complement value is written to the control DAC register that sets the IOUT2 output to a static dc level. Allowable hexadecimal values are 7FF (maximum) to 800 (minimum), with all 0s being midscale. The IOUT1 channel continues to output

a filtered sine wave programmed by the user. These two signals are routed to the comparator by using the 3-pin W2 and W8 header switches. Use of the configuration described in the Observing the Filtered IOUT1 and the Filtered IOUT2 section is required. Follow Step 1 through Step 4 in this section, and then install a shorting jumper on Pin 1 and Pin 2 (top two pins) of the 3-pin W2 and W8 headers.

The user can change the value of RSET Resistor R2 from 3.9 kΩ to 1.95 kΩ to receive more robust signals at the comparator inputs. This decreases jitter and extends the operating range of the comparator. To implement this change install a shorting jumper at W6, which provides a second 3.9 kΩ chip resistor (R20) in parallel with that provided by R2.

单端配置

要连接成单端模式，使高速比较器占空比或脉冲宽度可控制，直流阈值电压必须接到比较器的一个输入端。用户可以使用控制的 DAC 提供电压。一个 12 位二进制补码写入到控制 DAC 寄存器，设置 IOUT2 为静态直流输出。允许设置范围为十六进制值 7FF（最大）到 800（最低），中间值为全 0。IOUT1 通道继续输出一个由用户编程经过过滤的正弦波。这两个信号 通过 3 针跳线头 W2 和 W8 连接到比较器。必需使用观察滤波后的 IOUT1 和 IOUT2 部分的配置。按照步骤 1 到 4，然后在 3 针跳线头 W2 和 W8 的引脚 1 和引脚 2（上两脚）安装跳线帽。

用户可以将 RSET 设定电阻 R2 的值从 3.9kΩ改为 1.95kΩ，以使比较器的输入接收更强的信号。这减少抖动和扩展了比较器的工作范围。要实现这个转变在 W6 安装跳线帽，以提供除 R2 外的第二个 3.9kΩ的片式电阻（R20 的）。

USING THE PROVIDED SOFTWARE

The evaluation software is provided on a CD, along with a brief set of instructions. Use the instructions in conjunction with the AD9852 or AD9854 data sheet and the AD9852 or AD9854 evaluation board schematic.

The CD contains the following:

- The AD9852/AD9854 evaluation software
- AD9854 evaluation board instructions
- AD9854 data sheet
- AD9854 evaluation board schematics
- AD9854 PCB layout

使用提供的软件

评估软件通过 CD 提供，以及一个简短的说明手册。将该手册与 AD9854 或 AD9852 的数据表、AD9854 和 AD9852 的评估板电路图配合使用。

该光盘包含以下内容：

•AD9852/AD9854 的评估软件

•AD9854 评估板说明

•AD9854 数据表

•AD9854 评估板电路图

•AD9854 PCB 布局

Several numerical entries, such as frequency and phase infor-mation, require pressing Enter to register the information. For example, if a new frequency is input but does not take effect when Load is clicked, the user probably neglected to press Enter after typing the new frequency information.

Normal operation of the AD9852/AD9854 evaluation board begins with a master reset. After this reset, many of the default register values are depicted in the software control panel. The reset command sets the DDS output amplitude to minimum and 0 Hz, zero phase offset, as well as other states that are listed in the Register Layout table (Table 8 for AD9854).

The next programming block should be the reference clock and multiplier because this information is used to determine the proper 48-bit frequency tuning words that are entered and later calculated.

The output amplitude defaults to the 12-bit, straight binary multiplier values of the I (cosine DAC) multiplier register of 000 hex; no output (dc) should be seen from the DAC. Set the multiplier amplitude in the Output Amplitude dialog box to a substantial value, such as FFF hex. The digital multiplier can be bypassed by selecting Output Amplitude is always Full Scale,

but this usually does not result in the best spurious-free dynamic range (SFDR). The best SFDR, achieving improvements of up to 11 dB, is obtained by routing the signal through the digital multiplier and then reducing the multiplier amplitude. For instance, FC0 hex produces less spurious signal amplitude than FFF hex. If SFDR must be maximized, this exploitable and repeatable phenomenon should be investigated in the given application. This phenomenon is more readily observed at higher output frequencies, where good SFDR becomes more difficult to achieve.

Refer to this data sheet and the evaluation board schematic to understand the available functions of the AD9854 and how the software responds to programming commands.

SUPPORT

Applications assistance is available for the AD9854, the AD9854 PCB evaluation board, and all other Analog Devices products. Call 1-800-ANALOGD or visit www.analog.com/dds.

几个数字框，如频率和相位信息，要求输入回车以确认寄存器信息。例如，如果输入一个新的频率，但当装载被点击后并不生效，用户可能输入新的频率信息后忽视了按回车。

AD9852/AD9854 评估板的正常操作从主复位开始。在此复位之后，寄存器的默认值显示在软件控制面板。复位命令设置 DDS 输出幅度为最小，输出频率 0 赫兹，零相位偏移，以及寄存器布局表上列出的其他状态（AD9854 表 8）。

接下来要编程参考时钟和倍增，因为这些信息被输入计算用来确定适当的 48 位频率调谐字的。

输出幅度默认为乘数寄存器乘 12 位，直接二进制的 I（余弦 DAC）数值为十六进制 000，没有输出（直流）。在输出设置对话框设置最大倍频振幅如 FFF。数字乘法器可以通过选择输出幅度总是最大值而绕过，但这种情况不会得到最好的无杂散动态范围（SFDR）。要实现最好的高达 11 分贝改的 SFDR，必须通过数字乘法器的数乘，然后减少信号的幅度。例如 FC0 与慢幅度输出相比产生更少的杂散信号。如果必须用最大的 SFDR，这一可重复利用的现象，应该在给定的应用中具体研究。在较高的输出频率良好的 SFDR 变得更加难以实现，这种现象更容易观察到。

参见本数据手册和评估电路板原理图，了解 AD9854 可用的软件功能和如何响应命令。

支持

要获得有关 AD9854，AD9854 评估板的 PCB 和所有其他 ADI 产品的技术支持。呼叫 1-800-ANALOGD 或访问 www.analog.com / DDS。