XT32H0xx Family

32-bit MCU based on ARM Cortex®-M0+

1.62~5.5V,8kV ESD,160kB FLASH,32kB SRAM, Capacitive Touch Sensing, LED

The XT32H0xx is a product family designed for harsh environment. In addition to a popular, performance-energy efficient ARM Cortex-M0+ core, the MCU also offer a versatile set of peripherals with robust design and environmental immunity which best suited for home appliances and industrial applications.

1 Features

- Core
  - 32bit ARM Cortex-M0+ core with MPU
  - Frequency up to 96 MHz
- Operation Characterization
  - Operation Temperature: -40℃ ~ 105℃
  - Single Power Supply: 1.62 V ~ 5.5 V
- On-chip Memory
  - 160KB Flash
  - 32KB SRAM
- Clock Source
  - 16MHz IRC oscillator (16 MHz±1%)
  - 4MHz ~ 48MHz Crystal Oscillator
  - internal PLL
  - 32kHz IRC
  - 32kHz Crystal Oscillator
  - high-speed/low-speed external clock
- Operation Modes
  - normal mode
  - idle mode
  - stop mode
  - deep-sleep mode w/ RTC or GPIO wake-up enable
- High performance analog peripherals
  - 12bit 2-Msps ADC，maximum 4 pairs differential-ended channels and 34 single-ended channels
  - 4x gain programmable amplifiers before ADC
  - 4x high-speed analog comparators，reference voltage source configurable (DAC output，bandgap voltage or from chip pins)
- Rich Digital Peripherals
  - 8 Channels DMA Controller
  - Hardware divider
  - CRC8, CRC16, CRC32
  - 14x timers, maximum support 40 single-ended PWM output or 12 pairs diff-ended PWM output and 16 single-ended PWM output
- HMI Interfaces
  - Capacitive Touch Sensing Module
    - dedicated algorithm processing co-processor
    - maximum 32x channels
    - self-capacitance and mutual capacitance
  - 8COMx9SEG LED Drive Unit
    - DMA Supported，fastest 60 frame/s
    - Support DIM and Blink
    - Support lighting mode and dimming mode
    - Maximum 8 digits segment LED, 8x8 LED matrix or 64 LEDs
- Serial Communication Interfaces
  - 4x UART
  - 2x I2C
  - 2x SPI
- Flexible IO
  - maximum 61 GPIO with VDDIO voltage level
- Debug Interface
  - 2-wire SWD debugger
- Packages
  - 64-pin LQFP
  - 48-pin LQFP
  - 44-pin LQFP
  - 32-pin LQFP
- Software/Hardware Platform
  - XT32 Software Development Kit (SDK)
  - XT-Link Debugger/J-Link Debugger
  - Configuration and Code auto-generation GUI tool
  - Compatible with IAR、Keil etc.

2 Applications

- Home appliances
- Industrial control
- General inverters
- PV optimizer
- PV micro-inverters
- Smart circuit breaker
- Uninterruptible power supplies
- Industrial sensors and actuators
- Sensor or sensor-less BLDC/PMSM Motor driver

3 Description

XT32H0xx family microcontrollers (MCUs) are part of the XTX highly integrated, ultra-low-power 32-bit MCU based on the enhanced 32-bit Arm® Cortex®-M0+ core platform operating at up to 96-MHz frequency. These cost-optimized MCUs offer high-performance analog peripheral integration, support extended temperature ranges from -40°C to 105°C, and operate with supply voltages ranging from 1.62 V to 5.5 V.

The XT32H0xx devices provide up to 160kB embedded flash program memory and up to 32kB SRAM. The devices also incorporate an 8-channel DMA, and a variety of high-performance analog peripherals such as four high speed rail-to-rail analog comparators, a 12-bit 2-Msps ADCs, configurable internal shared voltage reference and four pairs of differential programmable gain amplifiers. These devices also offer intelligent digital peripherals such as two 16-bit advanced control timers, four general purpose timers, two windowed-watchdog timers, and one RTC with alarm and calendar mode. These devices provide data integrity peripherals (CRC8, CRC16, CRC32), enhanced communication interfaces (four UART, two I2C, two SPI) and human machine interfaces (Capacitance Touch Sensing and LED Driver).

The XT32H0xx family of low-power MCUs consists of devices with varying degrees of analog and digital integration allowing for customers find the MCU that meets their project's needs. The XT32 MCU platform combines the Arm Cortex-M0+ platform with a holistic ultra-low-power system architecture, allowing system designers to increase performance while reducing energy consumption.

XT32H0xx MCUs are supported by an extensive hardware and software ecosystem with reference designs and code examples to get the design started quickly. XTX provides a free Software Development Kit (SDK), which is available for IAR, Keil and GCC based tool-chains.

For complete module descriptions, refer to XT32H0 Family Microcontrollers Technical Reference Manual and Programming Reference Manual.

4 Configuration Summary

Table 1 XT32H0xx Common Features

Core	ARM Cortex-M0+
Max. Frequency	96 MHz
Voltage range	1.62V - 5.5V
Temperature range	-40℃ - 105℃
Debug interface	SWD
Hardware divider	Yes
Sys-tick timer	1
Deep-sleep wakeup timer	1
Window watchdog(WWDT)	1
Independent watchdog(IWDT)	1
Real-time Counter(RTC)	1
DMA channels	8
Data integrity check(CRC)	CRC8/16/32
Power-on Reset(POR)	Yes
Programmable voltage detector(PVD)	Yes
External Interrupt line(EXTI)	16
Oscillators(OSC)	16MHz internal RC oscillator(HSI) 4-48MHz crystal oscillator(HSE) 32kHz internal RC oscillator(LSI) 32kHz crystal oscillator(LSE) 96MHz fractional digital phased locked loop(PLL)
Basic timer	2
ADC instances	1
DAC instances	1
Comparators	4
Programmable-gain amplifier(PGA)	4
UART	4
I2C	2
SPI	2

Table 2 XT32H0xx Specific Features

OPN	Series	Flash (KB)	SRAM (KB)	Package	GPIOs	TIM A/G/B	LED SEG x COM	CTSU Chx	ADC Chx diff/single	PWM Chx diff/single	PFC Accelerator	Math Accelerator
XT32H051B8L5	touch control	160	32	LQFP32	29	1/1/2	8 x 9	18	4/10	3/7	-	-
XT32H051C8L5	touch control	160	32	LQFP44	41	2/4/2	8 x 9	28	4/19	5/12	-	-
XT32H051D8L5	touch control	160	32	LQFP48	45	2/4/2	8 x 9	32	4/23	7/14	-	-
XT32H051F8L5	touch control	160	32	LQFP64	61	2/4/2	8 x 9	32	4/36	12/18	-	-
XT32H051B7L5	touch control	128	32	LQFP32	29	1/1/2	8 x 9	18	4/10	3/7	-	-
XT32H051C7L5	touch control	128	32	LQFP44	41	2/4/2	8 x 9	28	4/19	5/12	-	-
XT32H051D7L5	touch control	128	32	LQFP48	45	2/4/2	8 x 9	32	4/23	7/14	-	-
XT32H051F7L5	touch control	128	32	LQFP64	61	2/4/2	8 x 9	32	4/36	12/18	-	-
XT32H051B6L5	touch control	96	16	LQFP32	29	1/1/2	8 x 9	18	4/10	3/7	-	-
XT32H051C6L5	touch control	96	16	LQFP44	41	2/4/2	8 x 9	28	4/19	5/12	-	-
XT32H051D6L5	touch control	96	16	LQFP48	45	2/4/2	8 x 9	32	4/23	7/14	-	-
XT32H051F6L5	touch control	96	16	LQFP64	61	2/4/2	8 x 9	32	4/36	12/18	-	-
XT32H051B5L5	touch control	64	16	LQFP32	29	1/1/2	8 x 9	18	4/10	3/7	-	-
XT32H051C5L5	touch control	64	16	LQFP44	41	2/4/2	8 x 9	28	4/19	5/12	-	-
XT32H051D5L5	touch control	64	16	LQFP48	45	2/4/2	8 x 9	32	4/23	7/14	-	-
XT32H051F5L5	touch control	64	16	LQFP64	61	2/4/2	8 x 9	32	4/36	12/18	-	-
XT32H053B8L5	motor control	160	32	LQFP32	29	1/1/2	8 x 9	-	4/10	3/7	Yes	Yes
XT32H053C8L5	motor control	160	32	LQFP44	41	2/4/2	8 x 9	-	4/19	5/12	Yes	Yes
XT32H053D8L5	motor control	160	32	LQFP48	45	2/4/2	8 x 9	-	4/23	7/14	Yes	Yes
XT32H053F8L5	motor control	160	32	LQFP64	61	2/4/2	8 x 9	-	4/36	12/18	Yes	Yes
XT32H053B7L5	motor control	128	32	LQFP32	29	1/1/2	8 x 9	-	4/10	3/7	Yes	Yes
XT32H053C7L5	motor control	128	32	LQFP44	41	2/4/2	8 x 9	-	4/19	5/12	Yes	Yes
XT32H053D7L5	motor control	128	32	LQFP48	45	2/4/2	8 x 9	-	4/23	7/14	Yes	Yes
XT32H053F7L5	motor control	128	32	LQFP64	61	2/4/2	8 x 9	-	4/36	12/18	Yes	Yes
XT32H053B6L5	motor control	96	16	LQFP32	29	1/1/2	8 x 9	-	4/10	3/7	Yes	Yes
XT32H053C6L5	motor control	96	16	LQFP44	41	2/4/2	8 x 9	-	4/19	5/12	Yes	Yes
XT32H053D6L5	motor control	96	16	LQFP48	45	2/4/2	8 x 9	-	4/23	7/14	Yes	Yes
XT32H053F6L5	motor control	96	16	LQFP64	61	2/4/2	8 x 9	-	4/36	12/18	Yes	Yes
XT32H053B5L5	motor control	64	16	LQFP32	29	1/1/2	8 x 9	-	4/10	3/7	Yes	Yes
XT32H053C5L5	motor control	64	16	LQFP44	41	2/4/2	8 x 9	-	4/19	5/12	Yes	Yes
XT32H053D5L5	motor control	64	16	LQFP48	45	2/4/2	8 x 9	-	4/23	7/14	Yes	Yes
XT32H053F5L5	motor control	64	16	LQFP64	61	2/4/2	8 x 9	-	4/36	12/18	Yes	Yes

5 Functional Block Diagram

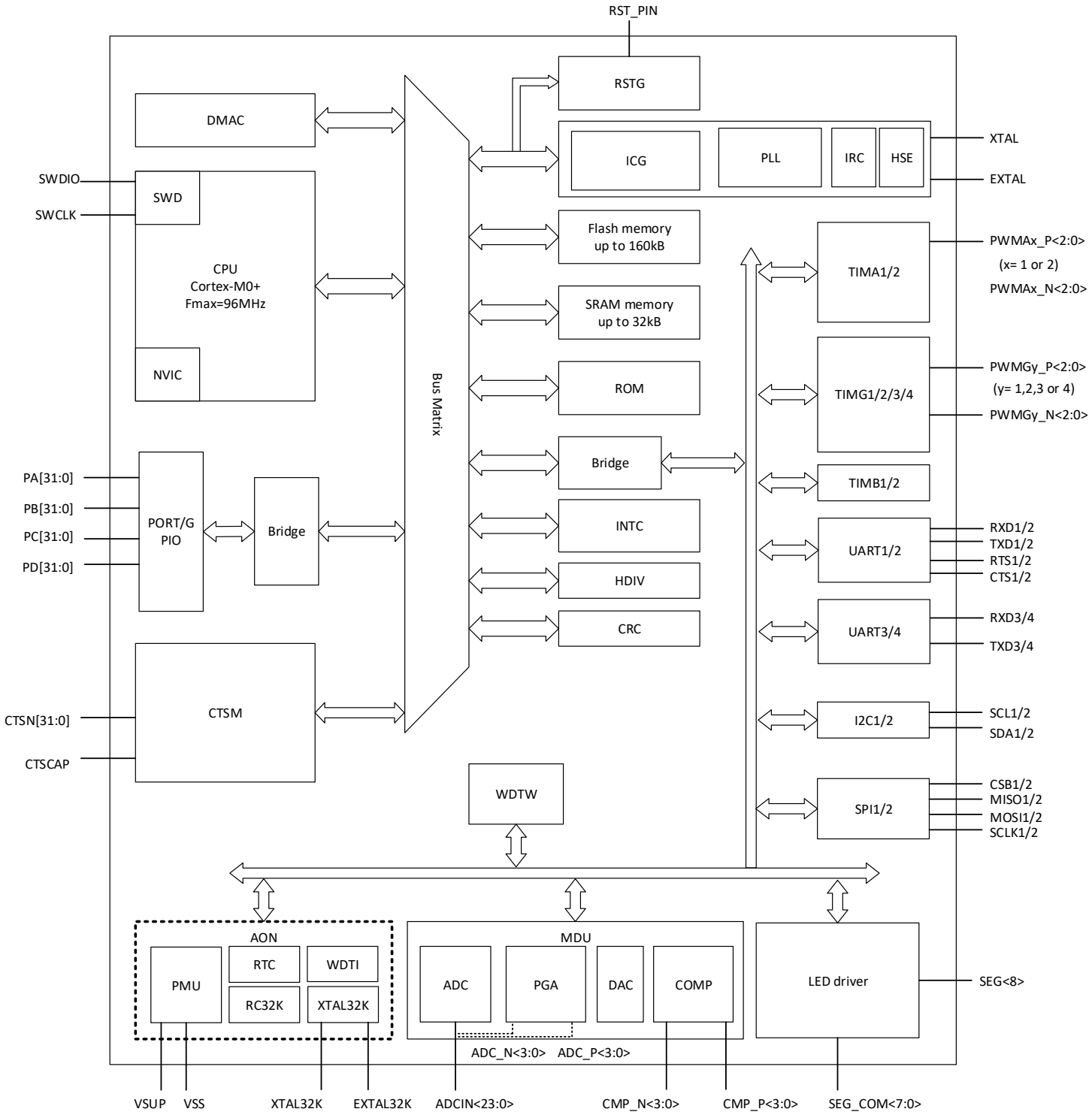

Figure 1 XT32H051 Functional Block Diagram

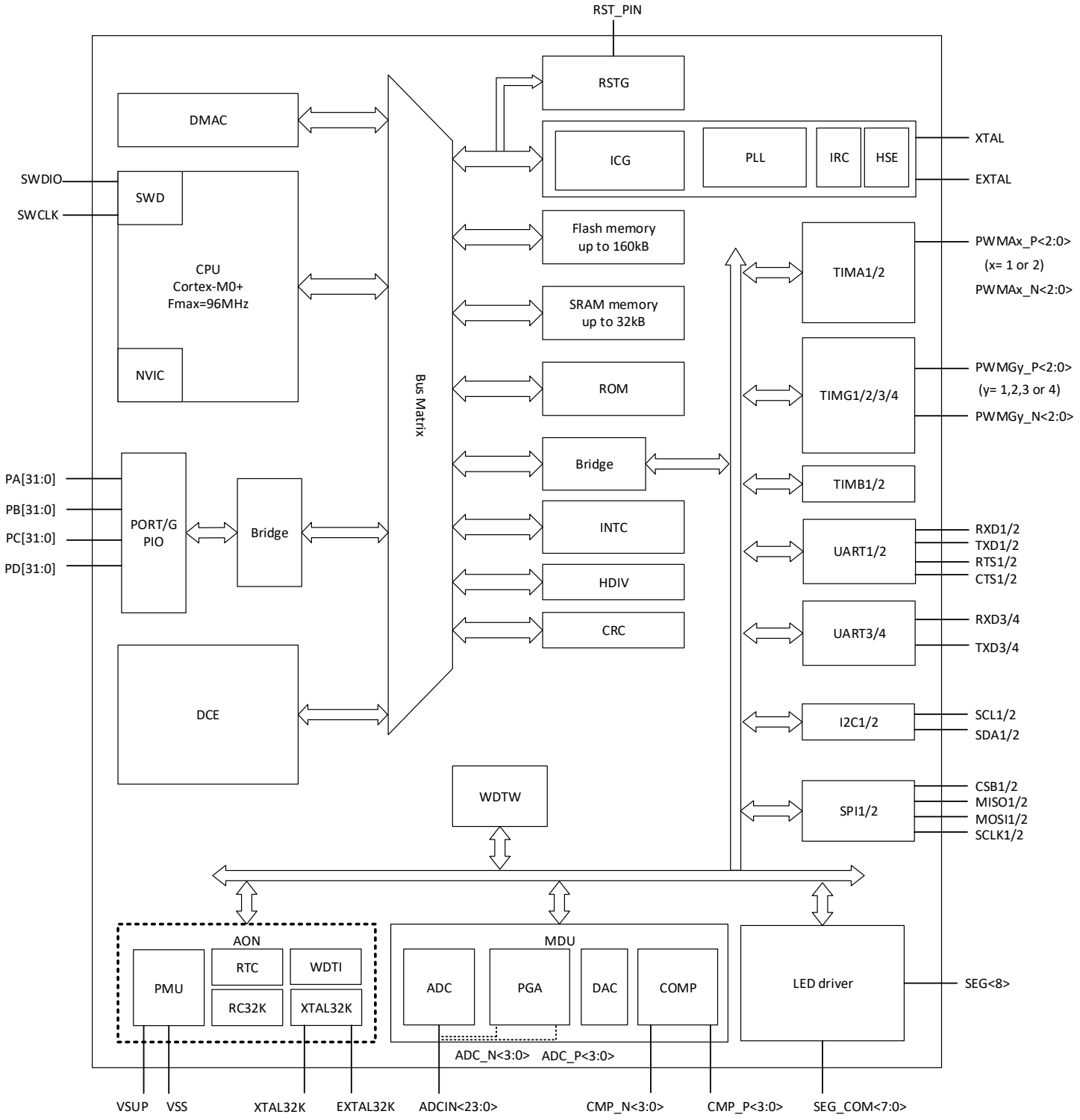

Figure 2 XT32H053 Functional Block Diagram

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6 Pinouts and alternate functions

6.1 Pinouts Diagram

6.1.1 XT32H051Fx (LQFP64) pinouts diagram

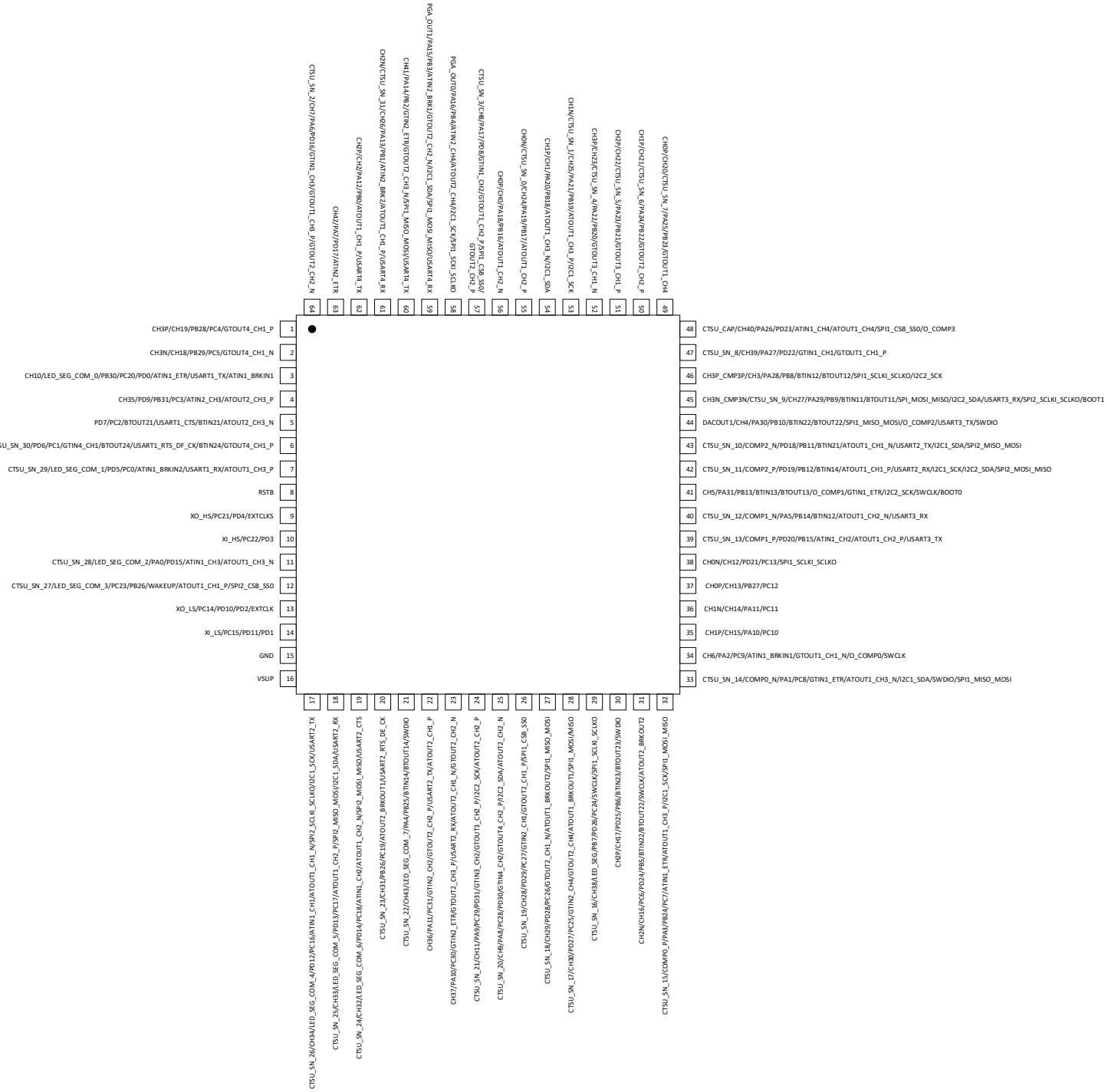


Figure 3 XT32H051Fx LQFP64 pinout

6.1.2 XT32H051Dx (LQFP48) pinouts diagram

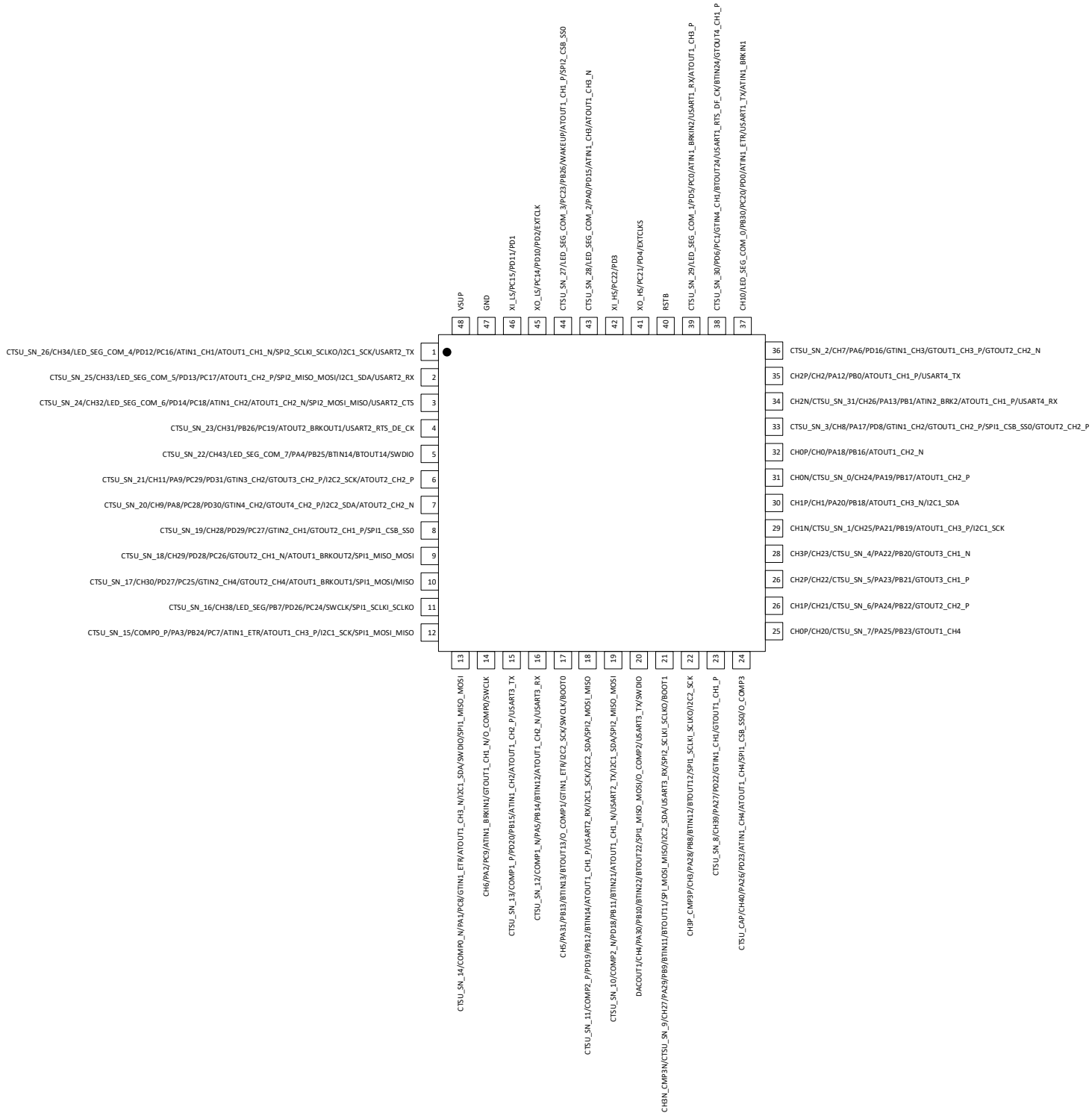


Figure 4 XT32H051Dx LQFP48 pinout

6.1.3 XT32H051Cx (LQFP44) pinouts diagram

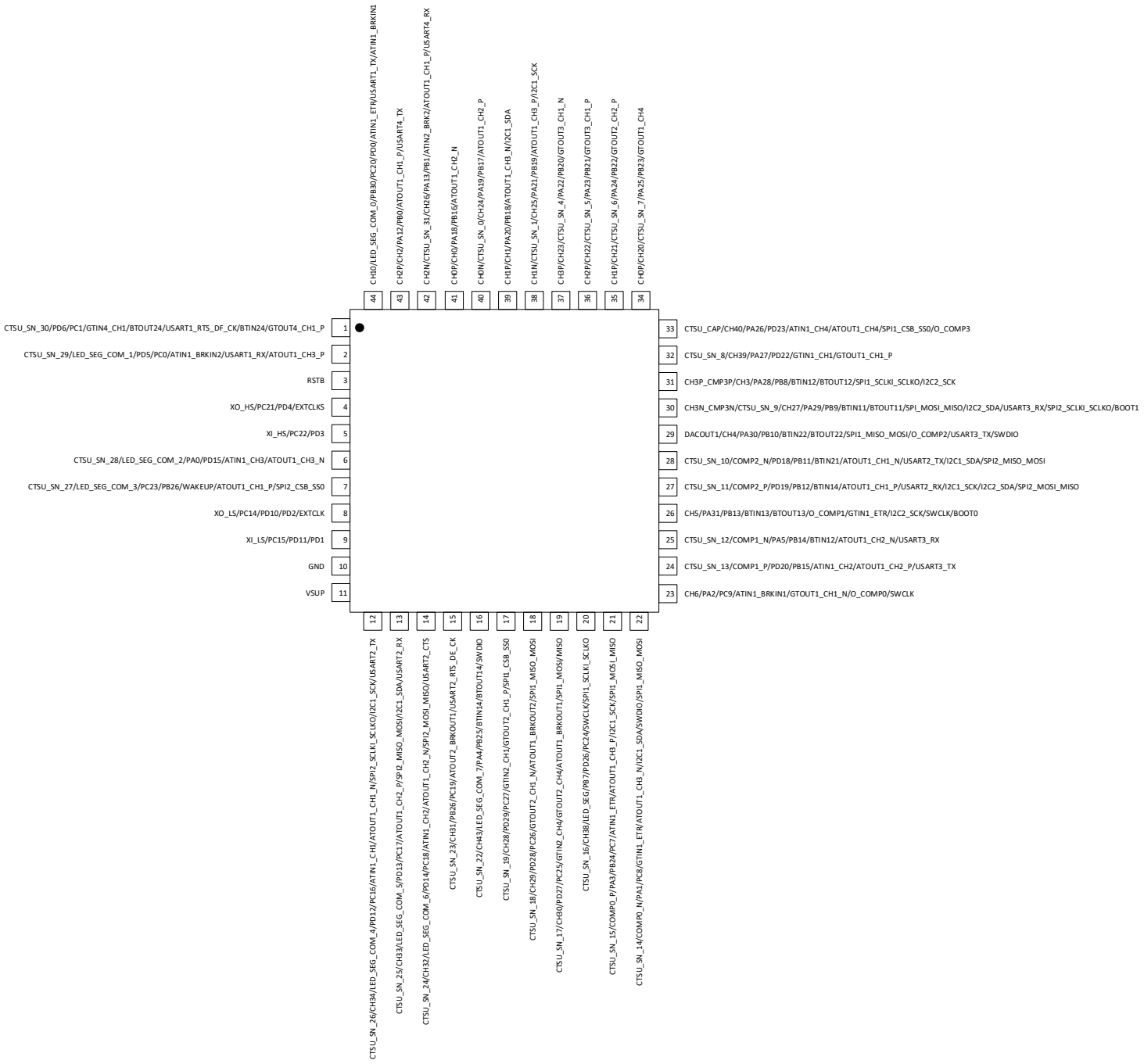


Figure 5 XT32H051Cx LQFP44 pinout

6.1.4 XT32H051Bx (LQFP32) pinouts diagram

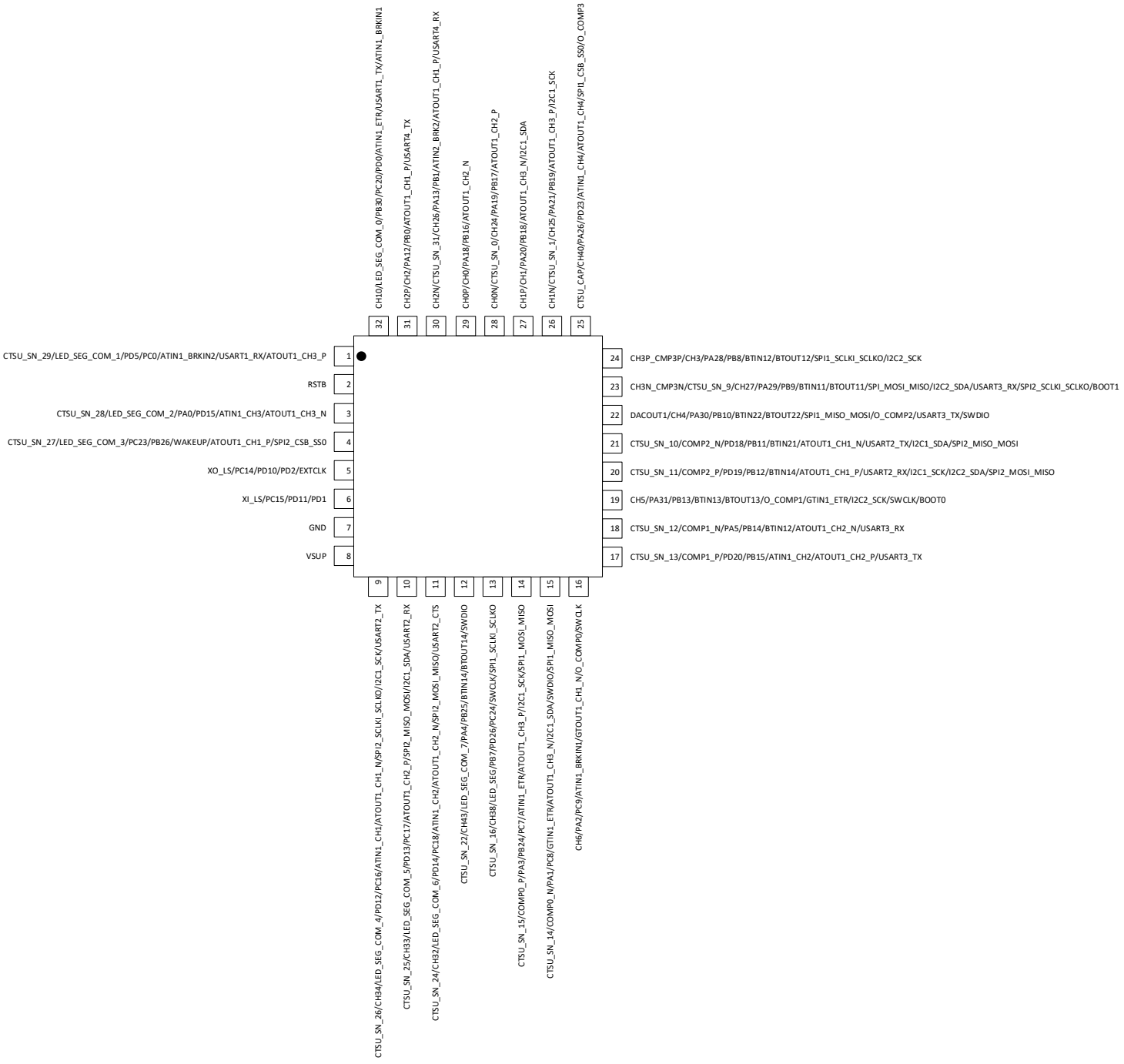


Figure 6 XT32H051Bx LQFP32 pinout

6.1.5 XT32H053Fx (LQFP64) pinouts diagram

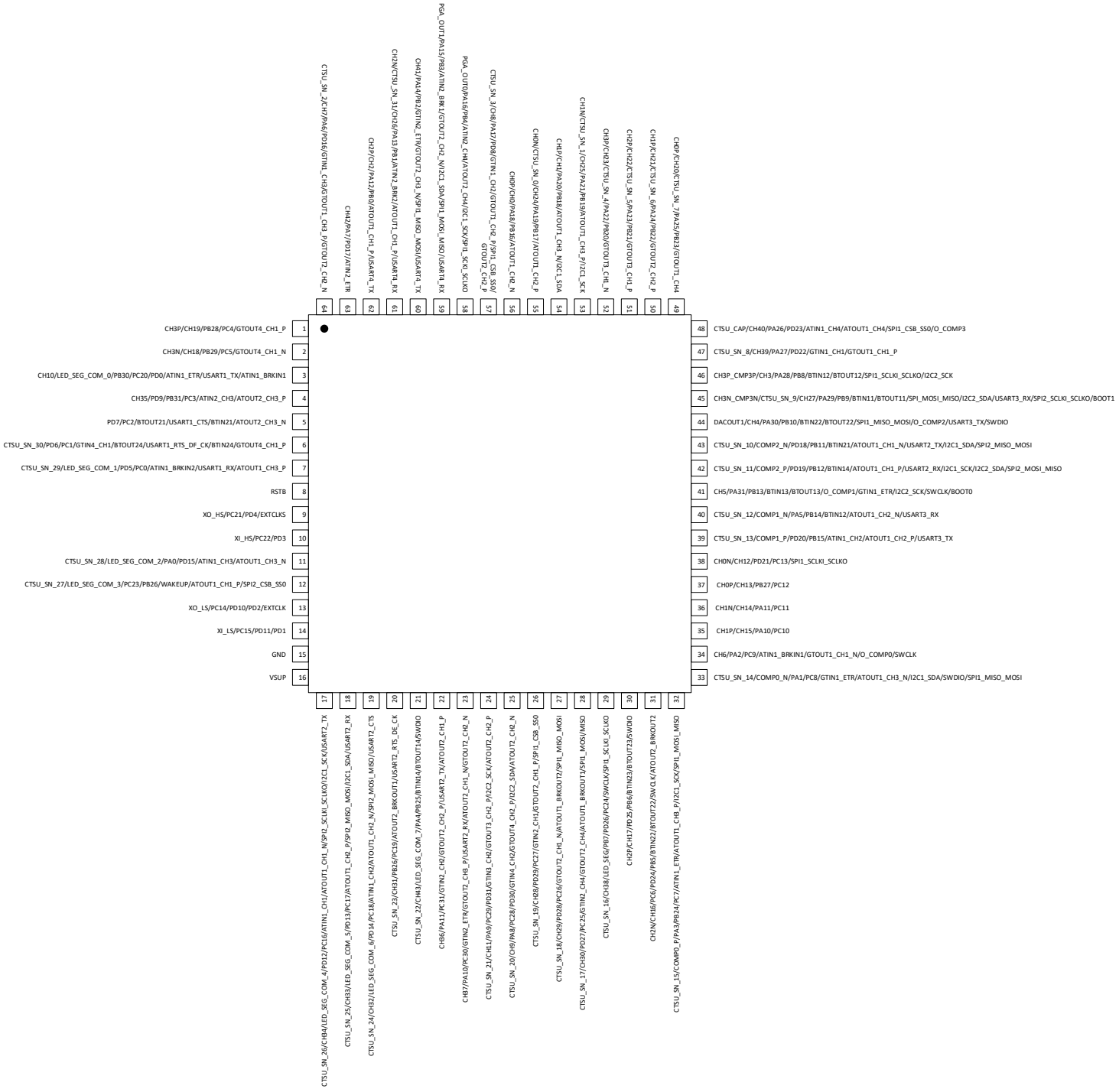


Figure 7 XT32H053Fx LQFP64 pinout

6.1.6 XT32H053Dx (LQFP48) pinouts diagram

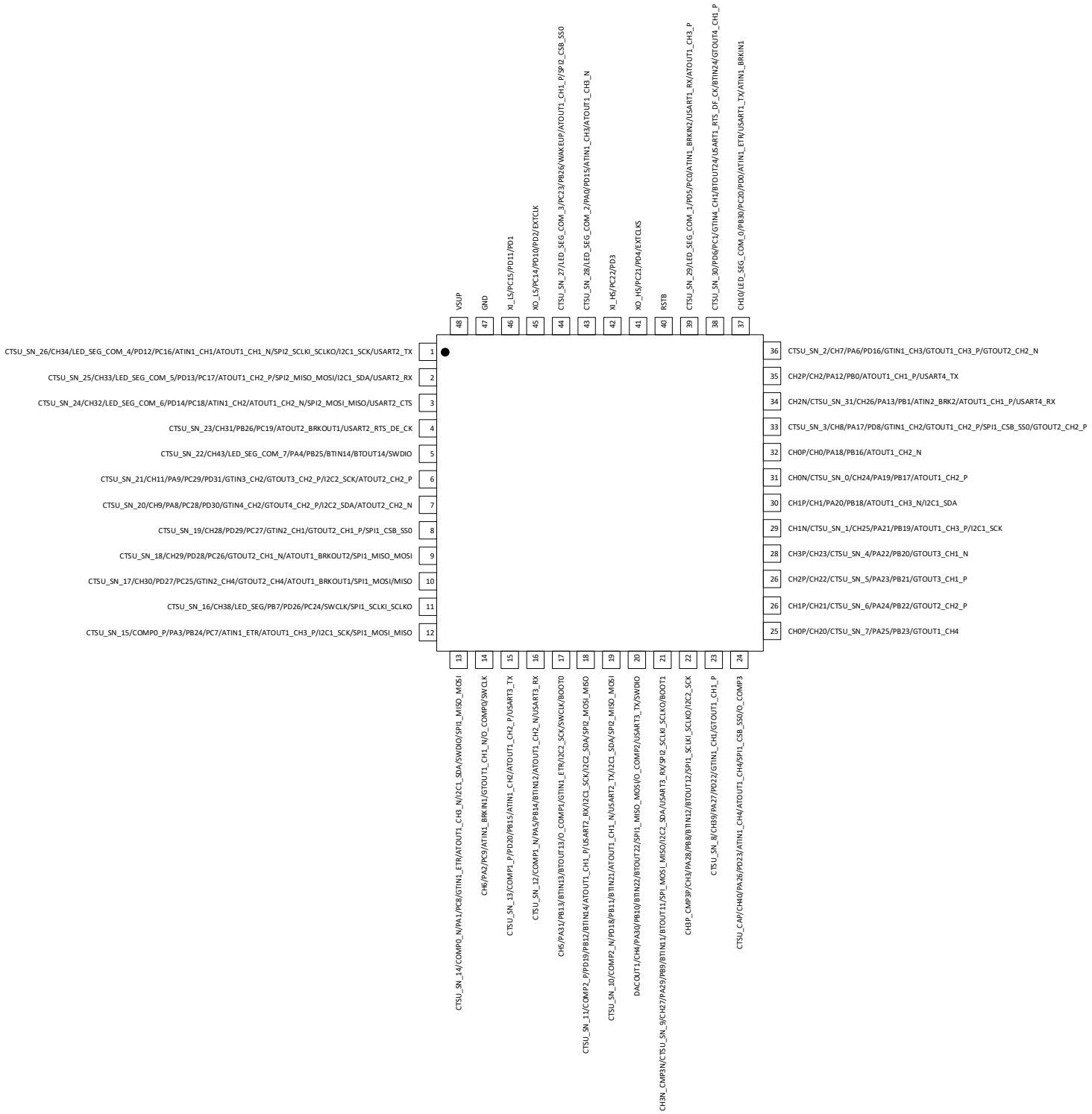


Figure 8 XT32H053Dx LQFP48 pinout

6.1.7 XT32H053Cx (LQFP44) pinouts diagram

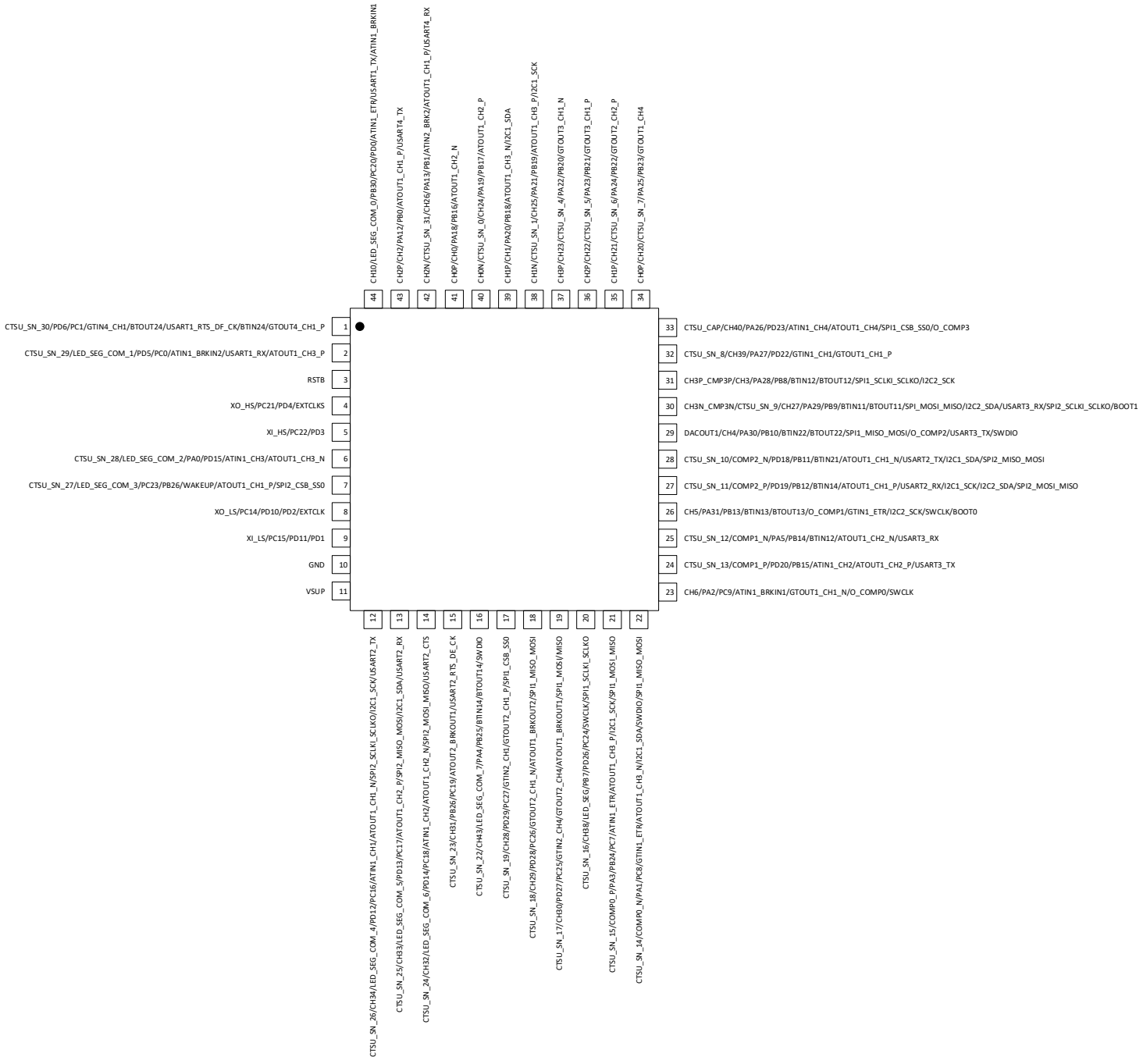


Figure 9 XT32H053Cx LQFP44 pinout

6.1.8 XT32H053Bx (LQFP32) pinouts diagram

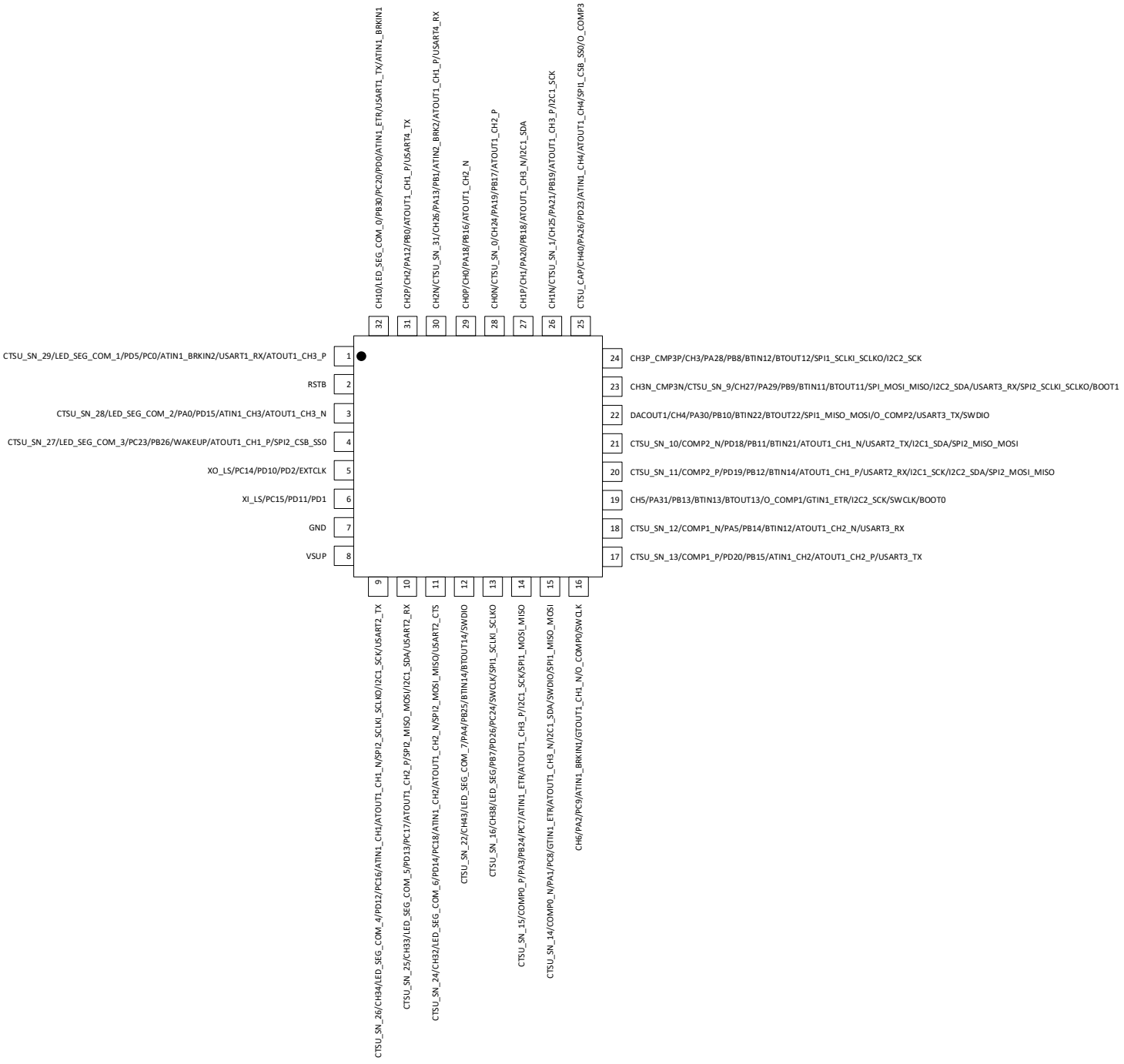


Figure 10 XT32H053Bx LQFP32 pinout

6.2 Pin List

6.2.1 XT32H051Fx (LQFP64) Pin List

Table 3 Pin list of XT32H051Fx

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	PGA	ADC	CMP	LED	Touch	XTAL
61	1		High-Z		PB28	PC4		GTO4_CH1P							CH3P/CH19				
62	2		High-Z		PB29	PC5		GTO4_CH1N							CH3N/CH18				
1	3		UART1_TX		PB30	PC20	PD0			UART1_TX					CH10		LED0		
2	4		High-Z		PB31	PC3	PD9								CH35				
3	5		High-Z			PC2	PD7		BTIN21 BTOUT21	UART1_CTS									
4	6		High-Z			PC1	PD6	GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS								CTSU30	
5	7		UART1_RX			PC0	PD5			UART1_RX							LED1	CTSU29	
6	8	RSTB	RSTB																
7	9		High-Z			PC21	PD4												XO_HS EXCLK_HS
8	10		High-Z			PC22	PD3												XI_HS
9	11		High-Z	PA0			PD15										LED2	CTSU28	
10	12		High-Z		PB26	PC23					SPI2_CSB						LED3	CTSU27	
11	13		High-Z			PC14	PD2/ PD10												XO_LS EXCLK_LS
12	14		High-Z			PC15	PD1/ PD11												XI_LS
-	15	GND	GND																
-	16	VSUP	VSUP																
13	17		High-Z			PC16	PD12			UART2_TX	SPI2_SCLK	I2C1_SCLK			CH34		LED4	CTSU26	
14	18		High-Z			PC17	PD13			UART2_RX	SPI2_MISO	I2C1_SDA			CH33		LED5	CTSU25	
15	19		High-Z			PC18	PD14			UART2_CTS	SPI2_MOSI				CH32		LED6	CTSU24	
16	20		High-Z		PB26	PC19				UART2_RTS					CH31			CTSU23	
17	21		High-Z	PA4	PB25				BTIN14/ BTOUT14				SWDIO		CH43		LED7	CTSU22	
18	22		High-Z	PA11		PC31		GTO2_CH2P GTIN2_CH2		UART2_TX					CH36				
19	23		High-Z	PA10		PC30		GTO2_CH2N GTO2_CH3P GTIN2_ETR		UART2_RX					CH37				
20	24		High-Z	PA9		PC29	PD31	GTO3_CH2P GTIN3_CH2				I2C2_SCK			CH11			CTSU21	
21	25		High-Z	PA8		PC28	PD30	GTO4_CH2P GTIN4_CH2				I2C2_SDA			CH9			CTSU20	
22	26		High-Z			PC27	PD29	GTO2_CH1P GTIN2_CH1			SPI1_CSB				CH28			CTSU19	
23	27		High-Z			PC26	PD28	GTO2_CH1N			SPI1_MISO				CH29			CTSU18	
24	28		High-Z			PC25	PD27	GTO2_CH4 GTIN2_CH4			SPI1_MOSI				CH30			CTSU17	
25	29		High-Z		PB7	PC24	PD26				SPI1_SCLK		SWCLK		CH38		LED8	CTSU16	
26	30		High-Z		PB6		PD25		BTIN23 BTOUT23				SWDIO		CH2P/CH17				
27	31		High-Z		PB5	PC6	PD24		BTIN22 BTOUT22				SWCLK		CH2N/CH16				
28	32		High-Z		PB24	PC7	PA3				SPI1_MOSI	I2C1_SCK				CMP0P		CTSU15	
29	33		High-Z	PA1		PC8		GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO			CMP0N		CTSU14	
30	34		High-Z	PA2		PC9		GTO1_CH1N					SWCLK		CH6				

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	PGA	ADC	CMP	LED	Touch	XTAL
31	35		High-Z	PA10		PC10									CH1P/CH15				
32	36		High-Z	PA11		PC11									CH1N/CH14				
33	37		High-Z		PB27	PC12									CH0P/CH13				
34	38		High-Z			PC13	PD21				SPI1_SCLK				CH0N/CH12				
35	39		High-Z		PB15		PD20			UART3_TX						CMP1P		CTSU13	
36	40		High-Z	PA5	PB14				BTIN12	UART3_RX	SPI2_CSB					CMP1N		CTSU12	
37	41	BOOT0	SWCLK	PA31	PB13			GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK		CH5	OCMP1			
38	42		High-Z		PB12		PD19		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA				CMP2P		CTSU11	
39	43		High-Z		PB11		PD18		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA				CMP2N		CTSU10	
40	44		SWDIO	PA30	PB10				BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO		CH4	OCMP2			
41	45	BOOT1	High-Z	PA29	PB9				BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA			CH3N/CH27	CMP3N		CTSU9	
42	46		High-Z	PA28	PB8				BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK			CH3P/CH3	CMP3P			
43	47		High-Z	PA27			PD22	GTO1_CH1P GTIN1_CH1							CH39			CTSU8	
44	48		High-Z	PA26			PD23				SPI1_CSB				CH40	OCMP3		CTSUCAP	
45	49		High-Z	PA25			PB23	GTO1_CH4							CH0P/CH20			CTSU7	
46	50		High-Z	PA24	PB22			GTO2_CH2P							CH1P/CH21			CTSU6	
47	51		High-Z	PA23	PB21			GTO3_CH1P							CH2P/CH22			CTSU5	
48	52		High-Z	PA22	PB20			GTO3_CH1N							CH3P/CH23			CTSU4	
49	53		High-Z	PA21	PB19							I2C1_SCK			CH1N/CH25			CTSU1	
50	54		High-Z	PA20	PB18							I2C1_SDA			CH1P/CH1				
51	55		High-Z	PA19	PB17										CH0N/CH24			CTSU0	
52	56		High-Z	PA18	PB16										CH0P/CH0				
53	57		High-Z	PA17			PD8	GTO1_CH2P GTO2_CH2P GTIN1_CH2			SPI1_CSB				CH8			CTSU3	
54	58		High-Z	PA16	PB4						SPI1_SCK	I2C1_SCK		PGA_OUT0					
55	59		High-Z	PA15	PB3			GTO2_CH2N		UART4_RX	SPI1_MOSI	I2C1_SDA		PGA_OUT1					
56	60		High-Z	PA14	PB2			GTO2_CH3N GTIN2_ETR		UART4_TX	SPI1_MISO				CH41				
57	61		High-Z	PA13	PB1					UART4_RX					CH2N/CH26			CTSU31	
58	62		High-Z	PA12	PB0					UART4_TX					CH2P/CH2				
59	63		High-Z	PA7			PD17								CH42				
60	64		High-Z	PA6			PD16	GTO1_CH3P GTO2_CH2N GTIN1_CH3							CH7			CTSU2	

6.2.2 XT32H051Fx (LQFP48) Pin List

Table 4 Pin list of XT32H051Dx

IO_ID	Pin #	Default Function		Alternative Function														
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	37		UART1_TX		PB30	PC20	PD0			UART1_TX				CH10		LED0		
4	38		High-Z			PC1	PD6	GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS							CTSU30	
5	39		UART1_RX			PC0	PD5			UART1_RX						LED1	CTSU29	
6	40	RSTB	RSTB															
7	41		High-Z			PC21	PD4											XO_HS EXCLK_HS
8	42		High-Z			PC22	PD3											XI_HS
9	43		High-Z	PA0			PD15									LED2	CTSU28	
10	44		High-Z		PB26	PC23					SPI2_CSB					LED3	CTSU27	
11	45		High-Z			PC14	PD2/ PD10											XO_LS EXCLK_LS
12	46		High-Z			PC15	PD1/ PD11											XI_LS
-	47	GND	GND															
-	48	VSUP	VSUP															
13	1		High-Z			PC16	PD12			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	2		High-Z			PC17	PD13			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	3		High-Z			PC18	PD14			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
16	4		High-Z		PB26	PC19				UART2_RTS				CH31			CTSU23	
17	5		High-Z	PA4	PB25				BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
20	6		High-Z	PA9		PC29	PD31	GTO3_CH2P GTIN3_CH2				I2C2_SCK		CH11			CTSU21	
21	7		High-Z	PA8		PC28	PD30	GTO4_CH2P GTIN4_CH2				I2C2_SDA		CH9			CTSU20	
22	8		High-Z			PC27	PD29	GTO2_CH1P GTIN2_CH1			SPI1_CSB			CH28			CTSU19	
23	9		High-Z			PC26	PD28	GTO2_CH1N			SPI1_MISO			CH29			CTSU18	
24	10		High-Z			PC25	PD27	GTO2_CH4 GTIN2_CH4			SPI1_MOSI			CH30			CTSU17	
25	11		High-Z		PB7	PC24	PD26				SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	12		High-Z		PB24	PC7	PA3				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	13		High-Z	PA1		PC8		GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	14		High-Z	PA2		PC9		GTO1_CH1N					SWCLK	CH6				
35	15		High-Z		PB15		PD20			UART3_TX					CMP1P		CTSU13	
36	16		High-Z	PA5	PB14				BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	17	BOOT0	SWCLK	PA31	PB13			GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	18		High-Z		PB12		PD19		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	19		High-Z		PB11		PD18		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	20		SWDIO	PA30	PB10				BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	21	BOOT1	High-Z	PA29	PB9				BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	

IO_ID	Pin #	Default Function		Alternative Function													
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
42	22		High-Z	PA28	PB8				BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
43	23		High-Z	PA27			PD22	GTO1_CH1P GTIN1_CH1						CH39			CTSU8	
44	24		High-Z	PA26			PD23				SPI1_CSB			CH40	OCMP3		CTSUCAP	
45	25		High-Z	PA25			PB23	GTO1_CH4						CH0P/CH20			CTSU7	
46	26		High-Z	PA24	PB22			GTO2_CH2P						CH1P/CH21			CTSU6	
47	27		High-Z	PA23	PB21			GTO3_CH1P						CH2P/CH22			CTSU5	
48	28		High-Z	PA22	PB20			GTO3_CH1N						CH3P/CH23			CTSU4	
49	29		High-Z	PA21	PB19							I2C1_SCK		CH1N/CH25			CTSU1	
50	30		High-Z	PA20	PB18							I2C1_SDA		CH1P/CH1				
51	31		High-Z	PA19	PB17									CH0N/CH24			CTSU0	
52	32		High-Z	PA18	PB16									CH0P/CH0				
53	33		High-Z	PA17			PD8	GTO1_CH2P GTO2_CH2P GTIN1_CH2			SPI1_CSB			CH8			CTSU3	
57	34		High-Z	PA13	PB1					UART4_RX				CH2N/CH26			CTSU31	
58	35		High-Z	PA12	PB0					UART4_TX				CH2P/CH2				
60	36		High-Z	PA6			PD16	GTO1_CH3P GTO2_CH2N GTIN1_CH3						CH7			CTSU2	

6.2.3 XT32H051Cx (LQFP44) Pin List

Table 5 Pin list of XT32H051Cx

IO_ID	Pin #	Default Function		Alternative Function														
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	44		UART1_TX		PB30	PC20	PD0			UART1_TX				CH10		LED0		
4	1		High-Z			PC1	PD6	GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS							CTSU30	
5	2		UART1_RX			PC0	PD5			UART1_RX						LED1	CTSU29	
6	3	RSTB	RSTB															
7	4		High-Z			PC21	PD4											XO_HS EXCLK_HS
8	5		High-Z			PC22	PD3											XI_HS
9	6		High-Z	PA0			PD15									LED2	CTSU28	
10	7		High-Z		PB26	PC23					SPI2_CSB					LED3	CTSU27	
11	8		High-Z			PC14	PD2/ PD10											XO_LS EXCLK_LS
12	9		High-Z			PC15	PD1/ PD11											XI_LS
-	10	GND	GND															
-	11	VSUP	VSUP															
13	12		High-Z			PC16	PD12			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	13		High-Z			PC17	PD13			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	14		High-Z			PC18	PD14			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
16	15		High-Z		PB26	PC19				UART2_RTS				CH31			CTSU23	
17	16		High-Z	PA4	PB25				BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
22	17		High-Z			PC27	PD29	GTO2_CH1P GTIN2_CH1			SPI1_CSB			CH28			CTSU19	
23	18		High-Z			PC26	PD28	GTO2_CH1N			SPI1_MISO			CH29			CTSU18	
24	19		High-Z			PC25	PD27	GTO2_CH4 GTIN2_CH4			SPI1_MOSI			CH30			CTSU17	
25	20		High-Z		PB7	PC24	PD26				SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	21		High-Z		PB24	PC7	PA3				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	22		High-Z	PA1		PC8		GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	23		High-Z	PA2		PC9		GTO1_CH1N					SWCLK	CH6				
35	24		High-Z		PB15		PD20			UART3_TX					CMP1P		CTSU13	
36	25		High-Z	PA5	PB14				BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	26	BOOT0	SWCLK	PA31	PB13			GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	27		High-Z		PB12		PD19		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	28		High-Z		PB11		PD18		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	29		SWDIO	PA30	PB10				BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	30	BOOT1	High-Z	PA29	PB9				BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	
42	31		High-Z	PA28	PB8				BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
43	32		High-Z	PA27			PD22	GTO1_CH1P GTIN1_CH1						CH39			CTSU8	

IO_ID	Pin #	Default Function		Alternative Function													
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
44	33		High-Z	PA26			PD23				SPI1_CSB			CH40	OCMP3		CTSUCAP	
45	34		High-Z	PA25			PB23	GTO1_CH4						CH0P/CH20			CTSU7	
46	35		High-Z	PA24	PB22			GTO2_CH2P						CH1P/CH21			CTSU6	
47	36		High-Z	PA23	PB21			GTO3_CH1P						CH2P/CH22			CTSU5	
48	37		High-Z	PA22	PB20			GTO3_CH1N						CH3P/CH23			CTSU4	
49	38		High-Z	PA21	PB19							I2C1_SCK		CH1N/CH25			CTSU1	
50	39		High-Z	PA20	PB18							I2C1_SDA		CH1P/CH1				
51	40		High-Z	PA19	PB17									CH0N/CH24			CTSU0	
52	41		High-Z	PA18	PB16									CH0P/CH0				
57	42		High-Z	PA13	PB1					UART4_RX				CH2N/CH26			CTSU31	
58	43		High-Z	PA12	PB0					UART4_TX				CH2P/CH2				

6.2.4 XT32H051Fx (LQFP32) Pin List

Table 6 Pin list of XT32H051Bx

IO_ID	Pin #	Default Function		Alternative Function														
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	32		UART1_TX		PB30	PC20	PD0			UART1_TX				CH10		LED0		
5	1		UART1_RX			PC0	PD5			UART1_RX						LED1	CTSU29	
6	2	RSTB	RSTB															
9	3		High-Z	PA0			PD15									LED2	CTSU28	
10	4		High-Z		PB26	PC23					SPI2_CSB					LED3	CTSU27	
11	5		High-Z			PC14	PD2/ PD10											XO_LS EXCLK_LS
12	6		High-Z			PC15	PD1/ PD11											XI_LS
-	7	GND	GND															
-	8	VSUP	VSUP															
13	9		High-Z			PC16	PD12			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	10		High-Z			PC17	PD13			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	11		High-Z			PC18	PD14			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
17	12		High-Z	PA4	PB25				BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
25	13		High-Z		PB7	PC24	PD26				SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	14		High-Z		PB24	PC7	PA3				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	15		High-Z	PA1		PC8		GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	16		High-Z	PA2		PC9		GTO1_CH1N					SWCLK	CH6				
35	17		High-Z		PB15		PD20			UART3_TX					CMP1P		CTSU13	
36	18		High-Z	PA5	PB14				BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	19	BOOT0	SWCLK	PA31	PB13			GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	20		High-Z		PB12		PD19		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	21		High-Z		PB11		PD18		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	22		SWDIO	PA30	PB10				BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	23	BOOT1	High-Z	PA29	PB9				BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	
42	24		High-Z	PA28	PB8				BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
44	25		High-Z	PA26			PD23				SPI1_CSB			CH40	OCMP3		CTSUCAP	
49	26		High-Z	PA21	PB19							I2C1_SCK		CH1N/CH25			CTSU1	
50	27		High-Z	PA20	PB18							I2C1_SDA		CH1P/CH1				
51	28		High-Z	PA19	PB17									CH0N/CH24			CTSU0	
52	29		High-Z	PA18	PB16									CH0P/CH0				
57	30		High-Z	PA13	PB1					UART4_RX				CH2N/CH26			CTSU31	
58	31		High-Z	PA12	PB0					UART4_TX				CH2P/CH2				

6.2.5 XT32H053Fx (LQFP64) Pin List

Table 7 Pinouts of XT32H053Fx

IO_ID	Pin #	Default Function		Alternative Function																
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	PGA	ADC	CMP	LED	Touch	XTAL
61	1		High-Z		PB28	PC4			GTO4_CH1P							CH3P/CH19				
62	2		High-Z		PB29	PC5			GTO4_CH1N							CH3N/CH18				
1	3		UART1_TX		PB30	PC20	PD0	ATIN1_ETR ATIN1_BRK1			UART1_TX					CH10		LED0		
2	4		High-Z		PB31	PC3	PD9	ATO2_CH3P ATIN2_CH3								CH35				
3	5		High-Z			PC2	PD7	ATO2_CH3N		BTIN21 BTOUT21	UART1_CTS									
4	6		High-Z			PC1	PD6		GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS								CTSU30	
5	7		UART1_RX			PC0	PD5	ATO1_CH3P ATIN1_BRK2			UART1_RX							LED1	CTSU29	
6	8	RSTB	RSTB																	
7	9		High-Z			PC21	PD4													XO_HS EXCLK_HS
8	10		High-Z			PC22	PD3													XI_HS
9	11		High-Z	PA0			PD15	ATO1_CH3N ATIN1_CH3										LED2	CTSU28	
10	12		High-Z		PB26	PC23		ATO1_CH1P				SPI2_CSB						LED3	CTSU27	
11	13		High-Z			PC14	PD2/ PD10													XO_LS EXCLK_LS
12	14		High-Z			PC15	PD1/ PD11													XI_LS
-	15	GND	GND																	
-	16	VSUP	VSUP																	
13	17		High-Z			PC16	PD12	ATO1_CH1N ATIN1_CH1			UART2_TX	SPI2_SCLK	I2C1_SCLK			CH34		LED4	CTSU26	
14	18		High-Z			PC17	PD13	ATO1_CH2P			UART2_RX	SPI2_MISO	I2C1_SDA			CH33		LED5	CTSU25	
15	19		High-Z			PC18	PD14	ATO1_CH2N ATIN1_CH2			UART2_CTS	SPI2_MOSI				CH32		LED6	CTSU24	
16	20		High-Z		PB26	PC19		ATO2_BRK1			UART2_RTS					CH31			CTSU23	
17	21		High-Z	PA4	PB25					BTIN14/ BTOUT14				SWDIO		CH43		LED7	CTSU22	
18	22		High-Z	PA11		PC31		ATO2_CH1P	GTO2_CH2P GTIN2_CH2		UART2_TX					CH36				
19	23		High-Z	PA10		PC30		ATO2_CH1N	GTO2_CH2N GTO2_CH3P GTIN2_ETR		UART2_RX					CH37				
20	24		High-Z	PA9		PC29	PD31	ATO2_CH2P	GTO3_CH2P GTIN3_CH2				I2C2_SCK			CH11			CTSU21	
21	25		High-Z	PA8		PC28	PD30	ATO2_CH2N	GTO4_CH2P GTIN4_CH2				I2C2_SDA			CH9			CTSU20	
22	26		High-Z			PC27	PD29		GTO2_CH1P GTIN2_CH1			SPI1_CSB				CH28			CTSU19	
23	27		High-Z			PC26	PD28	ATO1_BRK2	GTO2_CH1N			SPI1_MISO				CH29			CTSU18	
24	28		High-Z			PC25	PD27	ATO1_BRK1	GTO2_CH4 GTIN2_CH4			SPI1_MOSI				CH30			CTSU17	
25	29		High-Z		PB7	PC24	PD26					SPI1_SCLK		SWCLK		CH38		LED8	CTSU16	
26	30		High-Z		PB6		PD25			BTIN23 BTOUT23				SWDIO		CH2P/CH17				
27	31		High-Z		PB5	PC6	PD24	ATO2_BRK2		BTIN22 BTOUT22				SWCLK		CH2N/CH16				
28	32		High-Z		PB24	PC7	PA3	ATO1_CH3P ATIN1_ETR				SPI1_MOSI	I2C1_SCK				CMP0P		CTSU15	

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	PGA	ADC	CMP	LED	Touch	XTAL
29	33		High-Z	PA1		PC8		ATO1_CH3N	GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO			CMP0N		CTSU14	
30	34		High-Z	PA2		PC9		ATIN1_BRK1	GTO1_CH1N					SWCLK		CH6				
31	35		High-Z	PA10		PC10										CH1P/CH15				
32	36		High-Z	PA11		PC11										CH1N/CH14				
33	37		High-Z		PB27	PC12										CH0P/CH13				
34	38		High-Z			PC13	PD21					SPI1_SCLK				CH0N/CH12				
35	39		High-Z		PB15		PD20	ATO1_CH2P ATIN1_CH2			UART3_TX						CMP1P		CTSU13	
36	40		High-Z	PA5	PB14			ATO1_CH2N		BTIN12	UART3_RX	SPI2_CSB					CMP1N		CTSU12	
37	41	BOOT0	SWCLK	PA31	PB13				GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK		CH5	OCMP1			
38	42		High-Z		PB12		PD19	ATO1_CH1P		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA				CMP2P		CTSU11	
39	43		High-Z		PB11		PD18	ATO1_CH1N		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA				CMP2N		CTSU10	
40	44		SWDIO	PA30	PB10					BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO		CH4	OCMP2			
41	45	BOOT1	High-Z	PA29	PB9					BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA			CH3N/CH27	CMP3N		CTSU9	
42	46		High-Z	PA28	PB8					BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK			CH3P/CH3	CMP3P			
43	47		High-Z	PA27			PD22		GTO1_CH1P GTIN1_CH1							CH39			CTSU8	
44	48		High-Z	PA26			PD23	ATO1_CH4 ATIN1_CH4				SPI1_CSB				CH40	OCMP3		CTSUCAP	
45	49		High-Z	PA25			PB23		GTO1_CH4							CH0P/CH20			CTSU7	
46	50		High-Z	PA24	PB22				GTO2_CH2P							CH1P/CH21			CTSU6	
47	51		High-Z	PA23	PB21				GTO3_CH1P							CH2P/CH22			CTSU5	
48	52		High-Z	PA22	PB20				GTO3_CH1N							CH3P/CH23			CTSU4	
49	53		High-Z	PA21	PB19			ATO1_CH3P					I2C1_SCK			CH1N/CH25			CTSU1	
50	54		High-Z	PA20	PB18			ATO1_CH3N					I2C1_SDA			CH1P/CH1				
51	55		High-Z	PA19	PB17			ATO1_CH2P								CH0N/CH24			CTSU0	
52	56		High-Z	PA18	PB16			ATO1_CH2N								CH0P/CH0				
53	57		High-Z	PA17			PD8		GTO1_CH2P GTO2_CH2P GTIN1_CH2			SPI1_CSB				CH8			CTSU3	
54	58		High-Z	PA16	PB4			ATO2_CH4 ATIN2_CH4				SPI1_SCK	I2C1_SCK		PGA_OUT0					
55	59		High-Z	PA15	PB3			ATIN2_BRK1	GTO2_CH2N		UART4_RX	SPI1_MOSI	I2C1_SDA		PGA_OUT1					
56	60		High-Z	PA14	PB2				GTO2_CH3N GTIN2_ETR		UART4_TX	SPI1_MISO				CH41				
57	61		High-Z	PA13	PB1			ATO1_CH1P			UART4_RX					CH2N/CH26			CTSU31	
58	62		High-Z	PA12	PB0			ATO1_CH1N			UART4_TX					CH2P/CH2				
59	63		High-Z	PA7			PD17	ATIN2_ETR								CH42				
60	64		High-Z	PA6			PD16		GTO1_CH3P GTO2_CH2N GTIN1_CH3							CH7			CTSU2	

6.2.6 XT32H053Dx (LQFP48) Pin List

Table 8 Pin list of XT32H053Dx

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	37		UART1_TX		PB30	PC20	PD0	ATIN1_ETR ATIN1_BRK1			UART1_TX				CH10		LED0		
4	38		High-Z			PC1	PD6		GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS							CTSU30	
5	39		UART1_RX			PC0	PD5	ATO1_CH3P ATIN1_BRK2			UART1_RX						LED1	CTSU29	
6	40	RSTB	RSTB																
7	41		High-Z			PC21	PD4												XO_HS EXCLK_HS
8	42		High-Z			PC22	PD3												XI_HS
9	43		High-Z	PA0			PD15	ATO1_CH3N ATIN1_CH3									LED2	CTSU28	
10	44		High-Z		PB26	PC23		ATO1_CH1P				SPI2_CSB					LED3	CTSU27	
11	45		High-Z			PC14	PD2/ PD10												XO_LS EXCLK_LS
12	46		High-Z			PC15	PD1/ PD11												XI_LS
-	47	GND	GND																
-	48	VSUP	VSUP																
13	1		High-Z			PC16	PD12	ATO1_CH1N ATIN1_CH1			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	2		High-Z			PC17	PD13	ATO1_CH2P			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	3		High-Z			PC18	PD14	ATO1_CH2N ATIN1_CH2			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
16	4		High-Z		PB26	PC19		ATO2_BRK1			UART2_RTS				CH31			CTSU23	
17	5		High-Z	PA4	PB25					BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
20	6		High-Z	PA9		PC29	PD31	ATO2_CH2P	GTO3_CH2P GTIN3_CH2				I2C2_SCK		CH11			CTSU21	
21	7		High-Z	PA8		PC28	PD30	ATO2_CH2N	GTO4_CH2P GTIN4_CH2				I2C2_SDA		CH9			CTSU20	
22	8		High-Z			PC27	PD29		GTO2_CH1P GTIN2_CH1			SPI1_CSB			CH28			CTSU19	
23	9		High-Z			PC26	PD28	ATO1_BRK2	GTO2_CH1N			SPI1_MISO			CH29			CTSU18	
24	10		High-Z			PC25	PD27	ATO1_BRK1	GTO2_CH4 GTIN2_CH4			SPI1_MOSI			CH30			CTSU17	
25	11		High-Z		PB7	PC24	PD26					SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	12		High-Z		PB24	PC7	PA3	ATO1_CH3P ATIN1_ETR				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	13		High-Z	PA1		PC8		ATO1_CH3N	GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	14		High-Z	PA2		PC9		ATIN1_BRK1	GTO1_CH1N					SWCLK	CH6				
35	15		High-Z		PB15		PD20	ATO1_CH2P ATIN1_CH2			UART3_TX					CMP1P		CTSU13	
36	16		High-Z	PA5	PB14			ATO1_CH2N		BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	17	BOOT0	SWCLK	PA31	PB13				GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	18		High-Z		PB12		PD19	ATO1_CH1P		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	19		High-Z		PB11		PD18	ATO1_CH1N		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	20		SWDIO	PA30	PB10					BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	21	BOOT1	High-Z	PA29	PB9					BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	

IO_ID	Pin #	Default Function		Alternative Function														
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
42	22		High-Z	PA28	PB8					BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
43	23		High-Z	PA27			PD22		GTO1_CH1P GTIN1_CH1						CH39			CTSU8	
44	24		High-Z	PA26			PD23	ATO1_CH4 ATIN1_CH4				SPI1_CSB			CH40	OCMP3		CTSUCAP	
45	25		High-Z	PA25			PB23		GTO1_CH4						CH0P/CH20			CTSU7	
46	26		High-Z	PA24	PB22				GTO2_CH2P						CH1P/CH21			CTSU6	
47	27		High-Z	PA23	PB21				GTO3_CH1P						CH2P/CH22			CTSU5	
48	28		High-Z	PA22	PB20				GTO3_CH1N						CH3P/CH23			CTSU4	
49	29		High-Z	PA21	PB19			ATO1_CH3P					I2C1_SCK		CH1N/CH25			CTSU1	
50	30		High-Z	PA20	PB18			ATO1_CH3N					I2C1_SDA		CH1P/CH1				
51	31		High-Z	PA19	PB17			ATO1_CH2P							CH0N/CH24			CTSU0	
52	32		High-Z	PA18	PB16			ATO1_CH2N							CH0P/CH0				
53	33		High-Z	PA17			PD8		GTO1_CH2P GTO2_CH2P GTIN1_CH2			SPI1_CSB			CH8			CTSU3	
57	34		High-Z	PA13	PB1			ATO1_CH1P			UART4_RX				CH2N/CH26			CTSU31	
58	35		High-Z	PA12	PB0			ATO1_CH1N			UART4_TX				CH2P/CH2				
60	36		High-Z	PA6			PD16		GTO1_CH3P GTO2_CH2N GTIN1_CH3						CH7			CTSU2	

6.2.7 XT32H053Cx (LQFP44) Pin List

Table 9 Pin list of XT32H053Cx

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	44		UART1_TX		PB30	PC20	PD0	ATIN1_ETR ATIN1_BRK1			UART1_TX				CH10		LED0		
4	1		High-Z			PC1	PD6		GTO4_CH1P GTIN4_CH1	BTIN24 BTOUT24	UART1_RTS							CTSU30	
5	2		UART1_RX			PC0	PD5	ATO1_CH3P ATIN1_BRK2			UART1_RX						LED1	CTSU29	
6	3	RSTB	RSTB																
7	4		High-Z			PC21	PD4												XO_HS EXCLK_HS
8	5		High-Z			PC22	PD3												XI_HS
9	6		High-Z	PA0			PD15	ATO1_CH3N ATIN1_CH3									LED2	CTSU28	
10	7		High-Z		PB26	PC23		ATO1_CH1P				SPI2_CSB					LED3	CTSU27	
11	8		High-Z			PC14	PD2/ PD10												XO_LS EXCLK_LS
12	9		High-Z			PC15	PD1/ PD11												XI_LS
-	10	GND	GND																
-	11	VSUP	VSUP																
13	12		High-Z			PC16	PD12	ATO1_CH1N ATIN1_CH1			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	13		High-Z			PC17	PD13	ATO1_CH2P			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	14		High-Z			PC18	PD14	ATO1_CH2N ATIN1_CH2			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
16	15		High-Z		PB26	PC19		ATO2_BRK1			UART2_RTS				CH31			CTSU23	
17	16		High-Z	PA4	PB25					BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
22	17		High-Z			PC27	PD29		GTO2_CH1P GTIN2_CH1			SPI1_CSB			CH28			CTSU19	
23	18		High-Z			PC26	PD28	ATO1_BRK2	GTO2_CH1N			SPI1_MISO			CH29			CTSU18	
24	19		High-Z			PC25	PD27	ATO1_BRK1	GTO2_CH4 GTIN2_CH4			SPI1_MOSI			CH30			CTSU17	
25	20		High-Z		PB7	PC24	PD26					SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	21		High-Z		PB24	PC7	PA3	ATO1_CH3P ATIN1_ETR				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	22		High-Z	PA1		PC8		ATO1_CH3N	GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	23		High-Z	PA2		PC9		ATIN1_BRK1	GTO1_CH1N					SWCLK	CH6				
35	24		High-Z		PB15		PD20	ATO1_CH2P ATIN1_CH2			UART3_TX					CMP1P		CTSU13	
36	25		High-Z	PA5	PB14			ATO1_CH2N		BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	26	BOOT0	SWCLK	PA31	PB13				GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	27		High-Z		PB12		PD19	ATO1_CH1P		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	28		High-Z		PB11		PD18	ATO1_CH1N		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	29		SWDIO	PA30	PB10					BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	30	BOOT1	High-Z	PA29	PB9					BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	
42	31		High-Z	PA28	PB8					BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
43	32		High-Z	PA27			PD22		GTO1_CH1P GTIN1_CH1						CH39			CTSU8	

IO_ID	Pin #	Default Function		Alternative Function														
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
44	33		High-Z	PA26			PD23	ATO1_CH4 ATIN1_CH4				SPI1_CSB			CH40	OCMP3		CTSUCAP	
45	34		High-Z	PA25			PB23		GTO1_CH4						CH0P/CH20			CTSU7	
46	35		High-Z	PA24	PB22				GTO2_CH2P						CH1P/CH21			CTSU6	
47	36		High-Z	PA23	PB21				GTO3_CH1P						CH2P/CH22			CTSU5	
48	37		High-Z	PA22	PB20				GTO3_CH1N						CH3P/CH23			CTSU4	
49	38		High-Z	PA21	PB19			ATO1_CH3P					I2C1_SCK		CH1N/CH25			CTSU1	
50	39		High-Z	PA20	PB18			ATO1_CH3N					I2C1_SDA		CH1P/CH1				
51	40		High-Z	PA19	PB17			ATO1_CH2P							CH0N/CH24			CTSU0	
52	41		High-Z	PA18	PB16			ATO1_CH2N							CH0P/CH0				
57	42		High-Z	PA13	PB1			ATO1_CH1P			UART4_RX				CH2N/CH26			CTSU31	
58	43		High-Z	PA12	PB0			ATO1_CH1N			UART4_TX				CH2P/CH2				

6.2.8 XT32H053Bx (LQFP32) Pin List

Table 10 Pin list of XT32H053Bx

IO_ID	Pin #	Default Function		Alternative Function															
		RSTB=0	RSTB=1	PA	PB	PC	PD	TIMA	TIMG	TIMB	UART	SPI	I2C	SWD	ADC	CMP	LED	Touch	XTAL
1	32		UART1_TX		PB30	PC20	PD0	ATIN1_ETR ATIN1_BRK1			UART1_TX				CH10		LED0		
5	1		UART1_RX			PC0	PD5	ATO1_CH3P ATIN1_BRK2			UART1_RX						LED1	CTSU29	
6	2	RSTB	RSTB																
9	3		High-Z	PA0			PD15	ATO1_CH3N ATIN1_CH3									LED2	CTSU28	
10	4		High-Z		PB26	PC23		ATO1_CH1P				SPI2_CSB					LED3	CTSU27	
11	5		High-Z			PC14	PD2/ PD10												XO_LS EXCLK_LS
12	6		High-Z			PC15	PD1/ PD11												XI_LS
-	7	GND	GND																
-	8	VSUP	VSUP																
13	9		High-Z			PC16	PD12	ATO1_CH1N ATIN1_CH1			UART2_TX	SPI2_SCLK	I2C1_SCLK		CH34		LED4	CTSU26	
14	10		High-Z			PC17	PD13	ATO1_CH2P			UART2_RX	SPI2_MISO	I2C1_SDA		CH33		LED5	CTSU25	
15	11		High-Z			PC18	PD14	ATO1_CH2N ATIN1_CH2			UART2_CTS	SPI2_MOSI			CH32		LED6	CTSU24	
17	12		High-Z	PA4	PB25					BTIN14/ BTOUT14				SWDIO	CH43		LED7	CTSU22	
25	13		High-Z		PB7	PC24	PD26					SPI1_SCLK		SWCLK	CH38		LED8	CTSU16	
28	14		High-Z		PB24	PC7	PA3	ATO1_CH3P ATIN1_ETR				SPI1_MOSI	I2C1_SCK			CMP0P		CTSU15	
29	15		High-Z	PA1		PC8		ATO1_CH3N	GTIN1_ETR			SPI1_MISO	I2C1_SDA	SWDIO		CMP0N		CTSU14	
30	16		High-Z	PA2		PC9		ATIN1_BRK1	GTO1_CH1N					SWCLK	CH6				
35	17		High-Z		PB15		PD20	ATO1_CH2P ATIN1_CH2			UART3_TX					CMP1P		CTSU13	
36	18		High-Z	PA5	PB14			ATO1_CH2N		BTIN12	UART3_RX	SPI2_CSB				CMP1N		CTSU12	
37	19	BOOT0	SWCLK	PA31	PB13				GTIN1_ETR	BTIN13 BTOUT13			I2C2_SCK	SWCLK	CH5	OCMP1			
38	20		High-Z		PB12		PD19	ATO1_CH1P		BTIN14	UART2_RX	SPI2_MOSI	I2C1_SCLK I2C2_SDA			CMP2P		CTSU11	
39	21		High-Z		PB11		PD18	ATO1_CH1N		BTIN21	UART2_TX	SPI2_MISO	I2C1_SDA			CMP2N		CTSU10	
40	22		SWDIO	PA30	PB10					BTIN22 BTOUT22	UART3_TX	SPI1_MISO		SWDIO	CH4	OCMP2			
41	23	BOOT1	High-Z	PA29	PB9					BTIN11 BTOUT11	UART3_RX	SPI2_SCLK/ SPI1_MOSI	I2C2_SDA		CH3N/CH27	CMP3N		CTSU9	
42	24		High-Z	PA28	PB8					BTIN12 BTOUT12		SPI1_SCLK	I2C2_SCK		CH3P/CH3	CMP3P			
44	25		High-Z	PA26			PD23	ATO1_CH4 ATIN1_CH4				SPI1_CSB			CH40	OCMP3		CTSUCAP	
49	26		High-Z	PA21	PB19			ATO1_CH3P					I2C1_SCK		CH1N/CH25			CTSU1	
50	27		High-Z	PA20	PB18			ATO1_CH3N					I2C1_SDA		CH1P/CH1				
51	28		High-Z	PA19	PB17			ATO1_CH2P							CH0N/CH24			CTSU0	
52	29		High-Z	PA18	PB16			ATO1_CH2N							CH0P/CH0				
57	30		High-Z	PA13	PB1			ATO1_CH1P			UART4_RX				CH2N/CH26			CTSU31	
58	31		High-Z	PA12	PB0			ATO1_CH1N			UART4_TX				CH2P/CH2				

6.3 Pins Functional Description

Table 11 XT32H05x Pins functional description

Function Pin Name	Signal Type	Function Description
VSUP	Power	Power supply of the chip, 1.8~5.5V
GND	Ground	ground
RSTB	DI	external chip reset pin
BOOT0	DI	boot mode selection pin 2'b00: boot from flash, 2'b01: boot from sram 2'b10: boot from sram, 2'b11: reserved
BOOT1	DI	
XO_HS	AIO	4~48MHz Crystal output pin
XI_HS	AIO	4~48MHz Crystal input pin
EXCLK_HS	DI	high speed external reference clock input
XO_LS	AIO	32kHz Crystal output pin
XI_LS	AIO	32kHz Crystal input pin
EXCLK_LS	DI	low speed external reference clock input
PA0/PB0/PC0/PD0	DIO	Configurable GPIO, PORT A/B/C/D bit 0
PA1/PB1/PC1/PD1	DIO	Configurable GPIO, PORT A/B/C/D bit 1
PA2/PB2/PC2/PD2	DIO	Configurable GPIO, PORT A/B/C/D bit 2
PA3/PB3/PC3/PD3	DIO	Configurable GPIO, PORT A/B/C/D bit 3
PA4/PB4/PC4/PD4	DIO	Configurable GPIO, PORT A/B/C/D bit 4
PA5/PB5/PC5/PD5	DIO	Configurable GPIO, PORT A/B/C/D bit 5
PA6/PB6/PC6/PD6	DIO	Configurable GPIO, PORT A/B/C/D bit 6
PA7/PB7/PC7/PD7	DIO	Configurable GPIO, PORT A/B/C/D bit 7
PA8/PB8/PC8/PD8	DIO	Configurable GPIO, PORT A/B/C/D bit 8
PA9/PB9/PC9/PD9	DIO	Configurable GPIO, PORT A/B/C/D bit 9
PA10/PB10/PC10/PD10	DIO	Configurable GPIO, PORT A/B/C/D bit 10
PA11/PB11/PC11/PD11	DIO	Configurable GPIO, PORT A/B/C/D bit 11
PA12/PB12/PC12/PD12	DIO	Configurable GPIO, PORT A/B/C/D bit 12
PA13/PB13/PC13/PD13	DIO	Configurable GPIO, PORT A/B/C/D bit 13
PA14/PB14/PC14/PD14	DIO	Configurable GPIO, PORT A/B/C/D bit 14
PA15/PB15/PC15/PD15	DIO	Configurable GPIO, PORT A/B/C/D bit 15
PA16/PB16/PC16/PD16	DIO	Configurable GPIO, PORT A/B/C/D bit 16
PA17/PB17/PC17/PD17	DIO	Configurable GPIO, PORT A/B/C/D bit 17
PA18/PB18/PC18/PD18	DIO	Configurable GPIO, PORT A/B/C/D bit 18
PA19/PB19/PC19/PD19	DIO	Configurable GPIO, PORT A/B/C/D bit 19

Function Pin Name	Signal Type	Function Description
PA20/PB20/PC20/PD20	DIO	Configurable GPIO, PORT A/B/C/D bit 20
PA21/PB21/PC21/PD21	DIO	Configurable GPIO, PORT A/B/C/D bit 21
PA22/PB22/PC22/PD22	DIO	Configurable GPIO, PORT A/B/C/D bit 22
PA23/PB23/PC23/PD23	DIO	Configurable GPIO, PORT A/B/C/D bit 23
PA24/PB24/PC24/PD24	DIO	Configurable GPIO, PORT A/B/C/D bit 24
PA25/PB25/PC25/PD25	DIO	Configurable GPIO, PORT A/B/C/D bit 25
PA26/PB26/PC26/PD26	DIO	Configurable GPIO, PORT A/B/C/D bit 26
PA27/PB27/PC27/PD27	DIO	Configurable GPIO, PORT A/B/C/D bit 27
PA28/PB28/PC28/PD28	DIO	Configurable GPIO, PORT A/B/C/D bit 28
PA29/PB29/PC29/PD29	DIO	Configurable GPIO, PORT A/B/C/D bit 29
PA30/PB30/PC30/PD30	DIO	Configurable GPIO, PORT A/B/C/D bit 30
PA31/PB31/PC31/PD31	DIO	Configurable GPIO, PORT A/B/C/D bit 31
UART1_RX	DI	RX of UART1
UART1_TX	DO	TX of UART1
UART1_CTS	DI	CTS of UART1, for flow control
UART1_RTS	DI	RTS of UART1, for flow control
UART2_RX	DI	RX of UART2
UART2_TX	DO	TX of UART2
UART2_CTS	DI	CTS of UART2, for flow control
UART2_RTS	DI	RTS of UART2, for flow control
UART3_RX	DI	RX of UART3
UART3_TX	DO	TX of UART3
UART4_RX	DI	RX of UART4
UART4_TX	DO	TX of UART4
SPI1_CSB	DIO	Chip selection of master/slave SPI 1
SPI1_MISO	DIO	master in slave out data of master/slave SPI 1
SPI1_MOSI	DIO	master out slave in data of master/slave SPI 1
SPI1_SCLK	DIO	SPI clock of master/slave SPI 1
SPI2_CSB	DIO	Chip selection of master/slave SPI 2
SPI2_MISO	DIO	master in slave out data of master/slave SPI 2
SPI2_MOSI	DIO	master out slave in data of master/slave SPI 2
SPI2_SCLK	DIO	SPI clock of master/slave SPI 2
I2C1_SCK	DIO	I2C clock of master/slave I2C 1
I2C1_SDA	DIO	I2C data of master/slave I2C 1
I2C2_SCK	DIO	I2C clock of master/slave I2C 2

Function Pin Name	Signal Type	Function Description
I2C2_SDA	DIO	I2C data of master/slave I2C 2
SWDIO	DIO	SWD debug interface, input/output data
SWCLK	DI	SWD debug interface, input clock
GTO1_CH1P	DO	epwm output of general purpose timer 1, it can be programmed as differential P or single-end
GTO1_CH1N	DO	epwm output of general purpose timer 1, it can be programmed as differential N or single-end
GTO1_CH2P	DO	epwm output of general purpose timer 1, it is single-end
GTO1_CH3P	DO	epwm output of general purpose timer 1, it is single-end
GTO1_CH4	DO	epwm output of general purpose timer 1, it is single-end
GTIN1_CH2	DI	input for general purpose timer 1
GTIN1_CH3	DI	input for general purpose timer 1
GTIN1_ETR	DI	input for general purpose timer 1
GTO2_CH1P	DO	epwm output of general purpose timer 2, it can be programmed as differential P or single-end
GTO2_CH1N	DO	epwm output of general purpose timer 2, it can be programmed as differential N or single-end
GTO2_CH2P	DO	epwm output of general purpose timer 2, it can be programmed as differential P or single-end
GTO2_CH2N	DO	epwm output of general purpose timer 2, it can be programmed as differential N or single-end
GTO2_CH3P	DO	epwm output of general purpose timer 2, it can be programmed as differential P or single-end
GTO2_CH3N	DO	epwm output of general purpose timer 2, it can be programmed as differential N or single-end
GTO2_CH4	DO	epwm output of general purpose timer 1, it is single-end
GTIN2_CH1	DI	input for general purpose timer 1
GTIN2_CH2	DI	input for general purpose timer 1
GTIN2_CH4	DI	input for general purpose timer 1
GTIN2_ETR	DI	input for general purpose timer 1
GTO3_CH1P	DO	epwm output of general purpose timer 3, it can be programmed as differential P or single-end
GTO3_CH1N	DO	epwm output of general purpose timer 3, it can be programmed as differential N or single-end
GTO3_CH2P	DO	epwm output of general purpose timer 3, it is single-end
GTIN3_CH2	DI	input for general purpose timer 3
GTO4_CH1P	DO	epwm output of general purpose timer 4, it can be programmed as differential P or single-end
GTO4_CH1N	DO	epwm output of general purpose timer 4, it can be programmed as differential N or single-end
GTO4_CH2P	DO	epwm output of general purpose timer 4, it is single-end
GTIN4_CH1	DI	input for general purpose timer 4
GTIN4_CH2	DI	input for general purpose timer 4
ATO1_CH1P	DO	epwm output of advanced timer 1, it can be programmed as differential P or single-end
ATO1_CH1N	DO	epwm output of advanced timer 1, it can be programmed as differential N or single-end

Function Pin Name	Signal Type	Function Description
ATO1_CH2P	DO	epwm output of advanced timer 1, it can be programmed as differential P or single-end
ATO1_CH2N	DO	epwm output of advanced timer 1, it can be programmed as differential N or single-end
ATO1_CH3P	DO	epwm output of advanced timer 1, it can be programmed as differential P or single-end
ATO1_CH3N	DO	epwm output of advanced timer 1, it can be programmed as differential N or single-end
ATO1_CH4	DO	epwm output of advanced timer 1, it is single-end
ATIN1_CH1	DI	input for advanced timer 1
ATIN1_CH2	DI	input for advanced timer 1
ATIN1_CH3	DI	input for advanced timer 1
ATIN1_CH4	DI	input for advanced timer 1
ATIN1_ETR	DI	input for advanced timer 1
ATIN1_BRK1	DI	input brk1 for advanced timer 1
ATIN1_BRK2	DI	input brk2 for advanced timer 1
ATOUT1_BRK2	DO	output brk1 for advanced timer 1
ATOUT1_BRK1	DO	output brk2 for advanced timer 1
ATO2_CH1P	DO	epwm output of advanced timer 2, it can be programmed as differential P or single-end
ATO2_CH1N	DO	epwm output of advanced timer 2, it can be programmed as differential N or single-end
ATO2_CH2P	DO	epwm output of advanced timer 2, it can be programmed as differential P or single-end
ATO2_CH2N	DO	epwm output of advanced timer 2, it can be programmed as differential N or single-end
ATO2_CH3P	DO	epwm output of advanced timer 2, it can be programmed as differential P or single-end
ATO2_CH3N	DO	epwm output of advanced timer 2, it can be programmed as differential N or single-end
ATO2_CH4	DO	epwm output of advanced timer 2, it is single-end
ATIN2_CH3	DI	input for advanced timer 2
ATIN2_CH4	DI	input for advanced timer 2
ATIN2_ETR	DI	input for advanced timer 2
ATIN2_BRK1	DI	input brk1 for advanced timer 2
ATOUT2_BRK1	DO	output brk1 of advanced timer 2
ATOUT2_BRK2	DO	output brk2 of advanced timer 2
PGA_OUT0	DO	output of pga 0
PGA_OUT1	DO	output of pga 1
CMP0P	AIO	differential positive input of comparator 0
CMP0N	AIO	differential negative input of comparator 0
OCMP0	DO	output of comparator 0
CMP1P	AIO	differential positive input of comparator 1

Function Pin Name	Signal Type	Function Description
CMP1N	AIO	differential negative input of comparator 1
OCMP1	DO	output of comparator 1
CMP2P	AIO	differential positive input of comparator 2
CMP2N	AIO	differential negative input of comparator 2
OCMP2	DO	output of comparator 2
CMP3P	AIO	differential positive input of comparator 3
CMP3N	AIO	differential negative input of comparator 3
OCMP3	DO	output of comparator 3
CH0P/CH0	AIO	adc differential positive input channel 0， or single-end channel 0
CH0N	AIO	adc differential negative input channel 0
CH1P/CH1	AIO	adc differential positive input channel 1， or single-end channel 1
CH1N	AIO	adc differential negative input channel 1
CH2P/CH2	AIO	adc differential positive input channel 2， or single-end channel 2
CH2N	AIO	adc differential negative input channel 2
CH3P/CH3	AIO	adc differential positive input channel 3， or single-end channel 3
CH3N	AIO	adc differential negative input channel 3
CH4	AIO	adc single-end input channel 4
CH5	AIO	adc single-end input channel 5
CH6	AIO	adc single-end input channel 6
CH7	AIO	adc single-end input channel 7
CH8	AIO	adc single-end input channel 8
CH9	AIO	adc single-end input channel 9
CH10	AIO	adc single-end input channel 10
CH11	AIO	adc single-end input channel 11
CH12	AIO	adc single-end input channel 12
CH13	AIO	adc single-end input channel 13
CH14	AIO	adc single-end input channel 14
CH15	AIO	adc single-end input channel 15
CH16	AIO	adc single-end input channel 16
CH17	AIO	adc single-end input channel 17
CH18	AIO	adc single-end input channel 18
CH19	AIO	adc single-end input channel 19
CH20	AIO	adc single-end input channel 20
CH21	AIO	adc single-end input channel 21
CH22	AIO	adc single-end input channel 22

Function Pin Name	Signal Type	Function Description
CH23	AIO	adc single-end input channel 23
CH24	AIO	adc single-end input channel 24
CH25	AIO	adc single-end input channel 25
CH26	AIO	adc single-end input channel 26
CH27	AIO	adc single-end input channel 27
CH28	AIO	adc single-end input channel 28
CH29	AIO	adc single-end input channel 29
CH30	AIO	adc single-end input channel 30
CH31	AIO	adc single-end input channel 31
CH32	AIO	adc single-end input channel 32
CH33	AIO	adc single-end input channel 33
CH34	AIO	adc single-end input channel 34
CH35	AIO	adc single-end input channel 35
CH36	AIO	adc single-end input channel 36
CH37	AIO	adc single-end input channel 37
CH38	AIO	adc single-end input channel 38
CH39	AIO	adc single-end input channel 39
CH40	AIO	adc single-end input channel 40
CH41	AIO	adc single-end input channel 41
CH42	AIO	adc single-end input channel 42
CH43	AIO	adc single-end input channel 43
LED0	AIO	LED SEG_COM_0
LED1	AIO	LED SEG_COM_1
LED2	AIO	LED SEG_COM_2
LED3	AIO	LED SEG_COM_3
LED4	AIO	LED SEG_COM_4
LED5	AIO	LED SEG_COM_5
LED6	AIO	LED SEG_COM_6
LED7	AIO	LED SEG_COM_7
LED8	AIO	LED_SEG_8
CTSUCAP	AIO	Touch sensor decoupling cap input pad
CTSU0	AIO	Touch sensor channel 0
CTSU1	AIO	Touch sensor channel 1
CTSU2	AIO	Touch sensor channel 2
CTSU3	AIO	Touch sensor channel 3

Function Pin Name	Signal Type	Function Description
CTSU4	AIO	Touch sensor channel 4
CTSU5	AIO	Touch sensor channel 5
CTSU6	AIO	Touch sensor channel 6
CTSU7	AIO	Touch sensor channel 7
CTSU8	AIO	Touch sensor channel 8
CTSU9	AIO	Touch sensor channel 9
CTSU10	AIO	Touch sensor channel 10
CTSU11	AIO	Touch sensor channel 11
CTSU12	AIO	Touch sensor channel 12
CTSU13	AIO	Touch sensor channel 13
CTSU14	AIO	Touch sensor channel 14
CTSU15	AIO	Touch sensor channel 15
CTSU16	AIO	Touch sensor channel 16
CTSU17	AIO	Touch sensor channel 17
CTSU18	AIO	Touch sensor channel 18
CTSU19	AIO	Touch sensor channel 19
CTSU20	AIO	Touch sensor channel 20
CTSU21	AIO	Touch sensor channel 21
CTSU22	AIO	Touch sensor channel 22
CTSU23	AIO	Touch sensor channel 23
CTSU24	AIO	Touch sensor channel 24
CTSU25	AIO	Touch sensor channel 25
CTSU26	AIO	Touch sensor channel 26
CTSU27	AIO	Touch sensor channel 27
CTSU28	AIO	Touch sensor channel 28
CTSU29	AIO	Touch sensor channel 29
CTSU30	AIO	Touch sensor channel 30
CTSU31	AIO	Touch sensor channel 31

7 Functional Description

7.1 Arm Cortex-M0+ core with MPU

The Cortex-M0+ processor is a highly area- and power-optimized CPU, implementing the Armv6-M instruction set architecture (ISA) with support for CPU clock speeds up to 96MHz. The Cortex-M0+ is a Von Neumann style 32-bit processor with a 2-stage ultra-low power pipeline and a single-cycle access port to the GPIO registers for efficient GPIO manipulation. It delivers high performance and low power to a broad range of embedded applications. Key features of the Cortex-M0+ implemented in device include:

- Supporting clocking frequencies from 32kHz to 96MHz
- Little-endian
- ARMv6-M Thumb instruction set with single-cycle 32x32 multiply instruction
- Integrated 24bit system tick timer (SysTick)
- Tightly integrated memory protection unit (MPU) with 4 programmable regions
- Four hardware breakpoints and two hardware watchpoints for debug
- Nested vectored interrupt controller (NVIC) with 4 programmable priority levels and tail-chaining
- Support reset-all-registers
- Support vector table offset

The Cortex-M0+ architecture enables excellent code density, deterministic interrupt handling, and upwards compatibility with other processor architectures in the ARM Cortex-M family. Owing to embedded ARM core, the XT32H05x devices are compatible with ARM tools and software.

7.2 Memory Mapping

Table 12 XT32H0 memory address

Type	Start Address	Stop Address	Size	Memory Area Description
AHB	0x8005_0000	0x8005_FFFF	64KB	CRC
	0x8003_0000	0x8003_FFFF	64KB	External interrupt controller
	0x8002_E000	0x8002_FFFF	8KB	CTSM
	0x8002_0000	0x8002_3FFF	16KB	SRAM
	0x8001_0000	0x8001_FFFF	64KB	Clock generator
	0x8000_0000	0x8000_FFFF	64KB	DMAC
APB	0x5000_0C00	0x5000_0FFF	1KB	GPIO
	0x5000_0800	0x5000_0BFF	1KB	IO integrate
	0x4000_3600	0x4000_36FF	256B	Always-on block
	0x4000_3500	0x4000_35FF	256B	RTC
	0x4000_3400	0x4000_34FF	256B	Independent WDT
	0x4000_3000	0x4000_30FF	256B	LED
	0x4000_2800	0x4000_2BFF	1KB	MDU
	0x4000_2700	0x4000_27FF	256B	SPI2 slave
	0x4000_2600	0x4000_26FF	256B	SPI2 master
	0x4000_2500	0x4000_25FF	256B	SPI1 slave
	0x4000_2400	0x4000_24FF	256B	SPI1 master
	0x4000_2100	0x4000_21FF	256B	I2C2
	0x4000_2000	0x4000_20FF	256B	I2C1
	0x4000_1F00	0x4000_1FFF	256B	UART4
	0x4000_1E00	0x4000_1EFF	256B	UART3
	0x4000_1D00	0x4000_1DFF	256B	UART2
	0x4000_1C00	0x4000_1CFF	256B	UART1
	0x4000_1800	0x4000_1BFF	1KB	General Timer
	0x4000_1500	0x4000_15FF	256B	Basic Timer group 2
	0x4000_1400	0x4000_14FF	256B	Basic Timer group 1
	0x4000_1000	0x4000_13FF	1KB	Advanced TIMER
	0x4000_0C00	0x4000_0FFF	1KB	Windows WDT

Type	Start Address	Stop Address	Size	Memory Area Description
	0x4000_0800	0x4000_0BFF	1KB	SYSCFG
SRAM	0x2000_0000	0x2000_7FFF	32KB	SRAM
ROM	0x1FFF_0000	0x1FFF_FFFF	64KB	ROM
FLASH	0x0809_2000	0x0809_3FFF	8kB	Flash info1 area
	0x0808_0000	0x0808_1FFF	8kB	Flash info area
	0x0804_0000	0x0804_7FFF	32kB	Flash data memory
	0x0800_0000	0x0801_FFFF	128kB	Flash code memory
Remapping	0x0000_0000	0x0001_FFFF	128kB	Mapped to one of the embedded flash memory, SRAM and ROM depending on the level of the BOOT0/1 pin

7.3 Embedded Flash memory

XT32H05x devices feature up to 160k Bytes of embedded Flash memory available for storing code and data.

7.4 Embedded SRAM

XT32H05x devices integrated up to 32k Bytes of SRAM. The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

7.5 Boot modes

At startup, the boot pins (BOOT0 and BOOT1) are used to select one of the three boot options:

- Boot from Flash memory
- Boot from ROM memory
- Boot from SRAM

Table 13 Boot modes

BOOT1	BOOT0	Boot Mode
0	0	Boot from eFlash (0x0800_0000)
0	1	Boot from ROM (0x1FFF_0000)
1	0	Boot from SRAM (0x2000_0000)
1	1	Reserved, default Boot from eFlash

The boot pins are shared with standard GPIO and they only work as boot mode selection function when chip reset pin is kept in low state. The BOOT0/1 logic state should be kept on the defined boot mode stably without any change before RSTB pin completed the toggling from low to high.

The bootloader program is saved in ROM. When the chip is booted from ROM, the bootloader will manage to do the Flash memory downloading through UART1 from UART1TX/UART1RX pins.

7.6 Clocks and Reset

7.6.1 Clock

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

It features:

- **Clock prescaler:** to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching:** clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source:** three different sources can deliver SYSCLK system clock:
  - 4-48 MHz high-speed oscillator with external crystal or ceramic resonator (HSE). It can supply clock to system PLL. The HSE can also be configured in bypass mode for an external clock.
  - 16 MHz high-speed internal RC oscillator (HSI16), trimmable by software. It can supply clock to system PLL.
  - System PLL with maximum output frequency of 96 MHz. It can be fed with HSE or HSI16 clocks.
- **Auxiliary clock source:** two ultra-low-power clock sources for the real-time clock (RTC):
  - 32.768 kHz low-speed oscillator with external crystal (LSE), supporting four drive capability modes. The LSE can also be configured in bypass mode for using an external clock.
  - 32 kHz low-speed internal RC oscillator (LSI) with ±5% accuracy, also used to clock an independent watchdog.
- **Peripheral clock sources:** several peripherals (UARTs, I2Cs, ADC) have their own clock independent of the system clock.

Several prescalers allow the application to configure AHB and APB domain clock frequencies, 96 MHz at maximum.

7.6.2 Reset

During and upon exiting reset, most of the IO are configured to high-Z output with input Schmitt trigger buffer disabled so as to reduce power consumption.

7.7 Power Supply Management and Operation Mode

7.7.1 Power supply schemes

The XT32H05x devices support single power supply (VSUP) from 1.8 V to 5.5 V, other core voltages are generated by internal integrated LDOs.

7.7.2 Power supply supervisor

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes except deep-sleep mode and ensuring proper operation upon power-on and power-down. It maintains the device in reset when the supply voltage is below $V_{POR/PDR}$ threshold, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the VSUP power supply and compares it to V_{PVD} threshold. It allows generating an interrupt when VSUP level crosses the V_{PVD} threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

7.7.3 Voltage regulator

Three embedded linear voltage regulators, analog regulator (ANA_LDO) supply most of analog circuitry in the device, core regulator (CORE_LDO) supply most of digital circuitry in the device, flash regulator (FLASH_LDO) supply the second power supply for embedded Flash macro in the device.

One dedicated ultra-low power regulator is integrated in the device to provide power supply for the circuits which are continue working under chip deep sleep mode.

7.7.4 Operation modes

By default, the microcontroller is in run mode after system or power reset. It is up to the user to select one of the low-power modes described below:

- Run Mode
- Sleep Mode
- Deep Sleep Mode (Standby Mode)

7.7.4.1 Run Mode

In run mode, all functional blocks can operate normally. To achieve low power consumption in run mode, users can config different functional modules to be enabled or disabled, and users can config system clock frequency to be higher or lower through software.

7.7.4.2 Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

7.7.4.3 Standby mode

The Standby mode is used to achieve the lowest power consumption. In this mode, only modules in always-on power domain are powered on. The other modules in V_{CORE} power domain are powered off. E.g. The PLL, as well as the HSI16 RC oscillator and the HSE crystal oscillator are powered off. The 32kHz XTAL, 32kHz RC Oscillator, and several Ios can remain active.

For each I/O not located in always-on power domain, it will be set as high-Z output automatically.

The device exits standby mode upon external reset wakeup trigger, WDTI reset event, RTC event (alarm, periodic wakeup, timestamp), dedicated wakeup controller.

7.8 General purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function (AF). Most of the GPIO pins are shared with special digital or analog functions.

Through a specific sequence, this special function configuration of I/Os can be locked, such as to avoid spurious writing to I/O control registers.

7.9 Direct Memory Access (DMA)

7.9.1 DMA Controller (DMAC)

The direct memory access controller (DMAC) works as an AHB master. It can access related modules through a 2-master 2-layer AHB bus matrix. It's configuration registers can be accessed by CPU as an AHB slaver.

With 8 channels, it can manage data transfers between memory-mapped peripherals and/or memories, to offload the CPU.

Each channel is dedicated to managing memory access requests from one or more peripherals. The unit includes an arbiter for handling the priority between DMA requests.

Main features of the DMA Controller:

- Single-AHB master
- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral data transfers
- Access, as source and destination, to on-chip memory-mapped devices such as Flash memory, SRAM, and AHB and APB peripherals

- All DMA channels independently configurable:
  - Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
  - Priority between the requests is programmable by software (four levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
  - Transfer size of source and destination are independent (byte, half-word, word), emulating packing and unpacking. Source and destination addresses must be aligned on the data size.
  - Support of transfers from/to peripherals to/from memory with circular buffer management
  - Programmable number of data to be transferred: 0 to 2^{16} - 1
- Generation of an interrupt request per channel. Each interrupt request originates from any of the three DMA events: transfer complete, half transfer, or transfer error.

7.9.2 DMA Request Multiplexer (DMAMUX)

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

7.10 Interrupt Controller (ICTL)

The device flexibly manages events causing interrupts of linear program execution, called exceptions. The Cortex-M0+ processor core, a nested vectored interrupt controller (NVIC) and an extended interrupt/event controller (EXTI) are the assets contributing to handling the exceptions. Exceptions include core-internal events such as, for example, a division by zero and, core-external events such as logical level changes on physical lines. Exceptions result in interrupting the program flow, executing an interrupt service routine (ISR) then resuming the original program flow.

The processor context (contents of program pointer and status registers) is stacked upon program interrupt and unstacked upon program resume, by hardware. This avoids context stacking and unstacking in the interrupt service routines (ISRs) by software, thus saving time, code and power. The ability to abandon and restart load-multiple and store-multiple operations significantly increases the device's responsiveness in processing exceptions.

7.10.1 Nested Vectored Interrupt Controller (NVIC)

The configurable nested vectored interrupt controller is tightly coupled with the core. It handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions. It provides flexible priority management.

The tight coupling of the processor core with NVIC significantly reduces the latency between interrupt events and start of corresponding interrupt service routines (ISRs). The ISR vectors are listed in a vector table, stored in the NVIC at a base address. The vector address of an ISR to execute is hardware-built from the vector table base address and the ISR order number used as offset.

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency.

Key features of the NVIC include:

- Low-latency interrupt processing
- priority levels
- Handling of a non-maskable interrupt (NMI)
- Handling of 32 maskable interrupt lines
- Handling of 10 Cortex-M0+ exceptions
- Later-arriving higher-priority interrupt processed first
- Tail-chaining
- Interrupt vector retrieval by hardware

7.10.2 Extended Interrupt/event controller (EXTI)

The extended interrupt/event controller adds flexibility in handling physical line events and allows identifying wake-up events at processor wakeup from stop mode.

The EXTI controller has a number of channels, of which some with rising, falling or rising, and falling edge detector capability. Any GPIO and a few peripheral signals can be connected to these channels. The channels can be independently masked.

The EXTI controller can capture pulses shorter than the internal clock period.

A register in the EXTI controller latches every event even in stop mode, which allows the software to identify the origin of the processor's wake-up from stop mode or, to identify the GPIO and the edge event having caused an interrupt.

7.11 Cyclic Redundancy Check (CRC)

The Cyclic Redundancy Check (CRC) calculation unit is used to get a CRC code using a configurable generator polynomial value and size. It can be used to verify data transmission or storage integrity, like verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location. The key features of CRC include:

- Support 4 polynomials
  - CRC-32 (0x41c11db7):
    $$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$$
  - CRC-16 (0x1021): $x^{16} + x^{12} + x^5 + 1$
  - CRC-16 (0x8005): $x^{16} + x^{15} + x^2 + 1$
  - CRC-8 (0x07): $x^8 + x^2 + x^1 + 1$
- Support the reflecting of input and output data
- Support XOR mask

7.12 Motor Drive Unit (MDU)

Motor Drive Unit (MDU) is a sub-system module for different motor drive applications. It includes Programmable-Gain Amplifier, ADC, ADC Controller, Analog comparator and DAC. The key features of MDU include:

- Support synchronous sampling for maximum 4 pairs of differential channels
- Support single conversion mode and continuous conversion mode
- Support hardware trigger and software trigger
  - 1 software trigger source
  - 14 hardware trigger sources configurable
  - rising/falling edge trigger configurable
- Support group operation:
  - Up to 8 regular groups with separated trigger sources
  - Up to 4 injection groups with separated trigger sources
  - Injection group conversion can break regular group conversion immediately
- Support single scan mode and dis-continuous scan mode
- EOC, EOS interrupt flag generation configurable
- 3 analog watch-dogs real-time monitoring the conversion results, and generate the overflow, in-range, under overflow event indicators
- Support DMA data transfer

7.12.1 Programmable-Gain Amplifiers (PGA)

Device integrates four programmable-gain amplifiers; the loop gains are configurable independently each other by software. It can be used as four pairs of differential pre-amplifiers or differential to single-end input buffers of ADC channels, also it can be used as gain amplifiers for analog comparators' input signals.

7.12.2 Analog-to-digital converter (ADC)

A native 12-bit analog-to-digital converter is embedded into XT32H05x devices. The resolution is 12bit, 10bit or 8bit configurable.

The ADC supports up to maximum 43 external channels. Channel 0 ~ 3, and channel 12 ~ 27 are single-end (without PGA) or differential-end (with PGA) configurable. Channel 4 ~ 11 and channel 28 ~ 43 are single-end channels without PGA. Channel 53 ~ 62 are reserved to chip internal channels for VBG, VTS, VBS and other defined reference voltages.

It performs conversions in single mode or scan mode. In scan mode, it supports continues conversion or discontinuous conversion to the channels defined in different groups. There are two types of priority groups, injection group and regular group. The priority of injection group is higher than the priority of regular group. Once there is a conversion trigger for injection group channels, ADC controller will stop the on-going regular group channels' conversions, and it will start the injection group channels conversion immediately. After all the injection group channels conversions are completed, ADC controller will resume the regular group channels conversion sequence from the un-finished conversion channel.

For injection groups, it can support maximum 4 channels with four dedicated triggers. For regular groups, it can support maximum 8 sub-groups, and maximum 32 channels in each sub-group.

The operation frequency of ADC clock is independent from the CPU system clock, it can be up to 32MHz for maximum sampling rate of ~2 Msps even with a low CPU speed.

The ADC can be served by the DMA controller. It can operate in the whole VSUP supply range.

Up to three analog watchdogs can help to monitor the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The conversion trigger source of each channel/group is software configurable, including the events generated by the General-purpose timers (TIM_G), Advanced timer (TIM_A), Basic timer (TIM_B) or other hardware/software events. They are wire connected to the ADC trigger source control directly, allowing the application to start A/D conversions with timer events or other events directly.

7.12.3 Digital-to-Analog Conversion

Device integrated two 8bit DAC to generate different reference voltages for the analog comparators inside the chip. Also the DACs can be used to generate programmed analog voltages to chip outside.

7.12.4 Comparators (COMP)

Four embedded high-speed rail-to-rail analog comparators are integrated, they can be used to wake up the device, generate interrupts, breaks or triggers for the timers and can be also combined into a window comparator. The reference voltage source is configurable, it can be the comparator's input voltage from chip outside or reference voltage from internal programmed DAC.

7.13 Digital Control Engine (DCE)

A digital control engine is designed to provide loop acceleration for digital PFC applications, also can provide math accelerator for sensor-less FOC applications. It is a hardware software co-design solution. SDK will provide related functions for parameters setting and results calling.

7.14 Timers and watchdogs

The device integrated two 16bit advanced timers, four 16bit general purpose timers, two 32-bit basic timers, two watchdog timers and a SysTick timer. Table 14 compares features of the advanced-control, and general-purpose timers.

Table 14 Timer feature comparison

Timer type	Timer name	Counter resolution	Counter type	Maximum operating frequency	Prescaler factor	DMA	Capture/ compare channels	Complementary outputs pairs
Advanced Timer	TIM-A1	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3
	TIM-A2	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3
General Purpose Timer	TIM-G1	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3
	TIM-G2	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3
	TIM-G3	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3
	TIM-G4	16-bit	Up, down, up/down	96 MHz	Integer from 1 to 2^{16}	Yes	4	3

7.14.1 Advanced Timer (TIMA1, TIMA2)

The advanced timer can be seen as a three-phase PWM unit multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time inserted. It can also be seen as a complete general-purpose timer.

Features of advanced timers include:

- 16-bit up, down, up and down auto-load counter
- 16-bit programming prescaler
- Up to 6 independent channels for:
  - Input capture (excluding channel 5 and channel 6)
  - Output comparation
  - PWM generation (edge and centre-aligned)
  - One-pulse mode output
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals or to connect several timers together as a timer link
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- 2 bidirectional break inputs
- Supports incremental encoder and hall-sensor circuitry for positioning purpose
- Interrupts generator
- Configure by DMA
- Trigger input for external clock

In debug mode, the advanced timer counter can be frozen and the PWM outputs disabled, so as to turn off any power

switches driven by these outputs.

Many features are shared with those of the general-purpose timers using the same architecture, so the advanced timers can work together with the TIMG via the Timer Link feature for synchronization or event chaining.

7.14.2 General-purpose timers (TIMG1, TIMG2, TIMG3, TIMG4)

The general-purpose timers are designed with the same architecture as the advanced timers.

The features of general-purpose timers include:

- 16-bit up, down, up and down auto-load counter
- 16-bit programming prescaler
- Up to 6 independent channels for:
  - Input capture (excluding channel 5 and channel 6)
  - Output comparation
  - PWM generation (edge and center-aligned)
  - One-pulse mode output
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals or to connect several timers together as a timer link

Many features are shared with those of the general-purpose timers using the same architecture, so the advanced timers can work together with the TIMG via the Timer Link feature for synchronization or event chaining.

7.14.3 Basic Timers (TIMB1, TIMB2)

The basic timer is 8~32bit programmable counting down timer, each timer includes four identical but separately programmable timers. The timers count down from a programmed value and generate an interrupt when the count reaches zero. Key features of the basic timer include:

- 8~ 32bits programmable counting down counter
- Support two operation modes:
  - Free-running mode: when a timer counts down to 0, it will load the maximum value and counter wrapping to this maximum value.
  - User-defined count mode: when a timer counts down to 0, it will load the pre-defined value in register TIMERx_LDR, and counter wrapping to this define value.
- Interrupt generation
  - Polarity configurable
  - Single or combined interrupt flag configurable
- Initial value is loaded for each timer when:
  - timer is enabled after being reset or disabled, or
  - timer counts down to 0.

7.14.4 Independent Watchdog Timer (WDTI)

The independent watchdog can be used to supervise the operation of the device, specifically code execution. It can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of WDTI include:

- 32-bit counting down counter
- 32 kHz RC or 32kHz XTAL selectable clock
- Interrupt generation configurable
- Operating in deep sleep mode supported

7.14.5 Window Watchdog Timer (WDTW)

The windowed watchdog can be used to supervise the operation of the device, specifically code execution. It can be used to generate a reset or an interrupt if the application software does not successfully reset the watchdog within a specified window of time. Key features of WDTW include:

- 32-bit counting down counter
- Programmable clock divider
- Programmable clock source

- interrupt generation configurable

7.14.6 SysTick Timer

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter. Key features of SysTick timer include:

- 24-bit down counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

7.15 Real-time clock (RTC)

The real-time clock (RTC) operates with a 32kHz clock source and provides a time base to the application with multiple options for interrupts to the CPU. Key features of the RTC include:

- Calendar with seconds, minutes, hours (12 or 24 format), weekday, date, month and year
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- One programmable alarm
- 32-bit auto-reload deep sleep wakeup timer for periodic events, with programmable period
- Multiple clock sources and references:
  - A 32.768 kHz external crystal (LSE)
  - An external 32kHz clock
  - A 32kHz internal low-power RC oscillator (LSI)
- Events can generate an interrupt and wake the device up from deep sleep mode

7.16 Inter-integrated circuit interface (I2C)

The inter-integrated circuit interface (I2C1, I2C2) peripherals in device provide bidirectional data transfer with other I2C devices on the bus. It controls all I2C-bus-specific sequencing, protocol, arbitration and timing. Two I2C modules are integrated in the device. Their key features include:

- 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
- Slave and master modes, multiple master capability
- Support standard mode with a bitrate up to 100 kbit/s
- Support fast mode with a bitrate up to 400 kbit/s
- Support fast mode plus with a bitrate up to 1000 kbit/s
- Support high-speed mode with a bitrate up to 3.4 Mbit/s
- Programmable setup and hold time
- Clock stretching
- Independent source clock
- Programmable digital noise filters
- Support DMA Operation

7.17 Universal Asynchronous Receiver Transmitter (UART1/2/3/4)

The device embeds universal synchronous/asynchronous receivers/transmitters (UART1, UART2, UART3, UART4) that communicate at speeds of up to 6 Mbit/s. UART1, UART2 can provide hardware management of the CTS, RTS and RS232 DE signals. UART3 and UART4 can only provide general two lines asynchronous data transmission. Key features of these UART include:

- Standard asynchronous communication bits for start, stop and parity
- Fully programmable serial interface
  - Programmable baud rate generation with oversampling by 16, 8 or 3
  - Programmable character of 5, 6, 7 or 8 data bits
  - 1, 1.5 or 2 stop bit generation
  - Even, odd, stick, or no-parity bit generation and detection
- Separated transmit and receive FIFOs support DMA data transfer
- Support transmit and receive loopback mode operation

- Support auto flow control mode (UART1, UART2)
- IrDA SIR mode with up to 115.2 kBaud data rate
- Generate interrupts

Table 15 UART implementation

UART modes/features	UART1 UART2	UART3 UART4
Hardware flow control for modem	X	
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

7.18 Serial peripheral interface (SPI1, SPI2)

The two serial peripheral interfaces (SPI1, SPI2) in the device support the following key features:

- Bit rate up to 12 Mbits/s
- Configurable as master or slaver
- Configurable chip selection for both master and slaver
- Programmable data frame size from 4 bits to 16 bits
- Programmable clock prescaler for master
- Support half-duplex, full-duplex and simplex communications
- Support TI mode and Motorola mode
- Separated transmit and receive FIFOs supporting DMA data transfer

7.19 LED Driver (LED)

A light-emitting diode (LED) driver is implemented in device. It is a constant current common-anode LED driver, and it can be used to drive LEDs or 7-segment digits directly. Key features of LED driver include:

- Up to 8 COM, 9 SEG
- Drive up to 8 monochrome 7-segment digits or 64 discrete LEDs
- Support two display mode: static mode and dimming mode
- Support two run mode: on-off mode and duty mode
- Slow turn-on and turn-off time programmable
- Support DMA data transfer
- Up to 20mA current capability per channel
- 5bit analog DC current control and 8bit digital PWM dimming control

7.20 Capacitance touch sensing module (CTSM)

The capacitive touch sensing module (CTSM) is a low-power, compact, flexible touch sensing module that converts capacitance generated between the human body and a conductive touch pad to digital data without any analog signal processing. The key features of the CTSM include:

- Support self-capacitance sensing

- Support mutual capacitance sensing
- Up to 32 self-capacitance channels or 16 pairs mutual capacitance channels
- Support auto-correction and auto judgement
- Support DC current measurement and offset current adjustment
- Measurement time programmable
- Measurement frequency programmable
- Support software trigger and external trigger
- Support data auto transfer for the measurement configuration data and measurement results data

7.21 Device Electronic Signature (UID - unique device ID)

The 96bit unique device identifier (UID) is implemented in device. It is unique for any device and can never be altered by the user. It can be read out by CPU and can be used as serial numbers or security keys for different usages.

7.22 Hardware divider (HDIV)

The hardware divider in XT32H05x device is a 32bit pipeline divider. It can offload the mathematical calculations performed by the CPU to improve efficiency and CoreMark performance. The key features of this hardware divider include:

- 32bit divider for signed number divider
- 2 pipeline stages

7.23 Serial wire debug port (SW-DP)

The ARM Cortex-M0+ core provides integrated on-chip debug function. It consists of the following parts:

- SW-DP: Serial Wire debug port
- AHP-AP: AHB access port
- FPB: Flash patch breakpoint
- DWT: Data watch point trigger

For more information about the debugging interface, please refer to the ARM official manual and the ARM development tool set technical reference manual.

XT32H05x serial device integrated the serial debug interface (SW-DP), which is a simplified version of the standard ARM Core Sight debug interface. The serial debug interface (SW-DP) provides a 2-pin (clock + data) interface for the AHP-AP module. The key features of this SW-DP interface include:

- Two wire debug interface
  - On-chip pullup and pulldown resistors for SWDIO and SWCLK, respectively, enabled by default
  - Support for disabling SWD functions to use SWD pins as general-purpose input/output pins
- Debug of the processor
  - Run, halt, and step debug support
  - 4 hardware breakpoints
  - 2 hardware watchpoints
  - Unlimited software breakpoints

8 Electrical characteristics

8.1 Absolute maximum ratings

Table 16 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
VSUP	External supply voltage	-0.3	6.0	V
VIN	Input voltage on any other pin	-0.3	6.0	V

Table 17. Current characteristics

Symbol	Ratings	Max	Unit
I_{VSUP}	Current into VSUP power pin (source)	250	mA
I_{VSS}	Current out of GND ground pin (sink)	250	
I_{IO}	Output current sink by any I/O and control pin	50	
	Output current sourced by any I/O and control pin (exclude LED function)	50	
I_{IO_SUM}	Total output current sink by sum of all I/Os and control pins	200	
	Total output current sourced by sum of all I/Os and control pins	200	

Table 18. Thermal characteristics

Symbol	Ratings	Min	Max	Unit
T_S	Storage temperature range	-65	150	°C
T_{J_MAX}	Maximum junction temperature		150	

8.2 Recommended Operating Conditions

Table 19. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VSUP	Power Supply Voltage	1.62		5.5	V
VSS	Ground		0		V
F_{HCLK}	Internal AHB clock frequency	0		96	MHz
F_{PCLK}	Internal APB clock frequency	0		48	
T_A	Ambient temperature	-40		105	°C
T_J	Junction temperature	-40		125	°C

8.3 DC Characteristics

Table 20. DC Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DDPST}	Operation Power Supply Voltage		1.8		5.5	V
V_{SS}	Power Ground		-0.3			V
V_{LDO}	LDO output Voltage			1.1		V
V_{BG}	Bandgap Voltage			1.1		V
I_{DD}	Operation Current of Normal run mode, executed from Flash	VDDPST = 5.0V, HCLK=96MHz			14	mA
I_{DD}		VDDPST = 3.3V, HCLK=96MHz			12	mA
I_{DD}		VDDPST = 2.5V, HCLK=96MHz			11	mA
I_{DD}		VDDPST = 1.8V, HCLK=96MHz			12	mA
I_{DD}	Operation Current of Normal run mode, executed from Flash	VDDPST = 5.0V, HCLK=48MHz			10	mA
I_{DD}		VDDPST = 3.3V, HCLK=48MHz			8	mA
I_{DD}		VDDPST = 2.5V, HCLK=48MHz			7.5	mA
I_{DD}		VDDPST = 1.8V, HCLK=48MHz			8	mA
I_{DD}	Operation Current of Normal run mode, executed from Flash	VDDPST = 5.0V, HCLK=16MHz			7.5	mA
I_{DD}		VDDPST = 3.3V, HCLK=16MHz			5.2	mA
I_{DD}		VDDPST = 2.5V, HCLK=16MHz			5.0	mA
I_{DD}		VDDPST = 1.8V, HCLK=16MHz			5.4	mA
I_{PWD}	Deepsleep Mode	VDDPST = 5.0V		5		uA
I_{PWD}		VDDPST = 3.3V		5		uA
I_{PWD}		VDDPST = 2.5V		5		uA
I_{PWD}		VDDPST = 1.8V		5		uA
R_{PLUP}	Internal Pull-Up Resistor	VDDPST = 5.0V		25		kΩ
R_{PLUP}		VDDPST = 3.3V		35		kΩ
R_{PLUP}		VDDPST = 2.5V		45		kΩ
R_{PLUP}		VDDPST = 1.8V		70		kΩ
R_{PLDN}	Internal Pull-Down Resistor	VDDPST = 5.0V		20		kΩ
R_{PLDN}		VDDPST = 3.3V		30		kΩ
R_{PLDN}		VDDPST = 2.5V		40		kΩ
R_{PLDN}		VDDPST = 1.8V		65		kΩ

8.4 AC Characteristics

8.4.1 Reset Timing

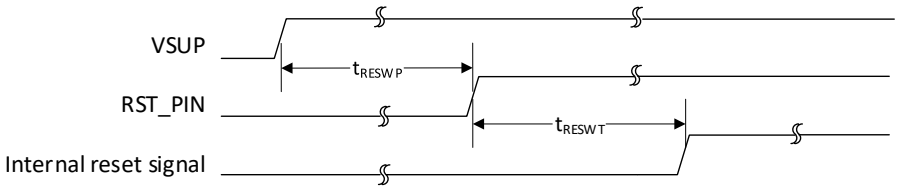


Figure 11 Reset Input Timing at Power-On

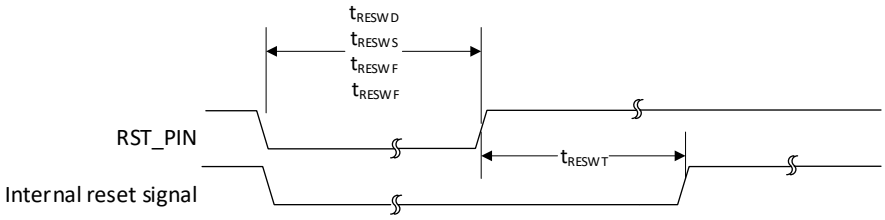


Figure 12 Reset Input Timing

8.4.2 SPI Interface Timing

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
f_{SPI}	SPI clock frequency				96	MHz
DC_{SCLK}	SCLK duty cycle		40	50	60	%
Master						
t_{SU_MISO}	MISO input data setup time		1			ns
t_{HD_MISO}	MISO input data hold time		0			ns
t_{VD_MOSI}	MOSI output data valid time				10	ns
t_{HD_MOSI}	MOSI output data hold time		6			ns
Slaver						
t_{SU_MOSI}	MOSI input data setup time		7			ns
t_{HD_MOSI}	MOSI input data hold time		0			ns
t_{VD_MISO}	MISO output data valid time				25	ns
t_{HD_MISO}	MISO output data hold time		5			ns

8.4.3 I2C Interface Timing

Symbol	Parameters	Test Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{I2C}	Input clock frequency		2	32	8	32	20	32	MHz
f_{SCL}	SCLK Clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	hold time (START)		4		0.6		0.26		us
t_{LOW}	Low period of SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us

8.4.4 UART Interface Timing

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
f_{SPI}	UART input clock frequency				96	MHz
DC_{SCLK}	Baud rate clock frequency				96	MHz

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Table 21. LDO Characteristics

(VSUP-VSS = 1.8 ~ 5.5V, T_A = -40 ~ 105ºC)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{LDO_CORE}	Output Voltage (LDO_CORE)		0.9	1.1	1.2	V
V_{LDO_ANA}	Output Voltage (LDO_ANA)		0.9	1.1	1.2	V
V_{LDO_ULL}	Output Voltage (LDO_ULL)		1.0	1.1	1.2	V
V_{LDO_FLASH}	Output Voltage (LDO_FLASH)		1.6	1.9	2.5	V

Notes:
All LDOs integrated inside the chip are capless LDO, so there is no package pins for 1.1V VDD.

8.5.2 High-Speed Crystal Oscillator

Table 22. High-speed crystal oscillator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Nominal Frequency		4	8	48	MHz
Internal Programmable Load Capacitance				10	pF
Startup time			2		ms
Power down current			430		nA
Current Consumption			450	940	uA

8.5.3 Low-Speed Crystal Oscillator

Table 23. Low-speed crystal oscillator Characteristics

Parameter		Min	Typ	Max	Units
Nominal Frequency			32.768		kHz
Internal Programmable Load Capacitance				10	pF
Startup time			2		s
Power down current			10		nA
Current Consumption			350	630	nA

8.5.4 High-Speed Internal RC Oscillator

Table 24. High-Speed RC Oscillator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Nominal Frequency	Ta=30 °C	15.92	16	16.08	MHz
	Ta = -40 ~ 105 °C	15.84	16	16.16	MHz
Frequency trimming step			0.5	1	%
Frequency trimming range		-32		32	%
Duty Cycle		45		55	%
Startup time			0.8	1.2	us
Stabilization time			3	5	us
Quiescent Current			155	190	uA

8.5.5 Low-Speed Internal RC Oscillator

Table 25. Low-Speed RC Oscillator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Nominal Frequency	Ta = 30 °C	31.04	32	32.96	kHz
	Ta = -40 ~ 105 °C	29		34	kHz
Frequency Tolerance over Temperature		-5%		5%	
Stabilization time	5% of final frequency		125	180	us
Power down current			10		nA
Quiescent Current			300		nA

8.5.6 PLL

Table 26. PLL Characteristics

Parameter	Condition	Min	Typ	Max	Units
Reference Clock Frequency		4	16	48	MHz
Output Clock Frequency		10	96	100	MHz
VCO frequency		230		420	MHz
PLL lock time			25	40	us
RMS cycle-to-cycle jitter	System clock 96MHz		50		ps
Quiescent Current	VCO frequency 384MHz		1		mA

8.5.7 Comparator

Table 27. Comparator Characteristics

Parameter	Condition	Min	Typ	Max	Units
Operation Supply Voltage		2.0		5.5	
Common Mode Voltage Range		0		VSUP	V
Input voltage range		0		VSUP	V
Comparator offset error	Full common mode range		5	20	mV
Comparator hysteresis voltage	no hysteresis		0		mV
	Low hysteresis		10		mV
	Mid hysteresis		20		mV
	High hysteresis		30		mV
Internal reference from DAC		0		VSUP	V
Comparator start-up time				5	us
Propagation delay	High speed mode, 200mV		30	60	ns
Quiescent Current	High-speed mode, static		250	520	uA
	High-speed mode, 50kHz square		250		uA

8.5.8 Programmable Gain Amplifier

Table 28. PGA Characteristics

Parameter	Condition	Min	Typ	Max	Units
Input Voltage Amplitude		0		Vout_max/(2G)	V
Output Voltage Range		0.1*VSUP		0.9*VSUP	V
Gain		2		15	
Gain Error	Gain = 2,3,4,5		1	2	
	Gain = 7,9,11,15		1.5	3	
Operation Stabilization wait time				5	us

8.5.9 12-bit SAR-ADC

Table 29. A/D Conversion Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution				12	bit
FADC	ADC Operation Frequency		0.016	16	32	MHz
FS	Sampling Rate	12bit		1	2	Msps
DNL	Differential Nonlinearity Error	VSUP = 5.0V		0.8		LSB
INL	Integral Nonlinearity Error	VSUP = 5.0V		2		LSB
Eo	Offset Error	VSUP = 5.0V		1		LSB
Eg	Gain Error (Transfer Gain)	VSUP = 5.0V		1		LSB
Ea	Absolute Error	VSUP = 5.0V		3		LSB
	Monotonic		Guaranteed			
TACQ	Acquisition Time (Sample Stage)	N: 1~ 256	1		256	1/FADC
TCONV	Conversion Time (ADC Core)	CLK=32MHz			12	1/FADC
IDDA	Operation Current of 5V AVDD (Avg)	VSUP = 5.0V		2		mA
IDDD	Operation Current of 1.1V DVDD (Avg)	VSUP = 5.0V		150		uA
VIN	Analog Input Voltage		0		VSUP	V
CIN	Input Capacitance			5		pF

8.5.10 LED Driver

Table 30. LED Driver Characteristics

Parameter	Condition	Min	Typ	Max	Units
COM DC Current				160	mA
SEG DC Current (Dimming Range)		0		20	mA
Current matching between channels	Iseg=16mA		1	3	%
	Iseg=2.5mA		2	3	%
Absolute Channel Current Accuracy	Iseg=16mA			4	%
	Iseg=2.5mA			6	%
Minimum Vdrop on SEG	ISEG=20mA		500		mV
Minimum Vdrop on COM	ICOM=160mA		700		mV

8.5.11 Capacitive Touch Sensing Module

Table 31. Capacitive Touch Sensing Characteristics

Parameter	Condition	Min	Typ	Max	Units
External Capacitance to TSCAP pin		9	10	11	nF
Base Capacitive Loading				50	pF
Minimum Sensiable Capacitive		50		100	fF
Quiescent $_{Current}$			100		uA

8.6 Embedded Flash Characteristics

Table 32. Embedded Flash Characteristics

Parameter	Condition	Min	Typ	Max	Units
Endurance		10k		100k	Cycle
Data Retention		10			year
Page Erase Time	for 10K Endurance			20	ms
	for 100K Endurance			100	ms
Mass Erase Time				100	ms
Program Time	Per group			15	us
Read Cycle Time				20	ns
Read Current	VDD=1.1V, Tcyc=20ns			4.2	mA
Program Current				6.7	mA
Erase Current				4.7	mA

Note:
The spec is DC average current, Peak current is much higher than the average current.

8.7 ESD & Latch-up Characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

8.7.1 ESD

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 33. ESD Rating

Symbol	Ratings	Conditions	Level	Maximum Value	Unit
V_{ESD}(HBM)	Electrostatic discharge voltage (human body model)	TA = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	3B	8000	V
V_{ESD}(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C, conforming to ANSI/ESDA/JEDEC JS-002	C3	2000	V

8.7.2 Latch-up

Table 34. Latch-up Rating

Parameter	Conditions	Class
I Trigger (+)	TA = +105 °C conforming to JESD78, 200mA	II
I Trigger (-)	TA = +105 °C conforming to JESD78, 200mA	II
V Supply Over Voltage Test	TA = +105 °C conforming to JESD78, 8.25V	II

8.8 EFT Characteristics

Table 35. EFT Rating

Condition	Package	Pass Level	Unit
Fsys, Internal RC	QFP64	4000	V
	QFP48	4000	V
	QFP44	4000	V
	QFN32	4000	V

8.9 IO Characteristics

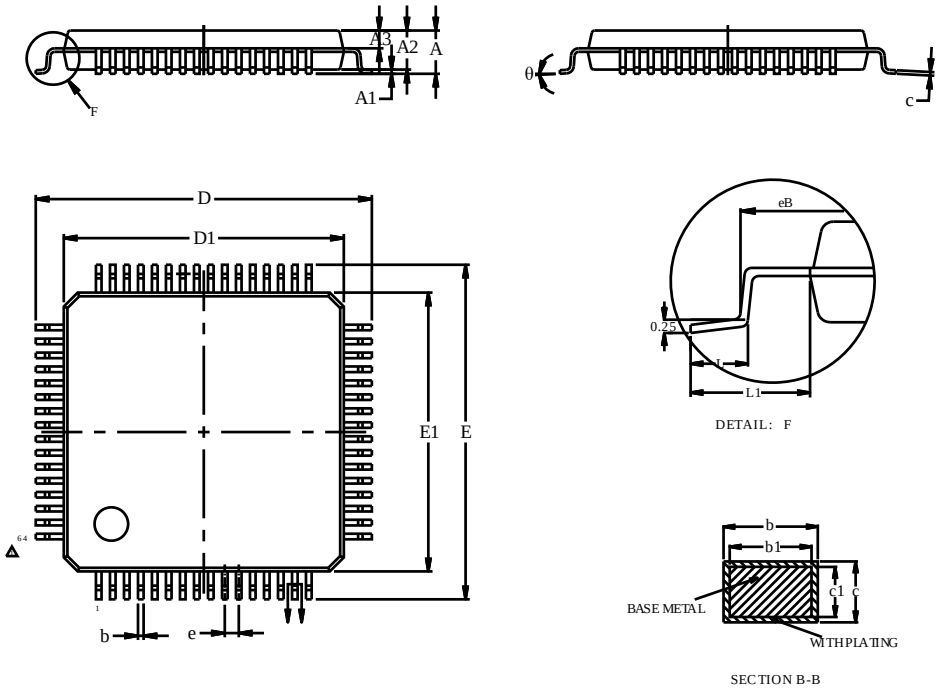
Table 36. IO Characteristics

Parameters	Condition	Min	Typ	Max	Unit
VDDPST		1.62	3.3	5.5	V
VDD		0.99	1.1	1.21	V
VIH		0.7*VSUP		6	V
VIL				0.3*VSUP	V
Vhys			200		mV
VOL	with IOL = 2mA			0.4	V
VOH	with IOH = 2mA	VSUP-0.4			V
Ileakage				3000	nA
Pullup	with VIN=VSUP	20	40	80	kΩ
Pulldown	with VIN=VSUP	20	40	80	kΩ
I/O pin cap			5		pF

9 Package Information

9.1 LQFP64 package information

LQFP64 is a 64-pin, 10 x 10 mm low-profile quad flat package

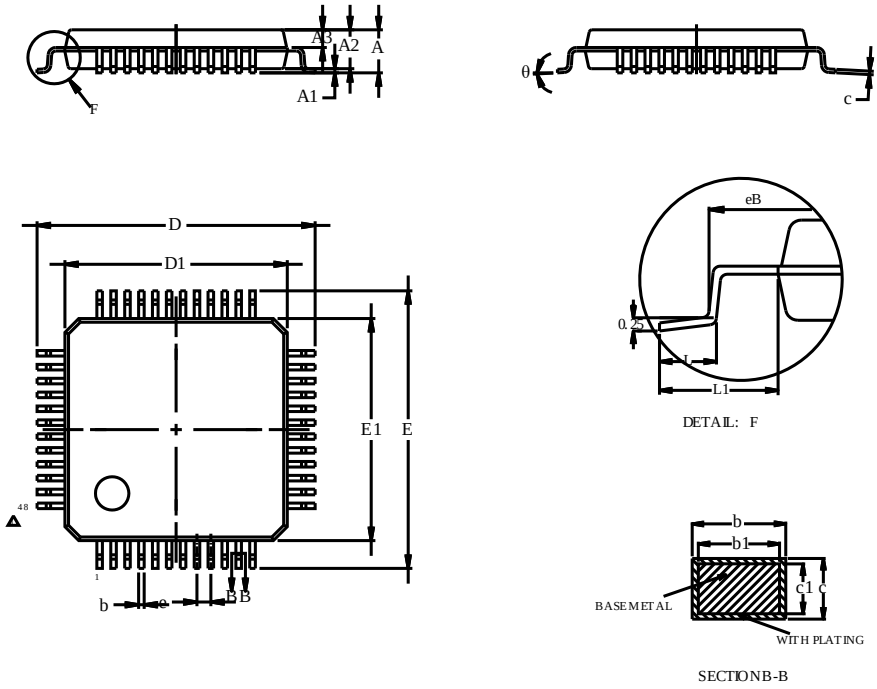


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.50BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 13 LQFP64 package outline

9.2 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package

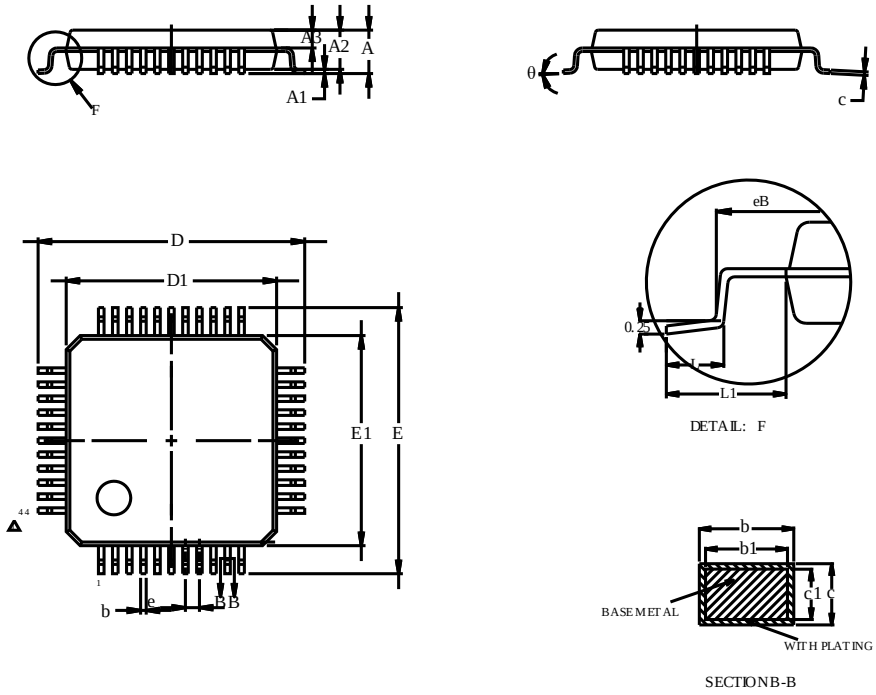


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
eB	8.10	—	8.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 14 LQFP48 package outline

9.3 LQFP44 package information

LQFP44 is a 44-pin, 10 x 10 mm low-profile quad flat package

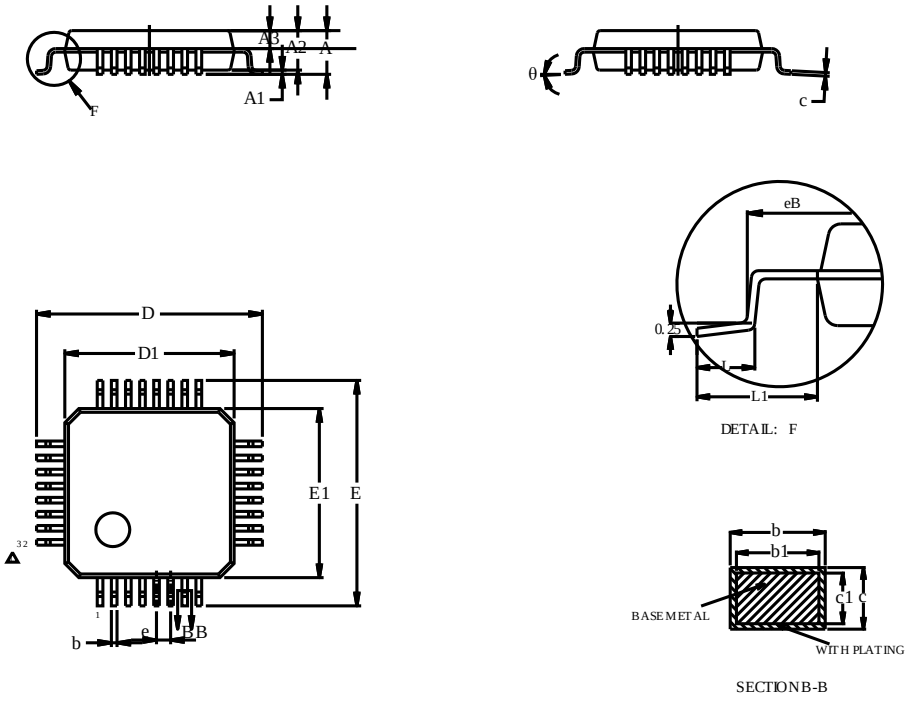


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.28	—	0.36
b1	0.27	0.30	0.33
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.80BSC		
eB	11.05	—	11.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 15 LQFP44 package outline

9.4 LQFP32 package information

LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
eB	8.10	—	8.25
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

Figure 16 LQFP32 package outline

9.5 Thermal characteristics

The operating junction temperature T_J must never exceed the maximum given in *Table 21: General operating conditions*.
The maximum junction temperature in °C that the device can reach if respecting the operating conditions, is:

$$T_J(max) = T_A(max) + P_D(max) \times \Theta_{JA}$$

where:

$$T_J(max) = T_A(max) + P_D(max) \times \Theta_{JA}$$

- $T_A(max)$ is the maximum operating ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D = P_{INT} + P_{I/O}$,
  - PINT is power dissipation contribution from product of IDD and VSUP
  - PI/O is power dissipation contribution from output ports
    where:
    $P_{I/O} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((VSUP_{IO1} - V_{OH}) \times I_{OH})$,
    taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 37 Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
ΘJA	Thermal resistance junction-ambient	LQFP64 10 × 10 mm	52	°C/W
		LQFP48 7 × 7 mm	69	
		LQFP44 10 × 10 mm	53	
		LQFP32 7 × 7 mm	55	

9.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (still air). Available from www.jedec.org

9.5.2 Selecting the product temperature range

The temperature range is specified in the ordering information scheme shown in Section 10: Ordering information.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and to a specific maximum junction temperature.

As applications do not commonly use microcontrollers at their maximum power consumption, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range best suits the application.

The following example shows how to calculate the temperature range needed for a given application.

Example:

Assuming the following worst application conditions:

- ambient temperature T_A = 50 °C (measured according to JESD51-2)
- I_{DD} = 50 mA; VSUP = 3.6 V
- 20 I/Os simultaneously used as output at low level with I_{OL} = 8 mA (V_{OL}= 0.4 V), and
- 8 I/Os simultaneously used as output at low level with I_{OL} = 20 mA (V_{OL}= 1.3 V)

the power consumption from power supply P_{INT} is:

P_{INT} = 50 mA × 3.6 V= 118 mW,

the power loss through I/Os P_{IO} is:

P_{IO} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW,

and the total power P_D to dissipate is:

P_{D} = 180 mW + 272 mW = 452 mW

For product in LQFP48 with Θ_{JA}= 75°C/W, the junction temperature stabilizes at:

T_J = 50°C + (75°C/W × 452 mW) = 50 °C + 33.9 °C = 83.9°C

As a conclusion, product version with suffix 6 (maximum allowed T_J = 105° C) is sufficient for this application.

If the same application was used in a hot environment with maximum T_A greater than 71°C, the junction temperature would exceed 105°C and the product version allowing higher maximum T_J would have to be ordered.

10 Ordering information

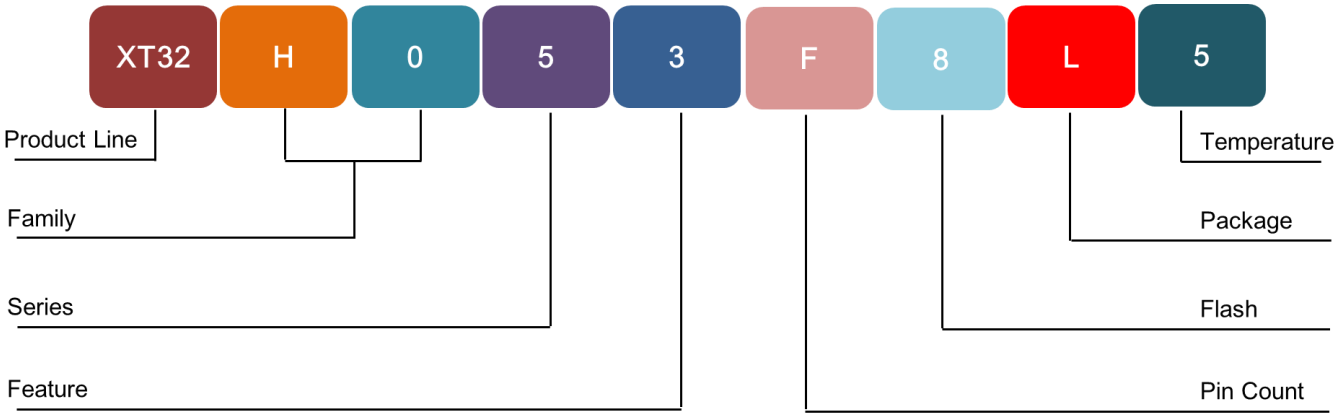


Figure 17 Device Nomenclature

Table 38 Device Nomenclature

Product Line	XT32: ARM Based 32Bit MCU
Family	H0: 5V I/O for harsh environment, Cortex-M0+ core
Series	5: High performance series
Feature	1: Touch control 3: Motor control
Pin Count	A: 20pin, B: 32pin, C: 44pin, D: 48pin E: 52pin, F:64pin, G: 80pin, H: 100pin
Flash	8: 160kB, 7: 128kB, 6: 96kB, 5: 64kB
Package Type	T: TSSOP L: LQFP Q: QFN
Temperature Range	3: -40 ~ 85 ℃ 5: -40 ~ 105 ℃ 7: -40 ~ 125 ℃

11 Revision History

Revision	Submission Date	Description of Change
0.1	25/5/2024	initial release
0.2	20/6/2024	update package and block diagram
0.3	4/7/2024	update ordering information
0.4	17/7/2024	update family members and ordering part number
0.5	19/7/2024	update block diagram and pinout
0.6	19/8/2024	update product and package information