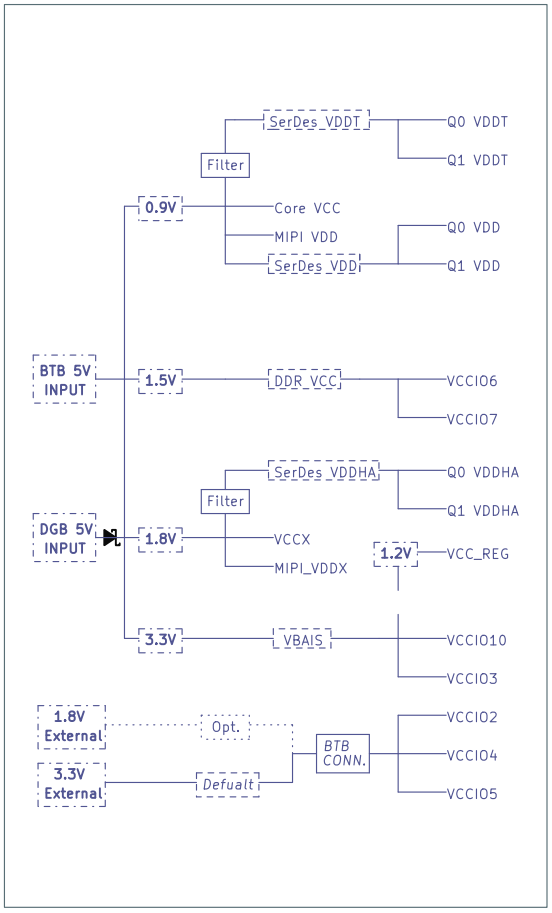

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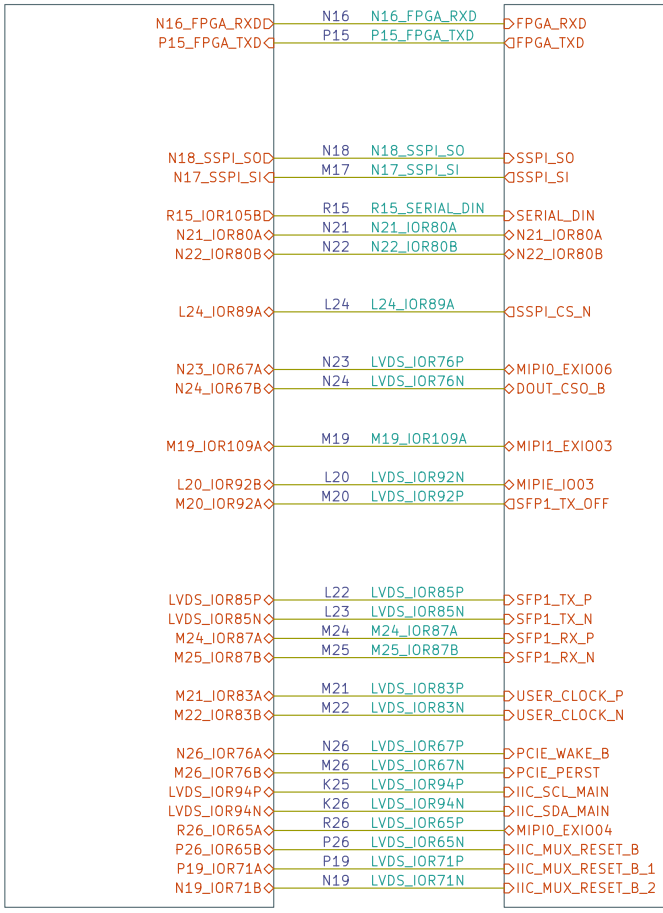

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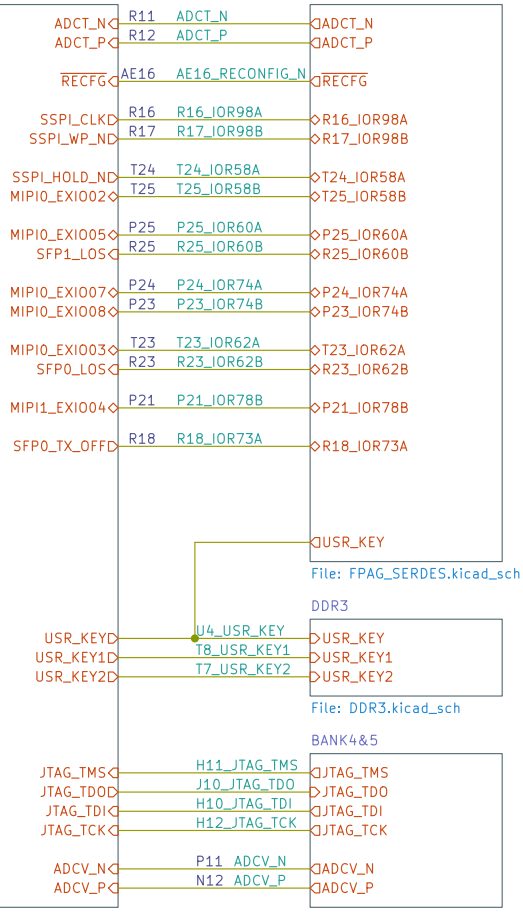
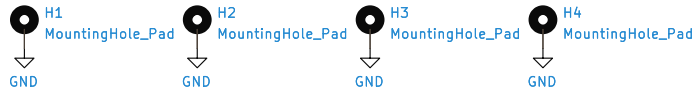




FPGA_VCC

File: FPGA_VCC.kicad_sch

FPGA_NC&GND

File: FPGA_NC&GND.kicad_sch

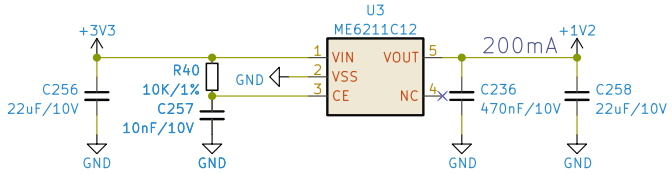
Shenzhen Sipeed Technology Co,Ltd.

Sheet: /
File: TANG_MEGA-138K_4071.kicad_sch

Title: TANG_MEGA-138K-Pro_4071_Schematics

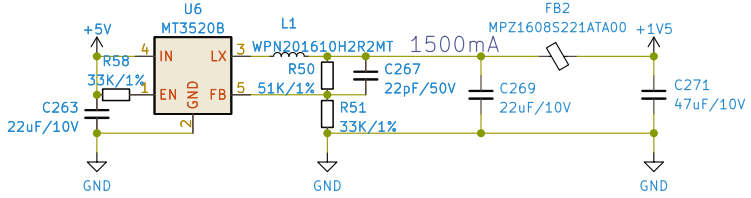
Size: A4	Date: 2023-07-07	**Rev: 1.00**
KiCad E.D.A. kicad (6.0.8)		Id: 1/9

1.2V LDO



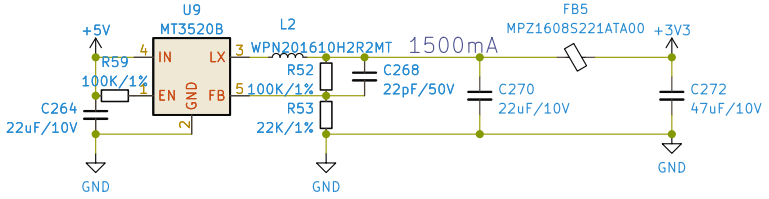
1V5 DC-DC

Vout=0.6*(1+51K/33K)≈1.53V



3V3 DC-DC

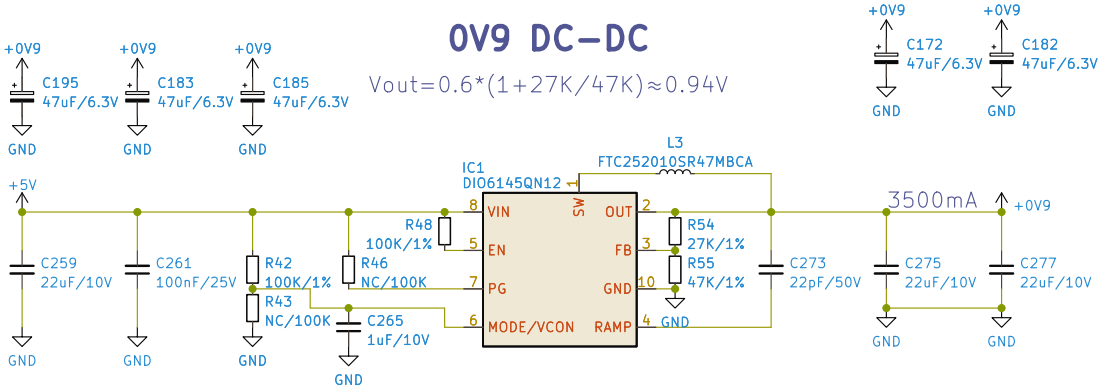
Vout=0.6*(1+100K/22K)≈3.33V



TEST POINTS

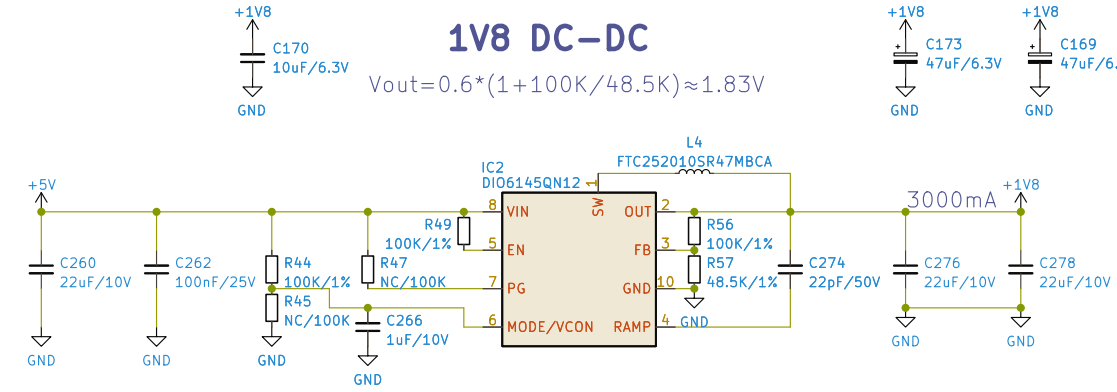
0V9 DC-DC

Vout=0.6*(1+27K/47K)≈0.94V



1V8 DC-DC

Vout=0.6*(1+100K/48.5K)≈1.83V



Shenzhen Sipeed Technology Co,Ltd.

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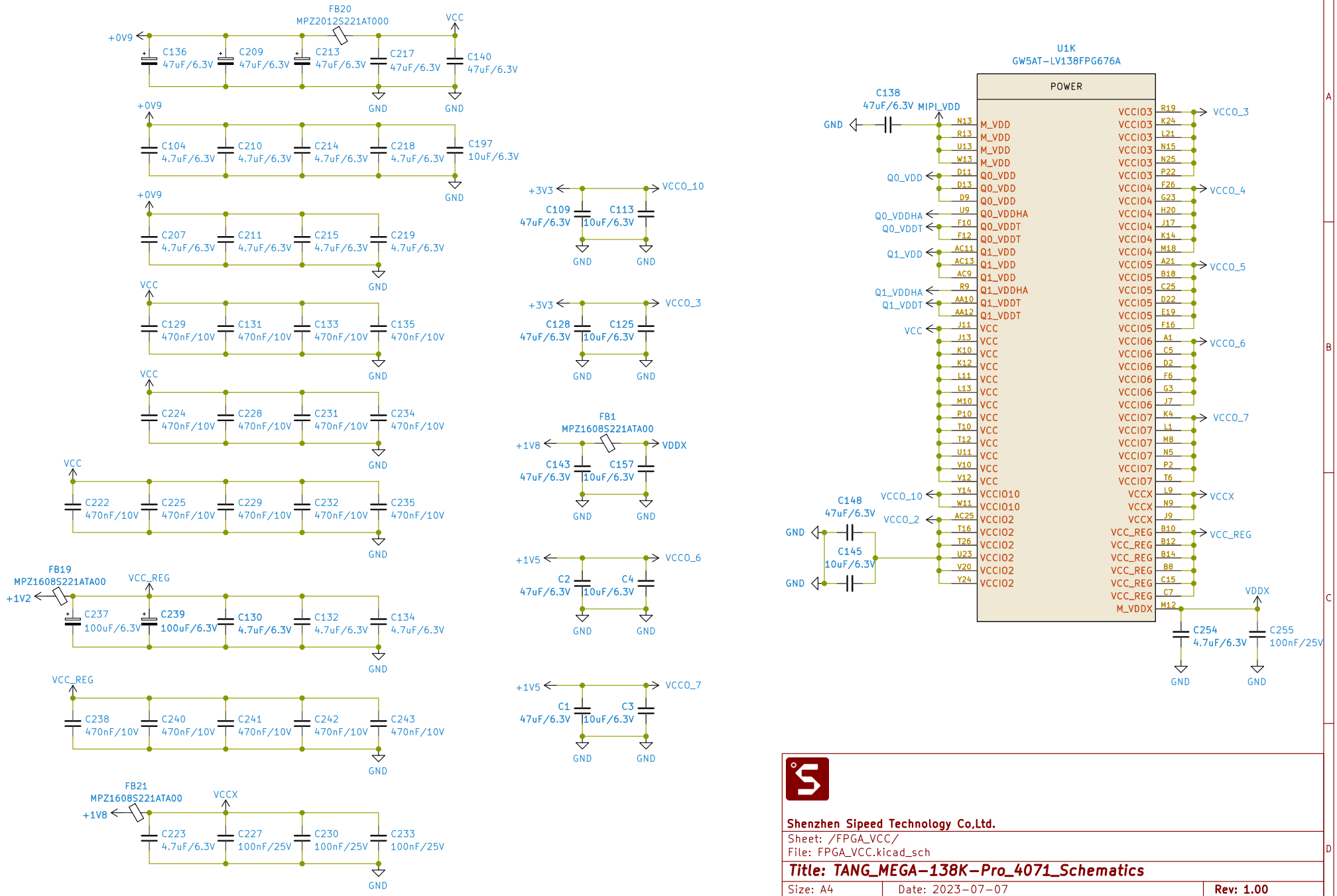
Title: TANG_MEGA-138K-Pro_4071_Schematics

Size: A4	Date: 2023-07-07	**Rev: 1.00**
KiCad E.D.A. kicad (6.0.8)		Id: 2/9



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Title: TANG_MEGA-138K-Pro_4071_Schematics	
Size: A4	Date: 2023-07-07
KiCad E.D.A. kicad (6.0.8)	Id: 3/9

Rev: 1.00


U1M
GW5AT-LV138FPG676A
GND
M11 VSS
AE15 VSS
B15 VSS
A10 VSS
A12 VSS
A14 VSS
A16 VSS
A26 VSS
A6 VSS
A8 VSS
AA14 VSS
AA16 VSS
AA26 VSS
AA6 VSS
AB10 VSS
AB12 VSS
AB14 VSS
AB23 VSS
AB3 VSS
AA9 VSS
AB8 VSS
AC15 VSS
AC20 VSS
AC7 VSS
AD11 VSS
AD13 VSS
AD6 VSS
AD9 VSS
AD16 VSS
AE24 VSS
AE4 VSS
AE6 VSS
AF1 VSS
AF10 VSS
AF12 VSS
AF14 VSS
AF21 VSS
AF16 VSS
AF6 VSS
AF8 VSS
B16 VSS
B23 VSS
B3 VSS
B6 VSS
C11 VSS
C13 VSS
C16 VSS
C20 VSS
C6 VSS
C9 VSS
D15 VSS
D17 VSS
D7 VSS
E10 VSS
E12 VSS
E14 VSS
E24 VSS
E4 VSS
E7 VSS
E8 VSS
VSS E9
VSS F1
VSS F14
VSS F21
VSS F9
VSS G10
VSS G11
VSS AB9
VSS G13
VSS Y12
VSS G18
VSS G12
VSS H25
VSS H5
VSS J12
VSS J22
VSS J2
VSS K11
VSS K13
VSS K19
VSS K9
VSS L10
VSS L12
VSS L16
VSS L26
VSS L6
VSS M13
VSS M23
VSS M3
VSS M9
VSS N10
VSS N20
VSS P13
VSS P17
VSS P7
VSS P9
VSS R10
VSS R24
VSS R4
VSS T1
VSS T11
VSS T13
VSS T21
VSS T9
VSS U10
VSS U12
VSS U18
VSS U8
VSS V15
VSS V25
VSS V5
VSS E15
VSS W12
VSS W2
VSS W22
VSS Y11
VSS Y10
VSS Y13
VSS Y19
VSS V13
GND
GND
U1L
GW5AT-LV138FPG676A
NC PADs
ATEST_O
AF15
NC/0R
R39
GND
AD15 NC
AD7 NC
AE10 NC
AE12 NC
AE14 NC
AE8 NC
AA1 NC
AC5 NC
AD2 NC
U3 NC
W7 NC
Y4 NC
G14 NC
P12 NC
N11 NC
AA21 NC
AB18 NC
AD22 NC
AE19 NC
AF26 NC
W17 NC
AA17 NC
AA18 NC
AA19 NC
AA20 NC
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AB16 NC
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AB19 NC
AB2 NC
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NC W15
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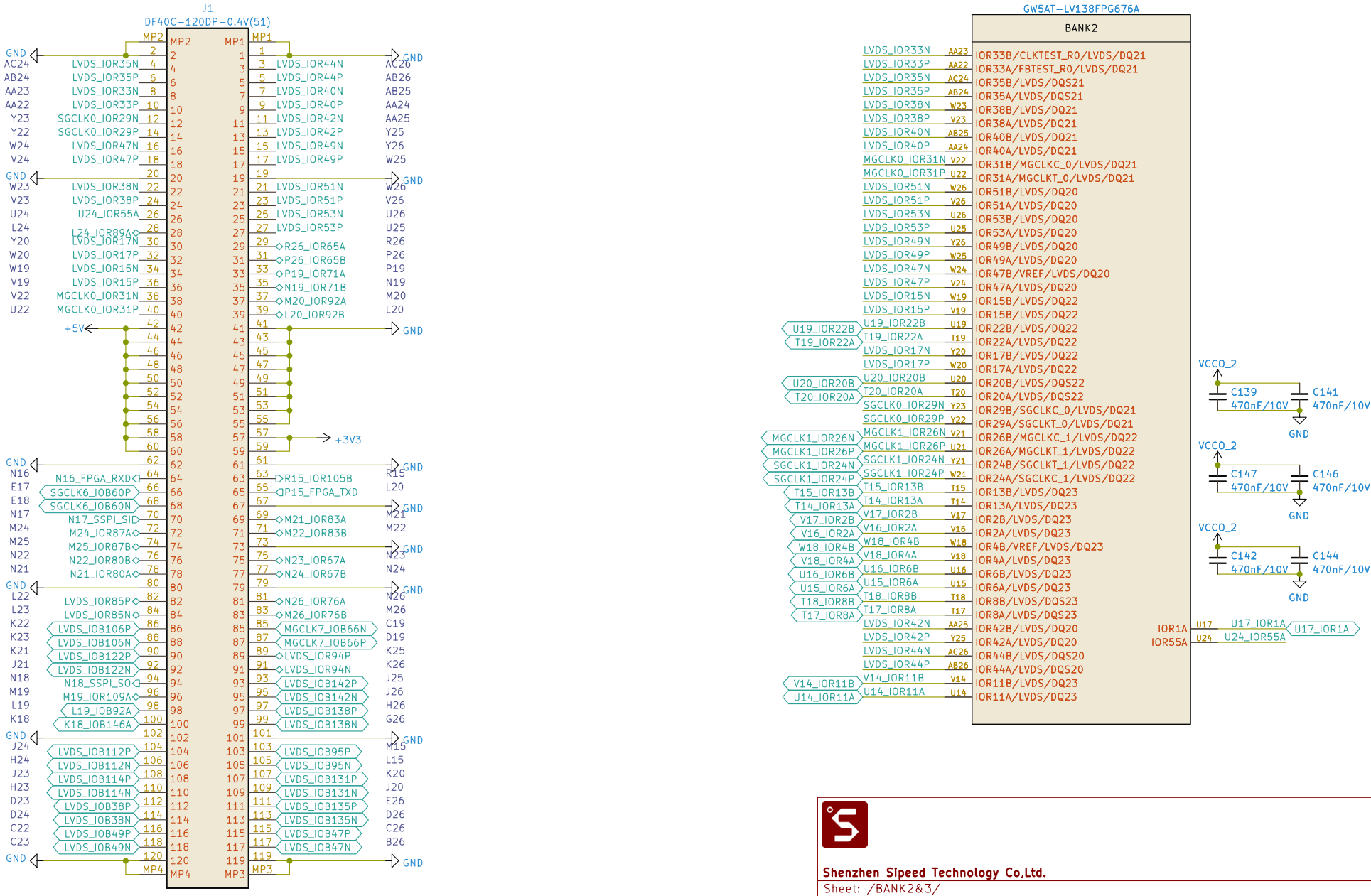
Size: A4
Date: 2023-07-07
Rev: 1.00
KiCad E.D.A. kicad (6.0.8)
Id: 4/9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DF40C-120DP-0.4V(51)
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IOR33A/FBTEST_R0/LVDS/DQ21
IOR35B/LVDS/DQS21
IOR35A/LVDS/DQS21
IOR38B/LVDS/DQ21
IOR38A/LVDS/DQ21
IOR40B/LVDS/DQ21
IOR40A/LVDS/DQ21
IOR31B/MGCLKC_0/LVDS/DQ21
IOR31A/MGCLKT_0/LVDS/DQ21
IOR51B/LVDS/DQ20
IOR51A/LVDS/DQ20
IOR53B/LVDS/DQ20
IOR53A/LVDS/DQ20
IOR49B/LVDS/DQ20
IOR49A/LVDS/DQ20
IOR47B/VREF/LVDS/DQ20
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IOR15B/LVDS/DQ22
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IOR22A/LVDS/DQ22
IOR17B/LVDS/DQ22
IOR17A/LVDS/DQ22
IOR20B/LVDS/DQS22
IOR20A/LVDS/DQS22
IOR29B/SGCLKC_0/LVDS/DQ21
IOR29A/SGCLKT_0/LVDS/DQ21
IOR26B/MGCLKC_1/LVDS/DQ22
IOR26A/MGCLKT_1/LVDS/DQ22
IOR24B/SGCLKT_1/LVDS/DQ22
IOR24A/SGCLKC_1/LVDS/DQ22
IOR13B/LVDS/DQ23
IOR13A/LVDS/DQ23
IOR2B/LVDS/DQ23
IOR2A/LVDS/DQ23
IOR4B/VREF/LVDS/DQ23
IOR4A/LVDS/DQ23
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IOR44B/LVDS/DQS20
IOR44A/LVDS/DQS20
IOR11B/LVDS/DQ23
IOR11A/LVDS/DQ23
IOR1A
IOR55A
VCCO_2
C139
470nF/10V
C141
470nF/10V
C147
470nF/10V
C146
470nF/10V
C142
470nF/10V
C144
470nF/10V
GND
+5V
+3V3
Shenzhen Sipeed Technology Co,Ltd.
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Date: 2023-07-07
Rev: 1.00
KiCad E.D.A. kicad (6.0.8)
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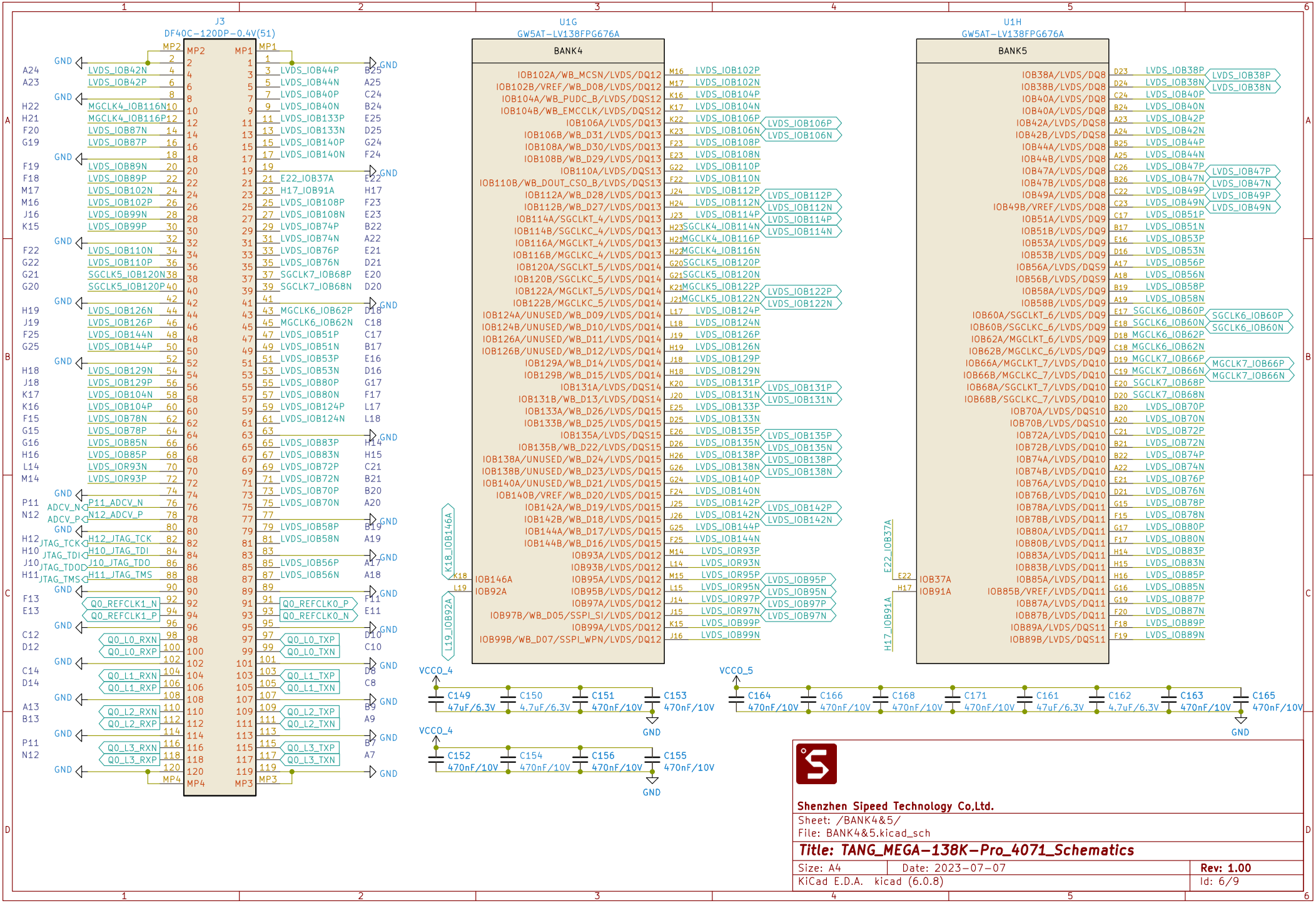
J3
DF40C-120DP-0.4V(51)
U1G
GW5AT-LV138FPG676A
BANK4
U1H
GW5AT-LV138FPG676A
BANK5
VCCO_4
VCCO_5
C149 47uF/6.3V
C150 4.7uF/6.3V
C151 470nF/10V
C153 470nF/10V
C152 470nF/10V
C154 470nF/10V
C156 470nF/10V
C155 470nF/10V
C164 470nF/10V
C166 470nF/10V
C168 470nF/10V
C171 470nF/10V
C161 47uF/6.3V
C162 4.7uF/6.3V
C163 470nF/10V
C165 470nF/10V
GND
Shenzhen Sipeed Technology Co,Ltd.
Sheet: /BANK4&5/
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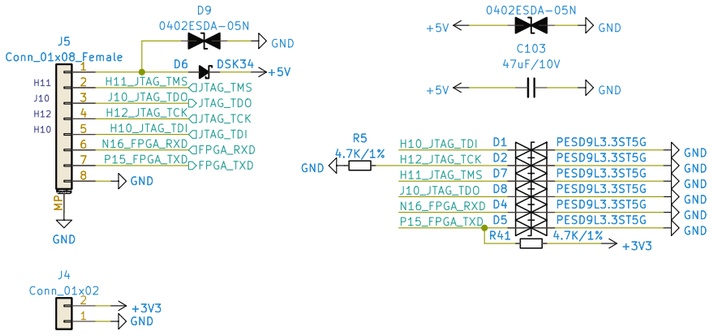
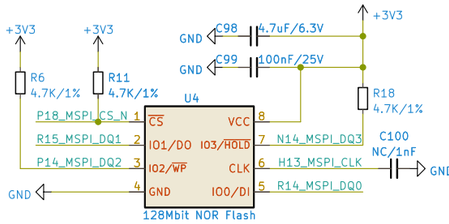
Title: TANG_MEGA-138K-Pro_4071_Schematics
Size: A4
Date: 2023-07-07
Rev: 1.00
KiCad E.D.A. kicad (6.0.8)
Id: 6/9

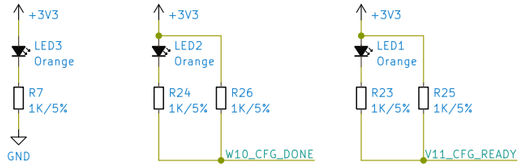
JTAG & UART



MSPI_FLASH



LEDs



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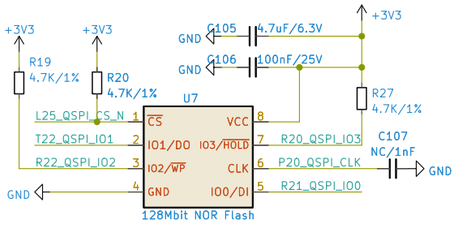
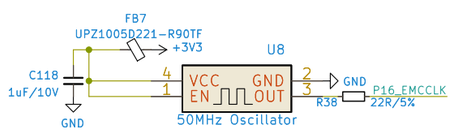
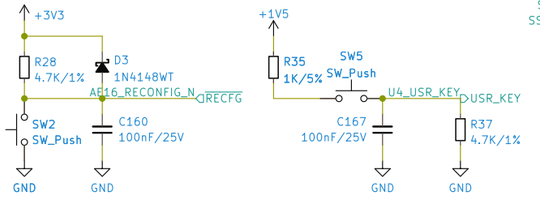


EMCCLK OSC.



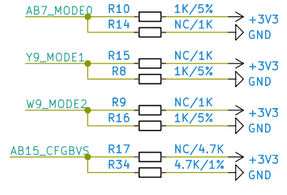
ADC INPUT

BUTTONs



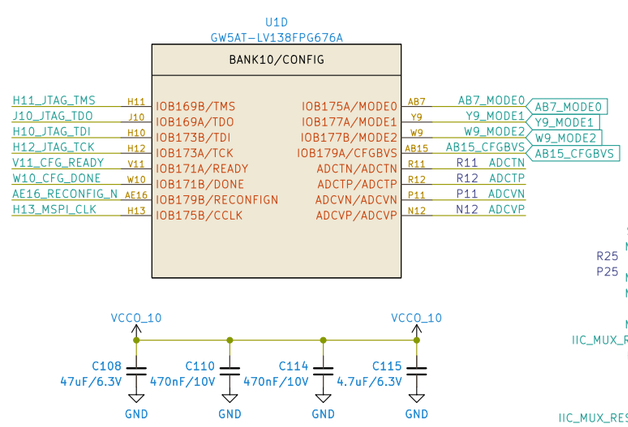
TESTPOINT

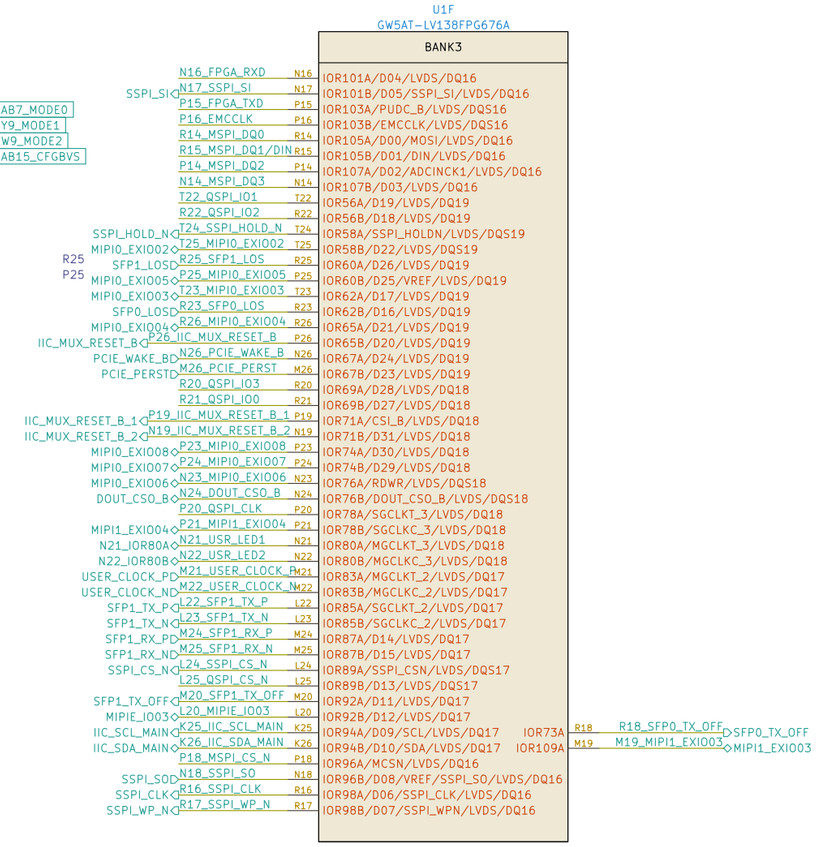
MODE SET

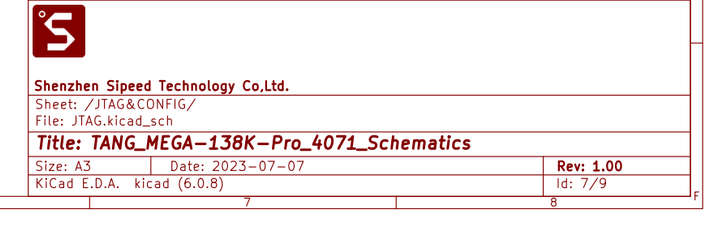


NOTE: MODE[0..2] is set to 001 by defualt.
Set CFGBVS to 1 to enable maximum driving of the pin during FPGA configuration

CONFIG	MODE2	MODE1	MODE0
JTAG	X	X	X
MSPI	0	0	1
SSPI	0	1	0
MSERIAL	0	0	0
SSERIAL	1	1	1
MCPU	1	0	0
SCPU	1	1	0







DDR3 512Meg x16 0#

DDR3 512Meg x16 1#

PIN TABLE FOR DDR

DATA DDR	DATA FPGA	MASK DDR	MASK FPGA	CLOCK DDR	CLOCK FPGA
D0	G4	LDM0	F4	CKP	M2
D1	J6	UDM0	H9	CKN	L2
D2	L8	LDM1	E3		
D3	G5	UDM1	A3		
D4	K7				
D5	J5	**DQS**			
D6	K8	**DDR**	**FPGA**		
D7	K6	SL0P	J4		
D8	E6	SL0N	H4		
D9	H8	SU0P	H7		
D10	H6	SU0N	G7		
D11	G8				
D12	D6	SL1P	B5		
D13	F8	SL1N	A5		
D14	G6	SL1P	C1		
D15	F7	SL1N	B1		
D16	C4	**CTRL**			
D17	F3	**DDR**	**FPGA**		
D18	B4	ODT	J1		
D19	E5	CKE	L3		
D20	D3	WE	J3		
D21	D5	CAS	H1		
D22	A4	RAS	H2		
D23	D4	CS	L4		
D24	E1	RST	N8		
D25	A2	**BANK**			
D26	G2	**DDR**	**FPGA**		
D27	C2	BA0	M4		
D28	F2	BA1	L5		
D29	E2	BA2	K3		
D30	G1				
D31	D1				

ADDR DDR	ADDR FPGA
A0	N1
A1	R1
A2	R2
A3	N2
A4	P1
A5	T2
A6	N4
A7	U1
A8	T4
A9	T3
A10	M1
A11	P4
A12	N3
A13	U2
A14	U5
A15	M6

DDR Power For VTT/VREF

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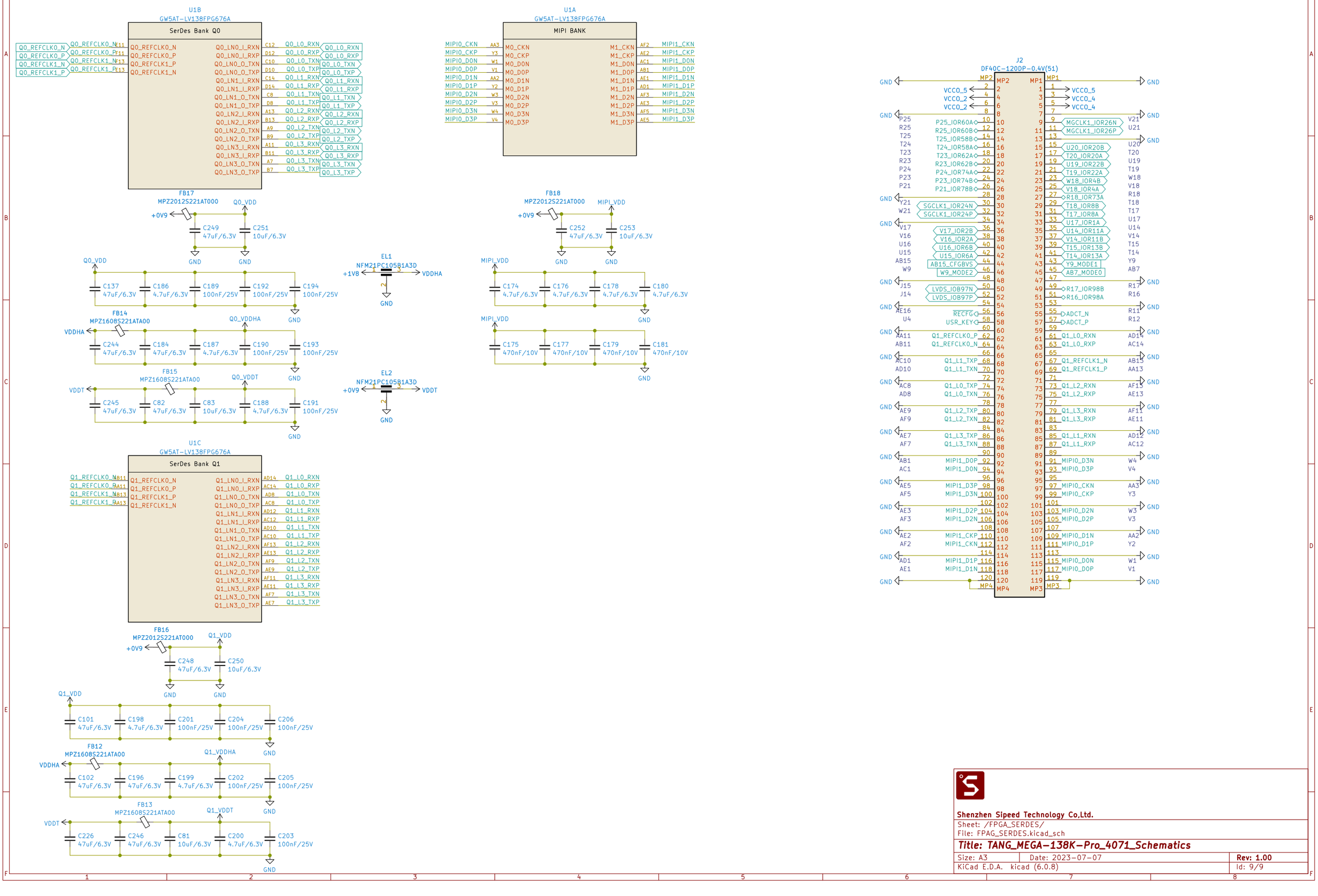
KiCad E.D.A. kicad (6.0.8)	**Rev: 1.00**
	Id: 8/9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GW5AT-LV138FPG676A
SerDes Bank Q0
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Q0_REFCLK0_P
Q0_REFCLK1_N
Q0_REFCLK1_P
Q0_LN0_I_RXN
Q0_LN0_I_RXP
Q0_LN0_O_TXN
Q0_LN0_O_TXP
Q0_LN1_I_RXN
Q0_LN1_I_RXP
Q0_LN1_O_TXN
Q0_LN1_O_TXP
Q0_LN2_I_RXN
Q0_LN2_I_RXP
Q0_LN2_O_TXN
Q0_LN2_O_TXP
Q0_LN3_I_RXN
Q0_LN3_I_RXP
Q0_LN3_O_TXN
Q0_LN3_O_TXP
U1A
GW5AT-LV138FPG676A
MIPI BANK
MIPI0_CKN
MIPI0_CKP
MIPI0_D0N
MIPI0_D0P
MIPI0_D1N
MIPI0_D1P
MIPI0_D2N
MIPI0_D2P
MIPI0_D3N
MIPI0_D3P
M0_CKN
M0_CKP
M0_D0N
M0_D0P
M0_D1N
M0_D1P
M0_D2N
M0_D2P
M0_D3N
M0_D3P
M1_CKN
M1_CKP
M1_D0N
M1_D0P
M1_D1N
M1_D1P
M1_D2N
M1_D2P
M1_D3N
M1_D3P
MIPI1_CKN
MIPI1_CKP
MIPI1_D0N
MIPI1_D0P
MIPI1_D1N
MIPI1_D1P
MIPI1_D2N
MIPI1_D2P
MIPI1_D3N
MIPI1_D3P
FB17
MPZ2012S221AT000
Q0_VDD
+0V9
C249
47uF/6.3V
C251
10uF/6.3V
GND
FB14
MPZ1608S221ATA00
VDDHA
Q0_VDDHA
C137
47uF/6.3V
C186
4.7uF/6.3V
C189
100nF/25V
C192
100nF/25V
C194
100nF/25V
C244
47uF/6.3V
C184
47uF/6.3V
C187
4.7uF/6.3V
C190
100nF/25V
C193
100nF/25V
FB15
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VDDT
Q0_VDDT
C245
47uF/6.3V
C82
47uF/6.3V
C83
10uF/6.3V
C188
4.7uF/6.3V
C191
100nF/25V
EL1
NFM21PC105B1A3D
+1V8
VDDHA
EL2
NFM21PC105B1A3D
+0V9
VDDT
FB18
MPZ2012S221AT000
MIPI_VDD
+0V9
C252
47uF/6.3V
C253
10uF/6.3V
C174
4.7uF/6.3V
C176
4.7uF/6.3V
C178
4.7uF/6.3V
C180
4.7uF/6.3V
C175
470nF/10V
C177
470nF/10V
C179
470nF/10V
C181
470nF/10V
U1C
GW5AT-LV138FPG676A
SerDes Bank Q1
Q1_REFCLK0_N
Q1_REFCLK0_P
Q1_REFCLK1_N
Q1_REFCLK1_P
Q1_LN0_I_RXN
Q1_LN0_I_RXP
Q1_LN0_O_TXN
Q1_LN0_O_TXP
Q1_LN1_I_RXN
Q1_LN1_I_RXP
Q1_LN1_O_TXN
Q1_LN1_O_TXP
Q1_LN2_I_RXN
Q1_LN2_I_RXP
Q1_LN2_O_TXN
Q1_LN2_O_TXP
Q1_LN3_I_RXN
Q1_LN3_I_RXP
Q1_LN3_O_TXN
Q1_LN3_O_TXP
FB16
MPZ2012S221AT000
Q1_VDD
+0V9
C248
47uF/6.3V
C250
10uF/6.3V
C101
47uF/6.3V
C198
4.7uF/6.3V
C201
100nF/25V
C204
100nF/25V
C206
100nF/25V
FB12
MPZ1608S221ATA00
VDDHA
Q1_VDDHA
C102
47uF/6.3V
C196
47uF/6.3V
C199
4.7uF/6.3V
C202
100nF/25V
C205
100nF/25V
FB13
MPZ1608S221ATA00
VDDT
Q1_VDDT
C226
47uF/6.3V
C246
47uF/6.3V
C81
10uF/6.3V
C200
4.7uF/6.3V
C203
100nF/25V
J2
DF40C-120DP-0.4V(51)
MP1
MP2
MP3
MP4
VCCO_5
VCCO_4
VCCO_2
MGCLK1_IOR26N
MGCLK1_IOR26P
U20_IOR20B
T20_IOR20A
U19_IOR22B
T19_IOR22A
W18_IOR4B
V18_IOR4A
R18_IOR73A
T18_IOR8B
T17_IOR8A
U17_IOR1A
U14_IOR11A
V14_IOR11B
T15_IOR13B
T14_IOR13A
Y9_MODE1
AB7_MODE0
R17_IOR98B
R16_IOR98A
ADCT_N
ADCT_P
Q1_L0_RXN
Q1_L0_RXP
Q1_REFCLK1_N
Q1_REFCLK1_P
Q1_L1_TXP
Q1_L1_TXN
Q1_L2_RXN
Q1_L2_RXP
Q1_L3_RXN
Q1_L3_RXP
Q1_L1_RXN
Q1_L1_RXP
MIPI0_D3N
MIPI0_D3P
MIPI0_CKN
MIPI0_CKP
MIPI0_D2N
MIPI0_D2P
MIPI0_D1N
MIPI0_D1P
MIPI0_D0N
MIPI0_D0P
P25_IOR60A
R25_IOR60B
T25_IOR58B
T24_IOR58A
T23_IOR62A
R23_IOR62B
P24_IOR74A
P23_IOR74B
P21_IOR78B
SGCLK1_IOR24N
SGCLK1_IOR24P
V17_IOR2B
V16_IOR2A
U16_IOR6B
U15_IOR6A
AB15_CFGBVS
W9_MODE2
LVDS_IOB97N
LVDS_IOB97P
RECFG
USR_KEY
Q1_REFCLK0_P
Q1_REFCLK0_N
Q1_L1_TXP
Q1_L1_TXN
Q1_L0_TXP
Q1_L0_TXN
Q1_L2_TXP
Q1_L2_TXN
Q1_L3_TXP
Q1_L3_TXN
MIPI1_D0P
MIPI1_D0N
MIPI1_D3P
MIPI1_D3N
MIPI1_CKP
MIPI1_CKN
MIPI1_D2P
MIPI1_D2N
MIPI1_D1P
MIPI1_D1N
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Title: TANG_MEGA-138K-Pro_4071_Schematics
Size: A3
Date: 2023-07-07
Rev: 1.00
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Id: 9/9