LAB2: Router Design and Simulation with EDA Tool

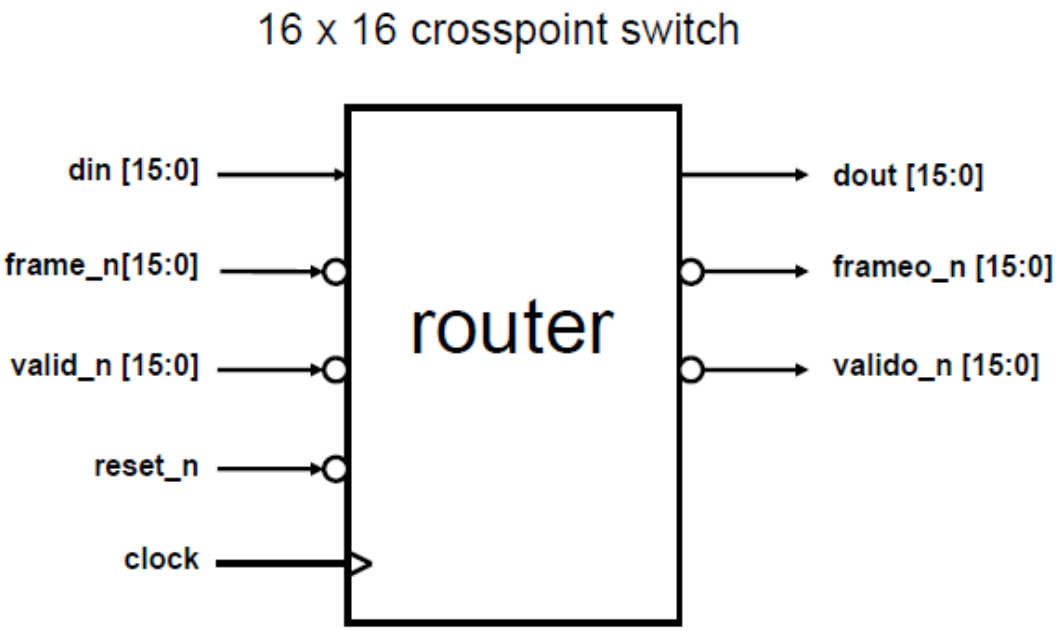
Learning Objectives

After completing this lab, you should be able to:

- Describe the function of the Device Under Test (DUT).
- Identify the control and data signals of the DUT
- Build testbench, write testcases and verifying the design using Vivado

- PART 1: Router Design

Introduction



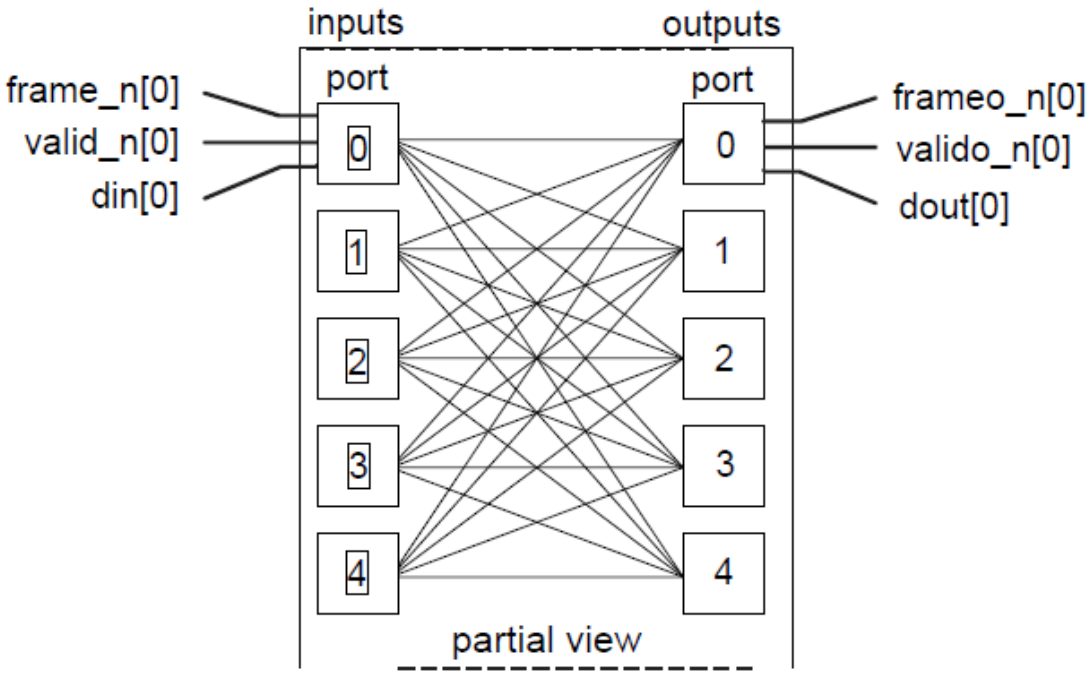
The router has 16 input and 16 output ports. Each input and output port consists of 3 signals, serial data, frame and valid. These signals are represented in a bit-vector format, din[15:0], frame_n[15:0],valid_n[15:0], dout[15:0], frameo_n[15:0] and valido_n[15:0].

To drive an individual port, the specific bit position corresponding to the port number must be specified. For example, if input port 3 is to be driven, then the corresponding signals shall be din[3], frame_n[3] and valid_n[3].

To sample an individual port, the specific bit position corresponding to the port number must be specified. For example, if output port 7 is to be sampled, then the corresponding signals shall be dout[7], frameo_n[7] and valido_n[7].

In this lab you will design a router in part 1 and then verify the design in part 2.

Description



Refer to the lecture slides to understand the specification of this router.

PART 2: Router Verification

Getting started

- Plan a check list which will list all test cases to cover all functions of your processor
- Build the testbench including all necessary components to drive the inputs and monitor the outputs of the DUT.
- Compile and simulate the design using Vivado tool.
- Check the functions of the DUT and debug issues if it happens.