Digital VLSI 2024 - Final Project Report

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***Abstract*—In this project, the Schematic and Layout of 16 bit Signed/Unsigned Radix-4 Booth Multiplier is presented. It is 2-stage Pipelined and Power Gated with a header switch. It includes the Partial Product Generation Stage [1], Wallace Tree stage [2] for the compression of Partial Products, and the Carry Bypass Adder[1] to get the final result. We present a fleixible architecture capable to processing both signed and unsigned numbers, therefore increasing the dynamic range of multiplications under unsigned category. It has a maximum Operating Frequency of 400MHz at SS corner after extraction, Average Power Consumption of 769.2 μW, Energy per Computation of 1.9pJ and Layout Area of 17424 sq. μm.**

I. Introduction

Booth Encoding is an efficient way to reducing the number of partial products, that are to be added to obtain the final multiplication result. Radix-4 Encoding reduces the no. of partial products in half, which can be added by using an array of Carry Save Adders(CSA)[2].

$$M = \frac{N}{\log_2 R} \tag{1}$$

Where M = Partial Products, N = No. of Bits, R = Radix. In this project, the Modified Booth encoding is used, which generated 9 Partial Products for unsigned and 8 Partial Products for signed multiplications. The partial products uses CSA array which reduces the number of addition operands. The two 32 bit CSA outputs are added by using a Carry Bypass/Skip adder, which provides less delay than Ripple Carry Adder and the layout has less complexity and area consumption than other advanced adder architectures.

II. Library and cell Creation

For leveraging the bottom-up design flow methodology. A cell library of basic combinational and sequential block is necessary. We start with this and design around 12 basic cells. For example INV, NAND2, NOR2, NAND3, AOI22, XOR2, Full Adder, Half Adder, 2-1 MUX, D-Flip Flop, BUFFER4, BUFFER5 etc. are created and used in the design for the making of schematic and layout.

III. Architecture

The 2-stage pipelined block diagram is as shown in Fig.1.

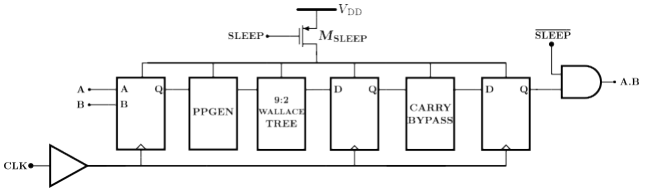

Fig. 1. Pipelined Block Diagram

A. Partial Product Generation Stage

This block generates Partial Products based on modified Booth Encoding[3] which encodes the 3 consecutive bits of multiplier and selects the multiplicand according to the encoder output. The circuit diagram is as shown in Fig.2. Here, the 0 extended multiplicand is sign extended in case of signed multiplication.

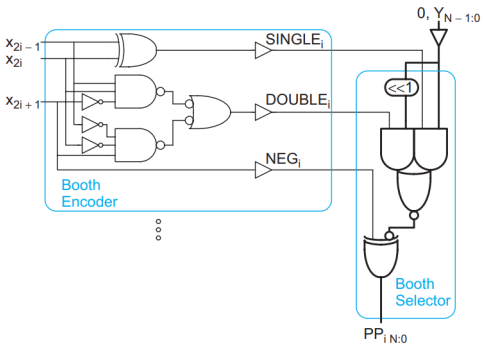

Fig. 2. Radix-4 Booth Encoder and Selector

Input Range	Value
Signed Binary	-2^{15} to $2^{15}-1$
Unsigned Binary	0 to $2^{16}-1$

We provide a flexible architecture for processing both signed and unsigned inputs. This is done by a slight modification of the partial products using a MUX that is triggered by the SIGNED input. This increases the range of inputs that can be processed utilizing the same hardware.

B. Wallace Tree Stage

Wallace trees reduce the number of operands at the earliest opportunity which tends to minimize the overall delay by making the final CPA as short as possible[2]. Wallace tree uses simple Full adders as 3:2 compressor, thus the delay equals the number of stage used times the delay of Full Adder.

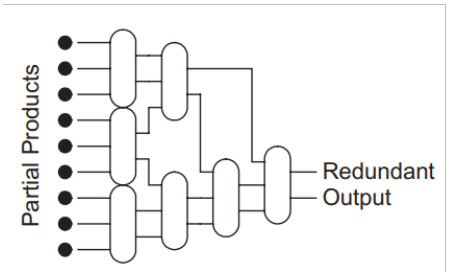

Fig. 3. Wallace Tree Stage

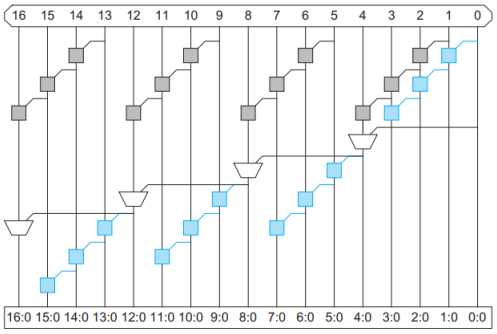

Fig. 4. Carry Skip Adder Architecture.

C. Carry Skip Adder

The two 32 bit redundant output is added using Carry Skip Adders which includes PG stage, 4-bit Ripple Carry Adder, 2-1 MUX for a carry selection and propagation (Fig.4). This a total of 8 stages of 4-bit ripple carry adder, 7 MUX and PG stage for each Ripple carry stage. The delay of the circuits is less than vanilla ripple carry adder and at the same time takes up less area than other advanced architectures.

D. Pipelining Registers

The registers are made using D-Flip flops, which has different sizes depending on the outputs of (PP Gen. + Wallace stage) and Carry Skip adder stage. It uses a buffered clock signal, which helps in capturing the token at the rising edge and maintaining 2-stage pipelining.

E. Power Gating Design

The power gating is done using large sized high-Vt PMOS transistor at the VDD supply rail and the output isolation is done by using AND gates, which isolates the circuit when SLEEP is ON as shown in Fig.1 [4].

We simulate the extracted multiplier with different sizes of PMOS header and to study various trade-offs. Based on the

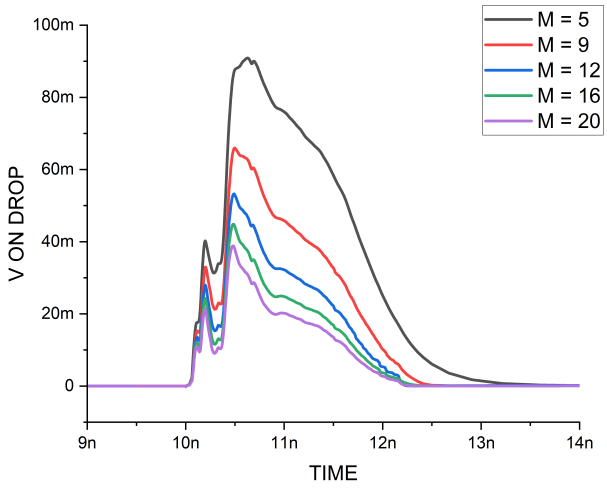

Fig. 5. ON state voltage drop

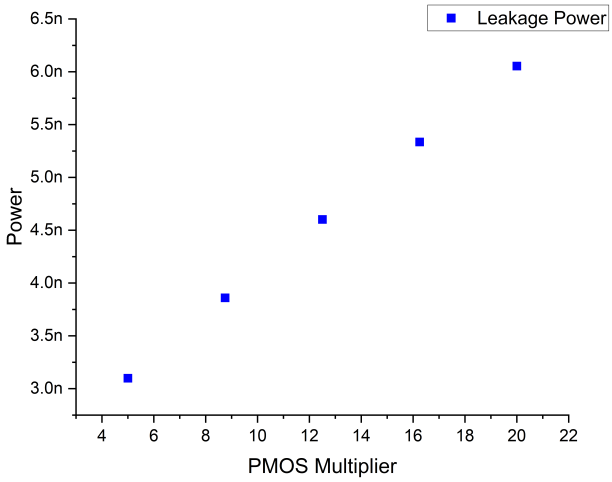

Fig. 6. Leakage Power with PMOS Size

above results between on state voltage drop and leakage power, we choose a multiple size of 12, with width of 2.34um and length 90nm.

Characteristics	Value
Active State Voltage Drop	45mV
Sleep Mode Power	4.5nW

IV. Testing

The testing of the circuit is done using various kinds of inputs at both signed and unsigned configuration. Refer to following tablke for the set of inputs. The operating frequency is 400 MHz ar SS corner and SLEEP=0. For SLEEP=1, the output converges to 0.

Signed	Input A	Input B	Output
1	0	0	0
1	0	Random	0
1	Random	0	0
1	Pos	Pos	Pos
1	LargeP	LargeP	LargeP
1	LargeP	LargeN	LargeN
1	LargeN	LargeP	LargeN
1	LargeN	LargeN	LargeP
0	Random	Random	Random
0	Large	Large	Large

V. Performance

A. Dynamic Power

The power consumption depends on switching activity and change of inputs and outputs.
Initial Inputs: SIGNED = 0, A = 0, B = 0, RESULT = 0
Next Inputs: SIGNED = 0, A = 2^{15}+1, B 2^{15}-1, RESULT = 2^{30}-1

This condition ensures maximum switching at the output nodes and hence more power consumption. This gives us an approximate estimate of power consumption in the multiplier. This Power consumption is evaluated at SS Corner, as the transistors become weaker than TT corner, consuming more current for charging and discharging. The Total Power Consumed is as shown in table.

Circuit	Average Power	Peak Power
Schematic	280 μW	1.68mW
PEX	769.2 μW	5.313mW

B. Static Power

This power consumption is measured at both conditions, when SLEEP = 0 and SLEEP = 1, which gives us an estimate of what is the static power consumption at both configuration. The static power is calculated at FF corner, as the threshold voltage reduces at FF, so it will contribute towards more leakage and hence, more static power consumption.

SLEEP	Circuit	Static Power
0	Schematic	0.478 μW
0	PEX	0.578 μW
1	Schematic	1.08 μW
1	PEX	1.39 μW

C. Delay

The delay of the system is defined for each pipelining stage, which depends the combinational logic used in that pipelining stage, Clock to Q delay of D flip flop and the setup time. The table given gives the delay of various blocks before PEX and after PEX is shown. The corner is chosen to be SS corner, as it will contribute to more delay, as both PMOS and NMOS are weak transistors. The frequency of operation at SS corner is 400MHz.

Block	Delay Type	Schematic	PEX
DFF	T_{pcq}	140ps	220ps
DFF	T_{setup}	42.8ps	60.2ps
PP GEN	T_{pd}	413.4ps	521.6ps
Wallace	T_{pd}	502.6ps	698.7ps
Skip Adder	T_{pd}	874.8ps	945.8ps

D. Area

The area of layout is shown in Fig.7. The dimensions are 180 μm $\times$ 96.5 μm.

Characteristics	Value
Operating Frequency	400 MHz
Power Consumption	762 uW
Sleep Mode Power	4.5 nW
Energy per Compute	1.9 pJ
Area	17424 squm
Area (kGates)	7770 kGates
Output T_{pcq}	340 ps

VI. Summary and Conclusion

This project is a good way of understanding various design trade-offs between choosing efficient architectures and their complexity in design, both at schematic and layout level, speed, performance and area. We learned how to take up work as a team, conduct review studies of different architectures, discuss their implementation and other trade-offs. After having an implementation on pen and paper, moving on to follow the bottom-up design flow, which includes preparing and maintaining a clean cell library, verifying the circuit at various levels in the schematic stage, only when the schematics are verified then taking up the full-layout of the block. This hierarchical design paradigm results in maximum throughput for given time frame.

References

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[4] K. Shi and D. Howard, "Sleep Transistor Design and Implementation - Simple Concepts Yet Challenges To Be Optimum," 2006 International Symposium on VLSI Design, Automation and Test - Hsinchu, Taiwan, 2006

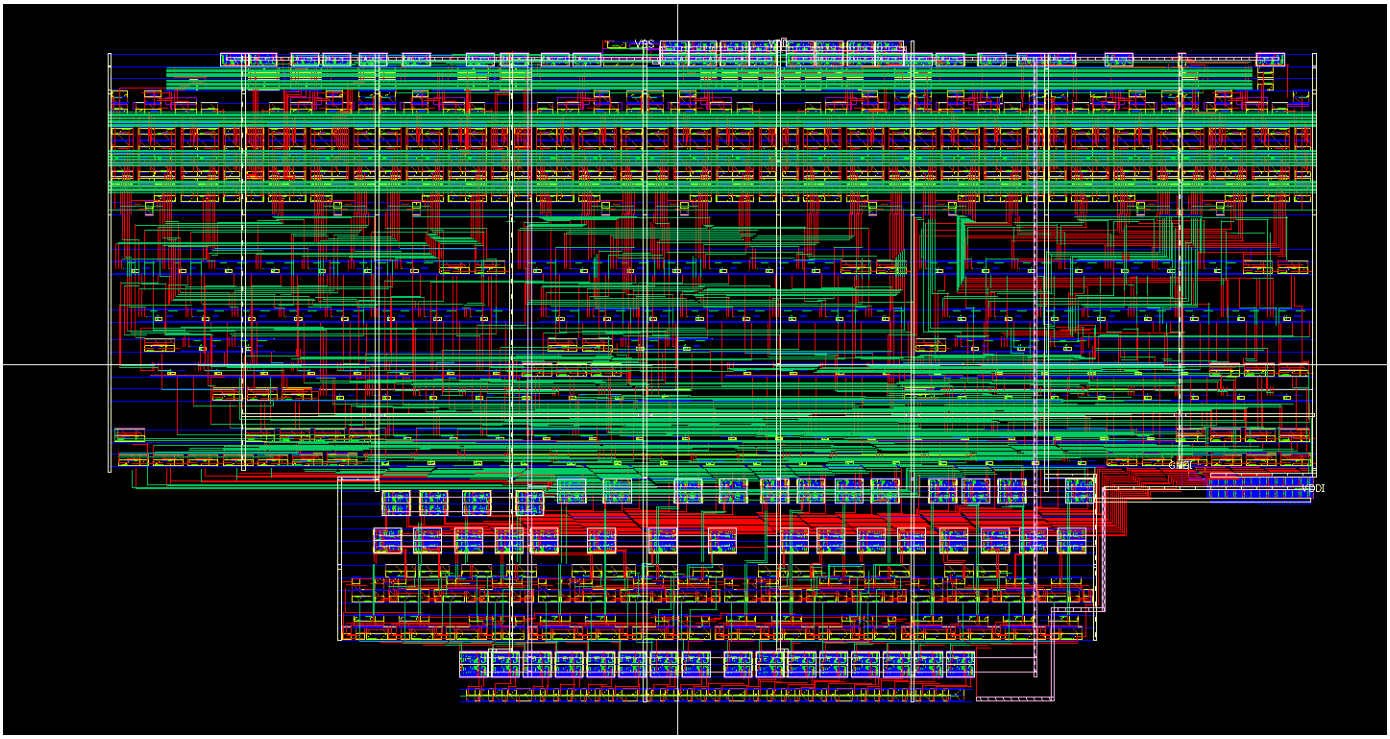

Fig. 7. Layout