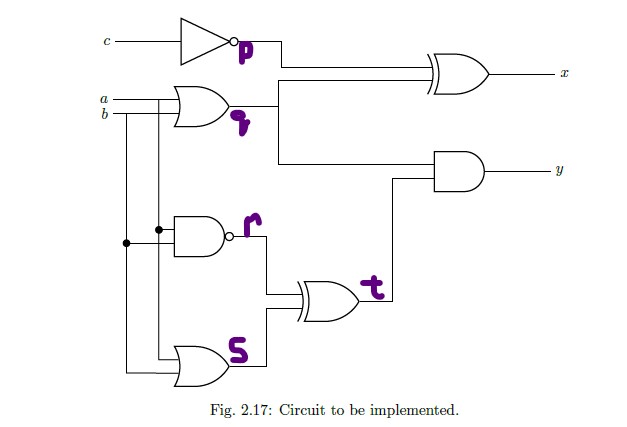
Name: Zain Saeed Roll no: 2022-EE-177 Section: D

Marks Obtained:

**Digital System Lab**

**Experiment 2**

**Combinational Circuits : Structural Modeling Simulation**

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*Task # 01*

**Truth Table**

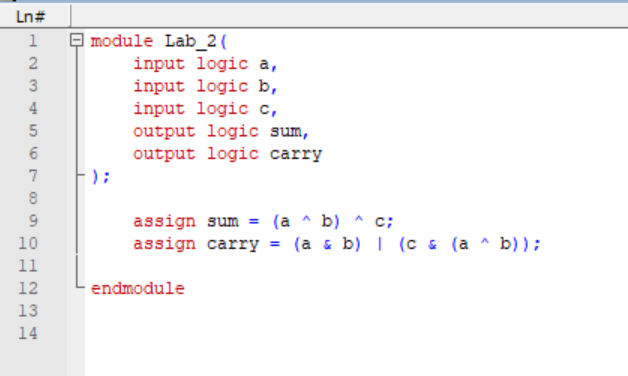
*Task # 02*

**Error Finding**

In Code # 01

* Adjusted output declaration syntax to remove trailing commas.
* Fixed the carry calculation expression by adding the missing '&' operator.
* Sum was not assigned.

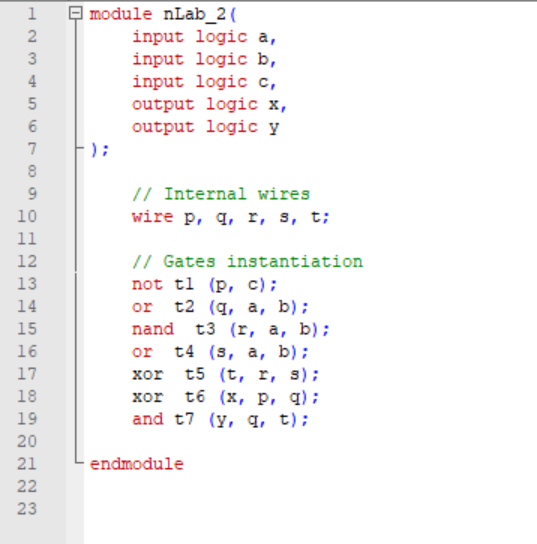
After correction, Code # 01 is

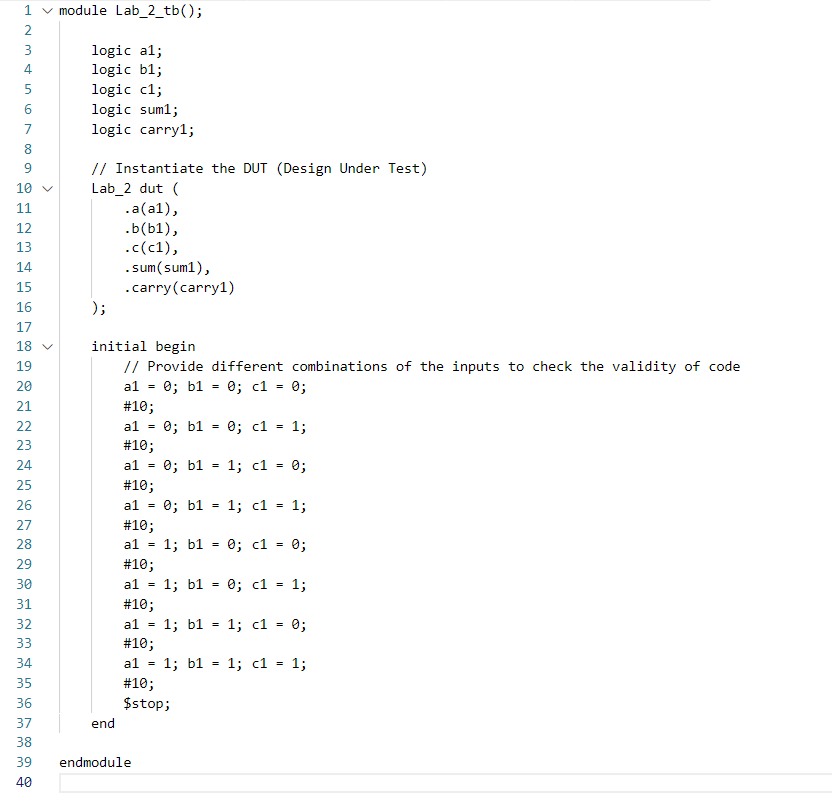


In Code # 02

* Removed unused signal declarations (a, b, c, sum, carry).
* Corrected instantiation of the DUT module to Lab\_2.
* Updated test cases to use signals a1, b1, and c1.
* Removed extra line breaks for clarity.

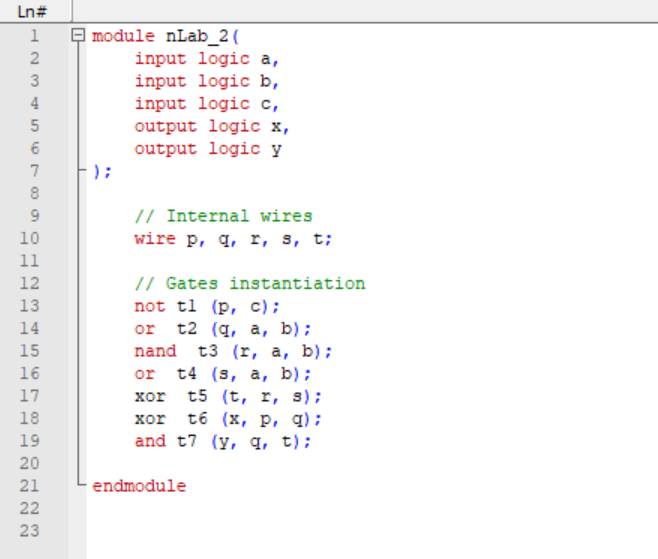
After correction Code # 02 is



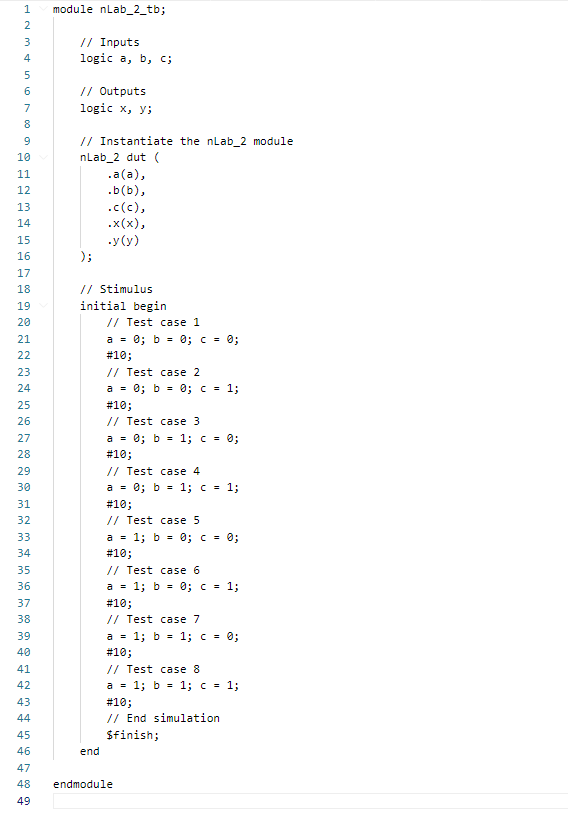


*Task # 03*

**Using Structural coding**



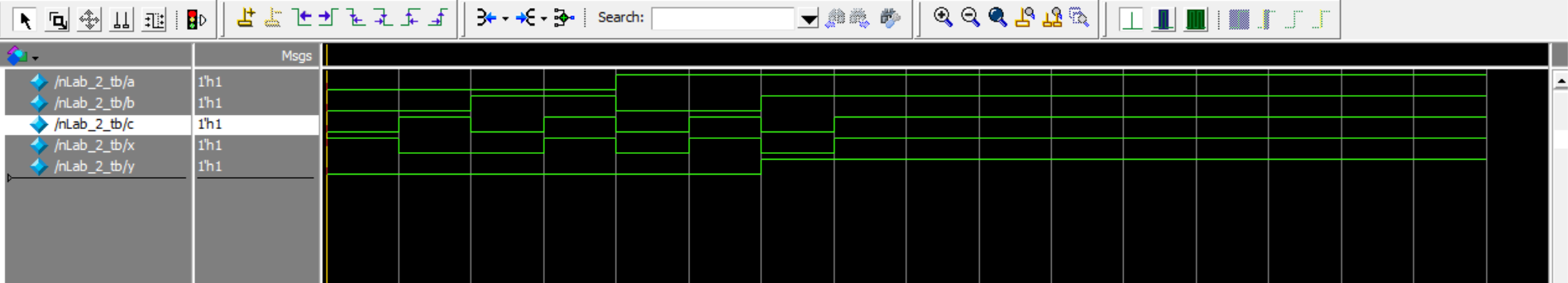
Test bench for Task # 03



***Waveforms***

***Task # 01***

***Task # 02***

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