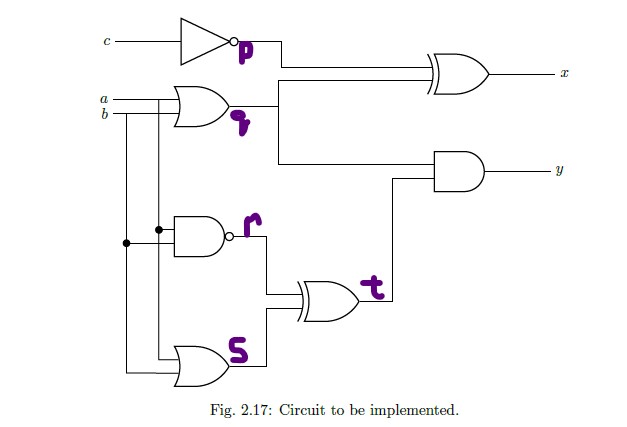
|  |  |
| --- | --- |
| Name: Zain Saeed | EE-272L Digital Systems Design |
| Reg. No / Section : 2022-EE-177 / D | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

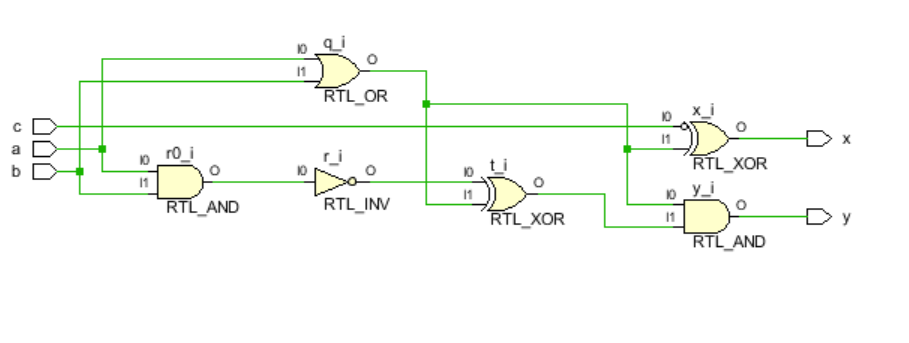
**Experiment 3**

**Combinational Circuits: Structural Modeling using Vivado**

In this lab, we are going to implement a simple combinational circuit given in Fig. 3.1 on our FPGA. For this purpose, we will learn about assigning I/O pins of our modules for synthesizing the designs on the FPGA. After that, we are going to use Vivado to burn our System Verilog code on the FPGA.

**Circuit Diagram:**

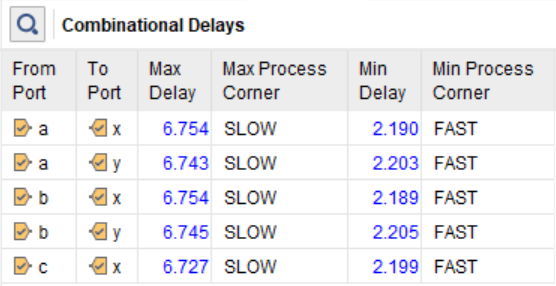
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**Truth Table of circuit:**

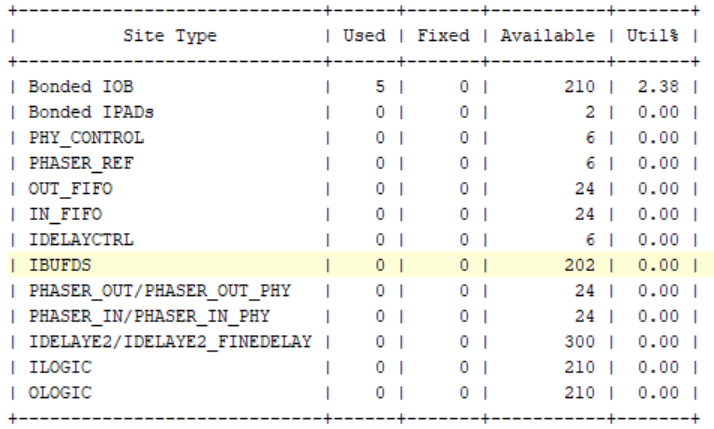


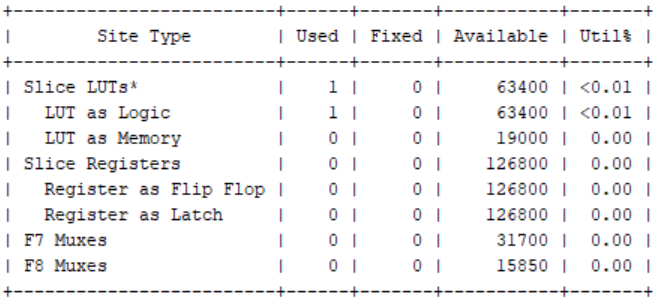
**Combinational delays in the circuit:**

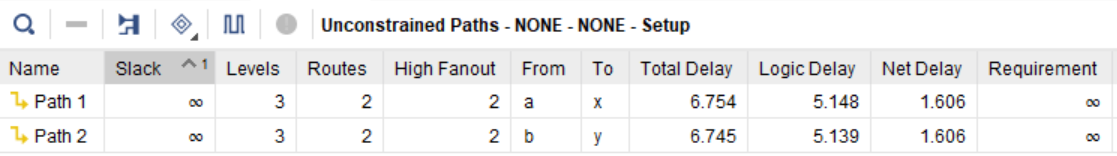
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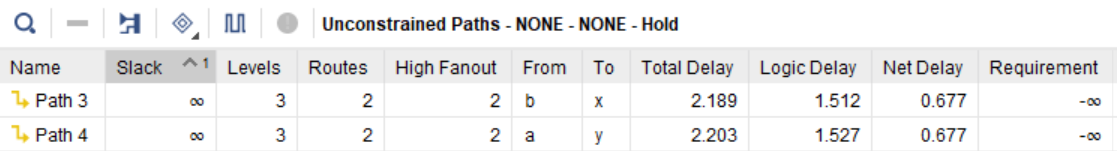
Maximum combinational delay:

**Resource Utilization:**

****



****

****

**System Verilog code for the circuit using structural modelling:**

module nLab3(

input logic a,

input logic b,

input logic c,

output logic x,

output logic y

);

logic p, q, r, s, t;

assign p = ~c;

assign q = a | b;

assign r = ~(a & b);

assign s = a | b;

assign t = r ^ s;

assign x = p ^ q;

assign y = q & t;

endmodule

**I/O Ports:**

****