**tpo**
A Toppoly and Philips
display company

*Tentative*

# LTPS LCD Specification

# Model Name: TD020THEG1

| Customer Signature |
|---|
|  |
| Date |
|  |

This technical specification is subjected to change without notice

**Table of Contents**

## Record of Revision

| Rev | Issue Date | Description |
|---|---|---|
| 0.00 | Jun. 2nd, 2006 | New create. |
| 0.01 | Aug. 8, 2006 | Page 8, Modify backlight driving reference table |
| 0.02 | Aug. 21, 2006 | Page 8, Modify backlight driving voltage & power consumption |
| 0.03 | Aug. 22, 2006 | Page 22, Update reliability spec of LED |
| 0.04 | Sep. 18, 2006 | Page 8, Modify reliability spec of LED |
| 0.05 | Sep. 21, 2006 | Page 24, Modify mechanical drawing |
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## 1. FEATURES

The 2.0" LCD module is the active matrix color TFT LCD module. LTPS (Low Temperature Poly Silicon) TFT technology is applied with vertical and horizontal drivers built on the panel.

Both of horizontal and vertical scan are reversible and controlled by the serial interface commands.

The product is designed for the requirement of the green product, and the specification complies with Toppoly's "Green Product Chemical Substance Specification Standard Hand Book".

## 2. GENERAL SPECIFICATIONS

| Item | Description | Unit |
|---|---|---|
| Display Size (Diagonal) | 2.0 | Inch |
| Display Type | Transmissive | - |
| Active Area (HxV) | 40.672 x 30.48 | mm |
| Number of Dots (HxV) | 640 x 240 | Dot |
| Dot Pitch (HxV) | 0.0635 x 0.127 | mm |
| Color Arrangement | RGB Delta | - |
| Color Numbers | 16Million | - |
| Outline Dimension (HxVxT) | 46.1 x 40.96 x 2.53* | mm |
| Weight | 8.5 | G |
| Panel surface treatment | Hard Coating(3H) | - |

*Exclude FPC and protrusions.

## 3. INPUT/OUTPUT TERMINALS

### 3.1 TFT LCD Panel

Recommend connector:

Compatible with Molex 51374-4073

| Pin | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | CP3 | C | Capacitor for power setting | |
| 2 | CP4 | C | Capacitor for power setting | |
| 3 | CP5 | C | Capacitor for charge pump | |
| 4 | CP6 | C | Capacitor for charge pump | |
| 5 | CP7 | C | Capacitor for charge pump | |
| 6 | CP8 | C | Capacitor for charge pump | |
| 7 | DUMMY | -- | Dummy | |
| 8 | DUMMY | -- | Dummy | |
| 9 | PCD | C | Capacitor for pre-charge data signal high | |
| 10 | VCOML | C | Capacitor for VCOM low | |
| 11 | VCOMH | C | Capacitor for VCOM high | |
| 12 | AGND | -- | Analog ground | |
| 13 | DUMMY | -- | Dummy | |
| 14 | AVDD | C | Regulation capacitor for analog voltage | |
| 15 | CP1 | C | Capacitor for charge pump | |
| 16 | CP2 | C | Capacitor for charge pump | |
| 17 | PWM | O | Power transistor gate signal for the boost converter | |
| 18 | FB | I | Main boost regulator feedback input. | |
| 19 | LED- | -- | LED power: cathode | Note 3-1 |
| 20 | DUMMY | -- | Dummy | |
| 21 | DUMMY | -- | Dummy | |
| 22 | LED+ | -- | LED power: anode | Note 3-1 |
| 23 | GND | -- | Ground | |
| 24 | VCC | -- | Power supply for digital circuit and charge pump circuit | |
| 25 | VSYNC | I | Vertical sync input. Negative polarity | |
| 26 | HSYNC | I | Horizontal sync input. Negative polarity | |
| 27 | DCLK | I | Clock signal, latch data onto line latches at the rising edge | |
| 28 | DIN0 | I | Data input | |
| 29 | DIN1 | I | Data input | |
| 30 | DIN2 | I | Data input | |
| 31 | DIN3 | I | Data input | |

| 32 | DIN4 | I | Data input | |
| 33 | DIN5 | I | Data input | |
| 34 | DIN6 | I | Data input | |
| 35 | DIN7 | I | Data input | |
| 36 | SDA | I/O | Serial interface data line | |
| 37 | SCL | I | Serial interface clock line | |
| 38 | SCEN | I | Serial interface chip enable line | |
| 39 | SHDB | I | Shutdown input | |
| 40 | GREST | I | System reset pin | |

Note 3-1: The figure below shows the connection of backlight LED.
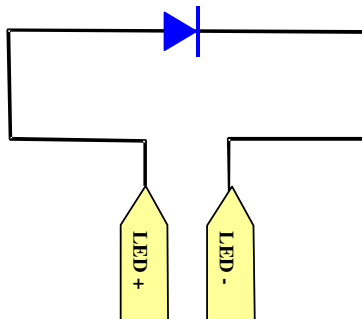
## 4. ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

| Item | Symbol | MIN | MAX | Unit | Remark |
|---|---|---|---|---|---|
| Logic Power Supply Voltage | $V_{CC}$ | -0.5 | 4.5 | V | |
| Input Signal Voltage | $V_{IN1}$ | 0 | $V_{CC}$ | V | VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB |
| Back Light Forward Current | $I_F$ | -- | 25 | mA | |
| Operating Temperature | $T_{OPR}$ | -10 | +60 | ℃ | |
| Storage Temperature | $T_{STG}$ | -30 | +80 | ℃ | |

## 5. ELECTRICAL CHARACTERISTICS

### 5.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Power Supply Voltage | | $V_{CC}$ | 2.85 | 3.0 | 3.6 | V | Note 5-1 |
| Input Signal Voltage | Low Level | $V_{IL}$ | GND | - | 0.2x Vcc* | V | VD, HD, DCLK, DIN[0:7], SDA, SCL, SCEN, SHDB, GRESTB |
| | High Level | $V_{IH}$ | 0.8x Vcc* | - | Vcc* | V | |
| PWM Output Voltage | | $V_{PWM}$ | 0 | - | Vcc* | V | |
| Feedback Voltage | | $V_{FB}$ | 0.55 | 0.6 | 0.65 | V | Note 5-2 |
| Panel Power Consumption | | $W_P$ | - | 50 | 60 | mW | |

Vcc* =Vcc(TYP)

Note 5-1: The Vcc power is provided for overall panel module supply voltage.

Note 5-2: DC/DC feedback control voltage

### 5.2 Driving Backlight

Ta=25℃

| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | -- | 23 | 25 | mA | |
| Forward Current Voltage | $V_F$ | -- | 3.4 | 3.6 | V | Note 5-3 |
| Backlight Power Consumption | $W_{BL}$ | -- | 78.2 | 90 | mW | |

Note 5-3: Backlight driving circuit is recommended as the fix current circuit.
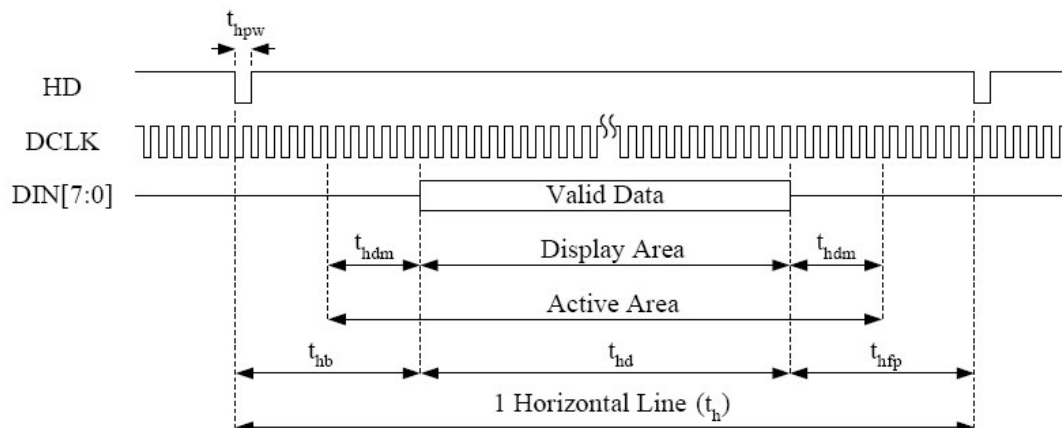
 * Ta: Ambient Temperature

 * High temperature operation: Test current refers the diagram as following.

 * High Temperature & High Humidity Operation: Test current is 15mA.
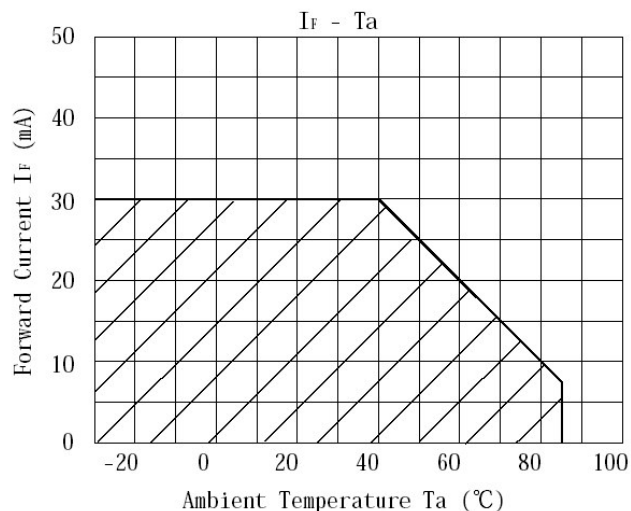
## 6. TIMING CHART

### 6.1 Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Horizontal



(1) YUV Mode: ITUR601-NTSC

| Item | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Dot Clock Frequency | DCLK | - | 27 | - | MHz |
| Horizontal Display Active | Display Area | - | 1440 | - | DCLK |
| Horizontal Line | $t_h$ | - | 1716 | - | DCLK |
| HSYNC Pulse Width | $t_{hpw}$ | 1 | 1 | - | DCLK |
| Horizontal Back Porch | $t_{hb}$ | - | 240 | - | DCLK |
| Horizontal Front Porch | $t_{hfp}$ | - | 36 | - | DCLK |
| Horizontal Dummy Time | $t_{hdm}$ | -- | 4 | -- | DCLK |

(2) YUV Mode: ITUR601-PAL

| Item | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Dot Clock Frequency | DCLK | - | 27 | - | MHz |
| Horizontal Display Active | Display Area | - | 1440 | - | DCLK |
| Horizontal Line | $t_h$ | - | 1728 | - | DCLK |
| HSYNC Pulse Width | $t_{hpw}$ | 1 | 1 | - | DCLK |
| Horizontal Back Porch | $t_{hb}$ | - | 240 | - | DCLK |
| Horizontal Front Porch | $t_{hfp}$ | - | 48 | - | DCLK |
| Horizontal Dummy Time | $t_{hdm}$ | -- | 4 | -- | DCLK |

(3) RGB Dummy Mode

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Dot Clock Frequency | QVGA | DCLK | - | 25 | - | MHz |
| | NTSC | | - | 24.54 | - | |
| | PAL | | - | 24.38 | - | |
| Horizontal Display Active | | Display Area | - | 1280 | - | DCLK |
| Horizontal Line | | $t_h$ | - | 1560 | - | DCLK |
| HSYNC Pulse Width | | $t_{hpw}$ | - | 1 | - | DCLK |
| Horizontal Back Porch | | $t_{hb}$ | - | 240 | - | DCLK |
| Horizontal Front Porch | | $t_{hfp}$ | - | 40 | - | DCLK |
| Horizontal Dummy Time | | $t_{hdm}$ | -- | 4 | -- | DCLK |

## 6.2 Serial RGB Dummy Mode and Serial YUV 4:2:2 Mode: Vertical
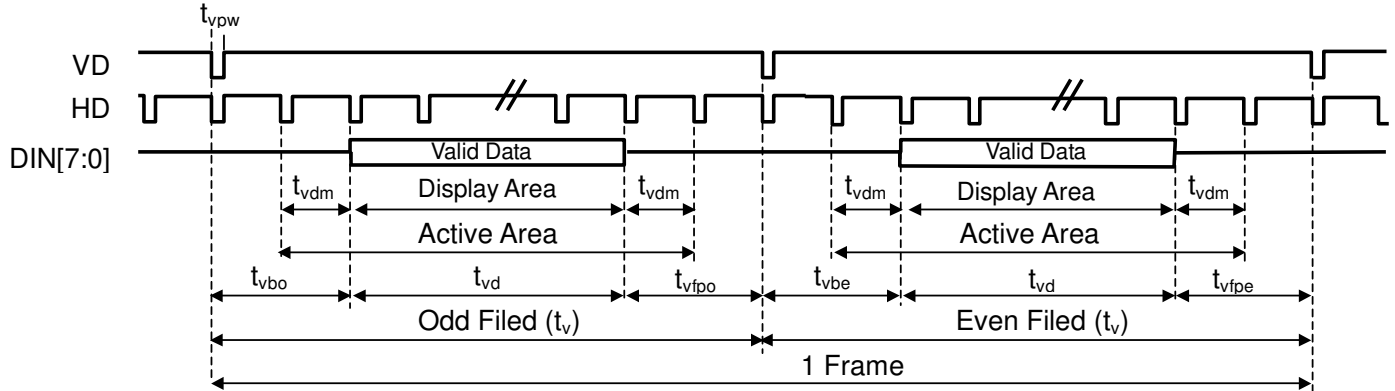


**Non-interlace Mode**
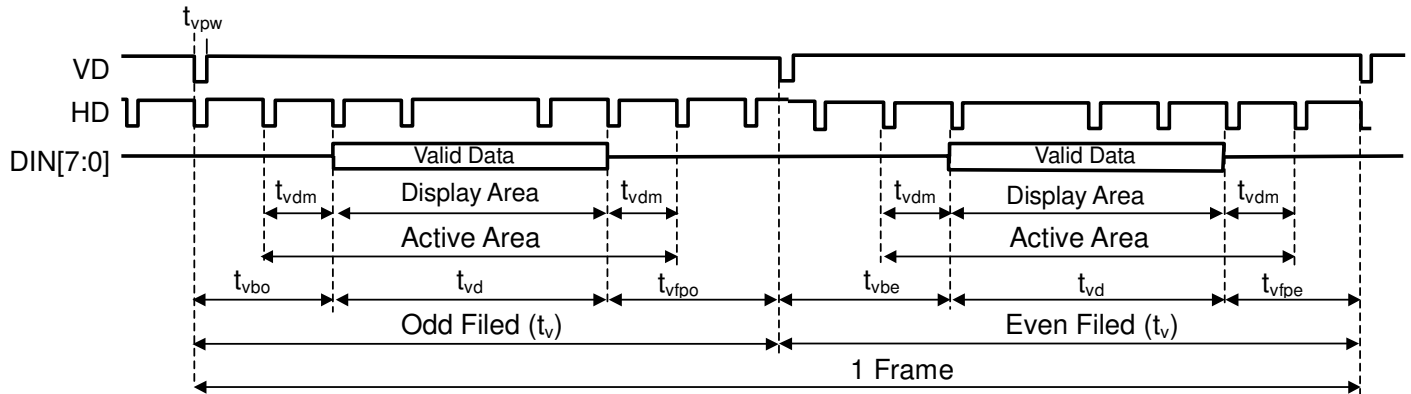


**Interlace Mode**

(1) Non-Interlace Mode: NTSC/QVGA

| Item | | Symbol | MIN | TYP | MAX | Unit |
|------|---|--------|-----|-----|-----|------|
| Vertical Display Active | | $t_{vd}$ | - | 240 | - | Line |
| Vertical Total Time | | $t_v$ | - | 262 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 21 | - | Line |
| | Even Field | $t_{vbe}$ | - | 21 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 1 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 1 | - | Line |
| Vertical Dummy Time | | $t_{vdm}$ | - | 0 | - | Line |

(2)   Non-Interlace Mode: PAL

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Vertical Display Active | | $t_{vd}$ | - | 288 | - | Line |
| Vertical Total Time | | $t_v$ | - | 312 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 24 | - | Line |
| | Even Field | $t_{vbe}$ | - | 24 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 0 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 0 | - | Line |
| Vertical Dummy Time | | $t_{vdm}$ | - | 0 | - | Line |

(3)   Interlace Mode: NTSC/QVGA

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Vertical Display Active | | $t_{vd}$ | - | 240 | - | Line |
| Vertical Total Time | | $t_v$ | - | 262.5 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 21 | - | Line |
| | Even Field | $t_{vbe}$ | - | 21.5 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 1.5 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 1 | - | Line |
| Vertical Dummy Time | | $t_{vdm}$ | - | 0 | - | Line |

(4)   Interlace Mode: PAL

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Vertical Display Active | | $t_{vd}$ | - | 288 | - | Line |
| Vertical Total Time | | $t_v$ | - | 312.5 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 24 | - | Line |
| | Even Field | $t_{vbe}$ | - | 24.5 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 0.5 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 0 | - | Line |
| Vertical Dummy | | $t_{vdm}$ | - | 0 | - | Line |

### 6.3 Through Mode: Horizontal
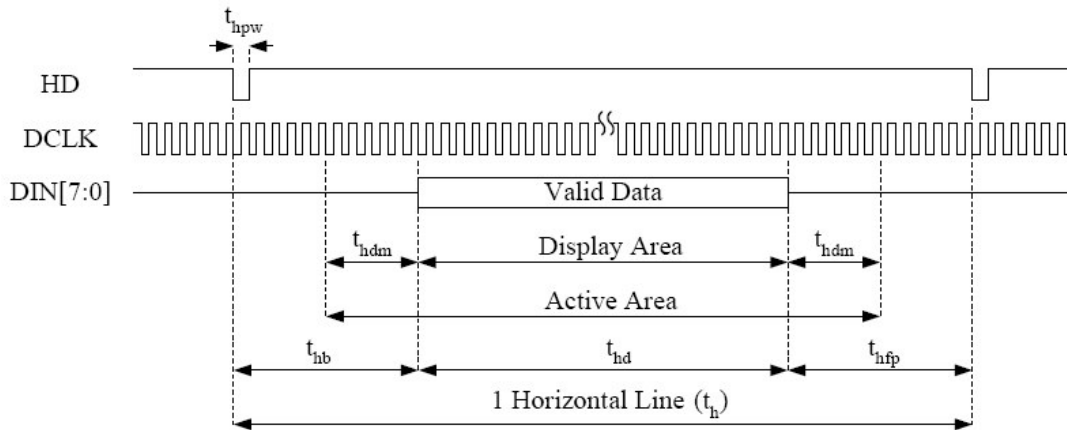


| Item | Symbol | MIN | TYP | MAX | Unit |
|------|--------|-----|-----|-----|------|
| Dot Clock Period | DCLK | | 12.90 | | MHz |
| Horizontal Display Active | Display Area | - | 640 | - | DCLK |
| Horizontal Line | $t_h$ | - | 820 | - | DCLK |
| HSYNC Pulse Width | $t_{hpw}$ | 1 | 1 | - | DCLK |
| Horizontal Back Porch | $t_{hb}$ | - | 117 | - | DCLK |
| Horizontal Front Porch | $t_{hfp}$ | - | 63 | - | DCLK |
| Horizontal Dummy Time | $t_{hdm}$ | -- | 4 | -- | DCLK |

### 6.4 Through Mode: Vertical
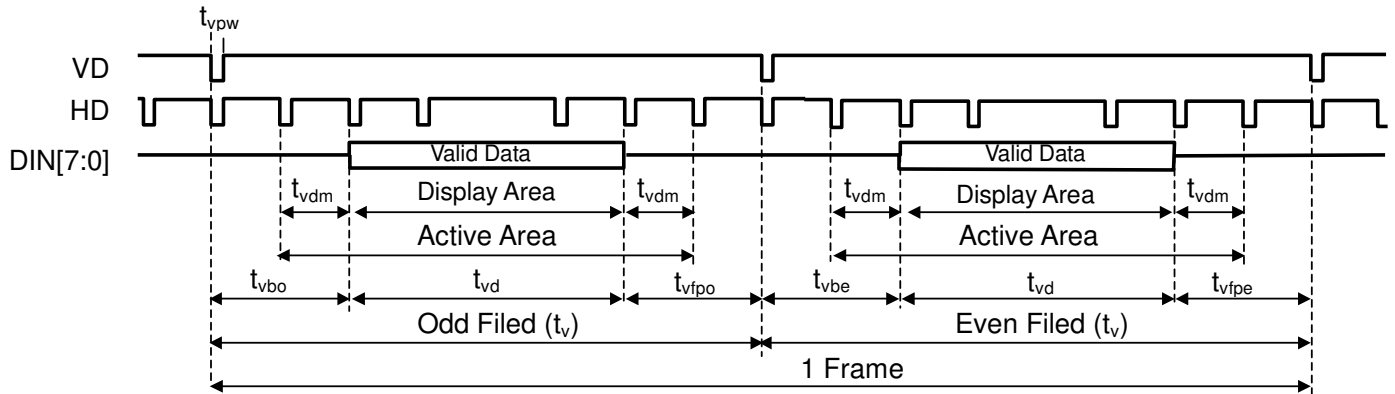


**Non-Interlace Mode**
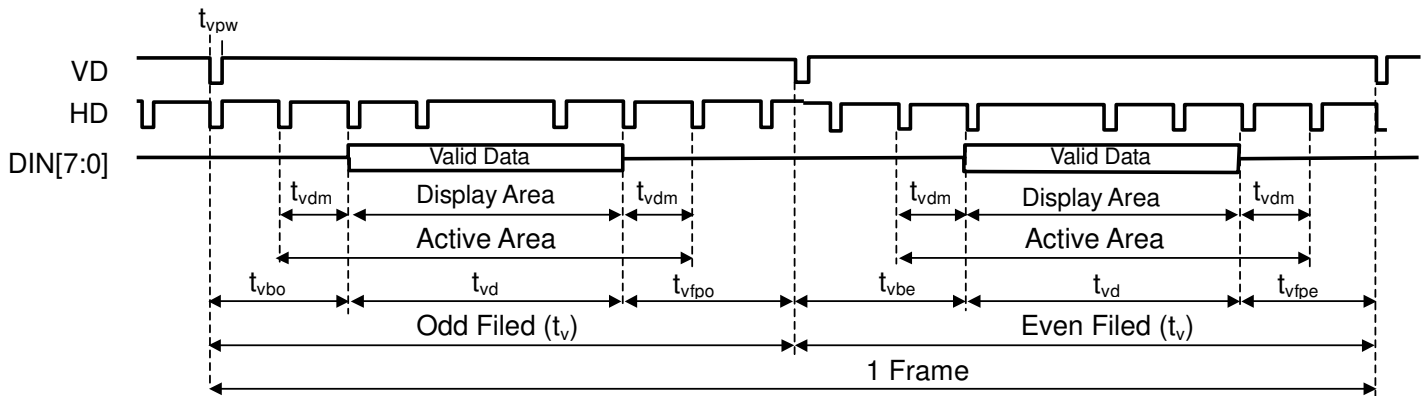


**Interlace Mode**

(1) Non-Interlace Mode

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Vertical Display Active | | $t_{vd}$ | - | 240 | - | Line |
| Vertical Total Time | | $t_v$ | - | 262 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 14 | - | Line |
| | Even Field | $t_{vbe}$ | - | 14 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 8 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 8 | - | Line |
| Vertical Dummy Time | | $t_{vdm}$ | - | 0 | - | Line |

(2)   Interlace Mode

| Item | | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| Vertical Display Active | | $t_{vd}$ | - | 240 | - | Line |
| Vertical Total Time | | $t_v$ | - | 262.5 | - | Line |
| VSYNC Pulse Width | | $t_{vpw}$ | 1 | 1 | - | DCLK |
| Vertical Back Porch | Odd Field | $t_{vbo}$ | - | 14 | - | Line |
| | Even Field | $t_{vbe}$ | - | 14.5 | - | Line |
| Vertical Front Porch | Odd Field | $t_{vfpo}$ | - | 8.5 | - | Line |
| | Even Field | $t_{vfpe}$ | - | 8 | | Line |
| Vertical Dummy Time | | $t_{vdm}$ | - | 0 | - | Line |

## 6.5 Setup Time and Hold Time

DIN[7:0]

$t_{ds}$ $t_{dh}$

DCLK

$t_{ss}$ $t_{sh}$

HD/VD
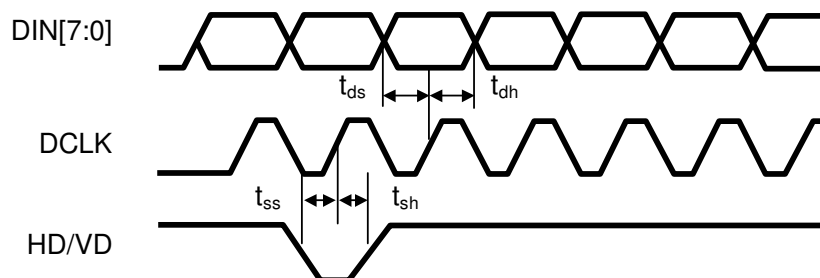
| Item | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| DCLK Duty Ratio | - | 40 | - | 60 | % |
| Data Setup Time | $t_{ds}$ | 12 | - | - | ns |
| Data Hold Time | $t_{dh}$ | 12 | - | - | ns |
| Control Signal Setup Time | $t_{ss}$ | 12 | - | - | ns |
| Control Signal Hold Time | $t_{sh}$ | 12 | - | - | ns |

6.6    Serial Interface Timing
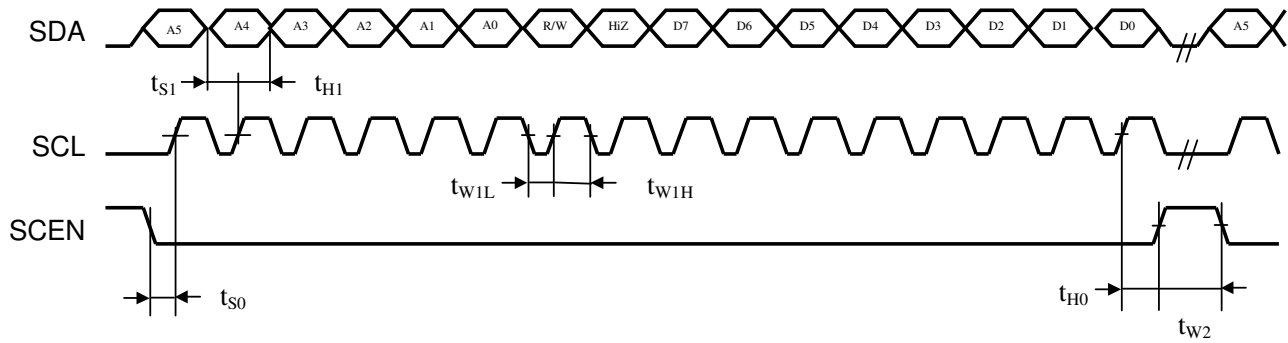


| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit |
|-----------|--------|-----------|-----|-----|-----|------|
| Data Setup Time | $t_{S0}$ | SCEN to SCL | 150 | - | - | ns |
| | $t_{S1}$ | SDA to SCL | 150 | - | - | ns |
| Data Hold Time | $t_{H0}$ | SCEN to SCL | 150 | - | - | ns |
| | $t_{H1}$ | SDA to SCL | 150 | - | - | ns |
| Pulse width | $t_{W1L}$ | SCL pulse width | 160 | - | - | ns |
| | $t_{W1H}$ | SCL pulse width | 160 | - | - | ns |
| | $t_{W2}$ | SCEN pulse width | 1.0 | - | - | us |
| Clock Duty | - | SCL duty ratio | 40 | 50 | 60 | % |

## 7. POWER SEQUENCE

### 7.1 Power on to normal mode sequence

**Power on (low power mode, global reset) to normal mode sequence**

Step1 : Wait VCC go stable and then send Normal command by 3 wire.
Step2 : Before turn on VCC, the VD/HD/DCLK input signal must keep still until Tpwr(2ms).
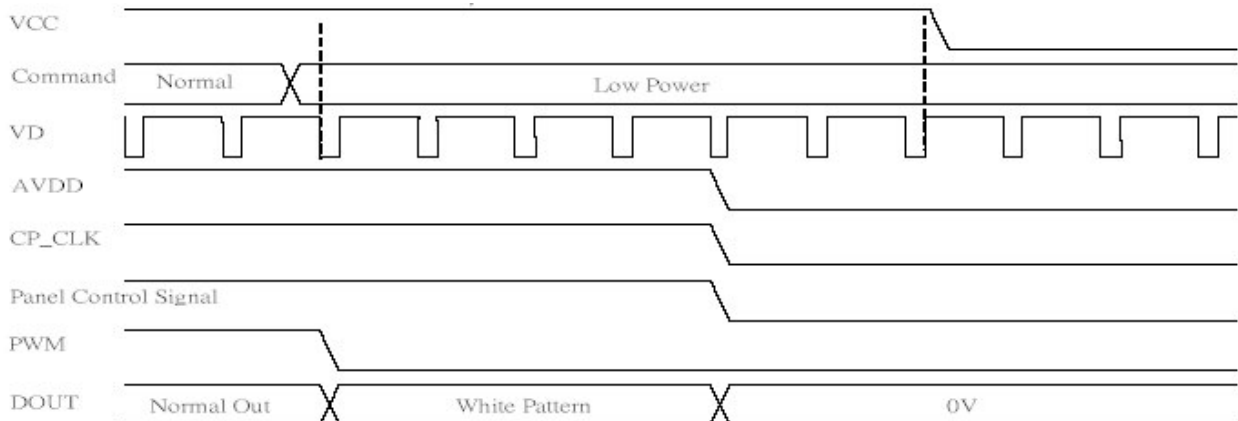Step3 : AVDD will start when second VD coming.
Step4 : CP_CLK will start when third VD coming.
Step5 : Panel Control Signal and Normal DOUT will start when ninth VD coming.
Start6 : PWM control signal will start when eleventh VD coming.
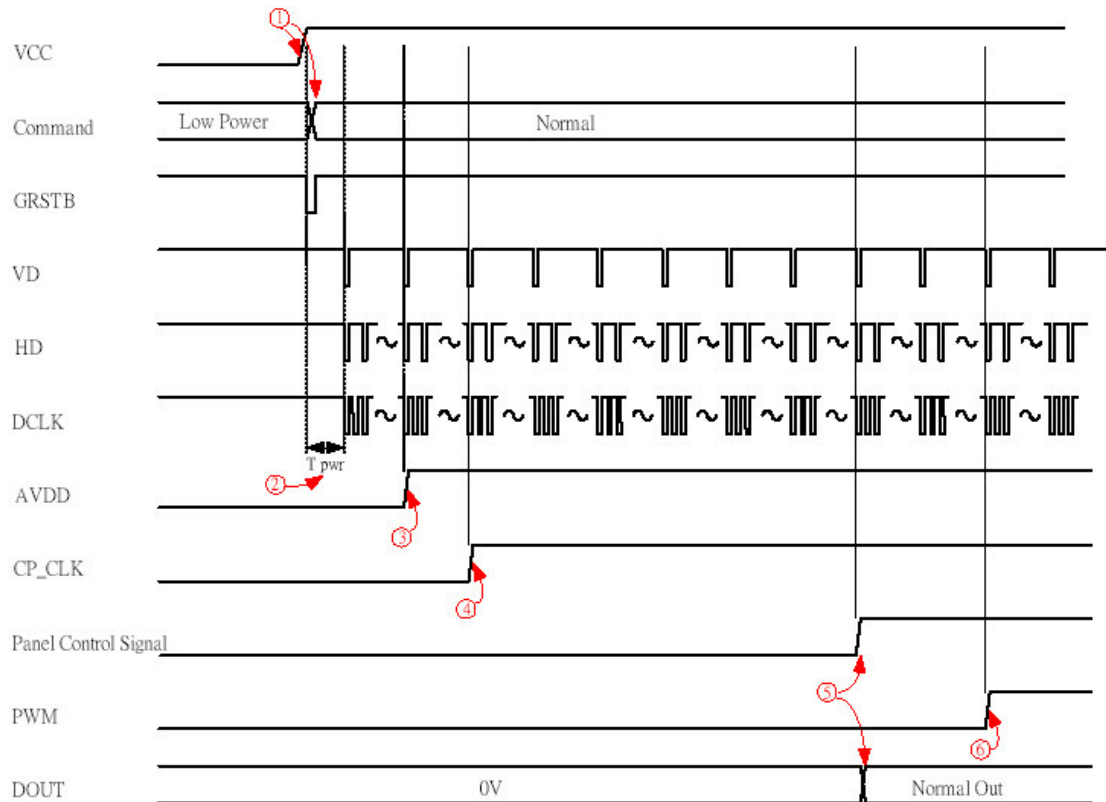


### 7.2 Normal mode to power off sequence

## 8. OPTICAL CHARACTERISTICS

### 8.1 Optical Specification

Ta=25℃

| Item | | Symbol | Condition | MIN | TYP | MAX | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angles | | $\Theta 11$ | CR ≥ 10 | 30 | 40 | - | Degree | Note 8-1 |
| | | $\Theta 12$ | | 30 | 40 | - | | |
| | | $\Theta 21$ | | 15 | 20 | - | | |
| | | $\Theta 22$ | | 40 | 50 | - | | |
| Contrast Ratio | | CR | $\Theta =0°$ | 200 | 300 | - | | Note 8-2 |
| Response Time | Rising | Tr | | | 13 | 20 | ms | Note 8-3 |
| | Falling | Tf | | | 22 | 30 | | |
| Luminance ($I_F$=23mA) | | L | | 200 | 250 | - | cd/m$^2$ | Note 8-4 |
| Chromaticity | White | $x_W$ | | 0.26 | 0.31 | 0.36 | | Note 8-5 |
| | | $y_W$ | | 0.29 | 0.34 | 0.39 | | |

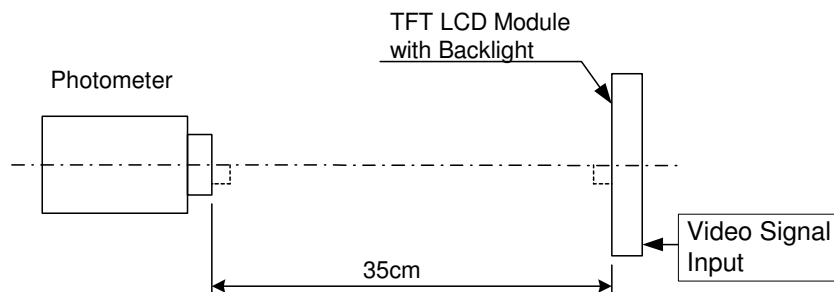### 8.2 Basic Measure Conditions

(1) Driving voltage

VCC= 3 V

(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle$\Theta$=0°

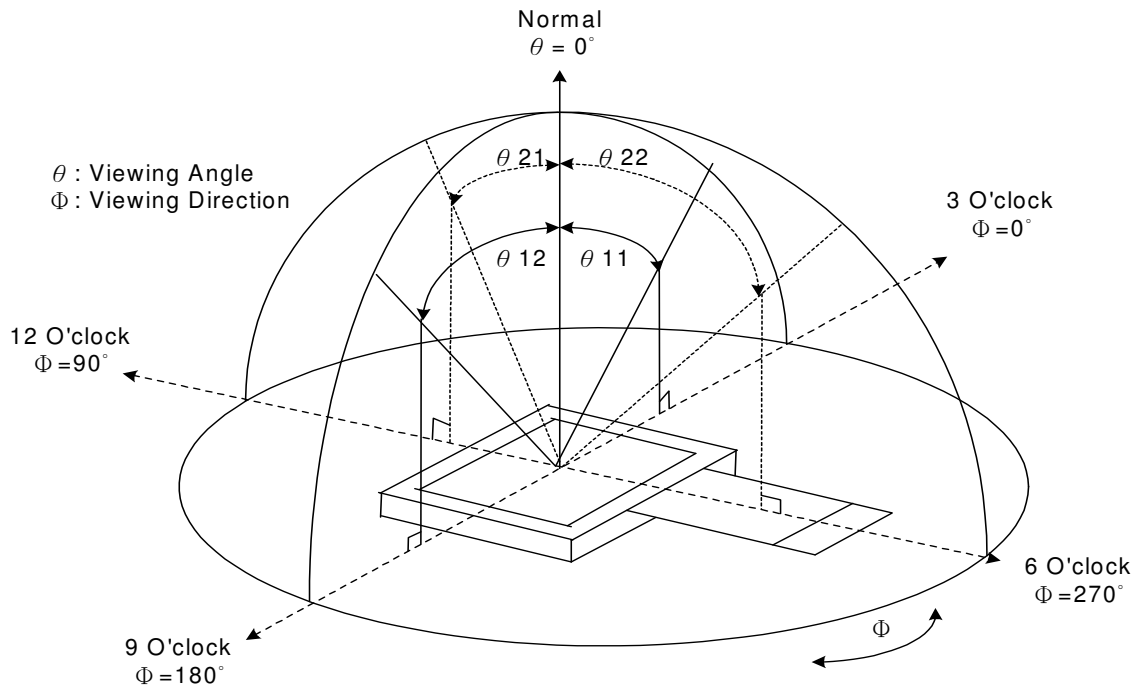(4) LED Current: $I_F$=23mA.

(5) Testing Facility

Environmental illumination: ≤ 1 Lux

Note 8-1: Viewing angle diagrams:

Normal
$\theta = 0°$

$\theta$ : Viewing Angle
$\Phi$ : Viewing Direction

$\theta\ 21$  $\theta\ 22$

$\theta\ 12$  $\theta\ 11$

3 O'clock
$\Phi = 0°$

12 O'clock
$\Phi = 90°$

6 O'clock
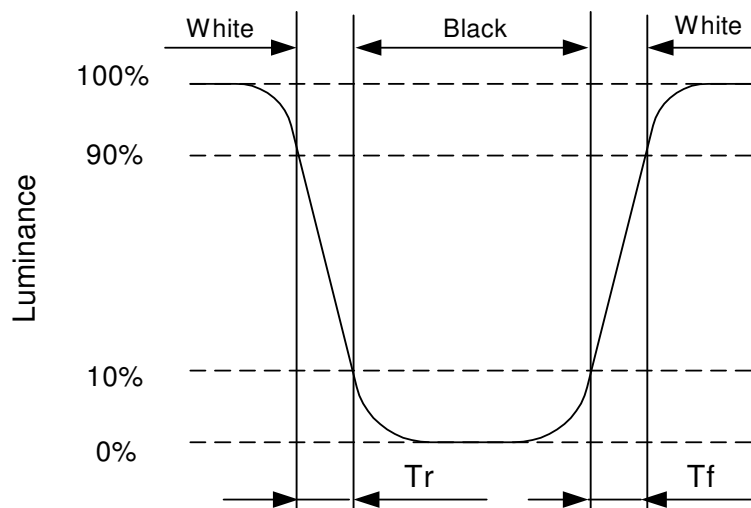$\Phi = 270°$

9 O'clock
$\Phi = 180°$

$\Phi$

Note 8-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 8-3: Definition of response time:

White          Black          White

100%

90%

Luminance

10%

0%

Tr          Tf

Note 8-4: Luminance:

Test Point: Display Center

Note 8-5: Chromaticity: The same test condition as Note 8-4.

## 9. RELIABILITY

| No | Test Item | Condition |
|---|---|---|
| 1 | High Temperature Operation | Ta=+60℃, 240hrs |
| 2 | High Temperature & High Humidity Operation | Ta=+40℃, 95% RH, 240hrs |
| 3 | Low Temperature Operation | Ta=-10℃, 240hrs |
| 4 | High Temperature Storage (non-operation) | Ta=+80℃, 240hrs |
| 5 | Low Temperature Storage (non-operation) | Ta=-30℃, 240hrs |
| 6 | Thermal Shock (non-operation) | -30℃ ←→ 80℃, 50 cycles<br>30 min    30 min |
| 7 | Surface Discharge (non-operation) | C=150pF, R=330Ω;<br>Discharge: Air: ±15kV; Contact: ±8kV<br>5 times / Point; 5 Points / Panel |
| 8 | Vibration (non-operation) | Frequency: 10~55Hz; Amplitude: 1.5mm<br>Sweep Time: 11min<br>Test Time: 2 hrs for each direction of X, Y, Z |
| 9 | Shock (non-operation) | Acceleration: 100G; Period: 6ms<br>Directions: ±X, ±Y, ±Z; Cycles: Twice |

* Ta: Ambient Temperature

## 10. HANDLING CAUTIONS

10.1      ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.

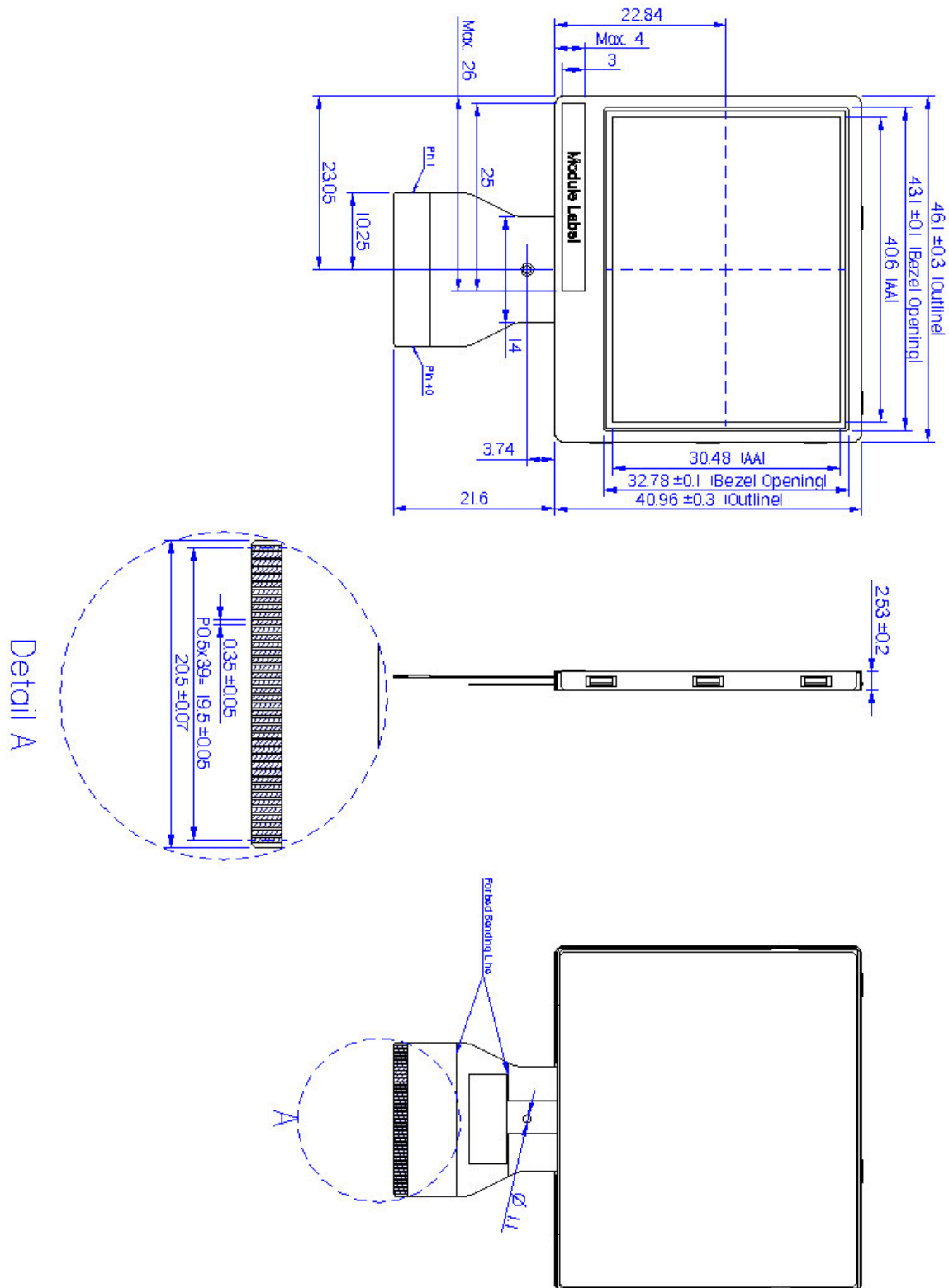(4) In the process of assembly the module, shield case should connect to the ground.

10.2      Environment

(1) Working environment of the panel should in the clean room.

(2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.
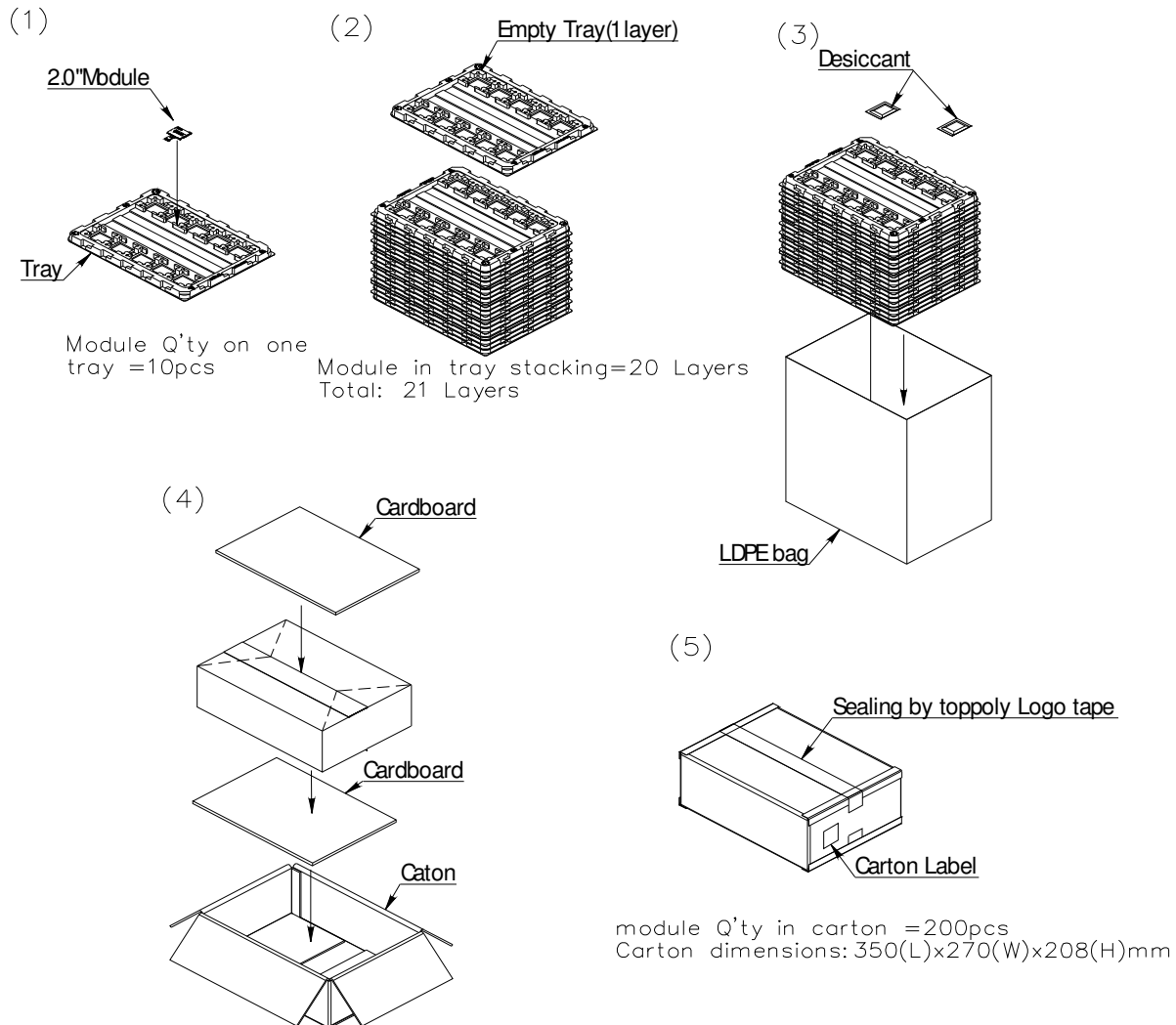
10.3      Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

## 11. MECHANICAL DRAWING

## 12. PACKING DRAWING

（1）

2.0"Module

Tray

Module Q'ty on one
tray =10pcs

（2） Empty Tray(1 layer)

Module in tray stacking=20 Layers
Total: 21 Layers

（3） Desiccant

LDPE bag

（4） Cardboard

Cardboard

Caton

（5）

Sealing by toppoly Logo tape

Carton Label

module Q'ty in carton =200pcs
Carton dimensions: 350(L)x270(W)x208(H)mm

2.0" module (TD020THEG1) delivery packing method

(1). Module packed into tray cavity (with Module display face down).

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
 2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put
 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape