FIR Filter Design using Distributed Arithmetic LookupTable

Project Scope:

FIR filter is a filter response to any finite length input in a finite duration, because it settles to zero in finite time. Generally FIR filter consists of Multipliers, Adders, Delay elements.FIR filter normally implemented in pulse shaping filter, digital phase-locked loop, as an anti-aliasing filter for sampling,it serve as an essential building block in most Digital Signal Processing (DSP) systems. A large application area is telecommunication, where filters are needed in receivers and transmitters, and an increasing portion of the signal processing is done digitally. FIR filter consists of many lookup table (LUTs) that multiply and accumulate bock and shift accumulator. The distributed arithmetic (DA) gives us a multiplication-free method to calculate its inner product based on LUT.

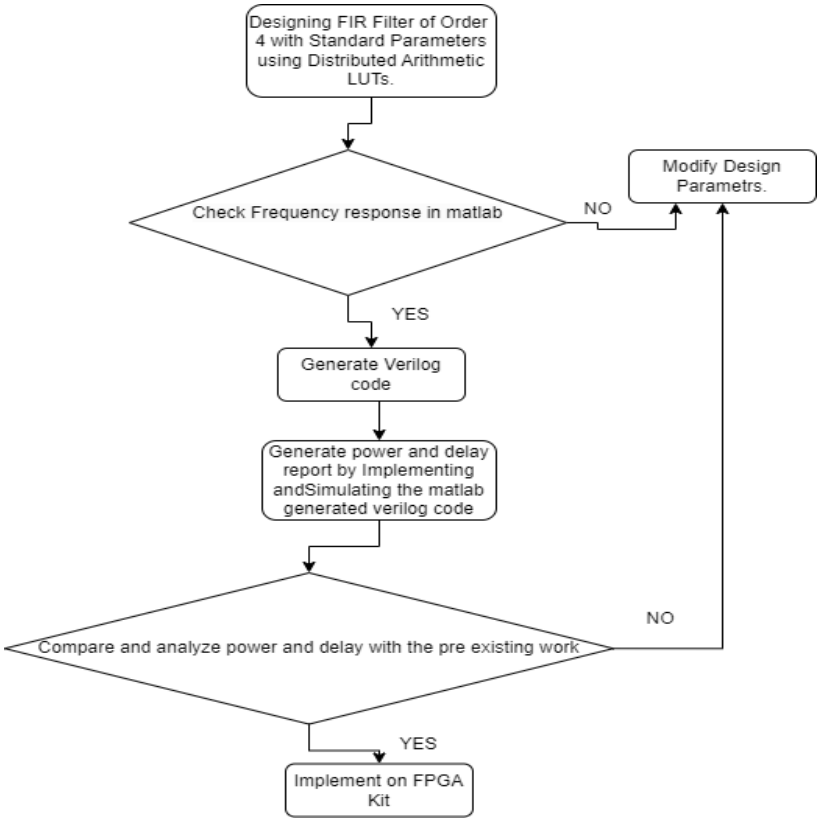
Objectives:

The main objectives of the project are:

1. To Study the different techniques to design a FIR Filter.
2. Analyzing the effect of Implementing Distributed Arithmetic techniques instead of multipliers in FIR filter circuit.
3. To achieve Optimization in terms power and delay for an FIR filter of order 8 &16.
4. Implementation on FPGA (preferably for order 4).

Methodology:

Our proposed design for FIR using Distributed Arithmetic technique.



Planning:

Here is a detailed plan for FIR Filter Design using Distributed Arithmetic of Lookup Table.

1. **Studying the different techniques of Designing FIR Filter:** Analyzing and comparing there frequency plots for FIR filters designed using different techniques

2. **Generating the verilog code from implemented FIR Filter using matlab:** With the components selected, you can start designing the hardware for the system. This will involve creating a schematic and laying out a printed circuit board (PCB) that incorporates all of the required components.

3. **Testing and implementing the generated verilog code in Xilinx software and Generating the Power and Delay Report**: In this step the generated verilog code is implemented and simulated in the xilinx software , we will be generating the RTL schematic , the technology schematic and the power and delay report using xpower analyzer.

4. **Comparing the power and delay of the designed fir filter with the pre-exsisting work**: Once the power and delay report is generated we will compare the results with the pre-exsisting work mentioned in our literature review and if the results are satisfying we will move forward otherwise we will observe the changes by modifying the other parameters.

5. **Selection of FPGA board :** After getting the satisfied result of power and delay calculations we will select an appropriate FPGA board for the implementation.

6. **Implementation on FPGA kit:** We will study the chosen FPGA kit and implement the generated code on the FPGA board and verify the results with the literature work.

Timeline:

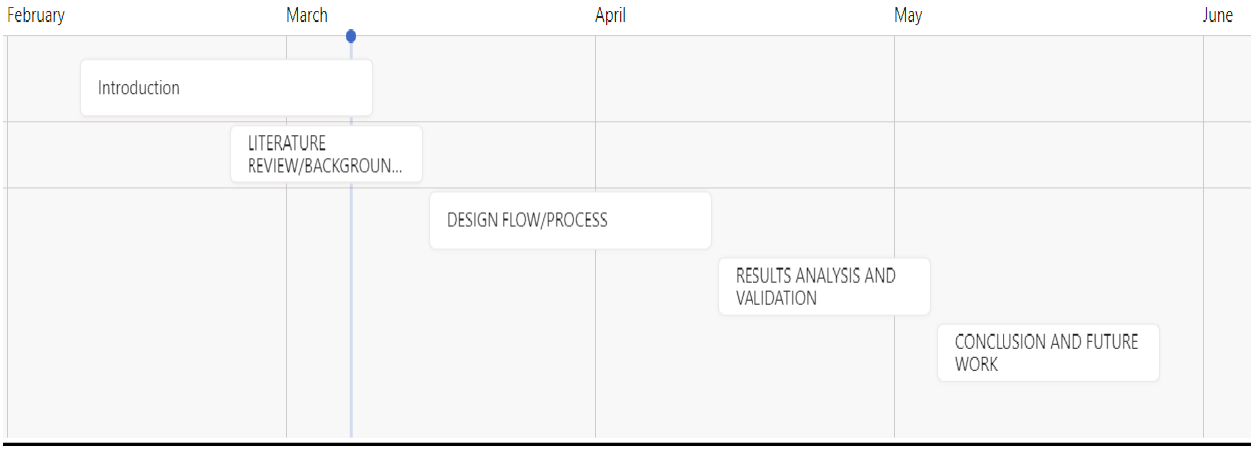


Figure 1.1: GANT CHAT

Task Definition:

1. **Study of different techniques to design FIR Filter**: Studying about different techniques to design FIR filters their features and functionalities and also about the application of FIR Filters in different areas/circuits like DSP,PLL Circuits, Hilbert Transformers etc.

2. **Analyzing the effect of Introducing Distributed arithmetic LookUpTables(LUTs) in place of multipliers**:We will understand the effect of LUTs on the FIR Filter designed using Distributed Arithmetic technique by comparing and analyzing their frequency response plots with the Filter designed through other techniques in Matlab.

3. **Optimization of the FIR Filter** : We will optimize the FIR Filter in terms of both power and delay where we will observe the change in power and delay of the circuit with respect to different parameters related to Distributed Arithmetic Structure of FIR filter.

4. **FPGA Implementation**:We will implement an fir filter(order three or four) designed using Distributed arithmetic technique on an a suitable FPGA Board and verify it's nature.

5. A project Report, which represents teams work.