LAYER DETAILS - BOARD STACKUP

LAYER	um	DETAILS	DATA REF
L1 TOP/SIG	18	PLATED TO 33.4 um MIN	*-L01.art
DIELECTRIC	115	PREPREG	
L2 GND	18	CU 1/2 OZ	*-L02.art
DIELECTRIC	355	CORE	
L3 PWR/SIG	18	CU 1/2 OZ	*-L03.art
DIELECTRIC		PREPREG TO SUIT OVERALL THICKNESS	
L4 PWR/SIG	18	CU 1/2 OZ	*-L04.art
DIELECTRIC	355	CORE	
L5 GND	18	CU 1/2 OZ	*-L05.art
DIELECTRIC	115	PREPREG	
L6 BOTTOM/SIG	18	PLATED TO 33.4 um MIN	*-L06.art

LAYER DETAILS - OTHER

LAYER	DETAILS	DATA REF
TOP PASTE MASK		*-TPM.art
TOP COMPONENT LEGEND	WHITE	*-TCL.art
TOP SOLDER MASK	GREEN	*-TSM.art
BOTTOM SOLDER MASK	GREEN	*-BSM.art
BOTTOM COMPONENT LEGEND	NONE	
BOTTOM PASTE MASK	NONE	
DRILL DWG/MECHANICAL		*-DRM.art
BOARD OUTLINE/EDGES		*-BRD.art
PLATED DRILL (LAYER X TO Y)	FORMAT: 3.3 / ABS / METRIC	*-X-Y.drl
NON-PLATED DRILL	FORMAT: 3.3 / ABS / METRIC	*-X-Y-np.drl
PLATED ROUTE	FORMAT: 3.3 / ABS / METRIC	*-X-Y.rou
NON-PLATED ROUTE	NONE	

DRILL CHART: TOP to BOTTOM

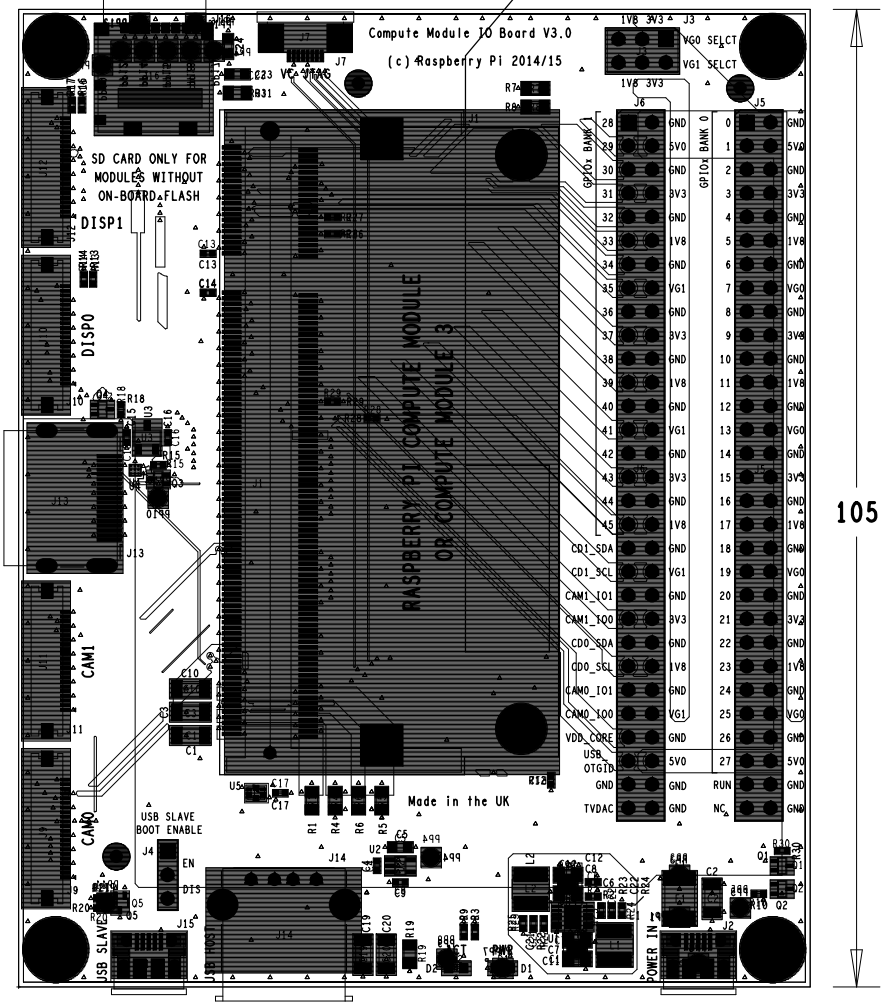
ALL UNITS ARE IN MILLIMETERS

FIGURE	SIZE	PLATED	QTY
△	0.25	PLATED	476
△	1.0	PLATED	133
△	2.3	PLATED	2
△	1.1	NON-PLATED	1
△	1.6	NON-PLATED	1
◯	2.4	NON-PLATED	2
△	3.4	NON-PLATED	4
○	1.05x0.65	PLATED	4
○	1.4x0.7	PLATED	4
⬭	1.7x0.9	PLATED	2
⬭	2.7x0.9	PLATED	2

DRILL DWG / MECHANICAL
TOP PASTE MASK
TOP COMPONENT LEGEND
TOP SOLDER MASK
BOTTOM SOLDER MASK
BOTTOM COMPONENT LEGEND

ADD MANUFACTURING CODES HERE
(ON TOP SIDE)

BOARD PANELISATION:
ROUTE TOP AND BOTTOM (SHORT) EDGES
V-SCORE LEFT AND RIGHT (LONG) EDGES



MANUFACTURING DETAILS

BOARD THICKNESS	1.6mm +/- 10%
BOARD FLATNESS	1% DEVIATION FROM MAX DIMENSION
PTH WALL THICKNESS	18um COPPER MINIMUM
HOLES (EXCL. VIAS)	ALL PLATED HOLES TO +/- 0.1mm ALL NON-PLATED HOLES TO +/- 0.05mm
VIAS	FINISHED HOLE SIZE NOT CRITICAL CHOOSE DRILL SIZE FOR BEST YIELD
FINISH	NICKEL/GOLD (ENIG)
SOLDER RESIST	GREEN LIQUID-IMAGED (BOTH SIDES)
LEGEND	WHITE PHOTO-IMAGED
MANUFACTURING CODES	ADD MANUF. CODES WHERE INDICATED
UL REQUIREMENTS	BOARD TO BE MANUFACTURED TO UL94-V0

CONTROLLED IMPEDANCE DATA

IMPEDANCE	90R		100R	100R
TYPE	EC MICSTP		EC MICSTP	EC MICSTP
LAYER(S)	L1		L1	L6
REF. PLANE(S)	L2		L2	L5
TRACE WID	136u		116u	116u
TRACE GAP	115u		135u	135u
TOLERANCE	+/- 10%		+/- 10%	+/- 10%

Raspberry Pi
www.raspberrypi.org

TITLE	RASPBERRY PI COMPUTE MODULE IO BOARD		
DATE	16/09/2015	REF	RPI-CMIO V3.0
DRAWN	James Adams	APVD	James Adams