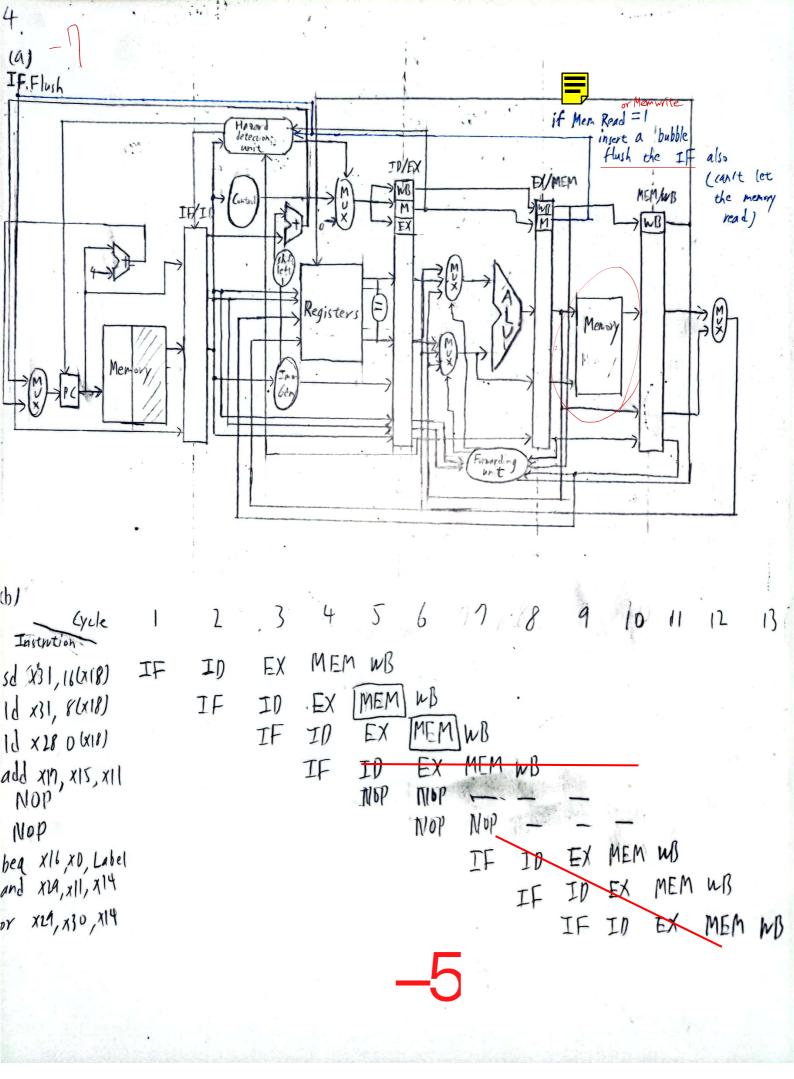
HW4 Computer Architecture (a) sd, beg () A, add, sub, beg (c) add, sub Branch Mem Read MemtoReg ALUOp MenWrite ALUSTE RegWrite (1) Reg [5] Reg [20] ld will be the instruction whose latency is the longest. 1d: 30 (PC Read) + 200 (I-Men) + 140 (Register File) + 30 (Mux) + 160 (ALU) + (200 (D-Mem) + 30 (Mux) + 20 (Register Setup) = 810 ps The shortest possible clock period should be long enough to process Id, so should be at least 80 ps, Cycle IF ITID TEX MEM 18 x5/0(x28) (sul x6, x6, x5 (d x5,0(x28)) Id X5, O(XXX) 5546 x6, x6, x5 sub x6, x6, x5 beg x18, x29, L1 Sonb x6, x6, x6, x6 (d x5, o (208) 4 5 sd 128,0(x19) beg 128, x29, L1 sub x6, x6, x5 hop 1d(x5, o(x28) exception handler nop 6 sub x6, x6, 15



Clock rate: 300MHz (a) 30 ns => 9 cycles = (7-1)+5=> 5=3 55=15 = 15+(1-1) = 21 Gales. => 10ns 4) NS = 27 cycles, S instructions (N-1) + S = 27 => S = 12, N=16 (b) 290 ms = 3 87 gcles, 65 instructions (N-1) + 65 = 87 7. (a) always-token: = 37.5% alrays-hot-taken: 5 = 62.5% (b) Accuracy: 4 = 50% (4) ST: Strongly taken SNT: Strongly Not taken SNT SNT SNT WIT SNT WT: Weakly taken WNJ. Weakly Not taken NT NT NT NT Accuracy: 8=62.5% (a) Id X5,-32(x4) (p) 19 x2 -35 (x4) (c) |d x5,-12(x4) (d) 5+4=9 cycles MOP Not I they 18 xb,-16(x4) NOP 4.11 x1,-16 (x4). NOP 211 x1, -11(x4) ald x6, x5, x6 ald x6, x5, x6 NOP add x6,x6,x6 add x6,x1,x6 MOP (i) 5 add xl,xs,xl Nop *1 1 (ii) 1)

3 (111) 6

NOP

ald xb, xl, xl