Department of Computer Science
National Tsing Hua University
EECS403000 Computer Architecture
Spring 2023 Homework 4

Deadline: 2023/5/18 10:10

1. (15 points) A common defect in silicon chips is for one signal wire to always get a constant logic value 0 (1, respectively); it is called a stuck-at-0 (stuck-at-1, respectively) fault. Consider the single-cycle processor for the following instructions: ld, sd, add, sub, and beq.
   (a) (5 points) Which instruction(s) could fail to operate correctly if the RegWrite wire is stuck at 1?
   (b) (5 points) Which instruction(s) could fail to operate correctly if the MemRead wire is stuck at 1?
   (c) (5 points) Which instruction(s) could fail to operate correctly if the ALUop1 wire is stuck at 0?
2. (10 points) Consider the execution of the machine instruction $FF4288E3_{hex}$ on the single-cycle processor.
   (a) (7 points) What are the values of the signals: Branch, MemRead, MemtoReg, ALUOp, MemWrite, ALUSrc, and RegWrite?
   (b) (3 points) What are the input values of the ALU? You can use Reg[x] to denote the value of register x.
3. (10 points) Assume that the positive edge-triggered clocking methodology, i.e., the clock takes effect on a rising clock edge, is adopted and the logic blocks used to implement the single-cycle processor have the following delay values:

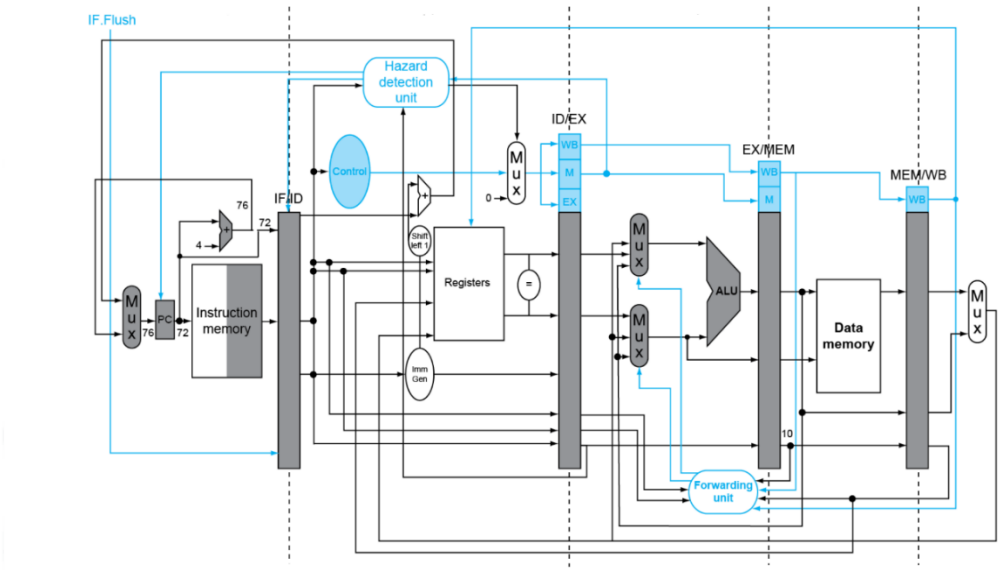
I-Mem/D-Mem	Register File	Mux	ALU	Adder
200 ps	140 ps	30 ps	160 ps	140 ps
AND Gate	PC Read	Register Setup	Imm Gen	Control
10 ps	30 ps	20 ps	40 ps	40 ps

"I-Mem/D-Mem" is the amount of time to access the Instruction or Data Memory.
"Register File" is the amount of time to read rs1 and rs2.
"PC Read" is the amount of time for the new PC value to appear on the output of the PC register after a rising clock edge; this delay value applies to the PC only.
"Register Setup" is the amount of time a register's data input must be stable before a rising clock edge; this delay value applies to both the PC and Register File.
"Control" is the total amount of time for the Control unit and the ALU control unit to produce the 4-bit "ALU operation".

What is the shortest possible clock period for the single-cycle processor? Justify your answer.

4. (15 points) Suppose that the pipelined processor now has only one memory to store both instructions and data, which means that there will be a structural hazard every time an instruction is fetched during the same cycle in which another instruction accesses data. Also suppose that the branch prediction strategy is always-not-taken.

   (a) (10 points) Show how to modify the following figure such that structural hazards are resolved by stalls.



   (b) (5 points) Consider the following sequence of instructions where the branch outcome of the beq instruction is not taken.

```
Label:  sd x31, 16(x18)
        ld x31, 8(x18)
        ld x28, 0(x18)
        add x17, x15, x11
        beq x16, x0, Label
        and x29, x11, x14
        or x29, x30, x14
```

   Fill in the table below to show how the instructions are executed on the processor given in (a). Note that you may increase or decrease the table size according to your answer.

Instructions	Cycle 1	Cycle 2	…	…	Cycle n
sd x31, 16(x18)	IF	ID	…		
…					
…					

5. (20 points) Consider the following sequence of instructions executed on the five-stage pipelined processor. Assume that the execution starts in clock cycle 1.

   ld x5, -32(x4)
   ld x6, -16(x4)
   add x6, x5, x6
   add x6, x6, x6

   (a) (4 points) Assume both the forwarding unit and hazard detection unit are not present in the processor. Show how to insert a minimum number of NOP (no operation) instructions to ensure correct execution.

   (b) (4 points) Assume the processor has only the forwarding unit. Show how to insert a minimum number of NOP instructions to ensure correct execution.

   (c) (9 points) Assume the processor has the forwarding unit and hazard detection unit. For each of the following three conditions, indicate in which clock cycle, it is true for the processor.

   (i) (3 points) All control signals to be stored in the ID/EX register are set to 0.

   (ii) (3 points) The correct data is forwarded from the EX/MEM register to one ALU input.

   (iii) (3 points) The correct data is forwarded from the MEM/WB register to one ALU input.

   (d) (3 points) Assume the processor has the forwarding unit and hazard detection unit. How many clock cycles does the processor take to complete the execution of the code?

6. (10 points) Answer the following questions by assuming the clock rate is 300MHz and no pipeline stalls occur.

   (a) (5 points) If a 7-stage pipelined processor takes 30 ns to execute S instructions, how long will it take to execute 5S instructions?

   (b) (5 points) Consider a pipelined processor which has N stages. Suppose it takes 90 ns to execute S instructions and 290 ns to execute 6S instructions. What are N and S, respectively?

7. (10 points) Consider the sequence of branch outcomes: T, NT, NT, NT, NT, T, NT, T, for a branch instruction that has been executed 8 times in a program, where T

denotes taken and NT denotes not-taken.

(a) (4 points) What are the accuracy rates of the always-taken and always-not-taken predictors for this sequence of branch outcomes, respectively?

(b) (3 points) Consider a 1-bit dynamic predictor which starts at the T state. What is the accuracy rate of the predictor for this sequence of branch outcomes?

(c) (3 points) Consider a 2-bit dynamic predictor which starts at the "strongly predict not taken" state. What is the accuracy rate of the predictor for this sequence of branch outcomes?

8. (10 points) Consider the execution of the following sequence of instructions on the five-stage pipelined processor that uses the always-not-taken strategy for branch prediction and has both the forwarding unit and hazard detection unit.

```
ld x5, 0(x28)
sub x6, x6, x5
beq x28, x29, L1
sd x28, 0(x29)
```

Suppose the third instruction is detected to have an invalid target address and cause an exception in the ID stage. Fill in the table below by showing what instructions are in the IF, ID, EX, MEM, and WB stages, respectively, in clock cycles 1, 2,…, 6. Note that each instruction in your answer should be one chosen from the given instructions, the bubble, and the first instruction of the exception handler.

	IF	ID	X	MEM	WB
Cycle 1		-	-	-	-
Cycle 2			-	-	-
Cycle 3				-	-
Cycle 4					-
Cycle 5					
Cycle 6					