VLSI HW2

Name: 徐竣霆
Student ID: 110060012

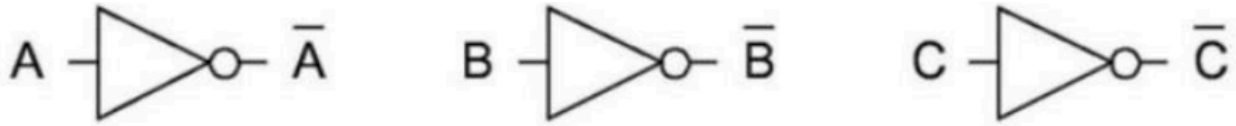
Some important design rule for .18

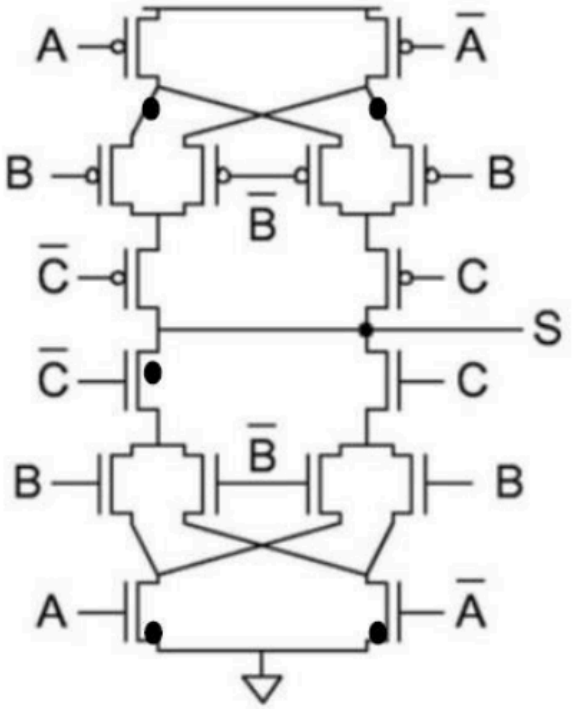
- $W_{cont} = 0.23$
- $S_{cont-diff} = 0.12$
- $W_{cont-diff} = 0.47$
- $S_{imp-diff} = 0.2$
- $S_{poly-cont} = 0.14$
- $S_{m1-m1} = 0.24$
- $S_{cont-cont} = 0.25$
- $S_{m2-m2} = 0.27$
- $W_{m1} = 0.23$
- $W_{m2} = 0.25$
- $W_{via(m1,m2)} = 0.25$
- $S_{diff-cont-poly} = 0.49$
- $S_{poly-cont-poly} = 0.51$
- $S_{poly-poly} = 0.25$
- $S_{poly-diff} = 0.2$
- $S_{m1-cont} = 0.1$

The circuit diagram of my design and explaining my design

HW2

Graph





Code

```
**Your code**
.subckt INV in inv_out VDD GND
Mp1 inv_out in VDD VDD p_18 l=0.18u w=0.47u
Mn1 inv_out in GND GND n_18 l=0.18u w=0.47u
.ends

**Your design**
.subckt hw2_XOR A B C S VDD GND
**Your code**
Xinv1 A inv_A VDD GND INV
Xinv2 B inv_B VDD GND INV
Xinv3 C inv_C VDD GND INV
Mp1 n1 A VDD VDD p_18 l=0.18u w=0.47u
Mp2 n2 inv_A VDD VDD p_18 l=0.18u w=0.47u
Mp3 n3 B n1 VDD p_18 l=0.18u w=0.47u
Mp4 n3 inv_B n2 VDD p_18 l=0.18u w=0.47u
Mp5 n4 inv_B n1 VDD p_18 l=0.18u w=0.47u
Mp6 n4 B n2 VDD p_18 l=0.18u w=0.47u
Mp7 S inv_C n3 VDD p_18 l=0.18u w=0.47u
Mp8 S C n4 VDD p_18 l=0.18u w=0.47u
Mn1 n5 A GND GND n_18 l=0.18u w=0.47u
Mn2 n6 inv_A GND GND n_18 l=0.18u w=0.47u
Mn3 n7 B n5 GND n_18 l=0.18u w=0.47u
Mn4 n7 inv_B n6 GND n_18 l=0.18u w=0.47u
Mn5 n8 inv_B n5 GND n_18 l=0.18u w=0.47u
Mn6 n8 B n6 GND n_18 l=0.18u w=0.47u
Mn7 S inv_C n7 GND n_18 l=0.18u w=0.47u
Mn8 S C n8 GND n_18 l=0.18u w=0.47u
.ends
```

Since I can only stick to the diagram, there is no much I can do(nothing left for me to design). I only use `w=0.47u` instead of `w=0.25u` due to the DRC in layout(physical) design.

Bonus

Graph

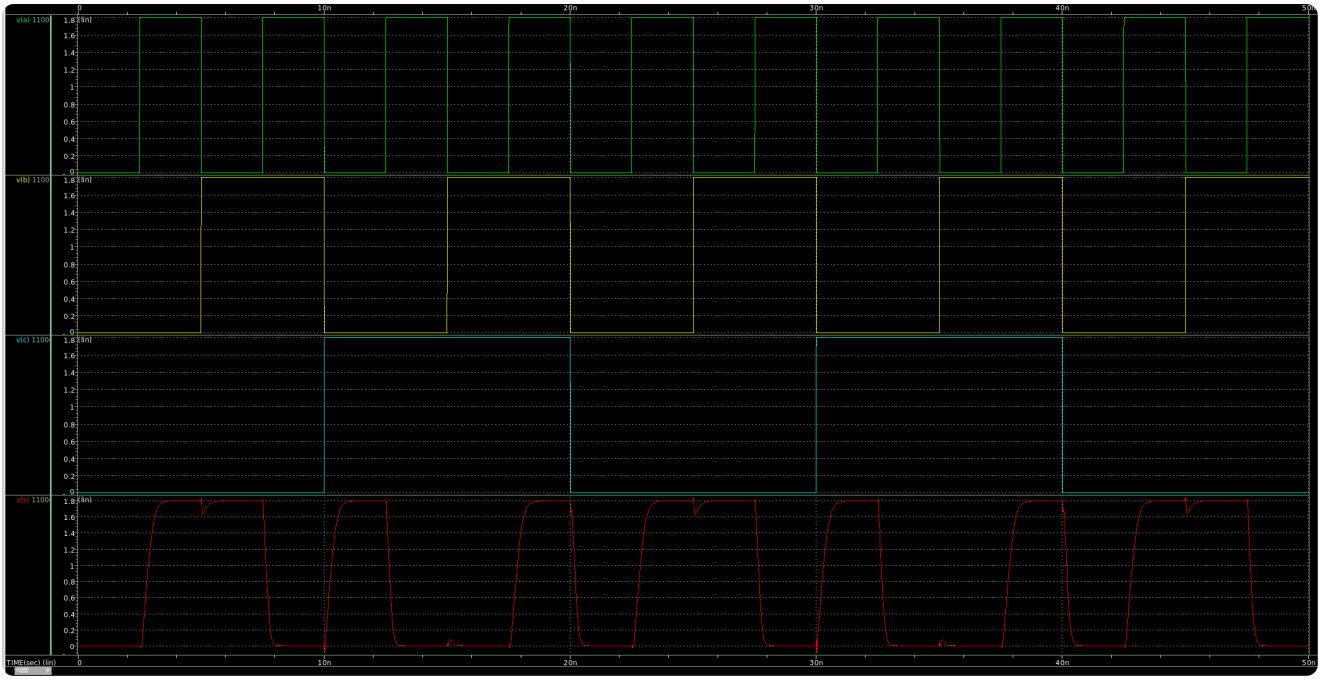
Code

```
**Your code**
.subckt INV in inv_out VDD GND
Mp1 inv_out in VDD VDD p_18 l=0.18u w=0.47u
Mn1 inv_out in GND GND n_18 l=0.18u w=0.47u
.ends

**Your design**
.subckt hw2_bonus A B C S VDD GND
**Your code**
Xinv1 A inv_A VDD GND INV
Xinv2 B inv_B VDD GND INV
Xinv3 C inv_C VDD GND INV
Mn1 n1 inv_B A GND n_18 l=0.18u w=0.47u
Mp1 n1 B A VDD p_18 l=0.18u w=0.47u
Mn2 n1 B inv_A GND n_18 l=0.18u w=0.47u
Mp2 n1 inv_B inv_A VDD p_18 l=0.18u w=0.47u *A ^ B
Xinv4 n1 inv_n1 VDD GND INV
Mn3 S inv_n1 C GND n_18 l=0.18u w=0.47u
Mp3 S n1 C VDD p_18 l=0.18u w=0.47u
Mn4 S n1 inv_C GND n_18 l=0.18u w=0.47u
Mp4 S inv_n1 inv_C VDD p_18 l=0.18u w=0.47u *A ^ B ^ C
.ends
```

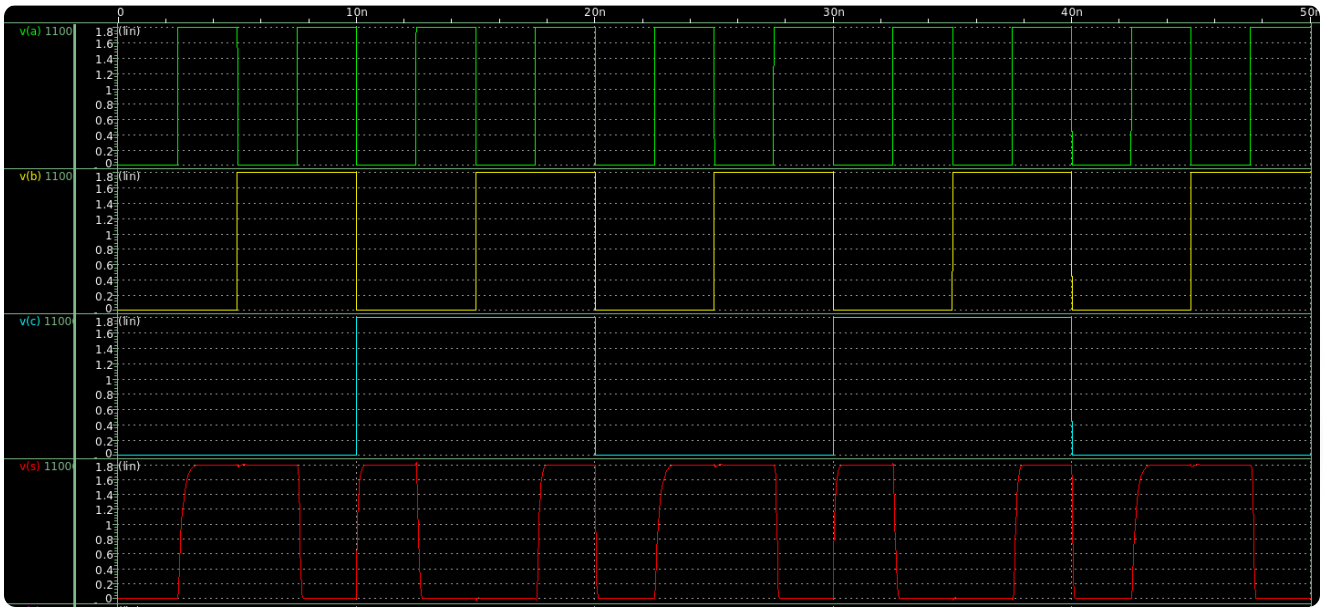
I have tried using n-mos only, but the voltage drop($V_d = max(V_s, V_g - V_{Th})$), so I choose to add p-mos as trasmission gate(which can also be considered as pass transisstor method).

Pre-sim waveform

HW2

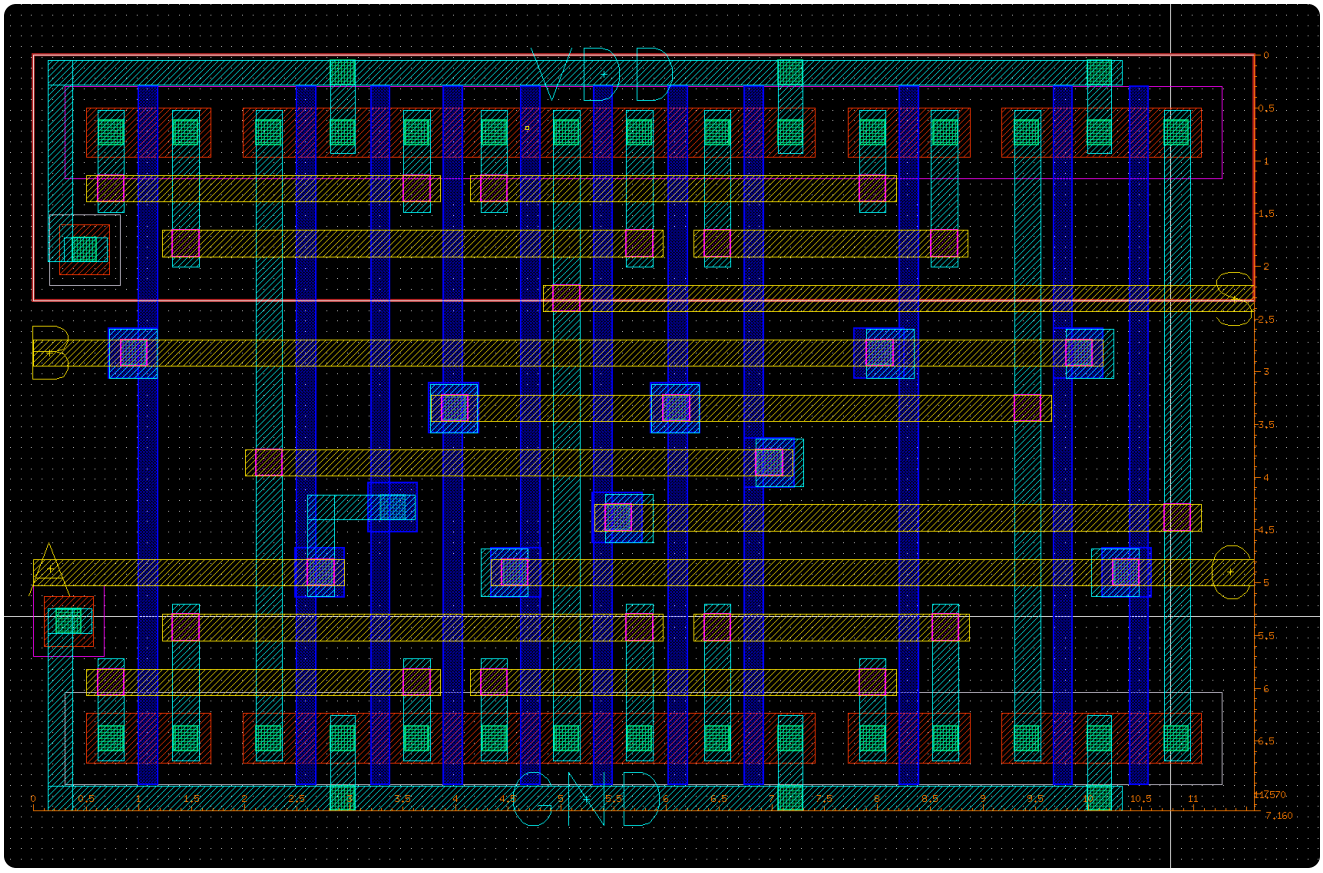


Bonus



Screenshot of my layout

HW2



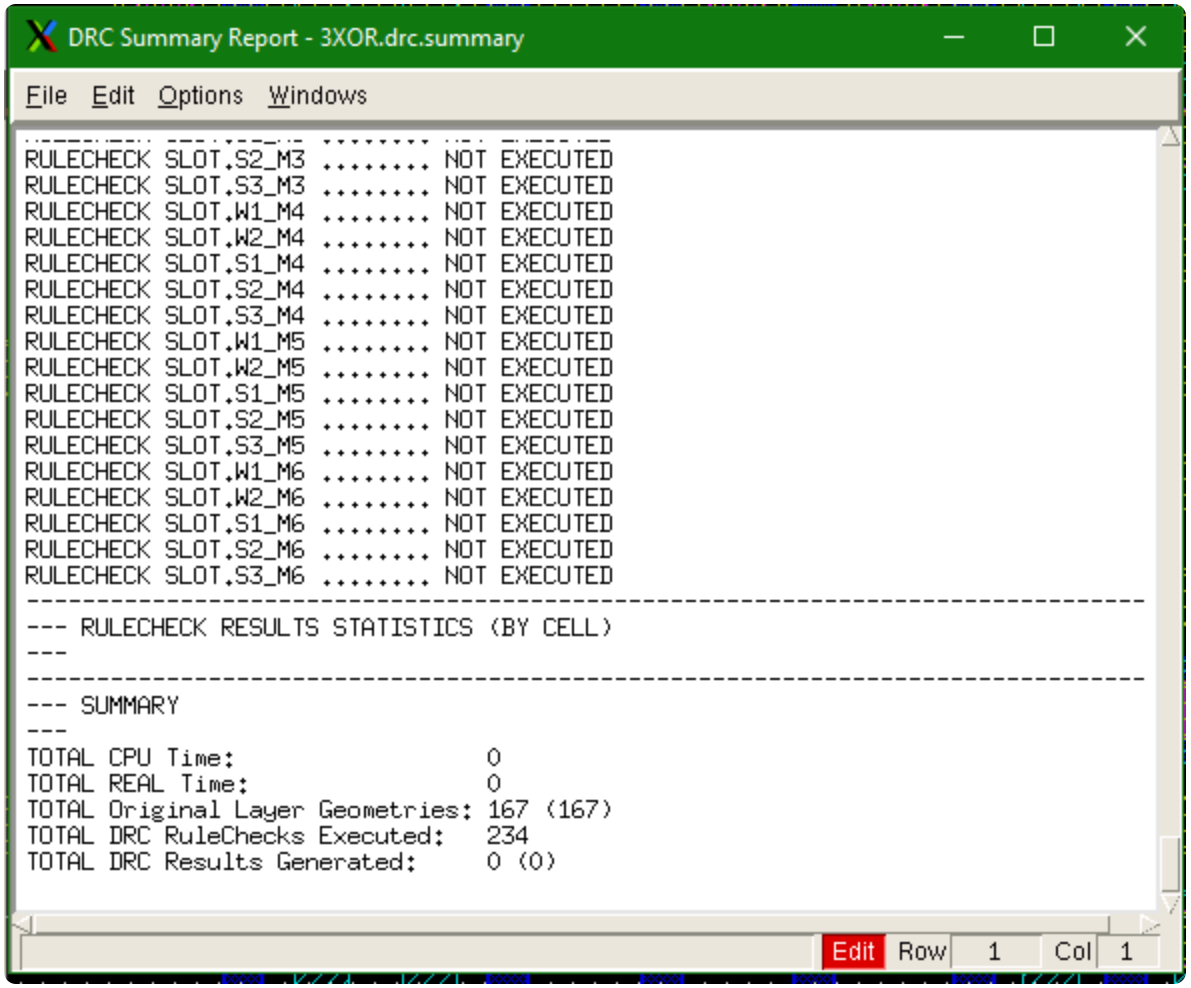
My area: $(0.79 - (-10.78)) * (5.32 - (-1.84)) = 11.57 * 7.16 = 82.8412(\mu m^2)$

Bonus

Drawing layout is driving me crazy, I choose not to prolong my suffering :).
Although the layout of this bonus part will be much easier, since I can design my own logic and thus save a lot of trassistors(in my design, only 16, and it can be less or share some diffusion or poly).

Screenshot of DRC summary report

HW2



Bonus

As mentioned above.

Screenshot of LVS report includes the message of passing LVS

HW2

Cell hw2_XOR Summary (Clean)

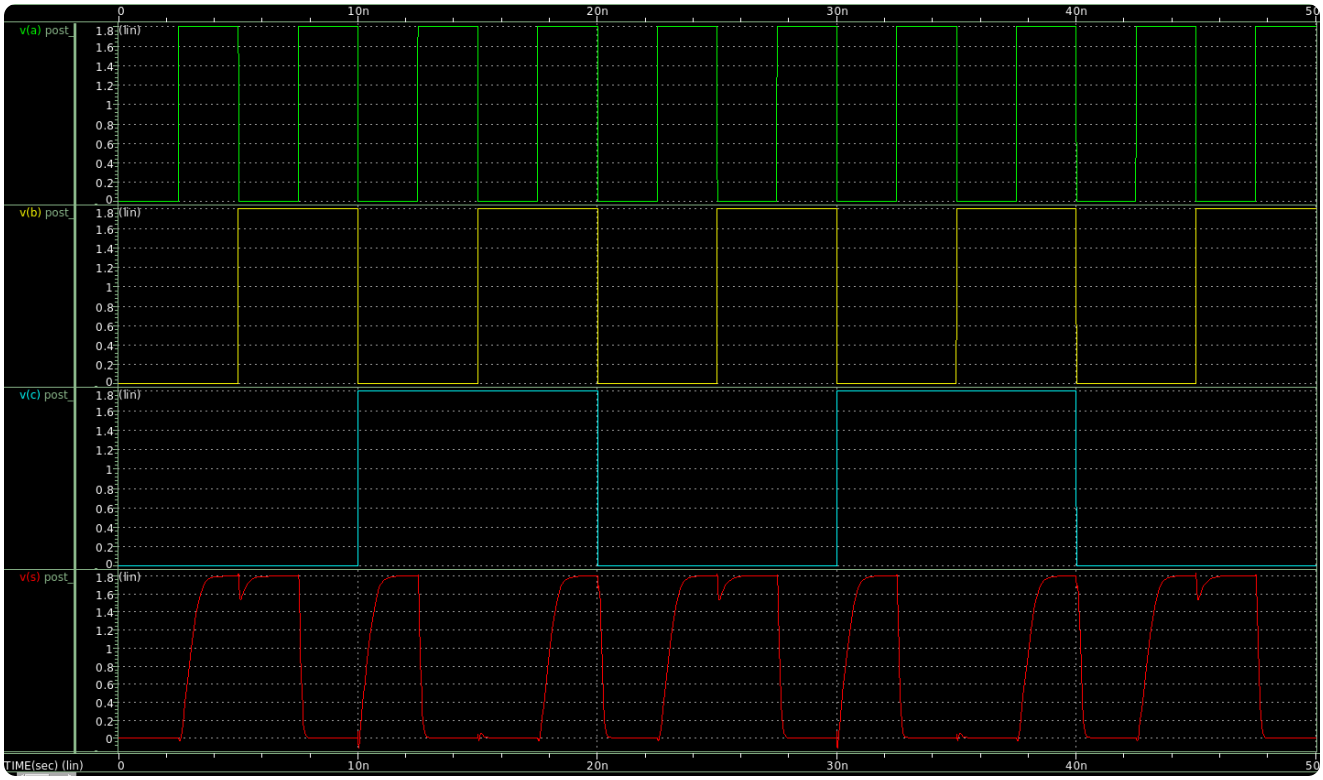
```
                  CELL COMPARISON RESULTS ( TOP LEVEL )



                       #       ####################       _   _
                     #         #                  #       *   *
                  #    #       #     CORRECT      #         |
                   # #         #                  #        \___/
                    #          ####################


LAYOUT CELL NAME:         hw2_XOR
SOURCE CELL NAME:         hw2_XOR

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              6         6

 Nets:              17        17

 Instances:         11        11         MN (4 pins)
                    11        11         MP (4 pins)
                ------    ------
 Total Inst:        22        22


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              6         6

 Nets:              17        17

 Instances:          8         8         MN (4 pins)
                     8         8         MP (4 pins)
                     3         3         _invv (4 pins)
                ------    ------
 Total Inst:        19        19


**************************************************************************************************************
                              INFORMATION AND WARNINGS
**************************************************************************************************************


                  Matched    Matched    Unmatched    Unmatched    Component
                   Layout     Source      Layout       Source     Type
                  -------    -------    ---------    ---------    ---------
   Ports:               6          6            0            0

   Nets:               17         17            0            0

   Instances:           8          8            0            0    MN(N_18)
                        8          8            0            0    MP(P_18)
                        3          3            0            0    _invv
                  -------    -------    ---------    ---------
   Total Inst:         19         19            0            0
```

Bonus

As mentioned above.

Post-sim waveform

HW2



Bonus

As mentioned above.

Screenshot of the post-simulation result

HW2

```
******
**110060012_hw2_xor**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=  18.2489u  from=   0.             to=  50.0000n
delay1_xor=  -2.0337n  targ=  17.9813n   trig=  20.0150n
delay2_xor=  -2.0086n  targ=   3.0064n   trig=   5.0150n

         ***** job concluded
******
**110060012_hw2_xor**
```

Bonus

As mentioned above.

Write down your delay and the difference in delay between rising and falling delay in the 3-input XOR gate.

HW2

Pre-sim

```
******
**110060012_hw2_xor**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=  11.3806u  from=   0.             to=  50.0000n
delay1_xor=  -2.1901n  targ=  17.8249n   trig=  20.0150n
delay2_xor=  -2.1801n  targ=   2.8349n   trig=   5.0150n

   |   |   |***** job concluded
******
**110060012_hw2_xor**
```

$Delay1_{XOR} = -2190.1\text{ps}$

$Delay2_{XOR} = -2180.1\text{ps}$

$|Delay1_{XOR} - Delay2_{XOR}| = 10\text{ps}$

Post-sim

```
******
**110060012_hw2_xor**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=  18.2489u  from=   0.             to=  50.0000n
delay1_xor=  -2.0337n  targ=  17.9813n   trig=  20.0150n
delay2_xor=  -2.0086n  targ=   3.0064n   trig=   5.0150n

         ***** job concluded
******
**110060012_hw2_xor**
```

$Delay1_{XOR} = -2033.7\text{ps}$
$Delay2_{XOR} = -2008.6\text{ps}$
$|Delay1_{XOR} - Delay2_{XOR}| = 25.1\text{ps}$

Bonus

Pre-sim

```
******
**110060012_hw2_bonus**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=   7.6692u  from=   0.             to=  50.0000n
delay1_xor=  -2.3665n  targ=  17.6485n   trig=  20.0150n
delay2_xor=  -2.3675n  targ=   2.6475n   trig=   5.0150n

   |    |    |***** job concluded
******
**110060012_hw2_bonus**
```

$Delay1_{XOR} = -2366.5\text{ps}$
$Delay2_{XOR} = -2367.5\text{ps}$
$|Delay1_{XOR} - Delay2_{XOR}| = 1\text{ps}$

Post-sim

As mentioned above.

The hardness of this assignment and how you overcome it

First of all, the issues caused by incompatible environment have made my layout-drawing journey unnecessary long and thorny. I tried Ubuntu(my major OS) first, the remote terminal kept saying that I have no sudoer permission(BadName, so I have to install something remotely). Then I tried my Mac, which worked after I installed some X11 forwarding tools, while it's extremely slow. I had no other choice but switch to windows and installed mobaXterm, not knowing there were a whole bunch of other problems were waiting for me. First of all, I think the tutorial of Virtuoso is imcomplete, and the online sources is very limited. For example, if I use the whole .sp file in the LVS process instead of .cir file with the circuit only, there will be some undebuggable errors. It took me almost a day to find out the reason. Second of all, a lot of important thing haven't been demonstrated in the video, and these are not easy to figure out by merely reading the pdf provided.

Any suggestions about this programming assignment

I think the tutorial video could be more thorough, so that a lot of troubles and discussions on eeclass can be saved. And most of the problems on eeclass get really prompt responses, I can sense the efforts TA put into that. Thanks for the hard work!