CS3120 Introduction of Integrated Circuit Design

Homework 2: Layout Design

Due Date: 2024/11/17(Sun) 23:59:59

- **Version: 20241105**
- **Version: 20241113**
- **Version: 20241114_1130**
- **Version: 20241114_1730**

Background

In VLSI circuit design, there are many fundamental building blocks, including memories, controllers, registers, and more. These modules are used to implement a wide range of complex functions. Layout methods and Electronic Design Automation (EDA) tools play crucial roles in helping designers transform circuit designs into manufacturable layouts. The physical arrangement directly impacts a circuit's performance, functionality, and reliability. As VLSI technology continues to advance, the demand for more sophisticated and power-efficient circuits grows. This places greater emphasis on optimizing not only the individual building blocks but also the overall system design. Additionally, the relentless pursuit of smaller chip sizes and lower manufacturing costs poses both challenges and opportunities for VLSI designers. A thoughtfully planned layout minimizes signal interference, reduces delays, and ensures efficient thermal management.

Description

In practical scenarios, IC designs need to have the ability to drive specific load, and make sure the operation of the load will work successfully. However, it is difficult to drive a load for a single combinational circuit. In this layout assignment, you are asked to generate a 50% duty cycle by an XOR gate.

- **3-input XOR gate**

  The XOR gate is widely used in digital circuits for addition, logical operations, and other functions. A 3-input XOR gate consists of 3 input channels, which are A, B, and C, and a output channel, S. When S = ABC + AB'C' + A'BC' + A'B'C, the output is 1. A XOR gate can be composed of inverters and transistors, or it can be

designed with different layout strategies to optimize for specific parameters. In this assignment, we hope to use the form below to complete the multiplexer (Fig.1). The input should include the combinations of **(C, B, A) = (0, 0, 0), (0, 0, 1), (0, 1, 0), (0, 1, 1), (1, 0, 0), (1, 0, 1), (1, 1, 0) and (1, 1, 1)** in sequence.

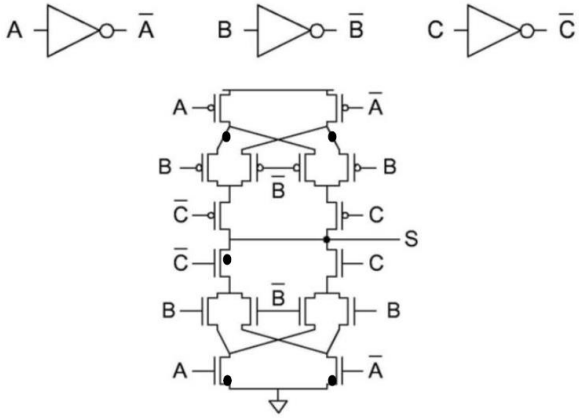


Fig. 1 3-input XOR gate

In the 3-input XOR gate, add a capacitance of 0.005 pF to the output S. Please make the power consumption as low as you can. We will make a comparison of the power consumption of all designs. The design with lower power consumption will get a higher grade.

Limitations

Below are the guidelines that must be adhered to for this assignment. **Any violation of these guidelines will result in 0 points for this HW.**

Environment setup and parameters

- The naming and pinouts of each input and output must match the figures provided in this document.
- The operating voltage (VDD) is set to 1.8V and the operating temperature is 30˚C.
- In 3-input XOR gate, the capacitive of S is 0.005pF.
- For transistors, please set the L = 0.18um, while the minimum value of W is 0.25um and the value of W can be adjusted as needed.
- Only Metal 1、Metal 2 and Via can be used when routing.
- You must use the same approach as 'cic018.l' and 'cic18.tf' in HW2 to do this assignment; otherwise, you will get 0 points.

Inputs and outputs

3-input XOR gate:

- In the design of the 3-input XOR gate, the signals A, B, and C has a 50% duty cycle. A operates at 200 MHz, B at 100 MHz, and C at 50 MHz.
- The order of input combinations **(C, B, A)** should match the sequence mentioned in this document.
- Set the rise/fall time of the input signals to 10ps.
- The highest logic level for all outputs must be greater than 0.9VDD, while the lowest logic level must be less than 0.1VDD.
- Delay1_XOR represents the delay when the signal A and S are falling, while Delay2_XOR represents the delay when the signal A and S are rising.

Input files

- spice_layout.tar

Output files

3-input XOR gate

If using .cir for .sp for circuit:

- **hw2_XOR.pex.cir**
- **hw2_XOR.pex.cir.HW2_XOR.pxi**
- **hw2_XOR.pex.cir.pex**

If using only .sp for circuit:

- **hw2_XOR.pex.netlist**
- **hw2_XOR.pex.netlist.HW2_XOR.pxi**
- **hw2_XOR.pex.netlist.pex**

Coding style

- Pre-simulation

3-input XOR gate

```
**StudentID_HW2_XOR**
**Environment setting**

**Your code**

**Your design**
.subckt hw2_XOR A B C S VDD GND
**Your code**
.ends

**Main circuit**
Xhw2_XOR A B C S VDD GND hw2_XOR
C1 S GND 0.005p

**Input signal**
**Your code**

**Simulation setting**
.tran   0.01n   50n
.measure tran power AVG POWER
.meas   tran    Delay1_XOR      trig    v(A)    val=0.9 fall=4
+                               targ    v(S)    val=0.9 fall=3
.meas   tran    Delay2_XOR      trig    v(A)    val=0.9 rise=1
+                               targ    v(S)    val=0.9 rise=1
.end
```

- Post-simulation

3-input XOR gate

```
**StudentID_HW2_XOR**
**Environment setting**

**Your code**

**Main circuit**
Xhw2_XOR A B C S VDD GND hw2_XOR
C1 S GND 0.005p

**Input signal**
**Your code**

**Simulation setting**
.tran   0.01n   50n
.measure tran power AVG POWER
.meas   tran    Delay1_XOR      trig    v(A)    val=0.9 fall=4
+                               targ    v(S)    val=0.9 fall=3
.meas   tran    Delay2_XOR      trig    v(A)    val=0.9 rise=1
+                               targ    v(S)    val=0.9 rise=1
.end
```

Bonus

Design 3-input XOR gate using pass transistors. Three inputs are A, B, and C; the output is S.

Limitations

Below are the guidelines that must be adhered to for this assignment. **Any violation of these guidelines will result in 0 points for this HW.**

Environment setup and parameters

- The naming and pinouts of each input and output must match the figures provided in this document.
- In 3-input XOR gate, the capacitive of S is 0.005pF.
- For transistors, please set the L = 0.18um, while the minimum value of W is 0.25um and the value of W can be adjusted as needed.
- You must use the same approach as 'cic018.l' and 'cic18.tf' in HW2 to do this assignment; otherwise, you will get 0 points.

Inputs and outputs

- The signals A, B, and C exhibit a 50% duty cycle. A operates at 200 MHz, B at 100 MHz, and C at 50 MHz.
- Set the rise/fall time of the input signals to 10ps.
- The order of input combinations **(C, B, A)** should match the sequence mentioned in this document.
- The highest logic level for all outputs must be greater than 0.9VDD, while the lowest logic level must be less than 0.1VDD.
- Delay1_XOR represents the delay when signals A and S are falling, while Delay2_XOR represents the delay when signals A and S are rising.
- The power of the bonus circuit layout must be smaller than that of the 3-input XOR gate which is composed of whole transistors and inverters.

Input files

- spice_layout.tar

Output files

If using .cir for .sp for circuit:

- **hw2_bonus.pex.cir**
- **hw2_bonus.pex.cir.HW2_bonus.pxi**
- **hw2_bonus.pex.cir.pex**

If using only .sp for circuit:

- **hw2_bonus.pex.netlist**
- **hw2_bonus.pex.netlist.HW2_bonus.pxi**

- **hw2_bonus.pex.netlist.pex**

Coding style

- Pre-simulation

```
**StudentID_HW2_bonus**
**Environment setting**

**Your code**

**Your design**
.subckt hw2_bonus A B C S VDD GND
**Your code**
.ends

**Main circuit**
Xhw2_bonus A B C S VDD GND hw2_bonus
C1 S GND 0.005p

**Input signal**
**Your code**

**Simulation setting**
.tran   0.01n   50n
.measure tran power AVG POWER
.meas   tran    Delay1_XOR      trig    v(A)    val=0.9 fall=4
+                               targ    v(S)    val=0.9 fall=3
.meas   tran    Delay2_XOR      trig    v(A)    val=0.9 rise=1
+                               targ    v(S)    val=0.9 rise=1
.end
```

- Post-simulation

```
**StudentID_HW2_bonus**
**Environment setting**

**Your code**

**Main circuit**
Xhw2_bonus A B C S VDD GND hw2_bonus
C1 S GND 0.005p

**Input signal**
**Your code**

**Simulation setting**
.tran   0.01n   50n
.measure tran power AVG POWER
.meas   tran    Delay1_XOR      trig    v(A)    val=0.9 fall=4
+                               targ    v(S)    val=0.9 fall=3
.meas   tran    Delay2_XOR      trig    v(A)    val=0.9 rise=1
+                               targ    v(S)    val=0.9 rise=1
.end
```

Submission Requirement

You have to submit a tar file named StudID_HW2.tar (ex: 9862534_HW2.tar). There are two folders in the tar file, HW2_XOR and HW2_bonus, and a report named StudID_Name_HW2_report.pdf (ex: 9862534_陳聿廣_HW2_report.pdf).

1. HW2_XOR contains following files:

- A pre-simulation file named pre_XOR.sp
  - **If using .cir in .sp, you need to attach a related .cir file (without the naming rule, you can define the file name yourself)**
- A post-simulation file named post_XOR.sp
  - **If using .cir in .sp, you need to attach a related .cir file (without the naming rule, you can define the file name yourself)**
- The DRC summary file named hw2_XOR.drc.summary
- The LVS report file named hw2_XOR.lvs.report
- Three output files of PEX

  (version 1)
  - **hw2_XOR.pex.cir**
  - **hw2_XOR.pex.cir.HW2_XOR.pxi**
  - **hw2_XOR.pex.cir.pex**

  (version 2)
  - **hw2_XOR.pex.netlist**
  - **hw2_XOR.pex.netlist.HW2_XOR.pxi**
  - **hw2_XOR.pex.netlist.pex**

2. HW2_bonus contains following files:
   - A pre-simulation file named pre_bonus.sp
     - **If using .cir in .sp, you need to attach a related .cir file (without the naming rule, you can define the file name yourself)**
   - A post-simulation file named post_bonus.sp
     - **If using .cir in .sp, you need to attach a related .cir file (without the naming rule, you can define the file name yourself)**
   - The DRC summary file named hw2_bonus.drc.summary
   - The LVS report file named hw2_bonus.lvs.report
   - Three output files of PEX

     (version 1)
     - **hw2_bonus.pex.cir**
     - **hw2_bonus.pex.cir.HW2_bonus.pxi**
     - **hw2_bonus.pex.cir.pex**

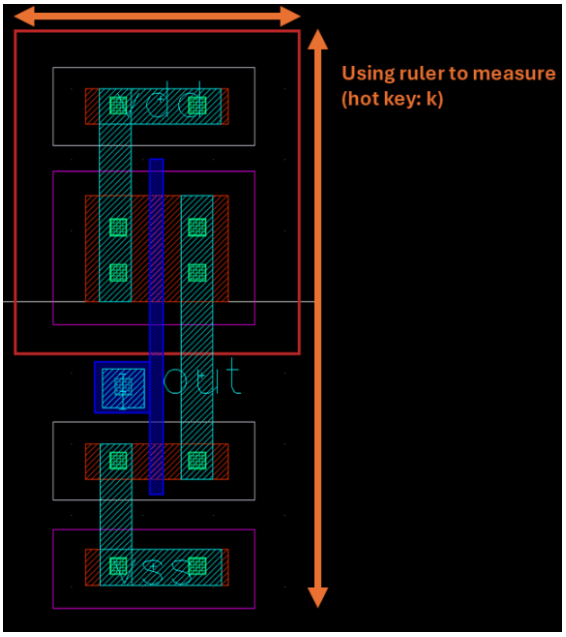
     (version 2)
     - **hw2_bonus.pex.netlist**
     - **hw2_bonus.pex.netlist.HW2_bonus.pxi**
     - **hw2_bonus.pex.netlist.pex**

Please upload it to ee-class with the original version. Note that the only acceptable report file format is .pdf, no .doc/.docx or other files are acceptable.

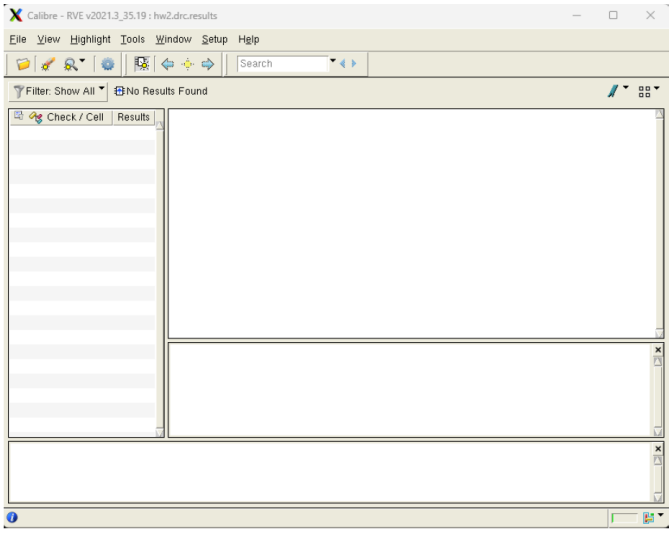
BE SURE to follow the naming rule mentioned above. Otherwise, your program will not be graded.

We don't restrict the report format and length. In your report, you must at least describe:

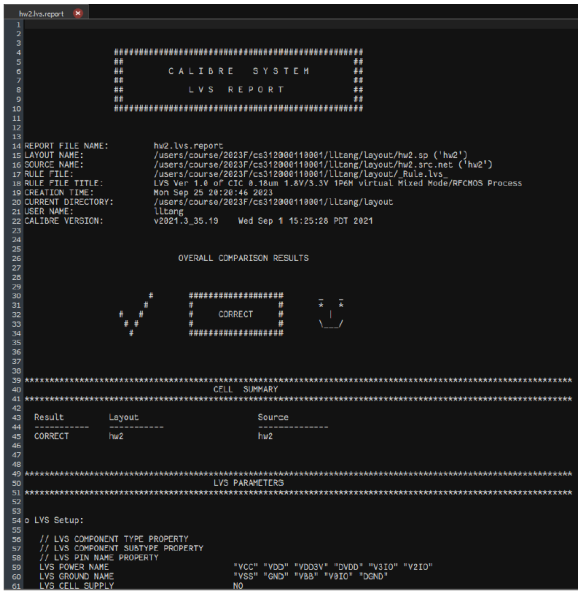
1. The circuit diagram of your design and explaining your design (You can use screenshots to explain)
2. Pre-sim waveform
3. Screenshot of your layout **(need to show the total area measurement with ruler in Virtuoso)**
   For example:



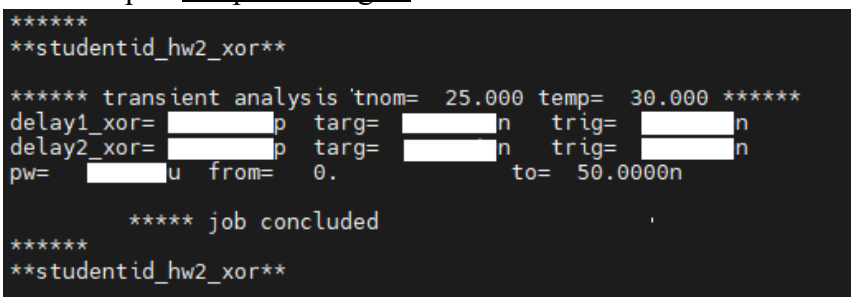
4. Screenshot of DRC summary report
   For example:



5. Screenshot of LVS report includes the message of passing LVS
   For example:



6. Post-sim waveform
7. Screenshot of the post-simulation result
   For example: 3-input XOR gate



8. Write down your delay and the difference in delay between rising and falling delay in the 3-input XOR gate.

$$\text{Delay1}_{\text{XOR}} = \_\_\_\_\_ \text{ ps}$$

$$\text{Delay2}_{\text{XOR}} = \_\_\_\_\_ \text{ ps}$$

$$|\text{Delay1}_{\text{XOR}} - \text{Delay2}_{\text{XOR}}| = \_\_\_\_\_ \text{ ps}$$

9. The hardness of this assignment and how you overcome it.
10. Any suggestions about this programming assignment

You can also put anything related to the PA in your report.

Grading

The grading is as follows:

(1) Correctness: 40%
- Pre-sim: 10%
- DRC: 10%
- LVS: 10%
- Post-sim: 10%

(2) Performance: power, area 10%

(3) Readability of hspice code: 10%

(4) The report: 10%

(5) Demo session: 30%

(6) Bonus:10%

Please submit your assignment on time. Otherwise, the penalty rule will apply:
- Within 72hrs delay: 20% off
- More than 3 days: 0 point

Be sure to attend a demo session (the time will be announced later). If you have questions, please E-mail to both me (andyygchen@ee.ncu.edu.tw) and TA 張孫婕 (ting200011@gmail.com)