Data Sheet

MS1793, BLE chip

32-bit Micro controller based on ARM Cortex M0

Revision History:

Rev. No.	History	Issue Date	Remark
1.0	Initial Release	Oct 31, 2018	Release

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1. Introduction

MS1793 is a single mode BLE chip, incorporate the high-performance ARM Cortex-M0 32-bit core operating at 48 MHz frequency, high-speed embedded memories, and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The device operates from a 2.0V ~ 3.6V power supply. They are available in both the -40℃ ~ +85℃ temperature range and the -40℃ ~ +105℃ extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications. This product is available in QFN32 package, and offers low cost solutions for:

- Beacon
- LED lighting
- Healthcare and fitness equipment
- Alarm system, wireless sensors

1.1 Product Features

- Core and system

- ARM®Cortex-M0 CPU
- Maximum operating frequency up to 48MHz

- Memories

- 128K Bytes of Flash memory
- 8K Bytes of SRAM
- Boot loader support chip Flash and ISP（In-System Programming）

- BLE transceiver

- Bluetooth smart 4.1
- GFSK encoding and decoding
- Single end antenna
- Programmable RF output：-28 ~ +3 dBm
- Receive sensitivity：-85 dBm

- Clock, reset and power management

– 2.0V ~ 3.6V application supply
– Power-on/Power-down reset (POR/PDR), Programmable voltage detector (PVD)
– Embedded factory-tuned 48MHz high speed oscillator
– Embedded 40KHz low speed oscillator
– PLL supports CPU running at 48MHz

- Low-power

– Sleep, Stop and Standby modes

- 1 12-bit ADC, 1μS transform time (up to 10 channels)

– Conversion range: 0 ~ VDDA
– Support sampling time and resolution configuration
– On-chip temperature sensor

- 2 Comparators

- 5 DMA controller

– Supported peripherals: Timer、UART、I2C、SPI、ADC and USB

- Up to 39 fast I/Os:

– All mappable on 16 external interrupt vectors

- Debug mode

– Serial wire debug (SWD)

- Up to 9 timers

– 1 16-bit 4-channel advanced-control timer for 4 channels PWM output, with deadtime generation and emergency stop
– 1 16-bit timer and 1 32-bit timer, with up to 4 IC/OC, usable for IR control decoding
– 2 16-bit timer, with 1 IC/OC, 1 OCN, deadtime generation and emergency stop and modulator gate for IR control
– 1 16-bit timer, with 1 IC/OC
– 2 watchdog timers (independent and window type)
– SysTick timer: 24-bit downcounter

- Up to 4 Communication interfaces

– 2 UARTs
– 1 I2C
– **1** SPIs

2. Specification

2.1 ARM Cortex-M0 and SRAM

The ARM Cortex-M0 is a generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.
The ARM Cortex-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The devices embed ARM core and are compatible with all ARM tools and software.

2.2 Memory

128K Bytes of embedded Flash memory.

2.3 SRAM

8K Bytes of embedded SRAM.

2.4 Nested vectored interrupt controller (NVIC)

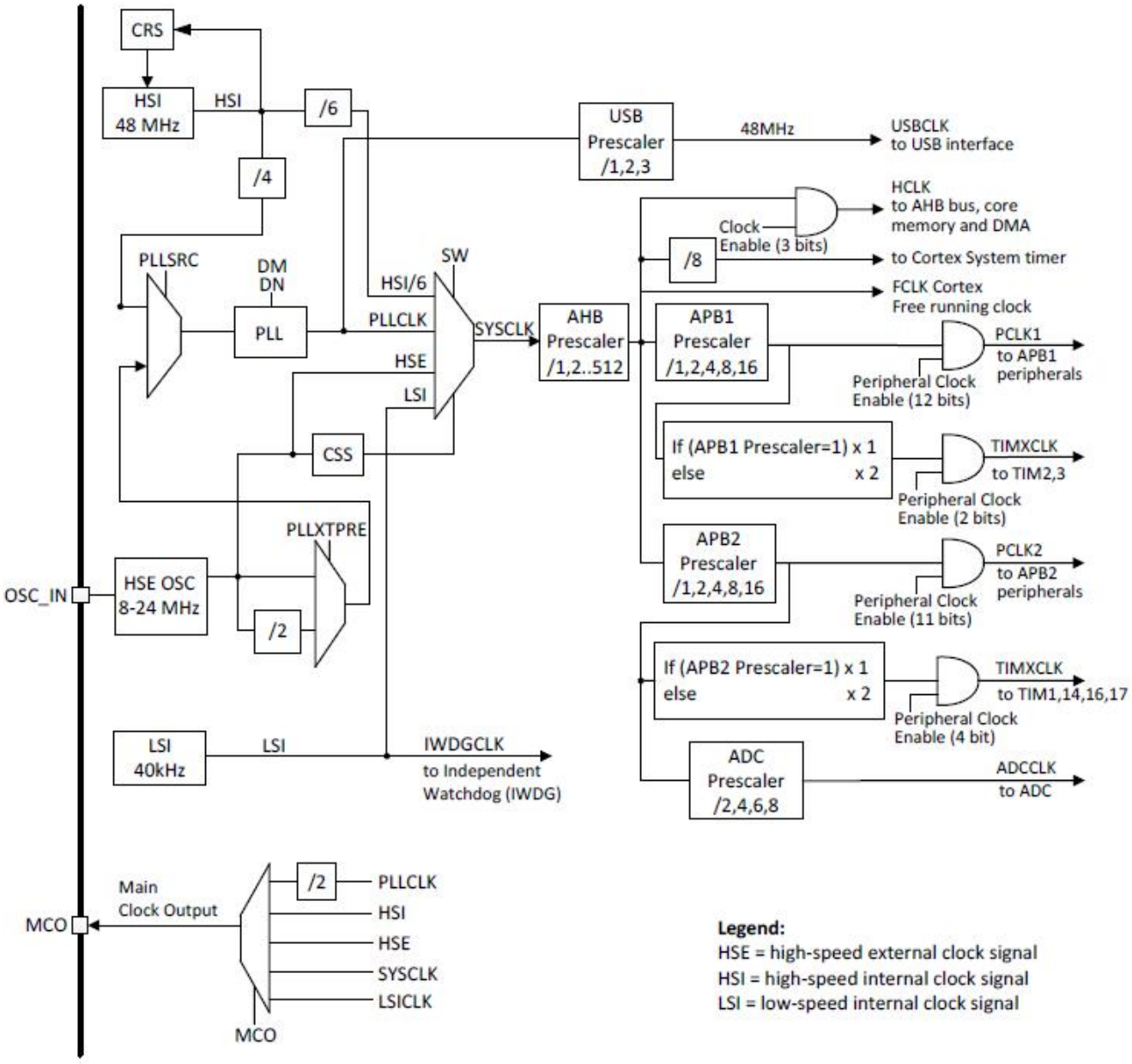
The device embeds a nested vectored interrupt controller able to handle up to 68 maskable interrupt channels (not including the 16 interrupt lines of Cortex-M0 and 16 priority levels.
• Closely coupled NVIC gives low latency interrupt processing
• Interrupt entry vector table address passed directly to the core
• Closely coupled NVIC core interface
• Allows early processing of interrupts
• Processing of late arriving higher priority interrupts
• Support for tail-chaining
• Processor state automatically saved
• Interrupt entry restored on interrupt exit with no instruction overhead
This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.5 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of many edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. All GPIOs can be connected to the 16 external interrupt lines.

2.6 Clocks and startup

System clock selection is performed on startup, however the internal 48 MHz oscillator is selected as default CPU clock on reset. An external 2 ↑ 24 MHz clock can be selected, in which case it is monitored for failure.
Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz. Refer to figure below for the clock drive block diagram.



2.7 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options：

- Boot from User Flash memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using UART1.

2.8 Power supply schemes

• VDD = 2.0V ~ 3.6V: external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
• V_{SSA}, V_{DDA}= 2.0V ~ 3.6V: external analog power supply for reset blocks, oscillators and PLL. V_{DDA} and V_{SSA} must be connected to VDD and VSS.

2.9 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 1.8V. The device remains in reset mode when the monitored supply voltage is below a specified threshold VPOR/PDR, without the need for an external reset circuit.
The device features an embedded programmable voltage detector (PVD) that monitors the VDD/VDDA power supply and compares it to the VPVD threshold. An interrupt can be generated when VDD drops below the VPVD threshold and/or when VDD is higher than the VPVD threshold.The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.10 Voltage regulator

The voltage regulator converts the external voltage to the internal digital logic and it is always enabled after reset.

2.11 Low-power modes

The device support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

Stop mode

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. the HSI and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

Standby mode

Standby mode achieves the lowest power consumption of the system. This mode turns off the voltage regulator in CPU deep sleep mode. The entire 1.5V power supply area is powered down. PLL、HSI and HSE oscillators are also powered down. SRAM and register contents are missing. Only the backup registers and standby circuits remain powered.

2.12 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.
DMA can be used with the main peripherals: UART、I2C、SPI、USB、CAN、ADC general purpose and advanced-control timers TIMx.

2.13 Backup register (BKP)

The backup registers are ten 16-bit registers used to store 20 bytes of user application data when VDD power is not present. They are still powered by VBAT. They are also not reset when the system is woken up in standby mode, or when the system is reset or power is reset.

2.14 Timers and watchdogs

Medium capacity device include 1 advanced control、5 general-purpose timers 、2 watchdog timers and 1 SysTick timer.
The following table compares the features of the different timers:

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA	Capture/compare channels	Complementary output
Advance control	TIM1	16-bit	Up/down	Integer from 1 to 65535	Yes	4	Yes
General purpose	TIM2	32-bit	Up/down	Integer from 1 to 2^{32}-1	Yes	4	No
	TIM3	16-bit	Up/down	Integer from 1 to 65535	Yes	4	No
Basic	TIM14	16-bit	Up	Integer from 1 to 65535	Yes	1	No
	TIM16 TIM17	16-bit	Up	Integer from 1 to 65535	Yes	1	Yes

Advanced-control timer (TIM1)
The advanced-control timer can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for：
• Input capture
• Output compare
• PWM generation (edge or center-aligned modes)
• One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the

16-bit PWM generator, it has full modulation capability (0 ~ 100%).

In debug mode, the counter can be frozen and the PWM output is disabled to cut off the switches controlled by these outputs.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are 5 synchronizable general-purpose timers (TIM2、TIM3).

General-purpose timers 32-bit

The timer is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.

General-purpose timers 16-bit

The timer is based on a 16-bit auto-reload up/down counter and a 16-bit prescaler. The feature is 4 independent channels each for input capture/output compare, PWM or one-pulse mode output.
The timer can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.
These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output. Their counter can be frozen in debug mode.

TIM16/TIM17

Every timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. They each have a single channel for input capture/output compare, PWM or one-pulse mode output.
TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation. Their counters can be frozen in debug mode.

Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 KHz internal oscillator and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.15 Universal asynchronous receiver/transmitter (UART)

UART provides hardware management of the CTS, RTS.
Support LIN master-slave function.
All UART interface can be served by the DMA controller.

2.16 I2C interface

The I2C interface can operate in multimaster or slave modes. It can support Standard mode,and Fast Mode.
It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask).

2.17 Serial peripheral interface (SPI)

The SPI interface, in slave or master mode, can be configured to 1~32 bits per frame.
All SPI interface can be served by the DMA controller.

2.18 Universal serial bus (USB)

NA

2.19 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

2.20 Analog-to-digital converter (ADC)

The one 12-bit analog-to-digital converters is embedded into microcontrollers and the ADC shares up to 10 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.
The ADC can be served by the DMA controller.
The analog watchdog function allows very precise monitoring of all the way, multiple or all selected channels, and an interruption occurs when the monitored signal exceeds the preset threshold. The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger to allow the application to synchronize A/D conversion and timers.

2.21 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature.
The temperature sensor is internally connected to the input channel which is used to convert the sensor output voltage into a digital value.

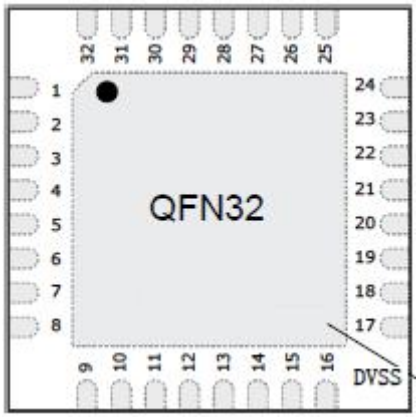
2.22 Serial single line SWD debug port (SW-DP)

Built-in ARM two-wire serial debug port (SW-DP) .
An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

2.23 Bluetooth Low Energy (BLE)

This product integrate a Bluetooth 4.1 engine and works on ISM license-free frequency band. Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range(2.0~3.6V).

3. Pin Definition



Pin No.	Symbol	I/O	Function Description	Alternate Functions
1	VBAT	Power	Power Supply	
2	SPI_MISO_RF	DO	SPI Slave Data Output, connect to pin27	
3	VDD_LDO	Power	Connect to 10uF capacitor	
4	IRQ_VPP	DO	Maskable Interrupt Output	
5	NRST	DI		
6	VBAT	Power	Power Supply	
7	PA0	DIO	PA0-WKUP	UART2_CTS/ADC_IN0
8	XO16M	A	Crystal Pin	
9	XI16M	A	Crystal Pin	
10	PA3	DIO		ADC_IN3/TIM2_CH4
11	PA4	DIO		ADC_IN4/TIM14_CH1
12	PA7	DIO		ADC_IN7/TIM17_CH1
13	VSS	Power	Ground (0V)	
14	Antp	A	Antenna interface	
15	VBAT	Power	Power Supply	
16	PA8	DIO		TIM1_CH1/MCO
17	PA9	DIO		UART1_TX/TIM1_CH2/UART1_RX/I2C_SCL/MCO
18	PA10	DIO		UART1_RX/TIM1_CH3/UART1_TX/I2C_SDA
19	VBAT	Power	Power Supply	

20	PA11	DIO		UART1_CTS/TIM1_CH4/I2C_SCL
21	PA12	DIO		UART1_RTS/TIM1_ERT/I2C_SDA
22	PA13	DIO		SWDIO
23	PD2	DIO		
24	PD3	DIO		
25	PA14	DIO		SWCLK/UART2_TX
26	PB3	DO	SPI clock output, connect to pin31	TIM2_CH2/SPI1_SCK
27	PB4/MISO	DI	SPI Master Data input, connect to pin2	TIM3_CH1/SPI1_MISO
28	PB5/MOSI	DO	SPI Master Data output, connect to pin32	TIM3_CH2/SPI1_MOSI
29	BOOT0	DI		
30	SPI_CSN	DIO	SPI chip select	PB8
31	SPI_SCK_RF	DI	SPI clock, connect to pin26	
32	SPI_MOSI_RF	DI	SPI Slave Data input, connect to pin28	

Table3.1 Pin Description

Alternate Functions

Pin	AF0	AF1	AF2	AF3	AF4	AF5
PA0		UART2_CTS	TIM2_CH1_ETR			
PA3		UART2_RX	TIM2_CH4			
PA4					TIM14_CH1	
PA7		TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1
PA8	MCO		TIM1_CH1		CRS_SYNC	
PA9		UART1_TX	TIM1_CH2	UART1_RX	I2C_SCL	MCO
PA10	TIM17_BKIN	UART1_RX	TIM1_CH3	UART1_TX	I2C_SDA	
PA11		UART1_CTS	TIM1_CH4			I2C_SCL
PA12		UART1_RTS	TIM1_ETR			I2C_SDA
PB3	SPI1_SCK		TIM2_CH2			

PB4	SPI1_MISO	TIM3_CH1				
PB5	SPI1_MOSI	TIM3_CH2	TIM16_BKIN			
PB8	SPI1_CSN*					
PD2						
PD3						

4. Memory Mapping

Bus	Boundary Address	Size	Peripheral
AHB	0x4800 1000 - 0x5FFF FFF	~384 MB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 6400 - 0x47FF FFFF	~128 MB	Reserved
	0x4002 2400 - 0x4002 63FF	16 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
APB2	0x4001 4C00 - 0x4001 7FFF	13 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM14
	0x4001 3C00 - 0x4001 3FFF	1 KB	CPT
	0x4001 3800 - 0x4001 3BFF	1 KB	UART1
	0x4001 3400 - 0x4001 37FF	1 KB	DBGMCU
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1

	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
APB1	0x4000 7400 - 0x4000 FFFF	35 KB	Reserved
	0x4000 7000 - 0x4001 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6000 - 0x4000 6BFF	3 KB	Reserved
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	UART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	BKP
	0x4000 0800 - 0x4000 27FF	8 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2
SRAM	0x2000 2000 - 0x2FFF FFFF	~512 MB	Reserved
	0x2000 0000 - 0x2000 1FFF	8 KB	SRAM
Flash	0x1FFF F810 - 0x1FFF FFFF	~2 KB	Reserved
	0x1FFF F800 - 0x1FFF F80F	16 B	Option Byte
	0x1FFF F400 - 0x1FFF F7FF	1 KB	System memory
	0x1FFE 1C00 - 0x1FF F3FF	~256 MB	Reserved
	0x1FFE 1000 - 0x1FFE 1BFF	3 KB	Security space
	0x1FFE 0200 - 0x1FFE 0FFF	3.5 KB	Reserved

	0x1FFE 0000 - 0x1FFE 01FF	0.5 KB	Protect Bytes
	0x0802 0000 - 0x1FFD FFFF	~256 MB	Reserved
	0x0800 0000 - 0x0801 FFFF	128 KB	Main Flash memory
	0x0002 0000 - 0x07FF FFFF	~128 MB	Reserved
	0x0000 0000 - 0x0001 FFFF	128 KB	Main flash memory, system memory, or SRAM, depends on BOOT configuration

5. Reference Schematic

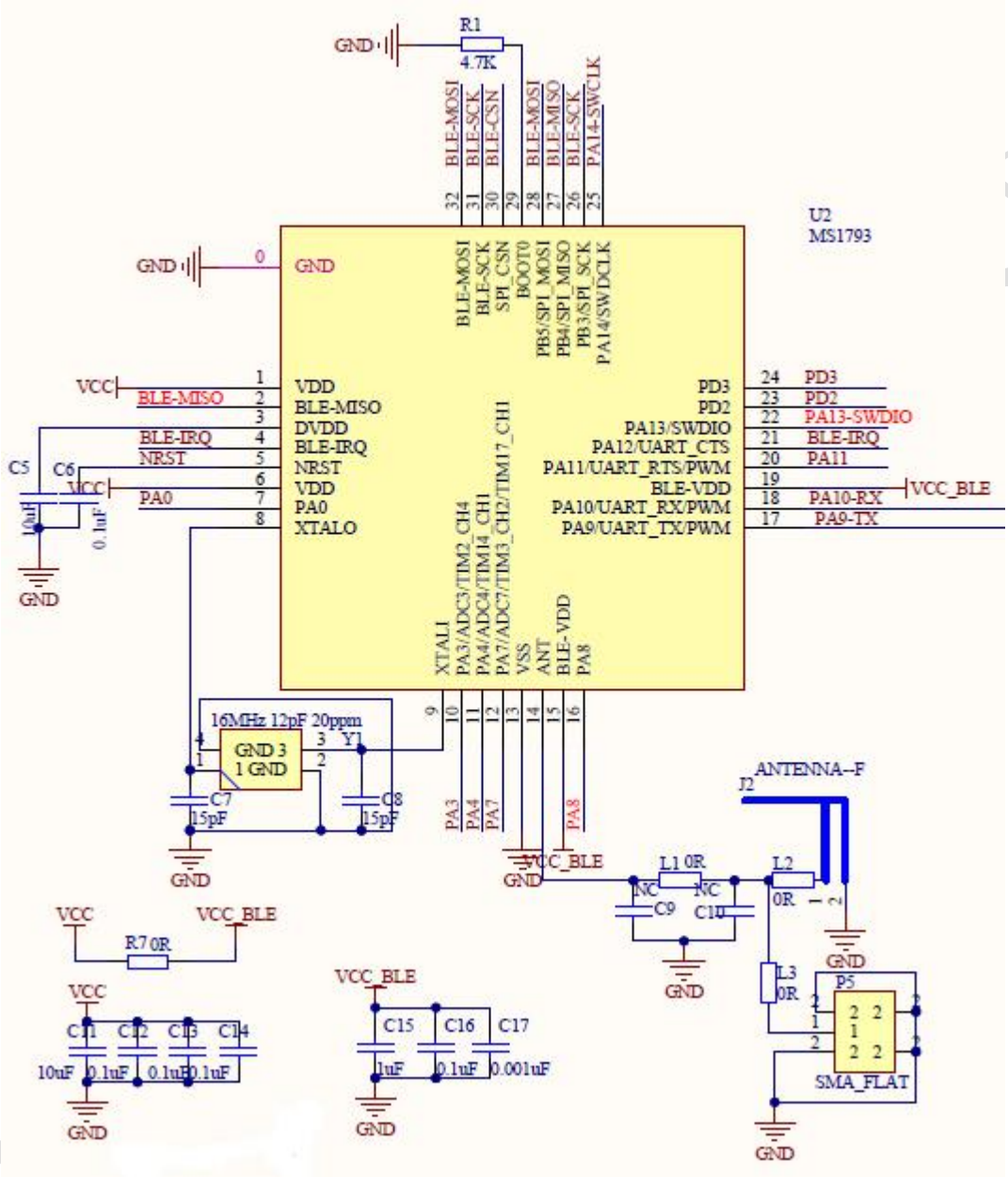


Figure 5.1 Example Application Schematic

6. Electrical Characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltage are referenced to VSS, and all the RF performance are under

antenna connector of 50Ω.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed with an ambient temperature at T_A=25℃, VDD=3.3V.

6.1.2 Typical values

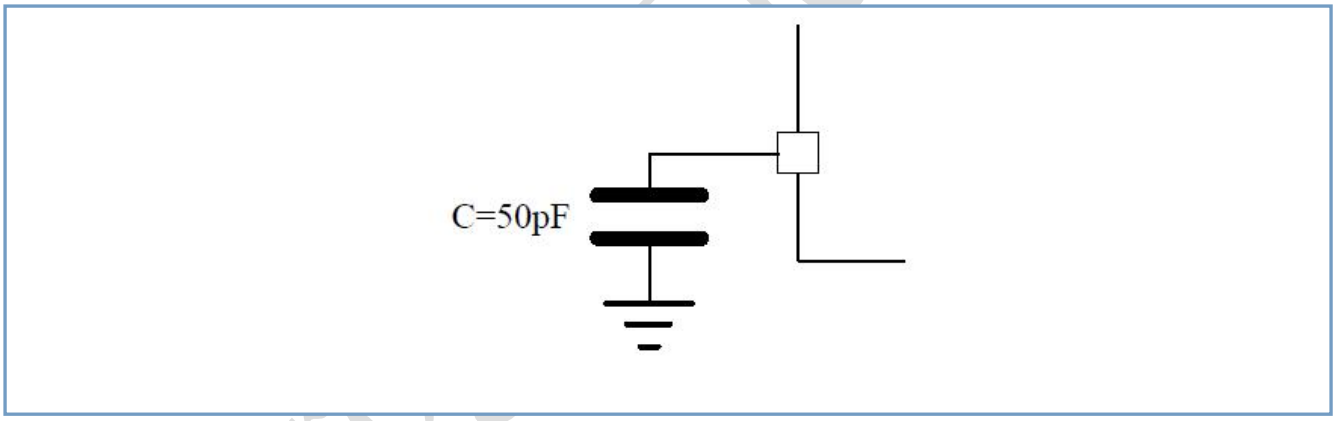
Unless otherwise specified, typical data are based on T_A=25℃ and VDD=3.3V. They are given only as design guideline and are not tested.

6.1.3 Typical curves

Unless otherwise specified, all typical curves re given only as design guidelines and are not tested.

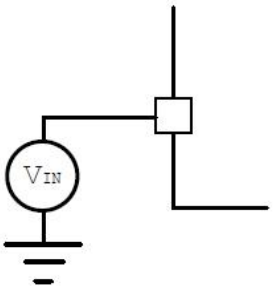
6.1.4 Loading capacitor

The load conditions used for pin parameter measurement are shown in the figure below.

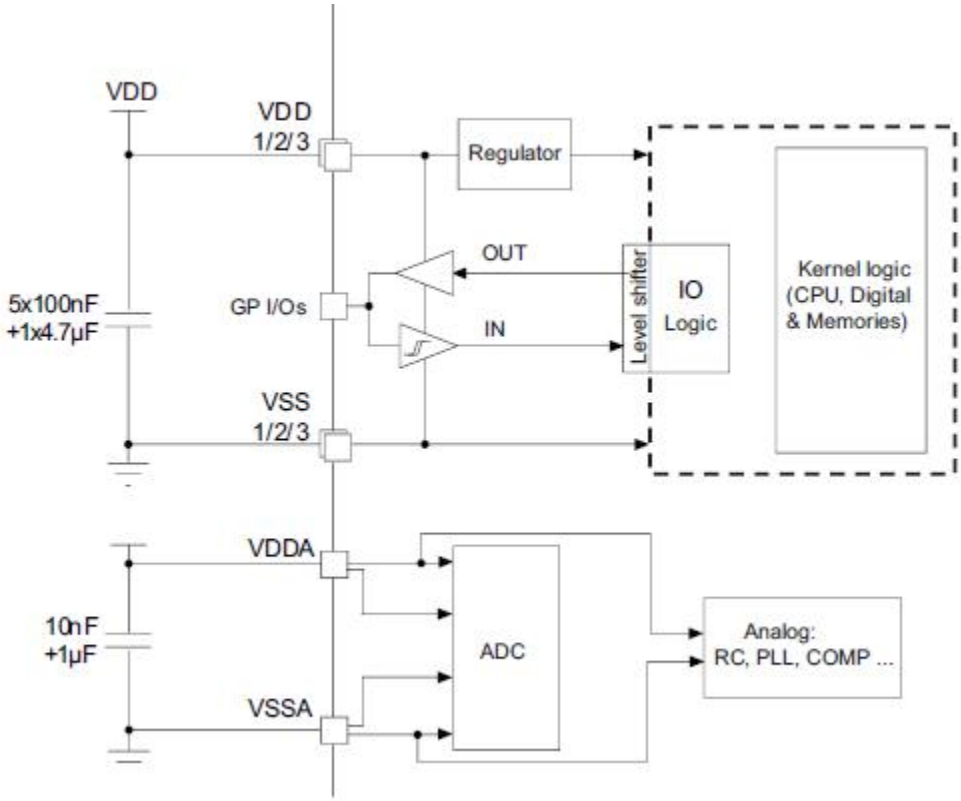


6.1.5 Pin input voltage

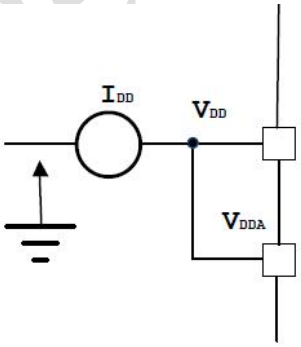
The input voltage measurement on a pin of the device is shown in the figure below.



6.1.6 Power supply scheme



6.1.7 Current consumption measurement



6.2 RF general characteristics

	Description	Condition	Min.	Typ	Max.	Unit

FREQ	Frequency range	VDD=3.0V, TA=25°C	2400		2480	MHz
FC	Freq gap	VDD=3.0V, TA=25°C		2		MHz
RFch	RF channel freq	VDD=3.0V, TA=25°C	2400		2480	MHz

6.3 RF Transmitter characteristics

	Description		Min	Typ	Max	Unit
MOD	modulation	GFSK				
BT				0.5		
M_{index}	Modulation index		0.45	0.5	0.55	
DR	Air Data Rate			1 Mbps		
P_{MAX}	Max RF output				+3	dBm
P_{BW1M}	6dB bandwidth（1Mbps）		500			KHz
P_{SPUR}	spur				-41	dBm
CF_{dev}	Central freq deviation				±150	KHz
$Freq_{drift}$	Freq drift				±50	KHz
$IFreq_{drift}$	Initial freq drift				±20	KHz

6.4 RF Receiver characteristics

	Description	Condition	Min	Typ	Max	Unit
RX_{SENS}	sensitivity	BER<0.1%		-85		dBm

6.5 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Tables(Table 6.5.1、Table 6.5.2、Table 6.5.3) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Definition	Min	Max	Unit
VDD-VSS	External main supply voltage（including VDDA and VDD）	-0.3	3.6	V
Vin	Input voltage on pins	VSS-0.3	3.6	V
|ΔVDDx|	Variations between different Vdd pins		50	mV

$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins		50	mV
$V_{ESD(HBM)}$	ESD（HBM）		2000	V

Table 6.5.1 Voltage characteristics

Symbol	Definition	Max	Unit
I_{VDD}	Total current into sum of all VDD/VDDA power lines	150	mA
I_{VSS}	Total current out of sum of all VSS ground lines	150	mA
I_{IO}	Output current sunk by any I/O and control pin	20	mA
	Output current source by any I/O and control pin	-18	mA
$I_{INJ(PIN)}$	Injected current on OSC_IN pin of HSE and OSC_IN pin of LSE	±5	mA
$\Sigma I_{INJ(PIN)}$	Total injected current(sum of all I/O and control pins)	±25	mA

Table 6.5.2 Current characteristics

Symbol	Definition	Max	Unit
T_{STG}	Storage temperature range	-45 ~ +150	℃
T_J	Maximum junction temperature	125	℃

Table 6.5.3 Thermal characteristics

6.6 Operating conditions

6.6.1 General operating conditions

symbol	Parameter	Condition	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK}	Internal APB clock frequency		0	48	MHz
VDD	Standard operating voltage		2.0	3.6	V
VDDA	Analog operating voltage	Must be the same as VDD	2.0	3.6	V
P_D	Power dissipation temperature:		-	594	mW

	T_A=85℃				
T_A	Ambient temperature: T_A=85℃	Maximum power dissipation	-40	85	℃
		Low power dissipation	-40	105	
	Ambient temperature: T_A=105℃	Maximum power dissipation	-40	95	℃
		Low power dissipation	-40	125	

6.6.2 Operating conditions at power-up/power-down

The parameters give in the table below are based on tests under normal operating conditions.

Symbol	Parameter	condition	Min	Max	Unit
t_{VDD}	VDD rise time rate	T_A=27 ℃	0	-	us/V
	VDD fall time rate		20	-	us/V

6.6.3 Embedded reset and power control block characteristics

Symbol	Parameter	condition	Min	Typ	Max	Unit
V_{PVD}	Level selection of programmable voltage detectors	PLS[3:0]=0000(rising edge)	1.813	1.819	1.831	V
		PLS[3:0]=0000(falling edge)		1.705		V
		PLS[3:0]=0001(rising edge)	2.112	2.116	2.124	V
		PLS[3:0]=0001(falling edge)		2.0		V
		PLS[3:0]=0010(rising edge)	2.411	2.414	2.421	V
		PLS[3:0]=0010(falling edge)		2.297		V
		PLS[3:0]=0011(rising edge)	2.711	2.714	2.719	V
		PLS[3:0]=0011(falling edge)		2.597		V
		PLS[3:0]=0100(rising edge)	3.011	3.013	3.018	V
		PLS[3:0]=0100(falling edge)		2.895		V
		PLS[3:0]=0101(rising edge)	3.311	3.313	3.317	V
		PLS[3:0]=0101(falling edge)		3.194		V
		PLS[3:0]=0110(rising edge)	3.611	3.613	3.616	V

		PLS[3:0]=0110(falling edge)		3.494		V
$V_{PVDhyst}$	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/down reset threshold	Falling edge	1.63	1.66	1.68	V
		Rising edge		1.75		V
$V_{PDRhyst}$	PDR hysteresis			100		mV
$T_{RSTTEMPO}$	Reset duration			20		mS

6.6.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
All Run-mode current consumption measurements given in this section are performed with a reduced code.

Maximum current consumption
The MCU is placed under the following conditions:
• All I/O pins are in analog input mode, and are connected to a static level —- VDD or VSS (no load)
• All peripherals are disabled except when explicitly mentioned
• The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period , 24 ~ 48 MHz is 1 waiting period).

• The instruction prefetching function is on. When the peripherals are enabled： $f_{PCLK1} = f_{HCLK}$.

Symbol	Parameter	condition	Max	Unit
I_{DD}	Supply current in Stop mode	Enter Stop mode after reset	200	μA
	Supply current in Standby mode	Enter Standby mode after reset	2	μA

Table 6.4.4.1 **Typical and maximum current consumption in stop and standby modes**

Typical current consumption
The MCU is placed under the following conditions:
• All I/O pins are in analog input configuration, and are connected to a static level - VDD or VSS (no load).
• All the peripherals are closed, unless otherwise specified.
• The Flash memory access time is adjusted to the f_{HCLK} (0 ~ 24 MHz is 0 waiting period, 24 ~ 48 MHz is 1 waiting period).
• The instruction prefetching function is on (Note： this parameter must be set before setting the clock and bus divider). When the peripherals are enabled： $f_{PCLK1} = f_{HCLK}$.

Symbol	Parameter	condition	f_{HCLK}	Typ		Unit
				All peripheral enabled	All peripheral disabled	
I_{DD}	Supply current in operating mode	Run at HSI, use AHB prescaler to reduce frequency	48MHz	7.63	4.28	mA
			8MHz	1.40	0.85	mA

Table 6.4.4.2 Typical current consumption in Run mode, code executing from Flash

1. The typical value is tested at T_A = 25℃ and V_{DD} = 3.3V.

Symbol	Parameter	condition	f_{HCLK}	Typ		Unit
				All peripheral enabled	All peripheral disabled	
I_{DD}	Supply current in sleep mode	Run at HSI, use AHB prescaler to reduce frequency	48MHz	5.89	2.49	mA
			8MHz	1.03	0.48	mA

Table 6.4.4.3 Typical current consumption in Sleep mode, code executing from Flash

1. The typical value is tested at T_A = 25℃ and V_{DD} = 3.3V.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
I_{BAT}	Supply current	RESET			5		uA
		STANDBY			2		uA
		RX			28		mA
		TX	+3 dBm		36		mA
			0 dBm		30		mA
			-3 dBm		28		mA

Table 6.4.4.4 Typical current consumption for RF(include MCU)

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table below. The MCU is placed under the following conditions:

• all I/O pins are in analog input mode, and are connected to a static level —- VDD or VSS (no load)
• all peripherals are disabled except when explicitly mentioned
• the given value is calculated by measuring the current consumption
– with all peripherals clocked OFF
– with only one peripheral clocked on

Peripheral		Typ	Unit	Peripheral		Typ	Unit
APB1	TIM2	0.49	mA	APB2	SPI1	0.49	mA
	TIM3	0.50	mA		UART1	0.52	mA

	I2C	0.49	mA				mA
APB2	TIM14	0.52	mA	AHB	GPIOA	0.53	mA
	TIM16	0.52	mA		GPIOB	0.53	mA
	TIM17	0.52	mA		GPIOC	0.53	mA
	TIM1	0.49	mA		GPIOD	0.53	mA

Table 6.4.4.5 **On-chip peripheral current consumption**

1. f_{HCLK} = 48MHz, f_{APB1} = f_{HCLK}/2, f_{APB2} = f_{HCLK}, the prescale coefficient for each device is the default value.

6.6.5 External clock source characteristics (NA)

6.6.6 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with general operating conditions.

High-speed internal(HSI) oscillator

Symbol	Parameter	condition	Min	Typ	Max	Unit
f_{HSI}	Frequency		39.94	48.26	64.14	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	T_A=-40~105°C	-10		9	%
		T_A=-10~85°C				
		T_A=0~70°C				
		T_A=25°C	-1		1	
$t_{SU(HSI)}$	HSI oscillator startup time				2	μs
$I_{DD(HSI)}$	HSI oscillator power consumption			80.53	122	μA

Low-speed internal(LSI) oscillator

Symbol	Parameter	condition	Min	Typ	Max	Unit
f_{LSI}	Frequency		31.3	50.58	74.83	KHz
$t_{SU(LSI)}$	LSI oscillator startup time				1	μs
$I_{DD(LSI)}$	LSI oscillator power consumption			1.082	1.652	μA

Wake-up times from low power mode

The wake-up times listed in the table below are measured during the wake-up phase of the internal clock HSI. The clock source used when waking up depends on the current operating mode:

• Stop or Standby mode: The clock source is the oscillator

• Sleep mode: The clock source used when entering sleep mode

All times are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Symbol	Parameter	condition	Max	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	HSI clock wakeup	4	μs
t_{WUSTOP}	Wakeup from Stop mode	HSI clock wakeup = 2μs	8	
$t_{WUSTDBY}$	Wakeup from Standby mode	HSI clock wakeup =2μs The regulator wakes up from off mode = 38μs	20000	

1. The wake-up time is measured from the start of the wake-up event to the user program to read the first instruction.

6.6.7 PLL characteristics

The parameters listed in the table below are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	8		24	MHz
	PLL input clock duty cycle	40		60	%
f_{PLL_OUT}	PLL multiplier output clock	40		100	MHz
t_{LOCK}	PLL lock time			100	μs

6.6.8 Memory characteristics

Flash memory

The characteristics are given at TA = - 40 ~ 105°C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{prog}	8-bit programming time	T_A=-40~105°C	4			μs
t_{ERASE}	page(512K bytes) erase time	T_A=-40~105°C	4		5	ms
t_{ME}	Mass erase time	T_A=-40~105°C	20		40	ms
I_{DD}	Supply current	Read mode, f_{HCLK}=48MHz		5	6	mA
		Write mode, f_{HCLK}=48MHz			7	mA
		Erase mode, f_{HCLK}=48MHz			2	mA
I_{SB}	Standby current			1@25°C	50@125°C	μA
I_{DEP}	Deep standby current			0.5	15@125°C	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{END}	Endurance(Erase number of times)	T_A=-40~85°C) T_A=-40~105°C	10			K cycle
t_{RET}	Data retention	1K cycle at T_A=85°C	30			Year
		1K cycle at T_A=105°C	10			
		10K cycle at T_A=55°C	20			

6.6.9 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports) ,the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

• Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.

• FTB： A Burst of Fast Transient voltage (positive and negative) is applied to VDD and VSS through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in the following table. They are based on the EMS levels and classes defined in application note.

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance	VDD = 3.3V, T_A = +25°C, f_{HCLK}=48MHz. Conforming to IEC 1000-4-4	

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre-qualification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

• Corrupted program counter

• Unexpected reset

• Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors.

6.6.10 Absolute Maximum (Electrical Sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance：

• A supply overvoltage is applied to each power supply pin

• A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD78A IC latch-up standard.

Symbol	Parameter	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A=+25°C, conforming to JESD22-A114	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charging device model)	T_A=+25°C, conforming to JESD22-C101	500	
I_{LU}	Latch-up current	T_A=+25°C, conforming to JESD78A	200	mA

6.6.11 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table below are derived from tests.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	3.3V CMOS port	-0.5		1.1	V
V_{IH}	High level input voltage		2.08			
V_{hys}	Schmitt trigger hysteresis	3.3V	500	700	800	mV
I_{lkg}	Input leakage current	3.3V			1	μA

R_{PU}	Weak pull-up equivalent resistor	3.3V $V_{IN}=V_{SS}$	30	50	100	kΩ
R_{PD}	Weak pull-down equivalent resistor	3.3V $V_{IN}=V_{DD}$	30	50	100	
C_{IO}	I/O pin capacitance	3.3V		5		pF

Table 6.6.11.1 I/O static characteristics

All I/Os are CMOS (no software configuration required). Their characteristics cover more than the strict CMOS-technology.

• For VIH：
  – If VDD is between [2.50V↑ 3.08V]; use CMOS features.
  – If VDD is between [3.08V↑ 3.60V]; include CMOS.

• For VIL：
  – Use CMOS features.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±20mA.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating:

•The sum of the currents obtained from VDD for all I/O ports, plus the maximum operating current that the MCU obtains on VDD, cannot exceed the absolute maximum rating I_{VDD}.

•The sum of the currents drawn by all I/O ports and flowing out of VSS, plus the maximum operating current of the MCU flowing out on VSS, cannot exceed the absolute maximum rating I_{VSS}.

Output voltage levels

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature.

All I/O ports are CMOS compatible.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an IO pin, when 8 pins absorb current	CMOS port, I_{IO}=+8mA 2.7V<V_{DD}<3.6V		0.4	V
V_{OH}	Output high level voltage for an IO pin, when 8 pins output current		0.8V_{DD}		
V_{OL}	Output low level voltage for an IO pin, when 8 pins absorb current	I_{IO}=+20mA 2.7V<V_{DD}<3.6V		0.4	
V_{OH}	Output high level voltage for an IO pin, when 8 pins output current		0.8V_{DD}		
V_{OL}	Output low level voltage for an IO pin, when 8 pins absorb current	I_{IO}=+6mA 2V<V_{DD}<2.7V		TBD	
V_{OH}	Output high level voltage for an IO pin, when 8 pins output current		TBD		

Table 6.6.11.2 Output voltage characteristics

Input/output AC characteristics

The definitions and values of the input and output AC characteristics are given in figure below.

Unless otherwise stated, the parameters listed in Table are measured using the ambient temperature.

OSPEEDRy [1:0] value	symbol	Parameter	Conditions	Min	Max	Unit
10 (2MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=2~3.6V		2	MHz
	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=2~3.6V		125	ns
	$t_{r(IO)out}$	Output rise time			125	
01 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=50pF, V_{DD}=2~3.6V		10	MHz
	$t_{f(IO)out}$	Output fall time	C_L=50pF, V_{DD}=2~3.6V		25	ns
	$t_{r(IO)out}$	Output rise time			25	
11 (50MHz)	$f_{max(IO)out}$	Maximum frequency	C_L=30pF, V_{DD}=2.7~3.6V		50	MHz
			C_L=50pF, V_{DD}=2.7~3.6V		30	
			C_L=50pF, V_{DD}=2~2.7V		20	
	$t_{f(IO)out}$	Output fall time	C_L=30pF, V_{DD}=2.7~3.6V		5	ns
			C_L=50pF, V_{DD}=2.7~3.6V		8	
			C_L=50pF, V_{DD}=2~2.7V		12	
	$t_{r(IO)out}$	Output rise time	C_L=30pF, V_{DD}=2.7~3.6V		5	
			C_L=50pF, V_{DD}=2.7~3.6V		8	
			C_L=50pF, V_{DD}=2~2.7V		12	
	t_{EXTIpw}	Pulse width of external signals detected by EXTI controller		10		

Table 6.6.11.3 I/O AC characteristics

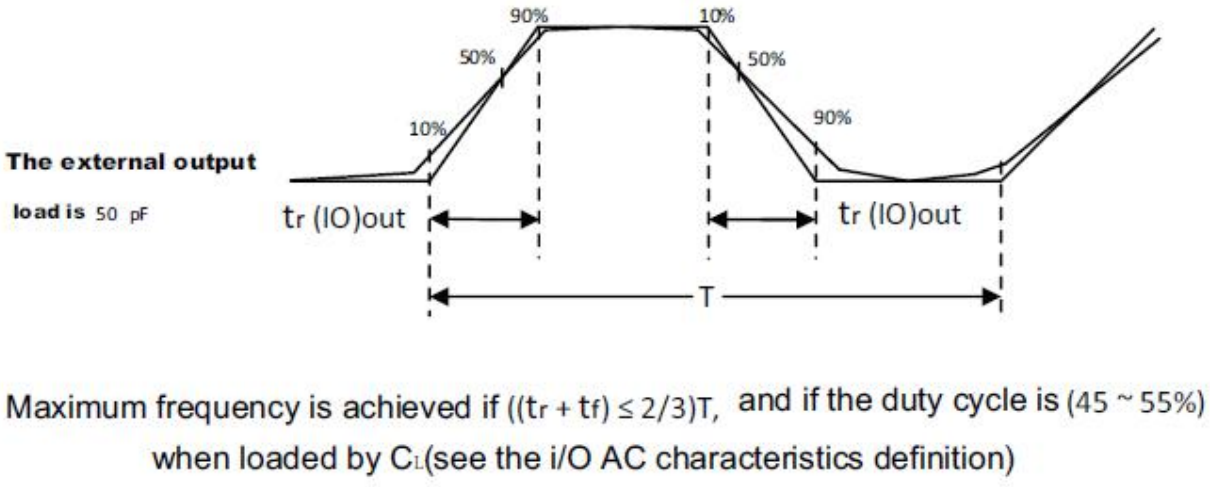


Figure 6.6.11.4 I/O AC characteristics

6.6.12 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pullup resistor, RPU.

Unless otherwise stated, the parameters listed in the table below are measured using the ambient temperature and VDD supply voltage in accordance with the condition of Table 6.1.2

symbol	Parameter	condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		-0.5		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage		2		V_{DD}	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			$0.2V_{DD}$		V
R_{PU}	Weak pull-up equivalent resistor	$V_{IN}=V_{SS}$		15		kΩ
$V_{F(NRST)}$	NRST input filtered pulse				100	ns
$V_{NF(NRST)}$	NRST input not filtered pulse		300			

Table 6.6.12.1 NRST pin characteristics

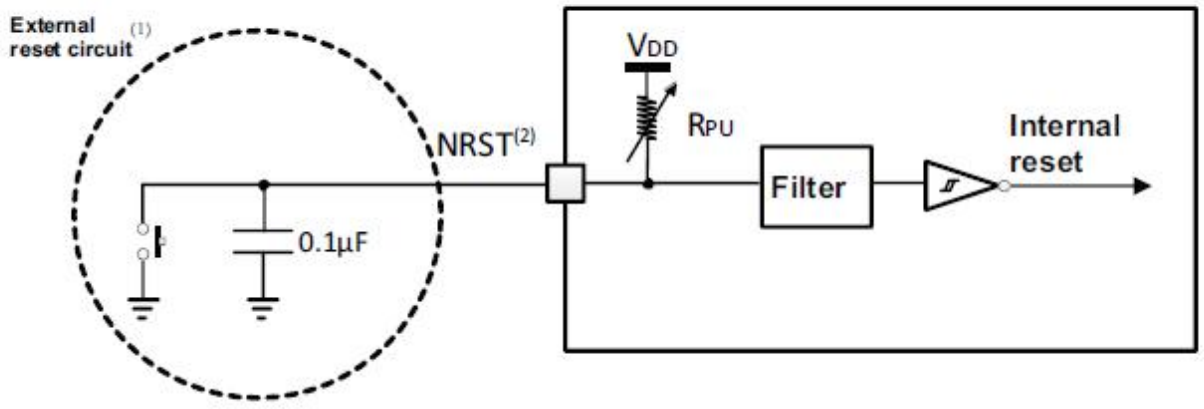


Figure 6.6.12.2 Recommended NRST pin protection

6.6.13 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz	10.4		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$=48MHz	0	24	
Res_{TIM}	Timer resolution			16	Bit
$t_{COUNTER}$	16-bit timer max period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz	0.0104	682	μs
t_{MAX_COUNT}	The max possible count			65536 x 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz		44.7	s

Table 6.6.13.1 TIMx characteristics

6.6.14 Communication interfaces

I2C interface characteristics

Unless otherwise specified, the parameters given in Table below are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and supply voltage conditions summarized in General operating conditions.

The I2C interface conforms to the standard I2C communication protocol, but has the following limitations: SDA and SCL are not true pins. When configured as open-drain output, the PMOS transistor between the pin and VDD Was closed but still exists.

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	2.0+0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		μs
$t_{su(STA)}$	Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	Time from stop condition to start condition	4.7		1.3		

C_b	Capacitive load of each bus		400		400	pF

Table 6.6.14.1 I2C characteristics

f_{PCLK1}must be at least 3MHz to achieve standard mode I2C frequencies. It must be at least 12MHz to achieve fast mode I2C frequencies.

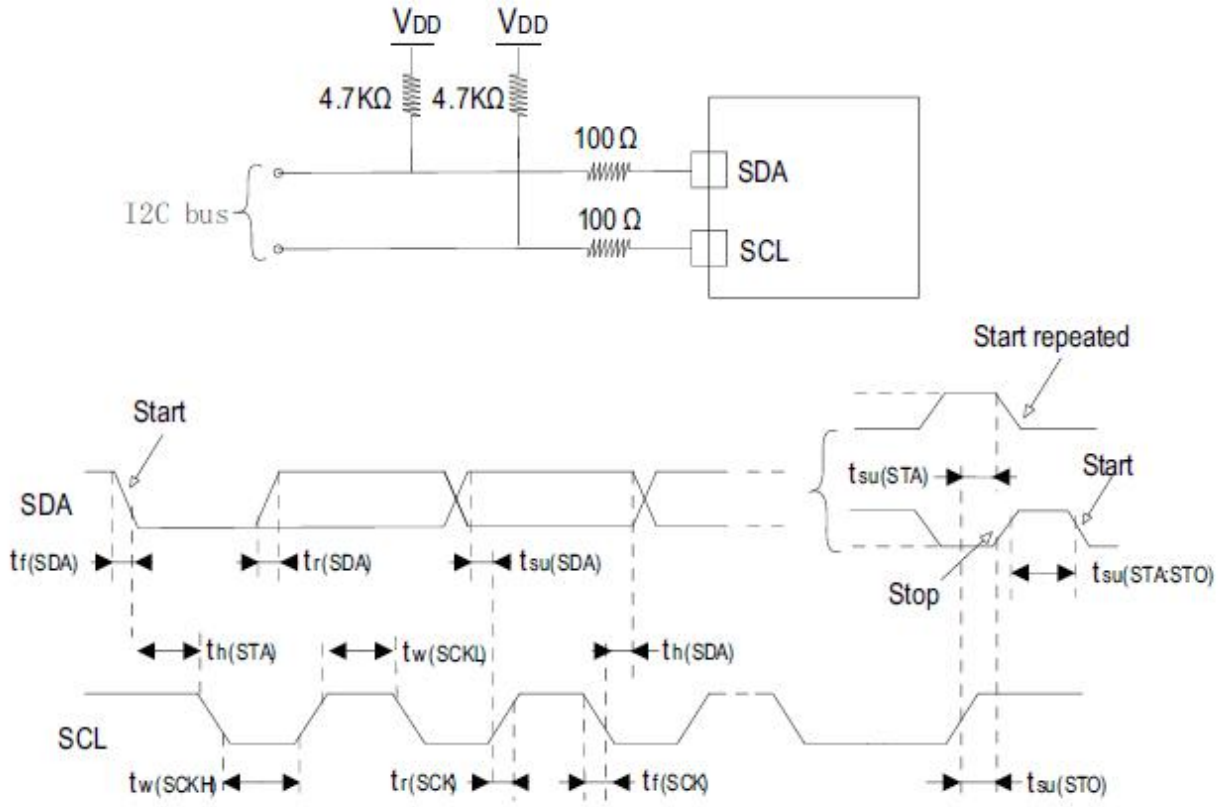


Figure 6.6.14.2 I2C bus AC waveform and measurement circuit

SPI characteristics

Unless otherwise specified, the parameters given in Table below are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in Table 6.1.2.

Symbol	Parameter	Conditions	Min	Max	Unit
$f_{SCK}1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	36	MHz
		Slave mode	0	18	

$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance：C=30pF		8	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{PCLK}$		
$t_{h(NSS)}$	NSS hold time	Slave mode	73		
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK}=36MHz, prescale coefficient=4	50	60	
$t_{su(MI)}$	Data input setup time, Master mode	SPI1	1		
$t_{su(SI)}$	Data input setup time , Slave mode		1		
$t_{h(MI)}$	Data input hold time, Master mode	SPI1	1		
$t_{h(SI)}$	Data input hold time, Slave mode		3		
$t_{a(SO)}$	Data output access time	Salve mode, f_{PCLK} = 36MHz, prescale coefficient=4	0	55	
		Slave mode, f_{PCLK}=24MHz		$4t_{PCLK}$	
$t_{dis(SO)}$	Data output disable time	Slave mode	10		
$t_{v(SO)}$	Data output valid time	Slave mode(after enable edge)		25	
$t_{v(MO)}$	Data output valid time	Master mode(after enable edge)		3	
$t_{h(SO)}$	Data output hold time	Slave mode(after enable edge)	25		
$t_{h(MO)}$		Master mode(after enable edge)	4		

Table 6.6.14.3 SPI parameters

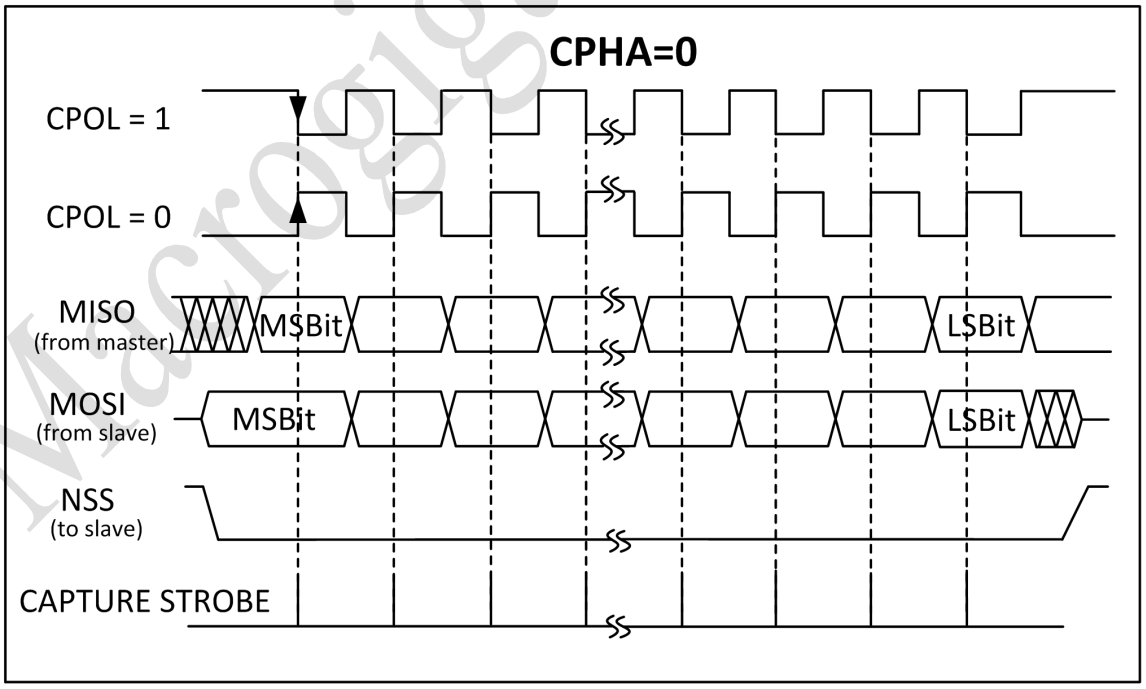


Figure 6.6.14.4 SPI timing – slave, CPHA=0

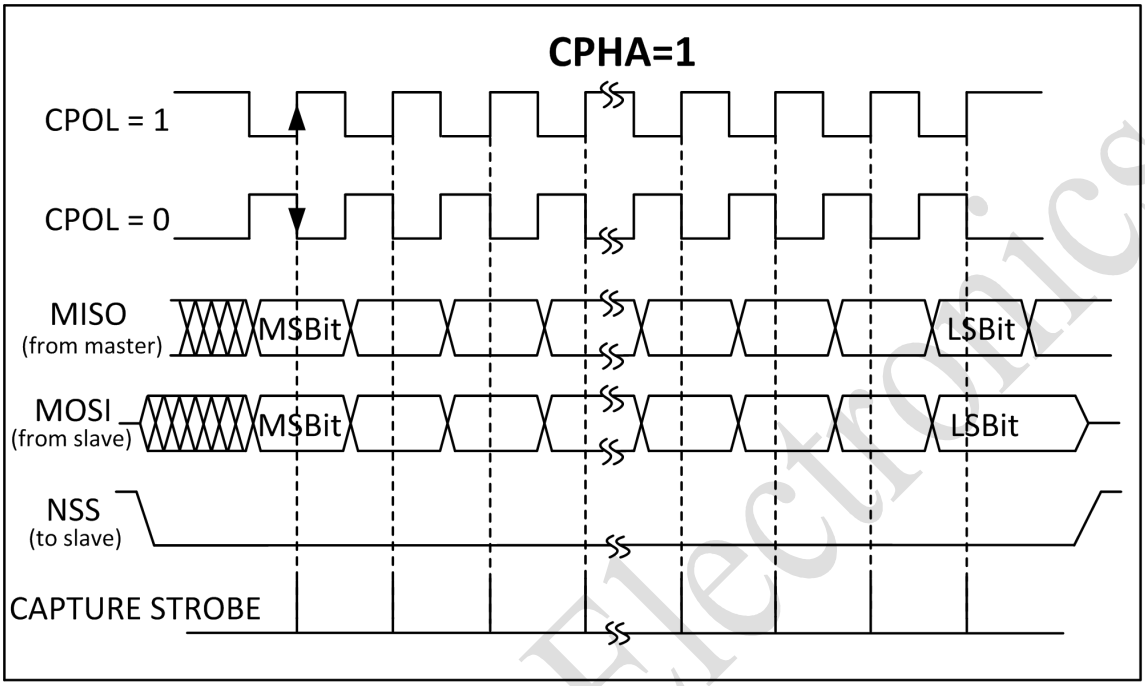


Figure 6.6.14.5 SPI timing – slave, CPHA=1

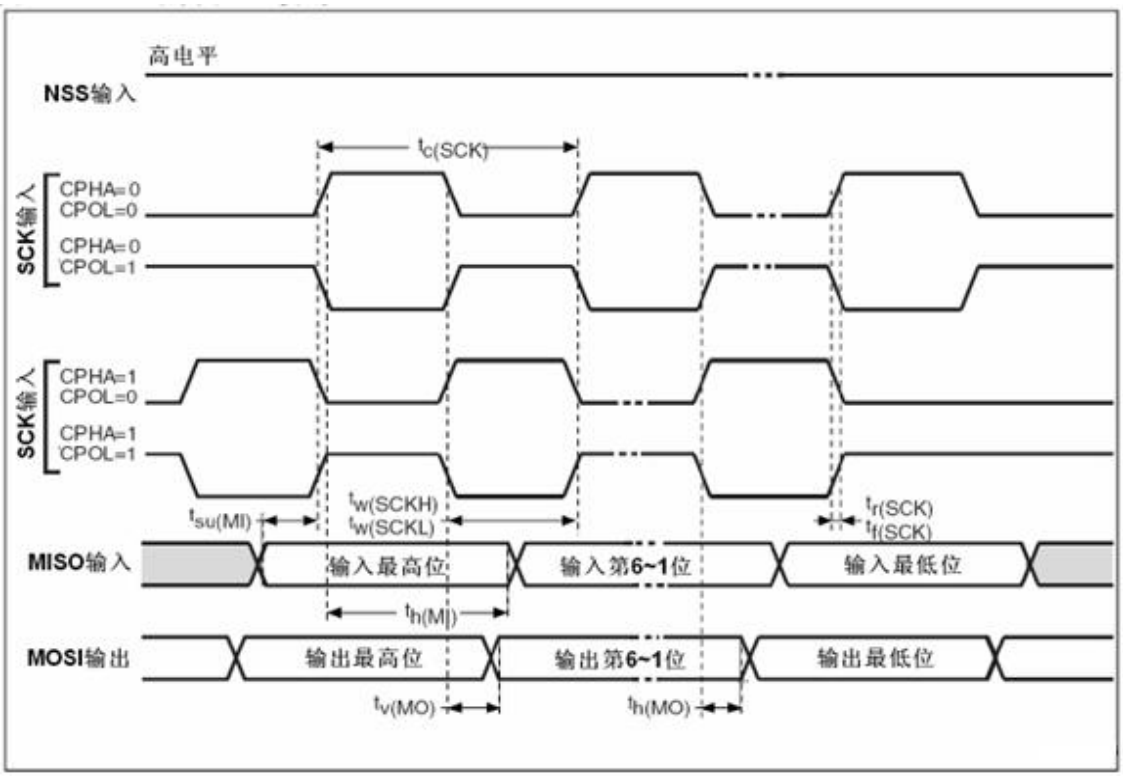


Figure 6.6.14.6 SPI timing - master

6.6.15 12-bit ADC characteristics

Unless otherwise specified, The parameters in the table below are measured using the ambient temperature, fPCLK2 frequency and VDDA supply voltage in accordance with the conditions of Table 6.1.2.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage		2	3.3	3.6	V
V_{REF+}	Positive reference voltage		2		V_{DDA}	V
f_{ADC}	ADC clock frequency				15	MHz
fs	Sampling rate				1	MHz
f_{TRIG}	External trigger frequency	f_{ADC}=15MHz				KHz
V_{AIN}	Conversion voltage range		0		V_{REF+}	V
R_{AIN}	External input resistance					KΩ
R_{ADC}	Sampling switch resistance				1	KΩ
C_{ADC}	Internal sample and hold capacitor			10		pF

ts	Sampling time	f_{ADC}=15MHz	0.1		16	uS
t_{STAB}	Stabilization time			1		uS
t_{CONV}	Total conversion time	f_{ADC}=15MHz	1		16.9	uS

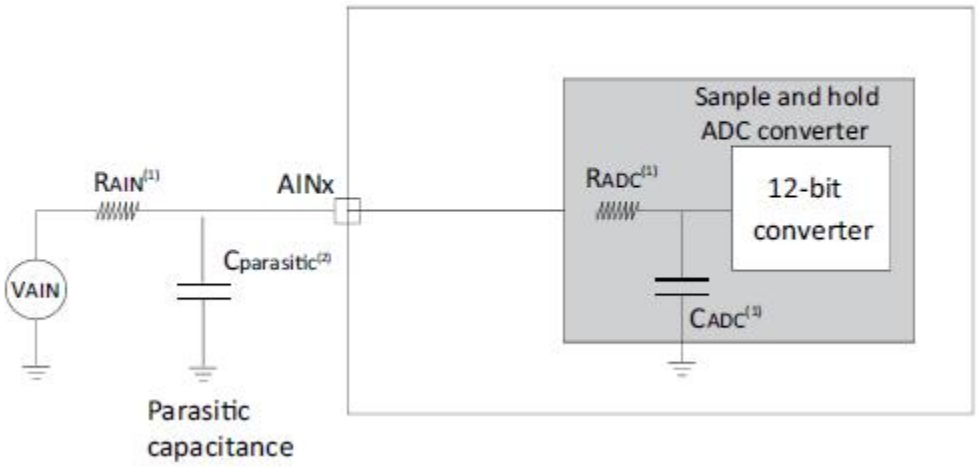
Table 6.6.15.1 ADC characteristics

The formula ： $$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$ is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution) .

Ts (cycles)	ts (uS)	R_{AIN} max(kΩ)
1.5	0.1	1.2
7.5	0.5	10
13.5	0.9	19
28.5	1.9	41
41.5	2.76	60
55.5	3.7	80
71.5	4.77	104
239.5	16.0	350

Table 6.6.15.2 max R_{AIN} at f_{ADC}=15MHz

Typical ADC application：



$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7pF) . A high Cparasitic value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

7. PCB Layout

7.1 Power supply

The power supply must be connected as shown below. The 10nFcapacitor in the figure must be a ceramic capacitor (good quality) , and they should be as close as possible to the MCU chip.

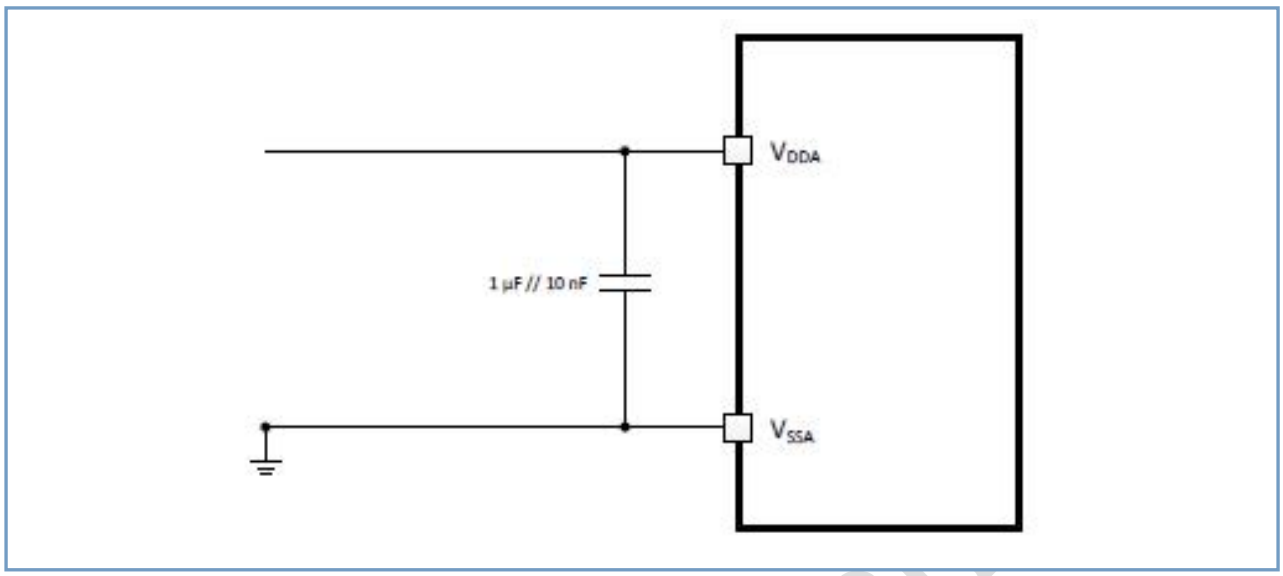


Figure 7.1 power supply and reference power supply decoupling circuit

7.2 2.4G antenna

Small changes of the antenna dimensions may have large impact on the performance. Therefore it is strongly recommended to make an exact copy of the reference design to achieve optimum performance. It is also recommended to use the same thickness and type of PCB material as used in the reference design. To compensate for a thicker/thinner PCB the antenna could be made slightly shorter/longer.

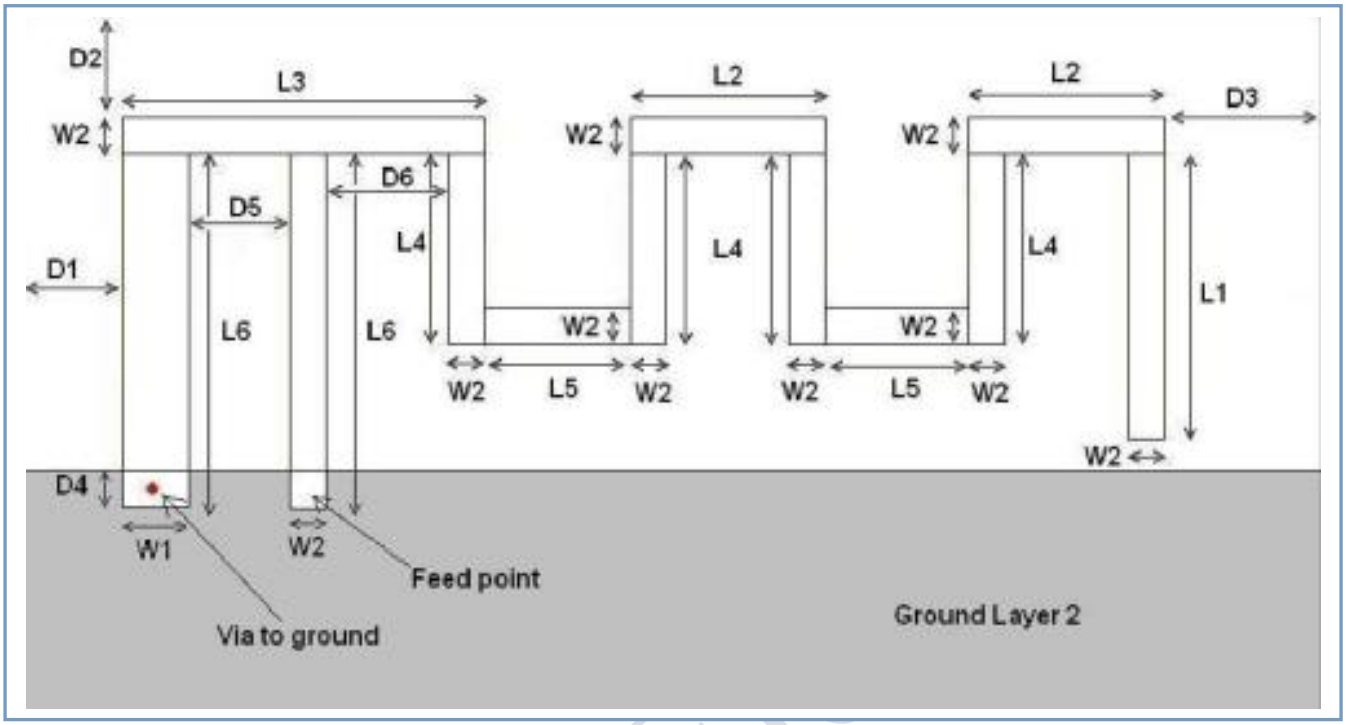
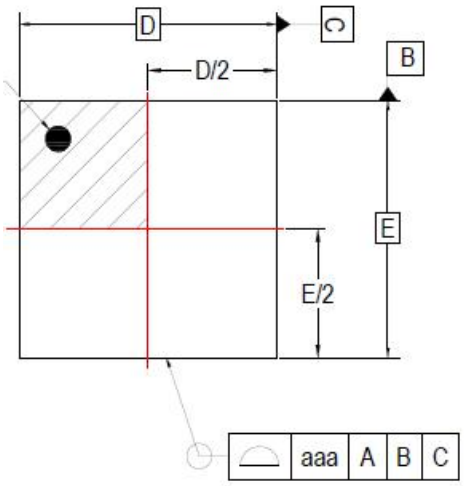


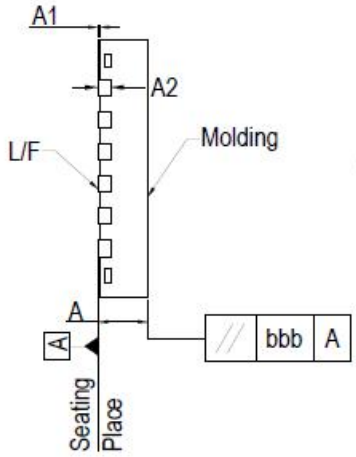
Figure 7.2 Typical Antenna

L1	3.94mm
L2	2.70mm
L3	5.00mm
L4	2.64mm
L5	2.00mm
L6	4.90mm
W1	0.90mm
W2	0.50mm
D1	0.50mm
D2	0.30mm
D3	0.30mm
D4	0.50mm
D5	1.40mm
D6	1.70mm

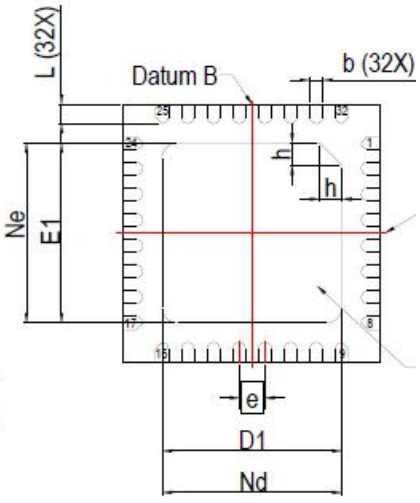
8. Package Information



Top View



Side View



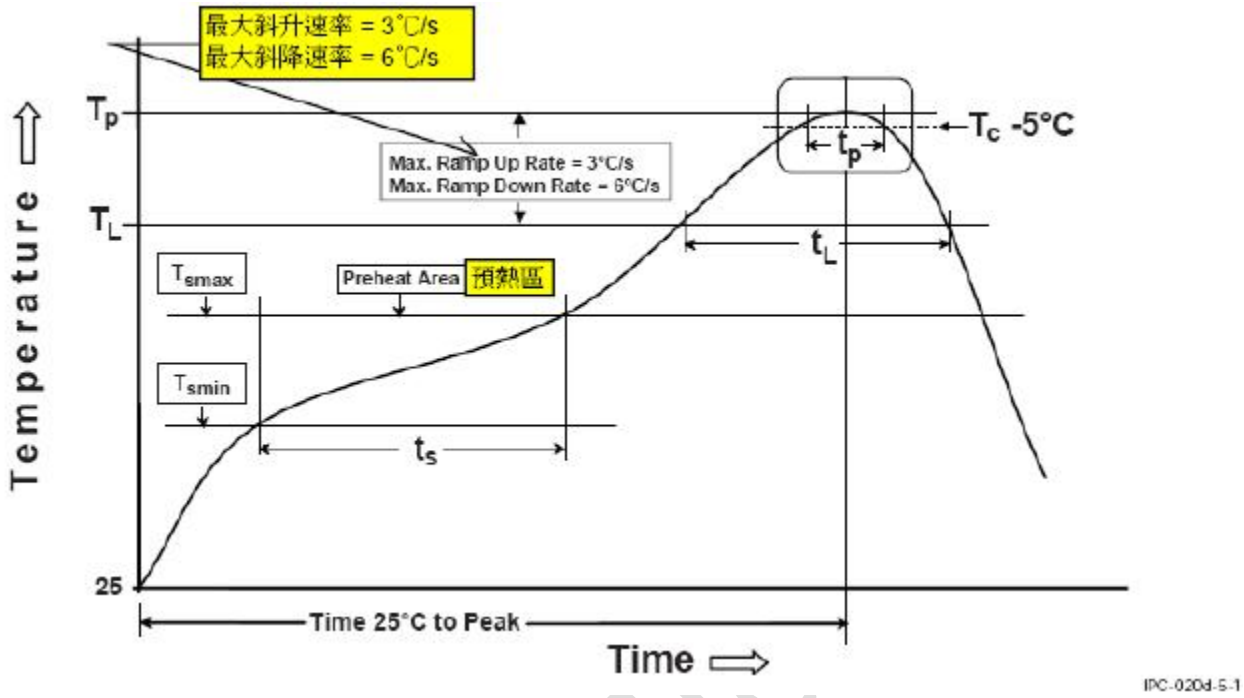
Bottom View

Dimensional References unit: mm

Ref.	MIN	NOR	MAX	Ref.	MIN	NOR	MAX
A	0.90	0.95	1.00	D	3.90	4.00	4.10
A1	0.00	-	0.05	E	3.90	4.00	4.10
A2	0.203 BCS			D1	2.70	2.80	2.90
Ne	2.80 BCS			E1	2.70	2.80	2.90
Nd	2.80 BCS			b	0.15	0.20	0.25
e	0.40 BCS			L	0.25	0.30	0.35
aaa	0.05			h	0.20	0.25	0.30
bbb	0.10						

9. Reflow Profiles

Follow：IPC/JEDEC J-STD-020D



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min（T_{Smin}）	100 ℃	150 ℃
Temperature max（T_{Smax}）	150 ℃	200 ℃
Time（t_{Smin} to t_{Smax}）(ts)	60 – 120 S	60 – 180 S
Average ramp-up rate ($T_{Smax\ to}\ T_P$)	3 ℃/S max	3 ℃/S max
Liquidous temperature(T_L)	183 ℃	217 ℃
Time ate liquidous (t_L)	60 - 150 S	60 - 150 S
Peak package body temperature(T_P)	235 ℃	260 ℃
Time(Tc) within 5℃ of the specified classification temperature(tp)	20 S	30 S
Average ramp-down rate（T_P to T_L）	6℃/S max	6℃/S max
Time 25℃ to peak temperature	6 minutes max	8 minutes max