Digital Red, Green and Blue Color Light Sensor with IR Blocking Filter

ISL29125

The ISL29125 is a low power, high sensitivity, RED, GREEN and BLUE color light sensor (RGB) with an I²C (SMBus compatible) interface. Its state-of-the-art photodiode array provides an accurate RGB spectral response and excellent light source to light source variation (LS2LS). The ISL29125 is designed to reject IR in light sources allowing the device to operate in environments from sunlight to dark rooms. The integrating ADC rejects 50Hz and 60Hz flicker caused by artificial light sources. A selectable range allows the user to optimize sensitivity suitable for the specific application. In normal operation mode the device consumes 56µA, which reduces to 0.5µA in power-down mode. The ISL29125 supports hardware and software user programmable interrupt thresholds. The Interrupt persistency feature reduces false trigger notification. The device operates on supplies (VDD) from 2.25V to 3.63V, I²C supply from 1.7V to 3.63V, and operating temperature across the -40°C to +85°C range.

Related Literature

AN1914, "Evaluation Hardware/Software User Manual for RGB Sensor"

AN1910, "Enhancing RGB Sensitivity and Conversion Time"

Features

- 56µA operating current, 0.5µA shutdown current
- Selectable range (Via I²C)
- I²C (SMBus compatible) output
- ADC resolution 16 bits
- Programmable interrupt windows
- Two optical sensitivity ranges
  - Range 0 = 5.7m lux to 375 lux
  - Range 1 = 0.152 lux to 10,000 lux
- Operating power supply 2.25 to 3.63V
- I²C power supply 1.7V to 3.63V
- 6 Ld ODFN (1.65x1.65x0.7mm) package

Applications

- Smart phone, PDA, GPS, tablet PCs, LCD-TVs, digital picture frames, digital cameras
- Dynamic display color balancing
- Printer color enhancement
- Industrial/commercial LED lighting color management
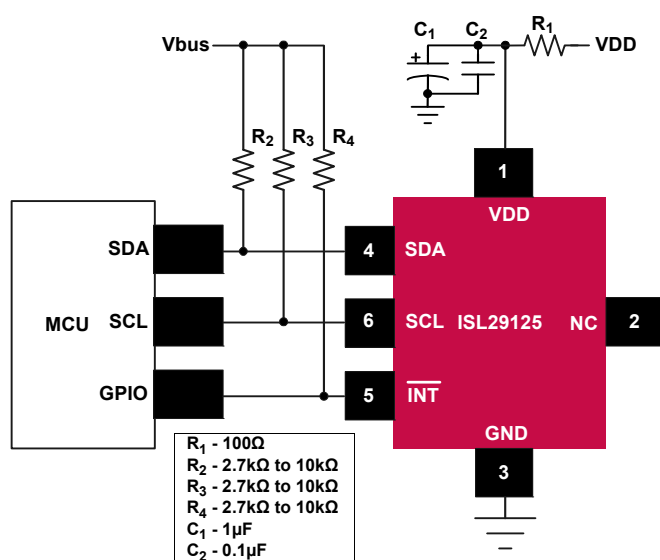- Ambient light color detection/correction
- OLED display aging compensation

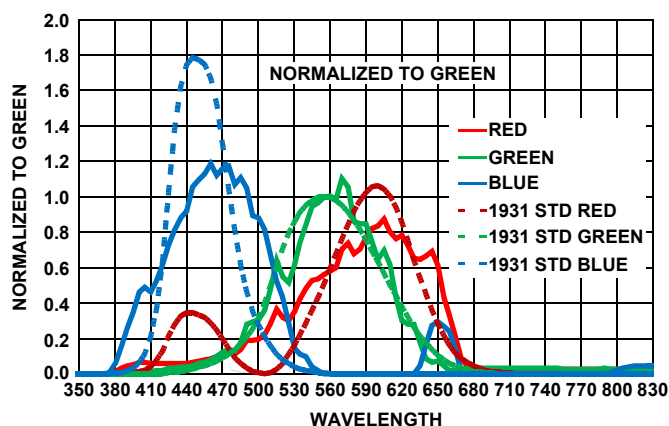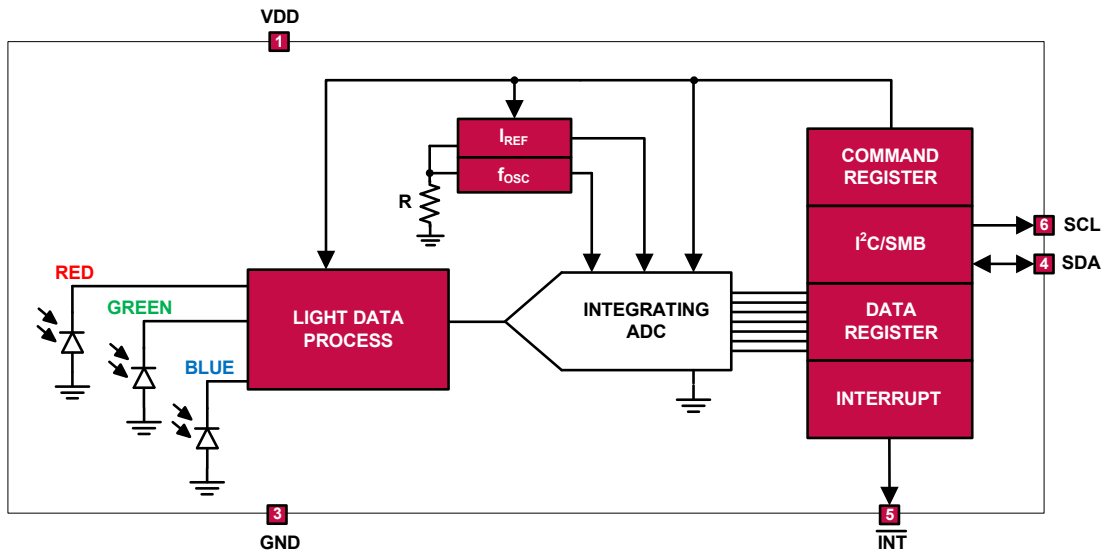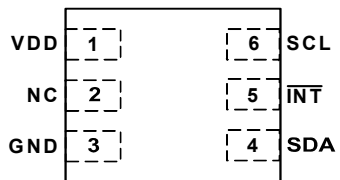FIGURE 1. TYPICAL APPLICATION DIAGRAM

R₁ - 100Ω
R₂ - 2.7kΩ to 10kΩ
R₃ - 2.7kΩ to 10kΩ
R₄ - 2.7kΩ to 10kΩ
C₁ - 1µF
C₂ - 0.1µF

FIGURE 2. NORMALIZED SPECTRAL RESPONSE FOR RED, GREEN AND BLUE SENSING

Block Diagram

Pin Configuration

ISL29125
(6 LD ODFN)
TOP VIEW

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VDD	Positive supply
2	NC	No Connect
3	GND	Ground
4	SDA	I^{2}C serial data
5	$\overline{INT}$	Interrupt; LOW for interrupt alarming. $\overline{INT}$ pin is an open drain. $\overline{INT}$ remains asserted until the interrupt status bit is reset. $\overline{INT}$ also becomes an input when it is set in SYNC mode.
6	SCL	I^{2}C serial clock

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP RANGE (°C)	TAPE AND REEL QUANTITY	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL29125IROZ-T7	-40 to +85	3,000	6 Ld ODFN	L6.1.65x1.65
ISL29125IROZ-T7A	-40 to +85	250	6 Ld ODFN	L6.1.65x1.65
ISL29125EVAL1Z	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.

2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), please see product information page for ISL29125. For more information on MSL please see tech brief TB477.

ISL29125

Absolute Maximum Ratings

VDD to GND . . . . +4.0V
I^2C Bus (SCL, SDA) and $\overline{INT}$ Pin Voltage. . . . . -0.2V to 4.0V
I^2C Bus (SCL, SDA) and $\overline{INT}$ Pin Current. . . . . <10mA
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
   Human Body Model (HBM) 2.5kV
   Machine Model (MM) 300V
   Charged Device Model (CDM) 2kV

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
   6 Ld ODFN Package (Note 4)   260
Maximum Junction Temperature (TJ_{MAX}). . . . . +90°C
Storage Temperature Range. . . . . -40°C to +100°C
Operating Temperature . . . . -40°C to +85°C
Pb-Free Reflow Profile . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD}	Power Supply Range		2.25		3.63	V
I_{DD}	Supply Current			56	85	µA
I_{DD1}	Supply Current when Standby	Software disabled		29	37	µA
I_{DD2}	Supply Current when Powered Down	Software disabled		0.50	1.45	µA
V_{I2C}	Supply Voltage Range for I^2C Interface		1.70		3.63	V
t_{INT}	ADC Integration/Conversion Time	16-bit ADC data		101		ms
f_{I2C}	I^2C Clock Rate Range			500		kHz
D_{Dark}	Count Output when Dark	Lux = 0 lux, Range = 0 (375 lux)		1	5	Counts
CCT	Corrected Color Temperature Accuracy	Illuminant A is at 300 lux (see Note 11 on page 11 and "References" on page 15 about CIE 1931, Planckian locus and standard illuminants)		±5		%
D_{FS}	Full Scale ADC Code	ADC 16 bits			65535	Counts
	Full Scale on Range 0	Green = 565nm		18		µW/cm^2
		Red = 620nm		20		µW/cm^2
		Blue = 485nm		30		µW/cm^2

NOTES:

5. 565nm Green, 620nm Red LED, 485nm Blue in white LED is used in production test. Its irradiance is calibrated to produce the same DATA count against an illuminance level of 130 lux fluorescent light.

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

7. SDA and INT current sinking capability are assured by design.

I²C Interface Specifications V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{IL}	SDA and SCL Input Buffer LOW Voltage				0.55	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		1.25			V
V_{Hys} (Note 8)	SDA and SCL Input Buffer Hysteresis			0.05xV_{DD}		V
V_{OL} (Note 8)	SDA Output Buffer LOW Voltage (Open-Drain), Sinking 4mA		0		0.4	V
C_{PIN} (Note 8)	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				500	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the maximum specification is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid				900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission		1300			ns
t_{LOW}	SCL LOW Time		1300			ns
t_{HIGH}	SCL HIGH Time		600			ns
$t_{SU:STA}$	START Condition Set-Up Time		600			ns
$t_{HD:STA}$	START Condition Hold Time		600			ns
$t_{SU:DAT}$	Input Data Set-Up Time		100			ns
$t_{HD:DAT}$	Input Data Hold Time		30			ns
$t_{SU:STO}$	STOP Condition Set-Up Time		600			ns
$t_{HD:STHD:ST}$	STOP Condition Hold Time		600			ns
$t_{HD:ST}$	Output Data Hold Time		0			ns
$t_{HD:ST}$ (Note 8)	SDA and SCL Rise Time		20+0.1xCb			ns
$t_{HD:ST}$ (Note 8)	SDA and SCL Fall Time		20+0.1xCb			ns
C_b (Note 8)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip			400	pF
R_{PU} (Note 8)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F For C_b = 400pF, maximum is about 2kΩ ~ 2.5kΩ For C_b = 40pF, maximum is about 15kΩ ~ 20kΩ	1			kΩ

NOTES:

8. Limits should be considered typical and are not production tested.

9. These are I²C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.

10. C_b is the capacitance of the bus in pF.
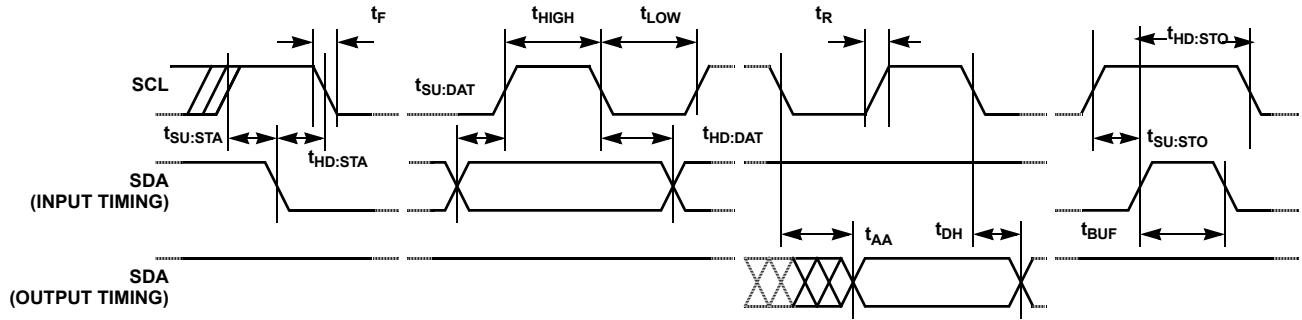
SDA vs SCL Timing

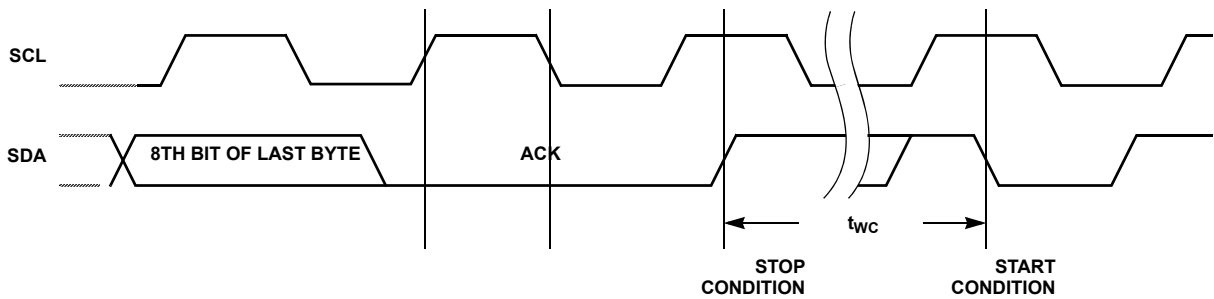FIGURE 3. I²C BUS TIMING

FIGURE 4. I²C WRITE CYCLE TIMING
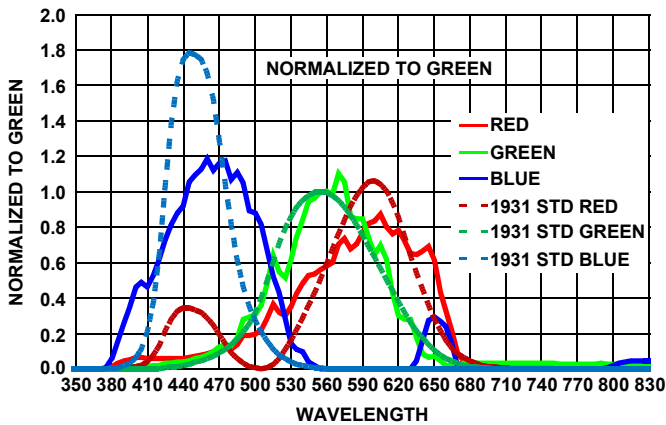
Typical Performance Curves

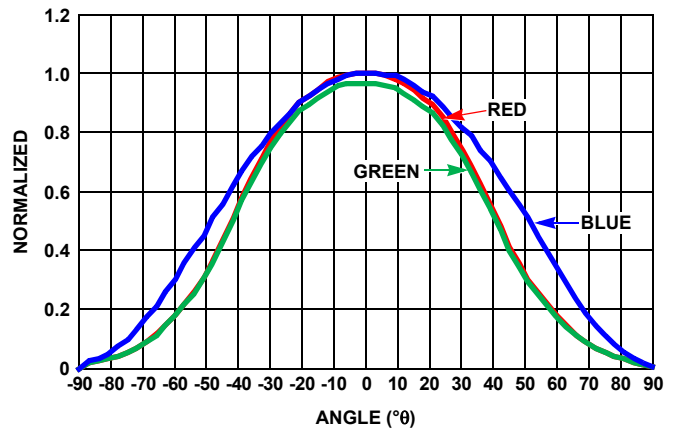FIGURE 5. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT
LIGHT SENSING

FIGURE 6. RADIATION PATTERN

Principles of Operation

Photodiodes and ADC

The ISL29125 contains three photodiode arrays, which convert light into current. The spectral response for RED, GREEN and BLUE color ambient intensity sensing is shown in Figure 2. After light is converted to current during the light to signal process, the current output is converted to a digital count by an on-chip Analog-to-Digital Converter (ADC). The ADC converter resolution is selectable from 12 or 16 bits. The ADC conversion time is inversely proportional to the ADC resolution.

The ADC converter uses an integrating architecture. This conversion method is ideal for converting small signals in the presence of a periodic noise. A 100ms integration time (16-bit mode) for instance, rejects 50Hz and 60Hz power line as well as florescent flicker noise.

The ADC integration time is determined by an internal oscillator and the n-bit (n = 12, 16) counter inside the ADC. A good balancing act of integration time and resolution depends on the application for optimum system performance.

The ADC provides two programmable ranges to dynamically accommodate different lighting conditions. For dim conditions, the ADC can be configured at its high sensitivity (low optical) range. For bright conditions, the ADC can be configured at its low sensitivity (higher optical) range. Note that the effective optical sensitivity of the ISL29125 in terms of counts/μW/cm^2 is directly proportional to the ADC integration time.

SYNC Mode

SYNC mode is when B5 at Reg0x1 is set to '1', the $\overline{INT}$ pin becomes an input pin. This mode is beneficial for some systems which have multiple sensors on I^{2}C bus. Once B5 is set, on the rising edge of INT the ADC starts conversion so that multiple devices would measure at exactly the same time. Yet, to read data out, the system needs to have a different I^{2}C address for each sensor or have a multiplexer. Moreover, if B5 is set to '0', then $\overline{INT}$ pin will be asserted whenever the sensor triggers an interrupt.

Interrupt Function

The active low interrupt pin is an open-drain pull-down configuration. The interrupt pin serves as an alarm or monitoring function to determine whether the ambient light level exceeds the upper threshold or goes below the lower threshold. It should be noted that the function of ADC conversion continues without stopping after interrupt is asserted. If the user needs to read the ADC count that triggers the interrupt, the reading should be done before the data registers are refreshed by the following conversions. The user can also configure the persistency of the interrupt pin. This reduces the possibility of false triggers, such as noise or sudden spikes in ambient light conditions. An unexpected camera flash, for example, can be ignored by setting the persistency to 8 integration cycles. ISL29125 interrupt modes can be selected at Bit[1:0] at Reg0x03 Table 11. The user can select Red, Green or Blue to be the interrupt target. An interrupt event (RGBTHF) bit at Reg0x08 is governed by Registers 4 through 7. The user writes a high and low threshold value to these registers and the ISL29125 will issue an interrupt flag if the actual count stored in Registers 0x9 and 0xA for Green or Registers 0xB and 0xC for Red or Register 0xD and 0xE for Blue are outside the user's programmed window. Once ISL29125 issues the interrupt flag, the interrupt status (RGBTHF) bit at Reg0x08 is asserted to logic HIGH and the $\overline{INT}$ pin goes low. Both the $\overline{INT}$ pin and the interrupt status bit are automatically cleared at the end of the 8-bit Device Register byte (0x08) transfer. By default (RGBTHF) bit is LOW or it is within the interrupt thresholds window.

Power-On Reset

The Power-On Reset (POR) circuitry protects the internal logic against powering up in the incorrect state. The ISL29125 will power up into Standby mode after VDD exceeds the POR trigger level and will power down into Reset mode when VDD drops below the POR trigger level. This bidirectional POR feature protects the device against 'brown-out' failure following a temporary loss of power.

The POR is an important feature because it prevents the ISL29125 from starting to operate with insufficient power supply voltage. The ISL29125 prevents communication to its registers and reduces the likelihood of data corruption on power-up.

Serial Interface

The ISL29125 supports the Inter-Integrated Circuit (I^{2}C) bus data transmission protocol. The I^{2}C bus is a two-wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I^{2}C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a "0" and releases it to transmit a "1". The master always initiates the data transfer, only when the bus is not busy and provides the clock for both transmit and receive operations. The ISL29125 operates as a slave device in all applications. The serial communication over the I^{2}C interface is conducted by sending the Most Significant Bit (MSB) of each byte of data first.

Start Condition

During data transfer, the SDA line must remain stable while the SCL line is HIGH. All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH (refer to Figure 9). The ISL29125 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (refer to Figure 9). A START condition is ignored during the power-up sequence.

Stop Condition

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (refer to Figure 9). A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before 1 full Data byte and ACK is sent, then the serial communication of ISL29125 resets itself without performing the read/write. The contents of the register array are not affected.

Acknowledge

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8 bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (refer to Figure 9). The ISL29125 responds with an ACK after recognition of a START condition followed by a valid Identification Byte and once again, after successful receipt of an Address Byte. The ISL29125 also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation

Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of ISL29125 are internally hard-wired as "1000100". The LSB of the Device Address byte is defined as read or write ($R/\overline{W}$) bit. When this $R/\overline{W}$ bit is a "1", a read operation is selected and when "0", a write operation is selected (refer to Figure 7). The master generates a START condition followed by Device Address byte 1000100x (x as $R/\overline{W}$) and the ISL29125 compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line (refer to Figure 9).
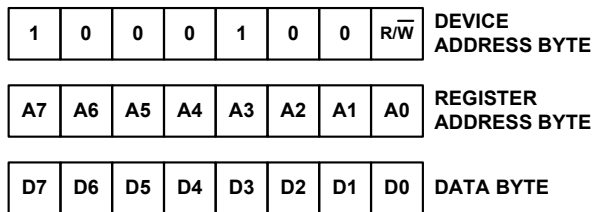
1	0	0	0	1	0	0	R/W̄	DEVICE ADDRESS BYTE

A7	A6	A5	A4	A3	A2	A1	A0	REGISTER ADDRESS BYTE

D7	D6	D5	D4	D3	D2	D1	D0	DATA BYTE

FIGURE 7. DEVICE ADDRESS, REGISTER ADDRESS AND DATA BYTE

Write Operation

BYTE WRITE

In a byte write operation, ISL29125 requires the Device Address byte, Register Address byte and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte and the Data byte, the ISL29125 responds with an acknowledge (ACK). Following the ISL29125 data acknowledge response, the master terminates the transfer by generating a STOP condition. The ISL29125 then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master (refer to Figure 8).

BURST WRITE

The ISL29125 has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ISL29125 responds with an acknowledge and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it "rolls over" and goes back to the first Register Address.
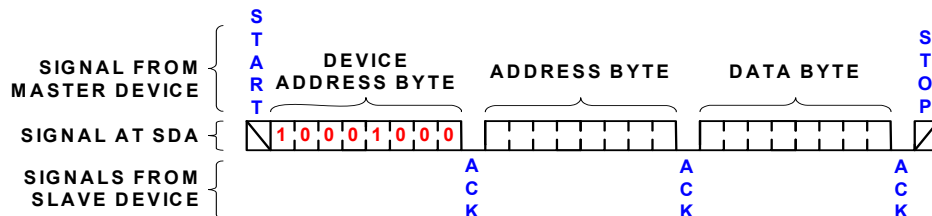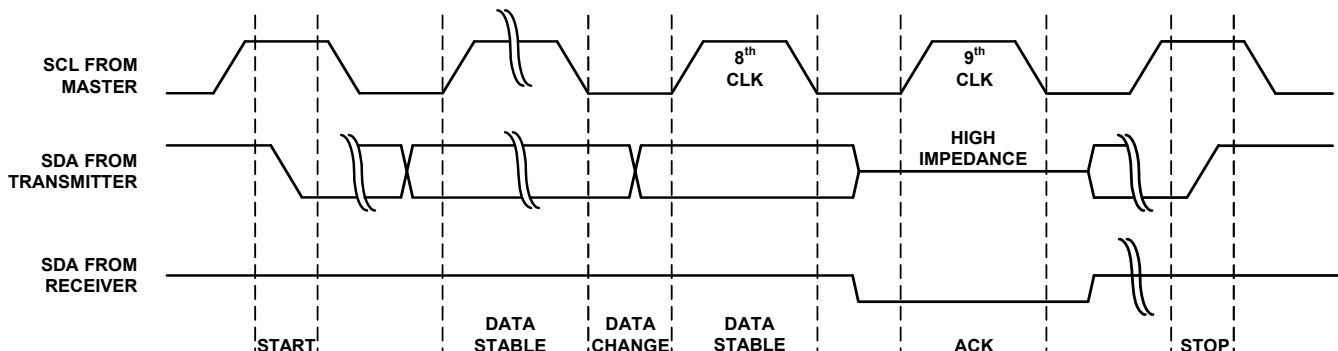
FIGURE 8. BYTE WRITE SEQUENCE

FIGURE 9. START, DATA STABLE, ACKNOWLEDGE AND STOP CONDITION

Read Operation

ISL29125 has two basic read operations: Byte Read and Burst Read.

BYTE READ

Byte read operations allow the master to access any register location in the ISL29125. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/$\overline{\text{W}}$ bit set to "0", receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/$\overline{\text{W}}$ bit set to "1". This is followed by an acknowledge from the device and then by the 8-bit data word.

The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 10.

BURST READ

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition (refer to Figure 11).

For more information about the I^{2}C standard, please consult the Phillips™ I^{2}C specification documents.
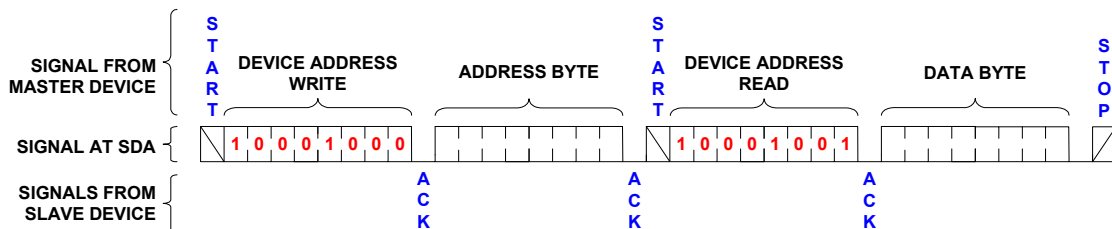

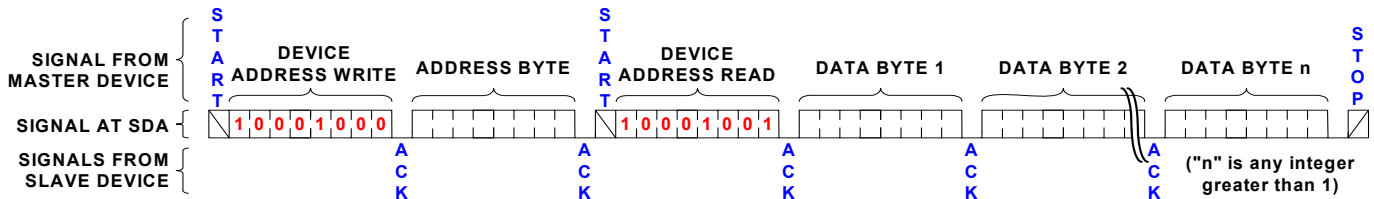**FIGURE 10. BYTE ADDRESS READ SEQUENCE**

FIGURE 11. BURST READ SEQUENCE

TABLE 1. REGISTER MAP

NAME	REGISTER ADDRESS DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT	ACCESS
Device ID	0	0x00	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x7D	RO
Device Reset			ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	NA	WO
CONFIGURATION - 1	1	0x01	RESERVED		SYNC	BITS	RNG	MODE[2]	MODE[1]	MODE[0]	0x00	RW
CONFIGURATION - 2	2	0x02	IRCOM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	0x00	RW
CONFIGURATION - 3	3	0x03	RESERVED			CONVEN	PRST[1]	PRST[0]	INTSEL[1]	INTSEL[0]	0x00	RW
LOW THRESHOLD - LOW BYTE	4	0x04	THL[7]	THL[6]	THL[5]	THL[4]	THL[3]	THL[2]	THL[1]	THL[0]	0x00	RW
LOW THRESHOLD - HIGH BYTE	5	0x05	THL[15]	THL[14]	THL[13]	THL[12]	THL[11]	THL[10]	THL[9]	THL[8]	0x00	RW
HIGH THRESHOLD - LOW BYTE	6	0x06	THH[7]	THH[6]	THH[5]	THH[4]	THH[3]	THH[2]	THH[1]	THH[0]	0xFF	RW
HIGH THRESHOLD - HIGH BYTE	7	0x07	THH[15]	THH[14]	THH[13]	THH[12]	THH[11]	THH[10]	THH[9]	THH[8]	0xFF	RW
STATUS FLAGS	8	0x08	RESERVED		GRBCF[1]	GRBCF[0]	RESERVED	BOUTF	CONVENF	RGBTHF	0x04	RO
GREEN DATA - LOW BYTE	9	0x09	GREEN[7]	GREEN[6]	GREEN[5]	GREEN[4]	GREEN[3]	GREEN[2]	GREEN[1]	GREEN[0]	0x00	RW
GREEN DATA - HIGH BYTE	10	0x0A	GREEN[15]	GREEN[14]	GREEN[13]	GREEN[12]	GREEN[11]	GREEN[10]	GREEN[9]	GREEN[8]	0x00	RW
RED DATA - LOW BYTE	11	0x0B	RED[7]	RED[6]	RED[5]	RED[4]	RED[3]	RED[2]	RED[1]	RED[0]	0x00	RW
RED DATA - HIGH BYTE	12	0x0C	RED[15]	RED[14]	RED[13]	RED[12]	RED[11]	RED[10]	RED[9]	RED[8]	0x00	RW
BLUE DATA - LOW BYTE	13	0x0D	BLUE[7]	BLUE[6]	BLUE[5]	BLUE[4]	BLUE[3]	BLUE[2]	BLUE[1]	BLUE[0]	0x00	RW
BLUE DATA - HIGH BYTE	14	0x0E	BLUE[15]	BLUE[14]	BLUE[13]	BLUE[12]	BLUE[11]	BLUE[10]	BLUE[9]	BLUE[8]	0x00	RW

Register Description

Following are detailed descriptions of the control registers related to the operation of the ISL29125 ambient light sensor device. These registers are accessed by the I^{2}C serial interface. For details on the I^{2}C interface, refer to "Serial Interface" on page 6.

All the features of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. All RESERVED bits are Intersil used bits ONLY. The value of the reserved bit can change without any notice.

Device Register (Address: 0x00)

TABLE 2. DEVICE ID REGISTER ADDRESS

NAME	REGISTER ADDRESS DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT	ACCESS
Device ID	0	0x00	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x7D	RO
Device Reset			ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	NA	WO

Register 0x00 performs two functions. If Reg 0x00 is in READ ONLY mode then it will be a Device ID. By default, the device ID is 0x7D in hex. Write 46h to register 0x00 in the WRITE ONLY, the device will reset all registers to their default states.

Confiugation-1 Register (Address: 0x01)

TABLE 3. CONFIGURATION-1

NAME	REGISTER ADDRESS DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT	ACCESS
Configuration-1	1	0x01	RESERVED	RESERVED	SYNC	BITS	RNG	MODE[2]	MODE[1]	MODE[0]	0x00	RW

RGB Operating Modes [B2:B0]

This device has various RGB operating modes. These modes are selected by setting B2:B0 bits in Table 4. The device powers up on a disable mode. All operating modes are in continuous ADC conversion. The following bits are used to enable the operating mode.

TABLE 4. OPERATION MODES

B2:B0	OPERATION
000	Power-Down (ADC conversion)
001	GREEN Only
010	RED Only
011	BLUE Only
100	Stand by (No ADC conversion)
101	GREEN/RED/BLUE
110	GREEN/RED
111	GREEN/BLUE

RGB Data Sensing Range [B3]

The Full Scale RGB Range has two different selectable ranges at bit 3. The range determines the ADC resolution (12 bits and 16 bits). Each range has a maximum allowable lux value. Higher range values offer better resolution and wider lux value.

TABLE 5. SENSING RANGES

B3	RANGES (lux)
0	375
1	10,000

ADC Resolution [B4]

ADC's resolution and the number of clock cycles per conversion is determined by this bit in Table 6. Changing the resolution of the ADC changes the number of clock cycles of the ADC which in turn changes the integration time. Integration time is the period the ADC samples the photodiode current signal for a measurement.

TABLE 6. ADC RESOLUTIONS

B4	RESOLUTION (bits)
0	16
1	12

RGB Start Synced at $\overline{INT}$ Pin

TABLE 7. SYNCED AT $\overline{INT}$

B5	OPERATION
0	ADC start at I2C write 0x01
1	ADC start at rising $\overline{INT}$

SYNC has two different selectable modes at bit 5. B5 sets to 0 then the INT pin gets asserted whenever the sensor interrupts. B5 sets to 1 then the $\overline{INT}$ pin becomes input pin. On the rising edge at $\overline{INT}$ pin, SYNC starts ADC conversion. The $\overline{INT}$ pin sets to interrupt mode by default. More information about SYNC at "Principles of Operation" on page 6.

Configuration-2 Register (Address: 0x02)

ACTIVE INFRARED (IR) COMPENSATION

The device is designed for operation under dark glass cover which significantly attenuates visible light and passes the infrared light without much attenuation. The device has an on chip passive optical filter designed to block (reject) most of the incident infrared. In addition, the device provides a programmable active IR compensation which allows fine tuning of residual infrared components from the output, which allows optimizing the measurement variation between differing IR-content light sources. B7 is "IR Comp Offset" and B[5:0] is "IR Comp Adjust", which provides means for adjusting IR compensation. B7 = '0' + B[5:0] is the effective IR compensation from 0 to 63 codes and B7 set to '1'+B[5:0] the effective IR compensation is from 106 to 169. Table 9 on page 11 shows lightweight for each IR compensation bit and Figure 12 is a typical system measure for both IR Comp Adjust and IR Comp Offset. More detail about how to IR compensation, see IR compensation in "Applications Information" on page 13.

Recommended to set BF at register 0x02 to max out IR compensation value. It make High range reach more than 10,000 lux.

TABLE 8. CONFIGURATION-2

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Configuration-2	2	0x02	IR-COM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	0x00	RW
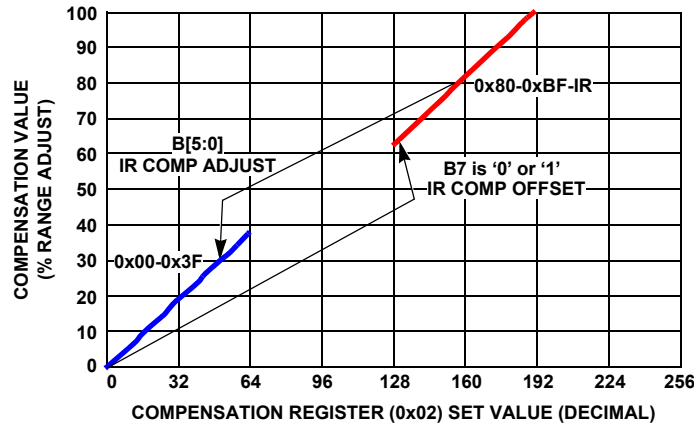
FIGURE 12. IR COMPENSATION SET

TABLE 9.

B7	B6	B5	B4	B3	B2	B1	B0	LIGHT-WEIGHT
IR-COM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	
106		32	16	8	4	2	1	Codes

NOTES:

11. A illuminant is intended to represent typical, domestic, tungsten-filament lighting. Its CCT is about 2856K.

12. D series of illuminants are constructed to represent natural daylight. D65 is used in lab to represent noon light to test. Its CCT is 6504K.

13. F series of illuminants represent various types of fluorescent lighting. F2 is cool white fluorescent used in lab to test. Its CCT is 4230K.

Configuration-3 Register (Address: 0x03)

TABLE 10. CONFIGURATION-3

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
CONFIGURATION-3	3	0x03	RESERVED	RESERVED	RESERVED	CONVEN	PRST[1]	PRST[0]	INTSEL[1]	INTSEL[0]	0x00	RW

INTERRUPT THRESHOLD ASSIGNMENT [B1:0]

The interrupt status bit (RGBTHF) bit0 at Reg0x08 is a status bit for light intensity detection. The bit is set to logic HIGH when the light intensity crosses the interrupt thresholds window (register address 0x04 - 0x07) and set to logic LOW when it's within the interrupt thresholds window. Once the interrupt is triggered, the $\overline{INT}$ pin goes low and the interrupt status bit goes HIGH until the status bit is polled through the I^{2}C read command. Both the $\overline{INT}$ pin and the interrupt status bit are automatically cleared at the end of the 8-bit Device Register byte (0x08) transfer. Table 11 shows selectable interrupt for the device.

TABLE 11. INTERRUPT STATUS

B1:0	INTERRUPT STATUS
00	No Interrupt
01	GREEN Interrupt
10	RED Interrupt
11	BLUE Interrupt

INTERRUPT PERSIST CONTROL [B3:2]

To minimize interrupt events due to 'transient' conditions, an interrupt persistency option is available. IN the event of a transient condition, an 'X-consecutive' number of interrupt must happen before the interrupt flag and P_{INT} ($\overline{INT}$) pin gets driven low. The interrupt is active-low and remains asserted until the status register (Addr: 0x08) is read to CLEAR the bit(s).

TABLE 12. INTERRUPT PERSIST

B3:2	NUMBER OF INTEGRATION CYCLE
00	1
01	2
10	4
11	8

RGB CONVERSION DONE TO $\overline{INT}$ CONTROL [B4]

TABLE 13.

B4	CONVERSION DONE
0	Disable
1	Enable

Lower Interrupt Register (Address: 0x04 and 0x05) and Higher Interrupt Register (Address: 0x06 and 0x07)

TABLE 14. CONFIGURATION-3

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Low Threshold - Low byte	4	0x04	THL[7]	THL[6]	THL[5]	THL[4]	THL[3]	THL[2]	THL[1]	THL[0]	0x00	RW
Low Threshold - High byte	5	0x05	THH[7]	THH[6]	THH[5]	THH[4]	THH[3]	THH[2]	THH[1]	THH[0]	0x00	RW
High Threshold - Low byte	6	0x06	THL[7]	THL[6]	THL[5]	THL[4]	THL[3]	THL[2]	THL[1]	THL[0]	0xFF	RW
High Threshold - High byte	7	0x07	THH[7]	THH[6]	THH[5]	THH[4]	THH[3]	THH[2]	THH[1]	THH[0]	0xFF	RW

Interrupt Threshold (Reg 0x4, Reg0x5, Reg0x6 and Reg0x7)

The interrupt threshold level is a 16-bit number (Low Threshold-1 and Low Threshold-2). The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the ALS value crosses below or is equal to the lower threshold, an interrupt is asserted on the interrupt pin (LOW) and the interrupt status bit (HIGH). Registers Low Threshold-1 (0x04 or 0x6) and Low Threshold-2 (0x05 or 0x7) provide the low and high bytes, respectively, of the lower interrupt threshold. The interrupt threshold registers default to 0x00 upon power-up. The user can also configure the persistency for the interrupt pin. This reduces the possibility of false triggers, such as noise or sudden spikes in ambient light conditions or an unexpected camera flash, for example, can be ignored by setting the persistency to 8 integration cycles.

Status Flag Register (Address: 0x08)

TABLE 15. STATUS FLAG REGISTER

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
Status Flag	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
	8	0x08	RESERVED	RESERVED	RGBCF[1]	RGBCF[0]	RESERVED	BOUTF	CONVENF	RGBTHF	0x04	RO

RGBTHF [B0]

This is the status bit of the interrupt. The bit is set to logic high when the interrupt thresholds have been triggered (out of threshold window) and logic low when not yet triggered. Once activated and the interrupt is triggered, the $\overline{\text{INT}}$ pin goes low and the interrupt status bit goes high until the status bit is polled through the I²C read command. Both the $\overline{\text{INT}}$ output and the interrupt status bit are automatically cleared at the end of the 8-bit (00h) command register transfer

TABLE 16. INTERRUPT FLAG

B0	OPERATION
0	Interrupt is cleared or not triggered yet
1	Interrupt is triggered

CONVENF [B1]

This is the status bit of conversion. The bit is set to logic high when the conversion have been completed and logic low when the conversion is not done or not conversion.

TABLE 17. CONVERSION FLAG

B1	OPERATION
0	Still convert or cleared
1	Conversion completed

BOUTF [B2]

Bit2 on register address 0x08 is a status bit for brownout condition (BOUT). The default value of this bit is HIGH, BOUT = 1, during the initial power-up. This indicates the device may possibly have gone through a brownout condition. Therefore, the status bit should be reset to LOW, BOUT = 0, by an I²C write command during the initial configuration of the device. The default register value is 0x04 at power-on.

TABLE 18. BROWNOUT FLAG

B2	OPERATION
0	No Brownout
1	Power-down or Brownout occurred

RGBCF [B5:B4]

B[5:4] are flag bits to display either Red Green or Blue is under conversion process at Table 19.

TABLE 19. CONVERSION FLAG

B5:4	RGB UNDER CONVERSION
00	No Operation
01	GREEN
10	RED
11	BLUE

Data Register (Address: 0x09,0x0A,0xB,0xC,0xD and 0xE)

TABLE 20. CONFIGURATION-3

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
GREEN Data - Low Byte	9	0x09	GREEN[7]	GREEN[6]	GREEN[5]	GREEN[4]	GREEN[3]	GREEN[2]	GREEN[1]	GREEN[0]	0x00	RW
GREEN Data - High Byte	10	0x0A	GREEN[15]	GREEN[14]	GREEN[13]	GREEN[12]	GREEN[11]	GREEN[10]	GREEN[9]	GREEN[8]	0x00	RW
RED Data - Low Byte	11	0x0B	RED[7]	RED[6]	RED[5]	RED[4]	RED[3]	RED[2]	RED[1]	RED[0]	0x00	RW
RED Data - High Byte	12	0x0C	RED15]	RED[14]	RED[13]	RED[12]	RED[11]	RED[10]	RED[9]	RED[8]	0x00	RW
RED Data - Low Byte	13	0x0D	BLUE[7]	BLUE[6]	BLUE[5]	BLUE[4]	BLUE[3]	BLUE[2]	BLUE[1]	RED[0]	0x00	RW
RED Data - High Byte	14	0x0E	BLUE[15]	BLUE[14]	BLUE[13]	BLUE[12]	BLUE[11]	BLUE[10]	BLUE[9]	RED[8]	0x00	RW

The ISL29125 has two 8-bit read-only registers to hold the higher and lower byte of the ADC value. The lower and higher bytes are accessed at address, respectively. For 16-bit resolution, the data is from D0 to D15; for 12-bit resolution, the data is from D0 to D11. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power-on. Because all the register are double buffered the data is always valid on the data registers.

Applications Information

Figure 13 is a plot of the 1931 standard normalized spectral response of various types of light sources for reference.
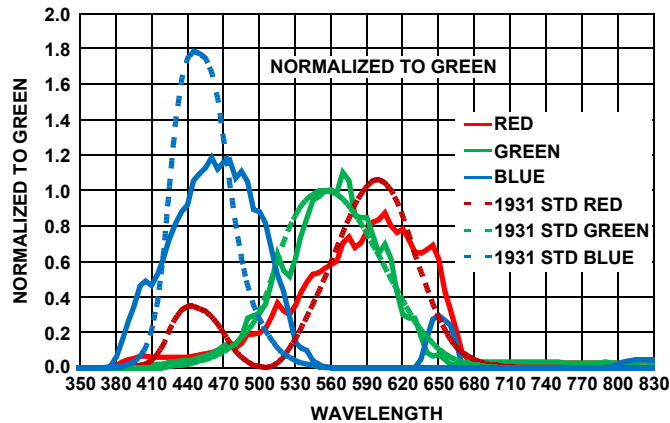
FIGURE 13. 1931 STANDARD NORMALIZED SPECTRAL RESPONSE OF LIGHT SOURCES

System Compensation and RGB to XYZ Transform (Chroma Meter)

The accuracy of the RGB sensor is extremely sensitive to the optomechanical design of the system in which it resides. The compensation setting and calculation of RGB to XYZ transform should be characterized within that environment with as many standard illuminants as possible. A minimal recommended set would include A, F2 and D65 illuminants (see Notes 11, 12, 13 and "References" on page 15 about IEC 1931, Planckian locus and standard illuminants). The two most important optomechanical features are FOV (Field Of View FWHM) and optical filters as example of tinted cell phone glass through which the sensor will detect the ambient lighting. With the combination of the FOV and a large sample for the filter (30x30mm) it is possible to determine the best compensation and XYZ transform coefficients. It is also possible to project the accuracy of the measurement system.

RGB → XYZ TRANSFORM

Once the proper compensation setting is determined, measure the RGB values of the various illuminates at this value. Calculate the RGB to XYZ transform coefficients based on the measured result against appropriate Chroma Meter Standard (using x and y values) as shown in Equation 1.

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} C_{XR} & C_{XG} & C_{XB} \\ C_{YR} & C_{YG} & C_{YB} \\ C_{ZR} & C_{ZG} & C_{ZB} \end{bmatrix} \times \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

(EQ. 1)

X, Y and Z are in the IEC system which specifies the color and brightness of a particular homogeneous visual stimulus.

R, G and B are digital output from the sensor.

Cs are coefficents. These coefficients will be changed respectively depending on the system setup.

COMPENSATION

The compensation adjustment is used to balance the various illuminates of interest (A, F2 and D65 recommended) such that the value measured at the same power level (measured with a lux meter) is the closed value. Since the compensation adjustment is piecewise linear the proper setting can be determined by extrapolating from a pair of measurements and calculating the closest intersection of the sources of interest.

The Configuration register (Reg 0x02[7:0]) allows coarse tuning B7 and fine tuning (B[5:0] of the residual infrared component from the ALS output.

The recommended procedure for determining ALS IR compensation is as follows:

- Illuminate the ISL29125 based design configuration with a no IR F2 light source. Record the ALS measurement and the lux level.

- Illuminate the device with A and D65 with heavy IR and the F2 light sources. Take an ALS measurement and lux level measurement.

- It really depends on the system setup in order to adjust the Configuration register (Reg 0x02, B7 and B[5:0]) to compensate for the IR contribution.

- Repeat steps above until the IR light source contribution to the ALS measurement is under 10 percent assuming no change in lux level due to IR light source.

Figure 14 is an example showing how to calculate the compensation for varying level of infrared components such as A, F2 and D65 (see Notes 11, 12 and 13 on page 11). With compensation adjustment from 0% to 100%. The crossing point is the IR compensation value which results in tighter variation with varying levels of infrared components. This setup system is a sensor without IR tinted glass and is illuminated with 3 different light sources. Since it is not under IR tinted glass, then reg0x2 setups like b7 = '0' and B[5:0] is at about 25% compensation adjust (%/range) which means about 40 codes.
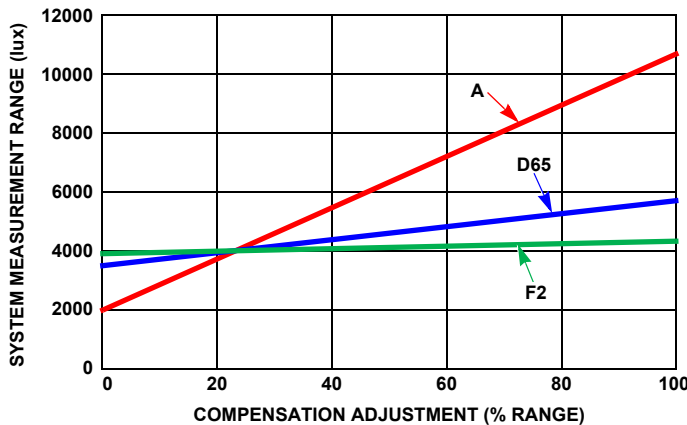
FIGURE 14. IR COMPENSATION VALUE

Calculating Lux

Y-coordinate is Ev measured in lux. The data can be converted to lux by using an equation. There are two different data sensing ranges (375 lux and 10,000 lux) and also two different resolution selections (16 bits and 12 bits) on this device. Equation 2 is dependent on both these parameters.

$$Ev = Y = (CYRxRed + CYGxGreen + CYBxBlue)xRange$$

(EQ. 2)

Noise Rejection

Electrical AC power worldwide is distributed at either 50Hz or 60Hz. Artificial light sources vary in intensity at the AC power frequencies. The undesired interference frequencies are infused on the electrical signals. This variation is one of the main sources of noise for the light sensors. Integrating type ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. By setting the sensor's integration time to an integer multiple of periodic noise signal, the performance of an ambient light sensor can be improved greatly in the presence of noise. In order to reject the AC noise, the integration time of the sensor must be adjusted to match the AC noise cycle. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms ($k = 1, 2...k_i$) is zero. Similarly, setting the device's integration time as an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise.

Layout and Board Mounting Considerations

Suggested PCB Footprint

It is important that users check TB477 "Surface Mount Assembly Guidelines for Optical Dual Flat Pack No Lead (ODFN) Package" before starting ODFN product board mounting.

Board Mounting

For applications requiring the light measurement, the board mounting location should be reviewed. The device uses an Optical Dual Flat Pack No Lead (ODFN) package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location.

Layout

The ISL29125 is relatively insensitive to layout. Similar to other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors, 1µF and 0.1µF, placed close to the device.

Soldering

Convection heating is recommended for reflow soldering; direct infrared heating is not recommended. The plastic ODFN package does not require a custom reflow soldering profile and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

Typical Circuit

A typical application for the ISL29125 is shown in [Figure 15](). The ISL29125's I^{2}C address is internally hard-wired as 1000100. The device can be tied onto a system's I^{2}C bus together with other I^{2}C compliant devices.
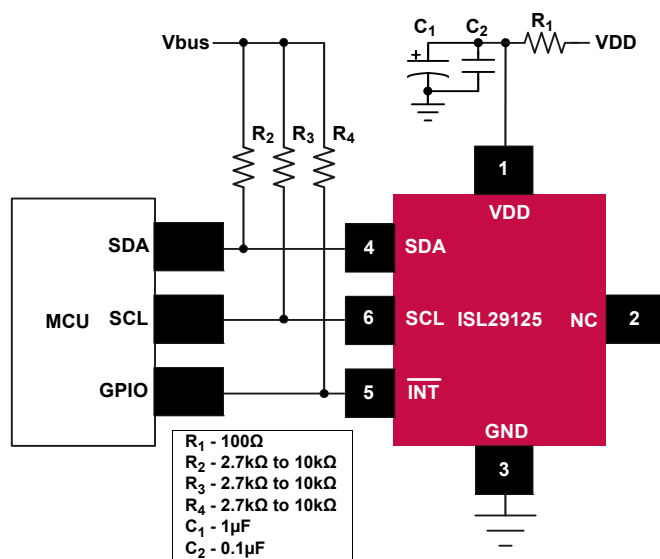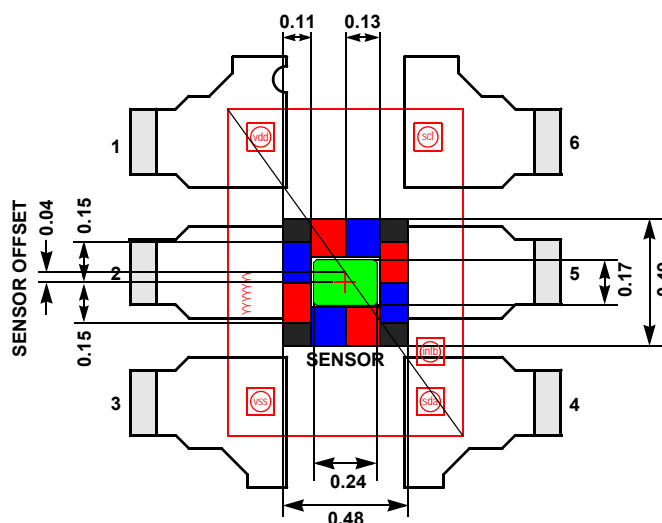

FIGURE 15. ISL29125 TYPICAL CIRCUIT

FIGURE 16. 6 LD ODFN SENSOR LOCATION OUTLINE

References

[1] [Standard illuminants]()

[2] [Planckian locus approximation]()

[3] [CIE 1931 2°, XYZ CMFs modified by Judd (1951) and Vos (1978)]()

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 15, 2016	FN8424.3	Made correction to "Block Diagram" on page 2.
		Page 3 Thermal Information - changed Note 4 from: "θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379." to: "θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details."
		Removed "Digital Inputs and Termination" and "Temperature Coefficient" sections from "Applications Information"
		Updated POD L6.1.65x1.65 from rev 1 to rev 2. Changes since rev 1: Tiebar Note updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
January 24, 2014	FN8424.2	Page 2, Ordering Information table: Changed Evaluation Board part # from: ISL29125IROZ-EVALZ to: ISL29125EVAL1Z Page 9 - added Device Reset row to Tables 1 and 2.
December 23, 2013	FN8424.1	Added Related Literature on page 1. Updated "Interrupt Function" on page 6. Edited last two rows in Table 20 on page 13. Changed RED to BLUE and Register DEC column from 11 and 12 to 13 and 14.
November 20, 2013	FN8424.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L6.1.65x1.65
6 LEAD OPTICAL DUAL FLAT NO-LEAD PLASTIC PACKAGE (ODFN)
Rev 2, 4/15

TOP VIEW

BOTTOM VIEW

TYPICAL RECOMMENDED LAND PATTERN

SIDE VIEW

DETAIL "X"
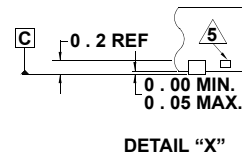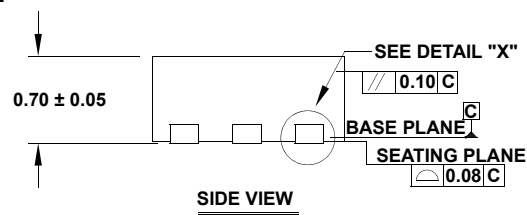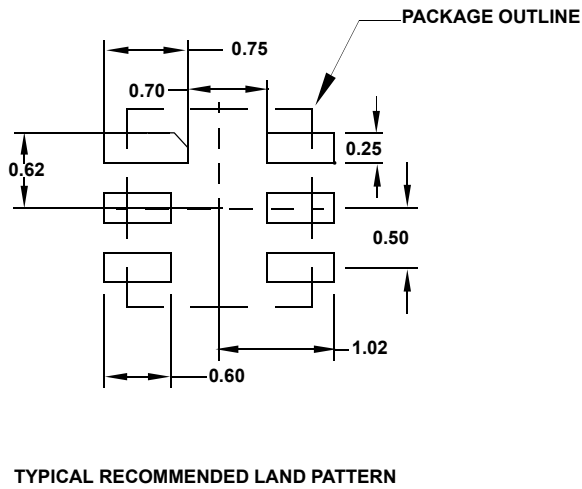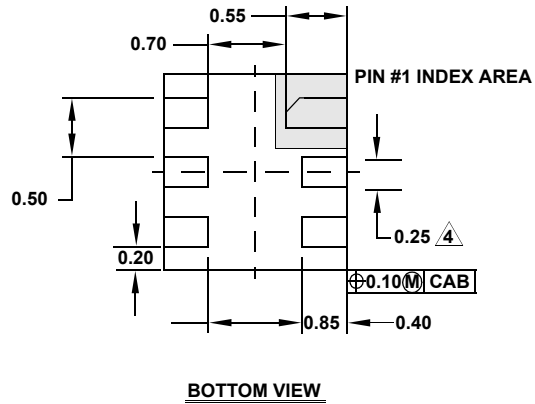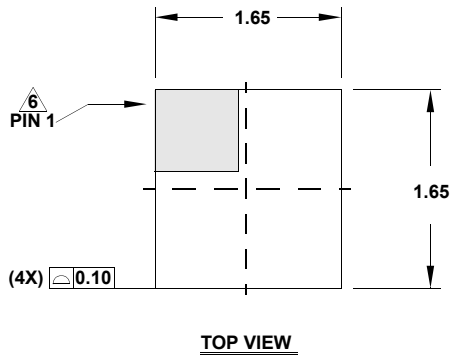
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.