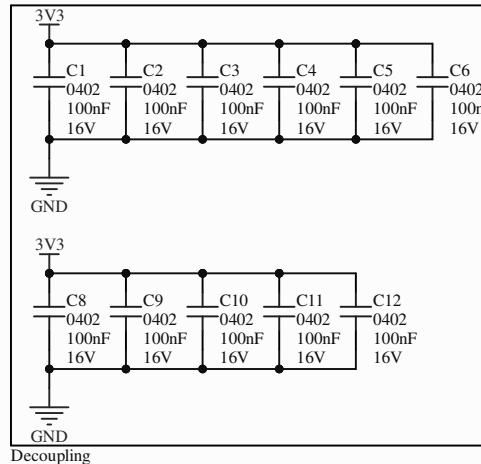
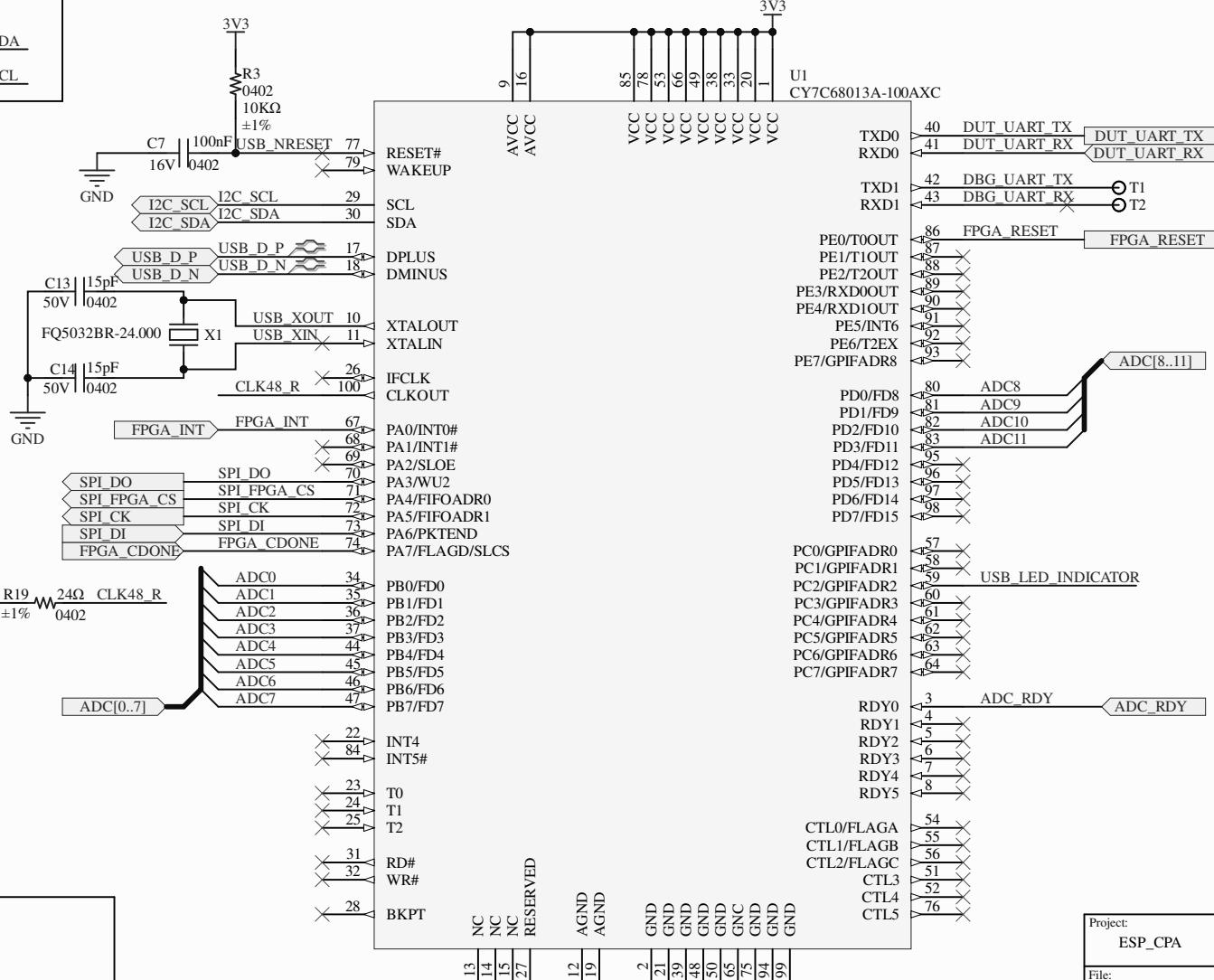
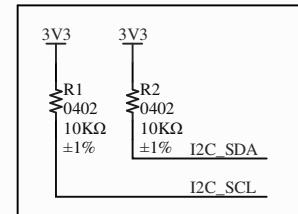


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Project: **ESP_CPA**

File: **EZ-USB.SchDoc**

Size: **A4** Notes:

Date: **26/08/2023** Revision: **2.1**

Sheet: **1** of **6**

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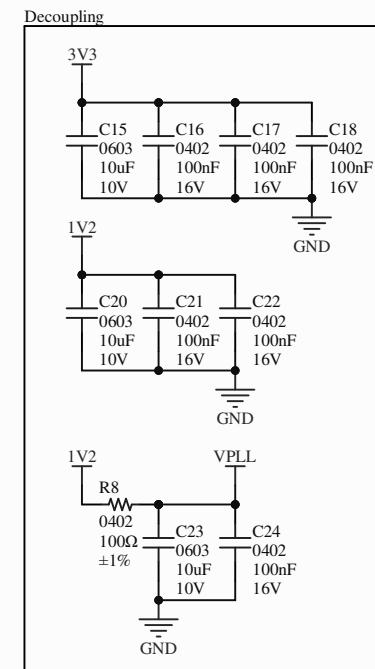
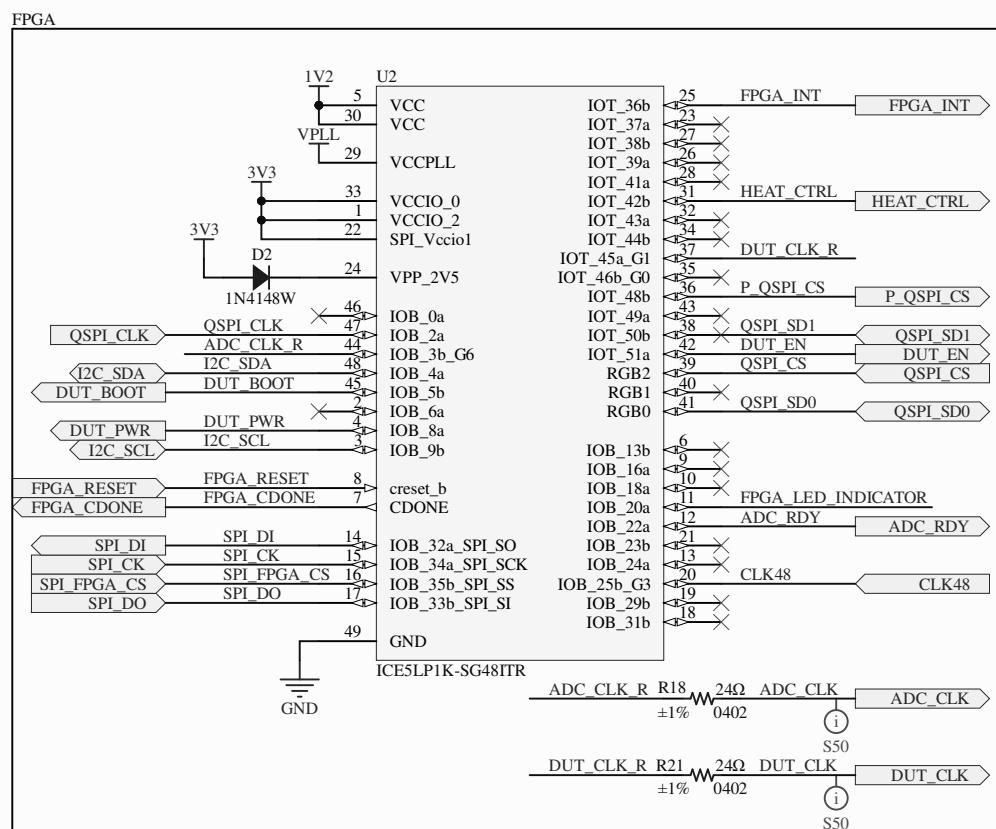
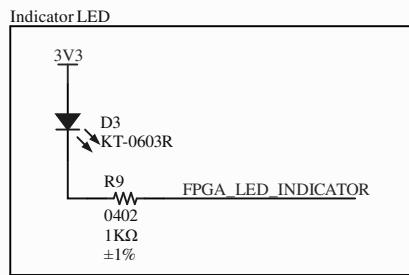
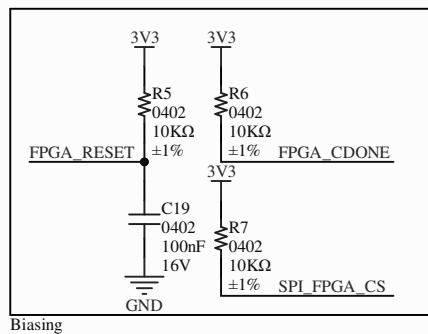
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File: FPGA.SchDoc			
Size: A4	Notes:		Revision: 2.1
Date: 26/08/2023		Sheet: 2	of 6
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A

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B

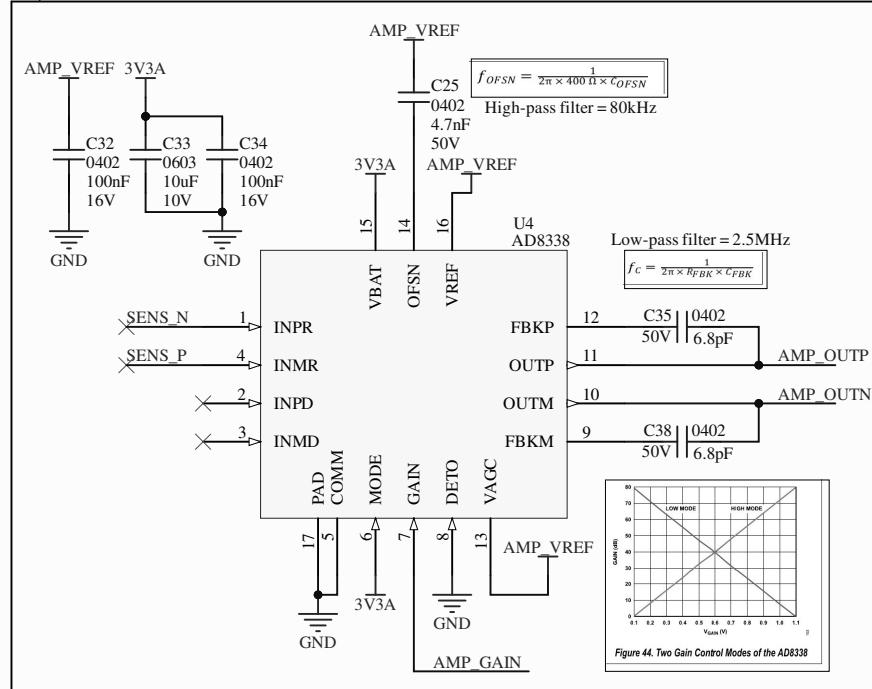
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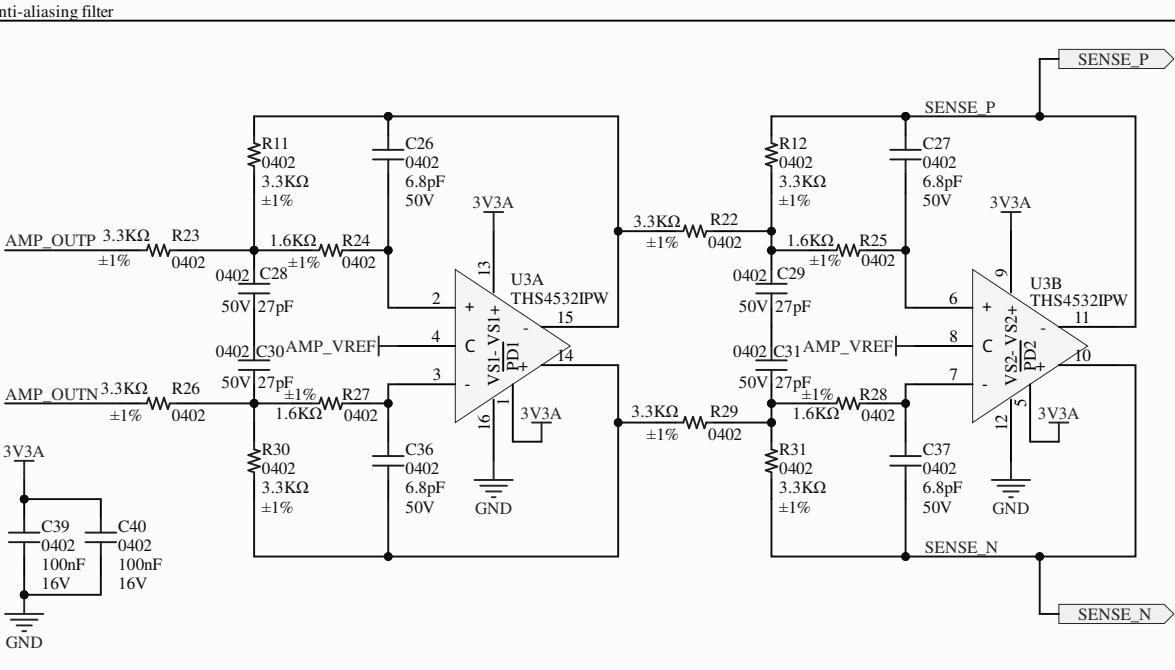
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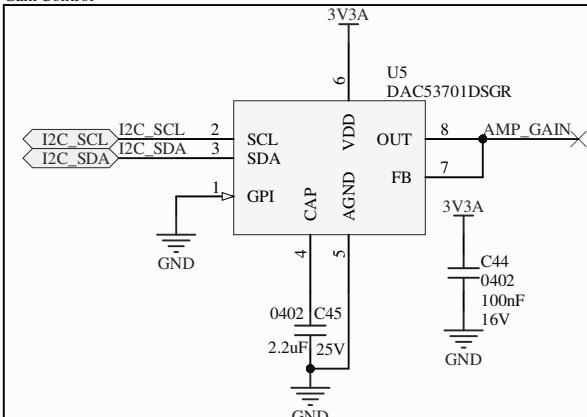
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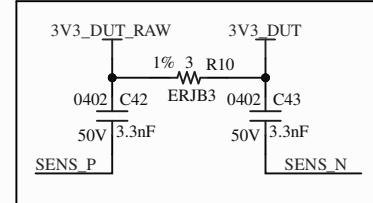
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Gain Control



Current Shunt



Project:
ESP_CPA



File:
CURRENT_SENSE.SchDoc

Size:
A4 Notes:
Revision:
2.1

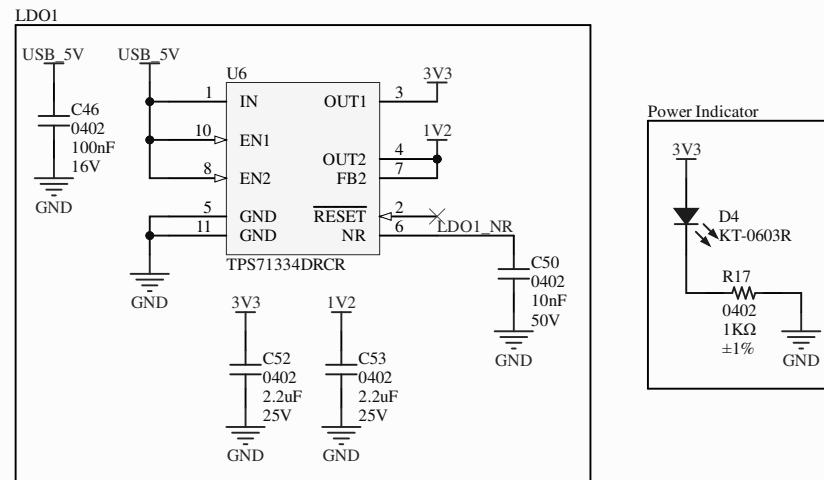
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26/08/2023

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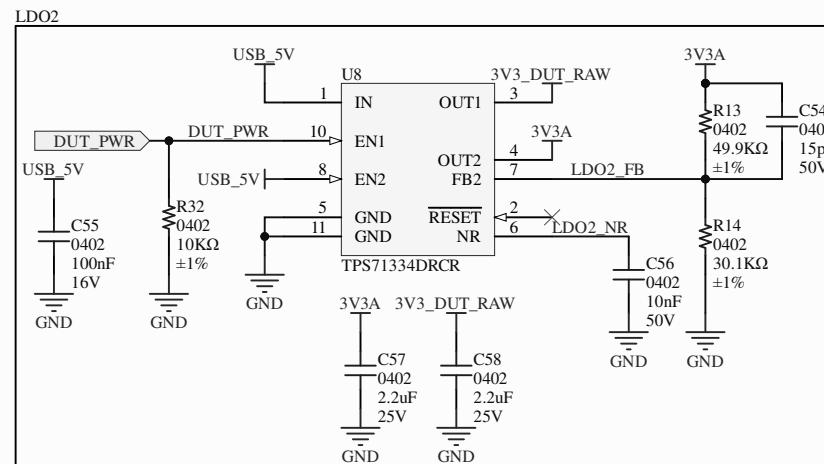
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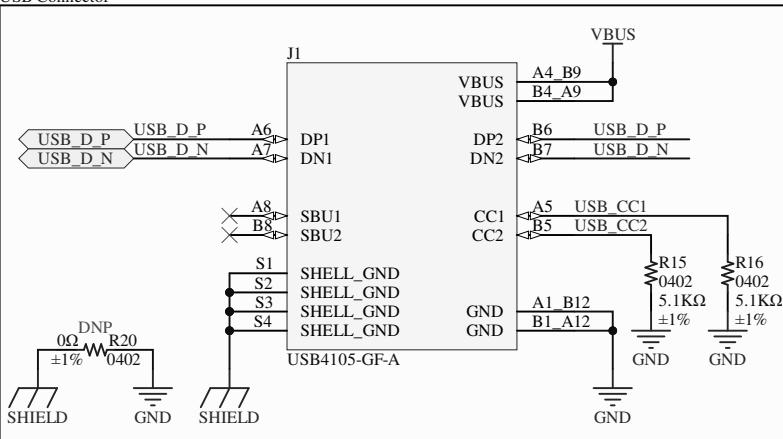


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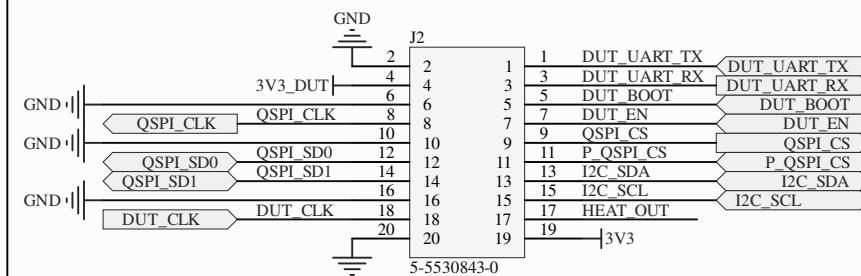
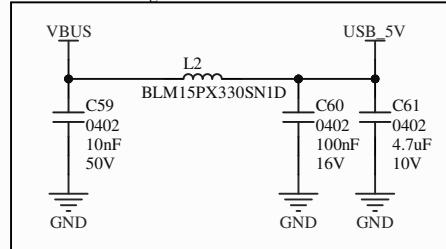
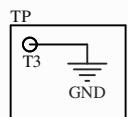
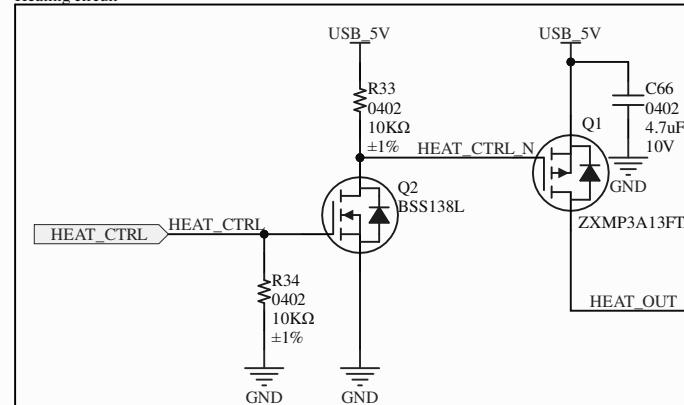


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File: POWER.SchDoc		
Size: A4	Notes:	Revision: 2.1
Date: 26/08/2023	Sheet: 4	of 6
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A
USB Connector

DUT Connector

B
USB VBUS FilteringC
Heating circuit

Project:
ESP_CPA



File:
CONNECTORS.SchDoc

Size:
A4

Notes:
Revision:
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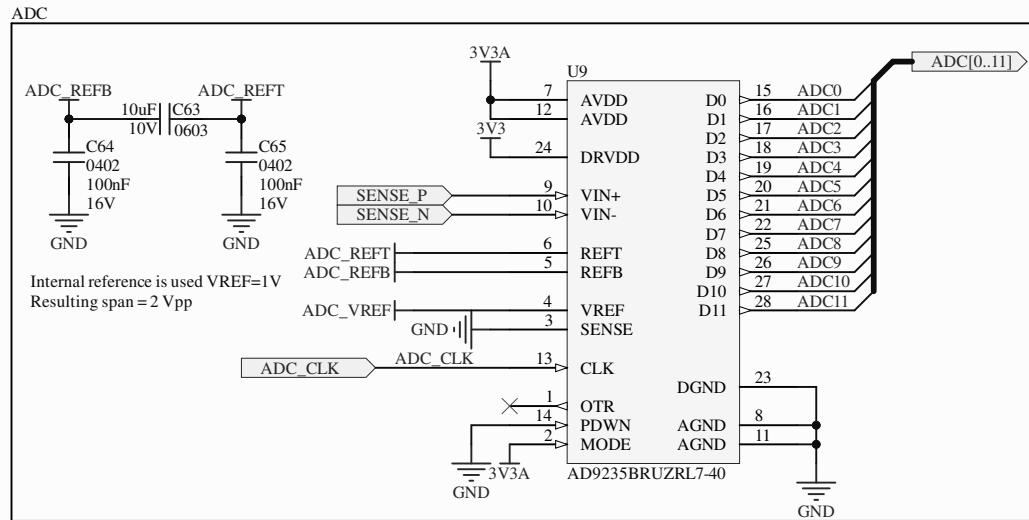
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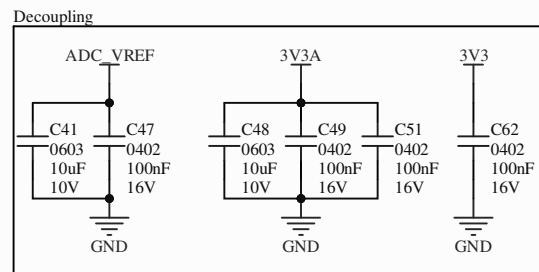
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A



B



C

Project:	ESP_CPA		
File:	ADC.SchDoc		
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