Hands on with FPGA's: Module 4

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Topics

- Pre-class: Open floor for questions
  - Module 3 solutions
- Waveforms
- State Machines:
  - What is a State Machine?
  - Why do we need a State Machine?
- Verilog State Machines
- Brief overview of upcoming tasks
- Open discussion

Review of Module 3

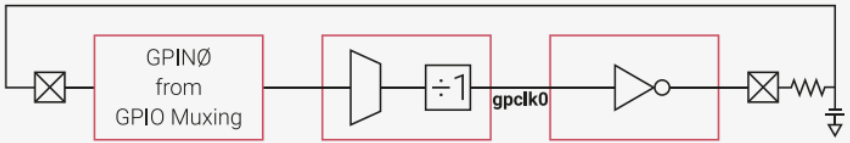
- Counter problem (Solution)
- Oscillator Questions

RP2040 Datasheet Excerpt

2.15.2.4. Relaxation Oscillators

If the user wants to use external clocks to replace or supplement the other clock sources but does not have an appropriate clock available, then 1 or 2 relaxation oscillators can be constructed using external passive components. Simply send the clock source (GPIN0 or GPIN1) to one of the gpclk0-3 generators, invert it through the GPIO inverter OUTOVER and connect back to the clock source input via an RC circuit.

Figure 29. Simple relaxation oscillator example



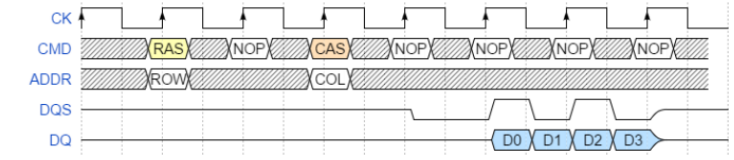
Documentation: Waveforms

- Digital circuits are documented using waveforms
- Can show interaction of multiple blocks
- Good tool to learn: Wavedrom
  - Text based, open source

The following source code describes a DDR DRAM access:

```
{ signal: [
  { name: "CK",   wave: "P.......",      period: 2  },
  { name: "CMD",  wave: "x.3x=x4x=x=x=x=x",
    data: "RAS NOP CAS NOP NOP NOP NOP", phase: 0.5 },
  { name: "ADDR", wave: "x.=x..=x........",
   data: "ROW COL",                     phase: 0.5 },
  { name: "DQS",  wave: "z.......0.1010z." },
  { name: "DQ",   wave: "z.........5555z.",
   data: "D0 D1 D2 D3" }
]}
```

Below is the rendered waveform.



State Machines: Practical uses

- RP2040 PIO peripheral

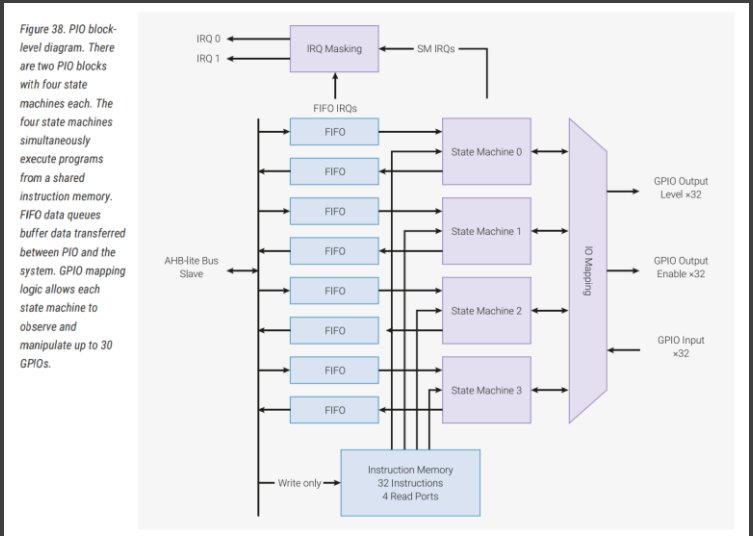


Figure 38. PIO block-level diagram. There are two PIO blocks with four state machines each. The four state machines simultaneously execute programs from a shared instruction memory. FIFO data queues buffer data transferred between PIO and the system. GPIO mapping logic allows each state machine to observe and manipulate up to 30 GPIOs.

State Machines

- SunBurst Design Paper
- Moore vs Mealy
  - Mealy outputs depend on inputs
  - Moore outputs only depend on current state
- Do not use Mealy unless necessary
  - Usually lowers max clock rate

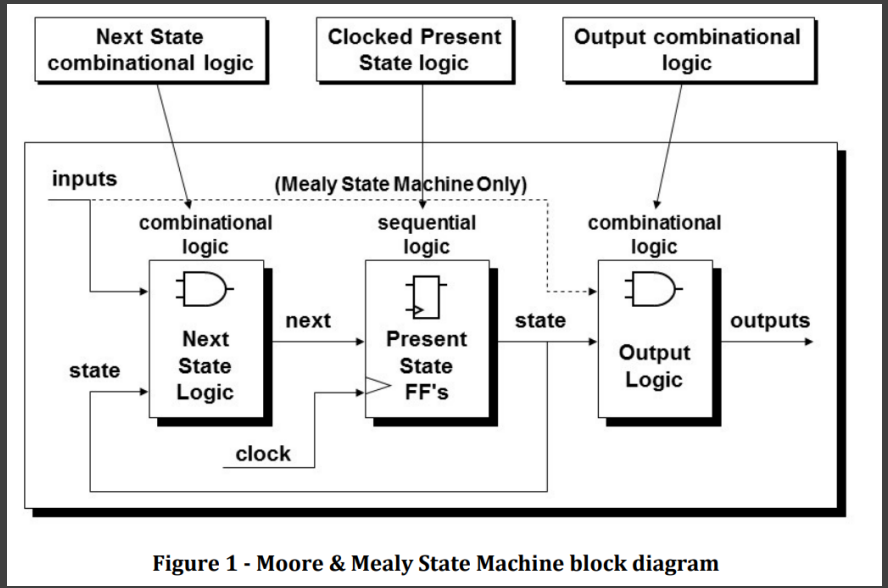


Figure 1 - Moore & Mealy State Machine block diagram

State Encoding

- One-hot vs. Binary vs. others
  - Preference: One-hot for FPGA's, Binary for ASIC
  - Other encoding schemes for error resistance/tolerance. E.g. space, military

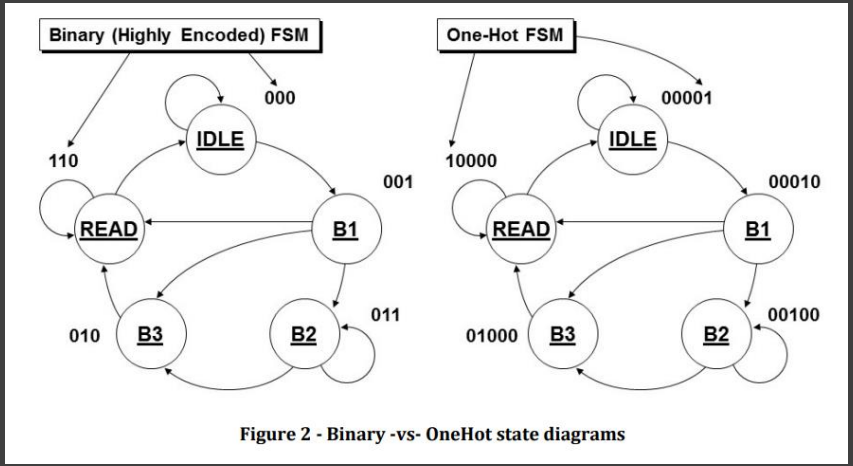


Figure 2 - Binary -vs- OneHot state diagrams

Verilog Coding Style for FSM's: 2 always blocks

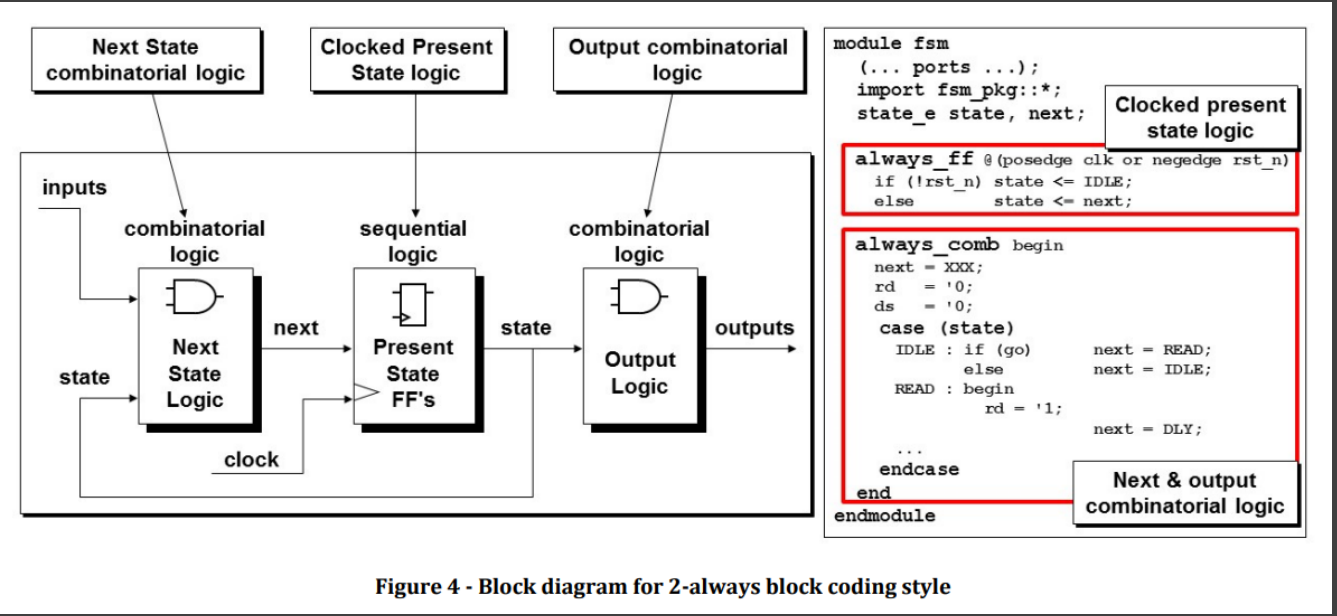


Figure 4 - Block diagram for 2-always block coding style

Verilog Coding Style for FSM's: 3 always blocks

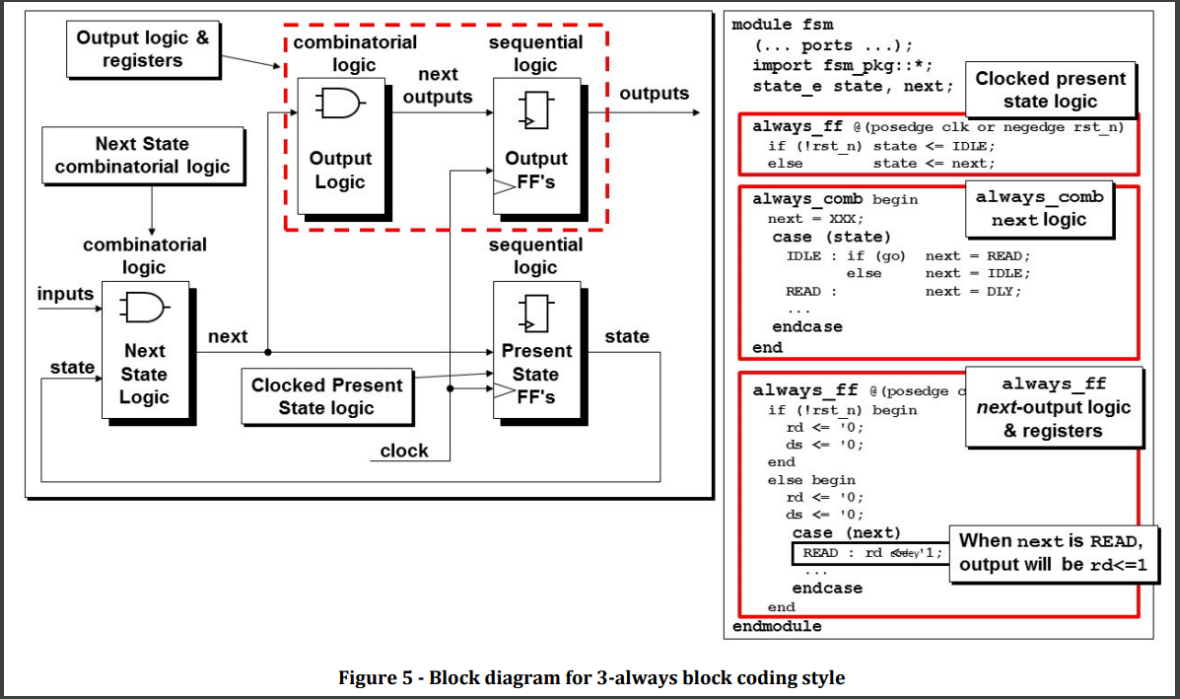
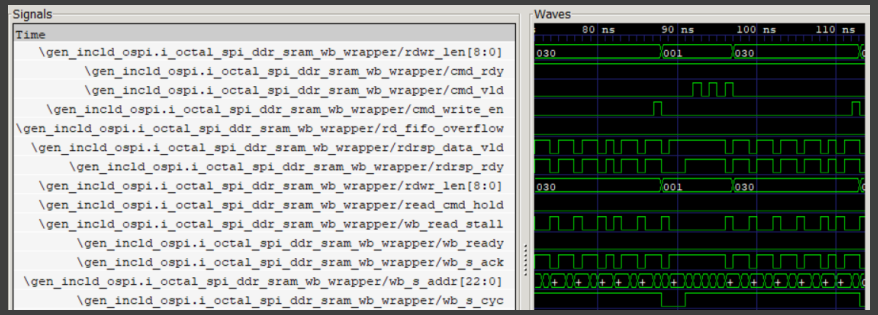


Figure 5 - Block diagram for 3-always block coding style

Verilog Deep Dive

- EDA Playground
  - Default FSM Example
    - No reset!
    - Poor readability, tough to debug
  - "Fixed" FSM Example
    - Added reset
    - Much more readable
    - Trap state for unknowns
- GTKWave
  - Open source waveform viewer
  - Critical tool for HW debug during simulations



Module 4: State Machines

- Tasks
  - Read the Sunburst design paper on state machines
  - Understand the various coding styles
  - Try it out!
- Challenge
  - Code up a state machine for a traffic light

Open Discussion