Hands on with FPGA's: Module 2

Venkat Rangan

Topics

- Pre-class: Open floor for questions
- Prof Pateros: Intro to Digital Logic
- Intro to Verilog/Simulations
- Open discussion

Intro to Digital Design

- HW frame of mind (fully parallel interacting blocks) vs SW (Sequential)
  - Think of communication between parallel HW as “wires”
  - Wires are uni-directional!

- Simulation of logic using verilator/verilog testbenches:
  - VHDL vs. Verilog vs System Verilog: Focus on System Verilog
  - SystemVerilog or Verilator for testbenches
  - More specialized testbench environments like UVM, cocotb

- Good Design Practice. See FPGA Hell.
  1. Follow good coding style for all your code. This helps avoid common mistakes.
  2. Make `` `default_nettype none `` the first line of your Verilog file
  3. Lint design: Use “`verilator -Wall`”
  4. Always simulate your design
  5. Then run synthesis, fix errors if any
  6. Whew! Ready to try things on a real board

Module 2: Logic Design and Simulations

- Challenge: Bitwidth analysis
  - Get a feel for how binary math works
  - Use any tool for this: SystemVerilog, Calculator

Open Discussion