EECS 112L/CSE 132L

Assignment 2 Deliverable

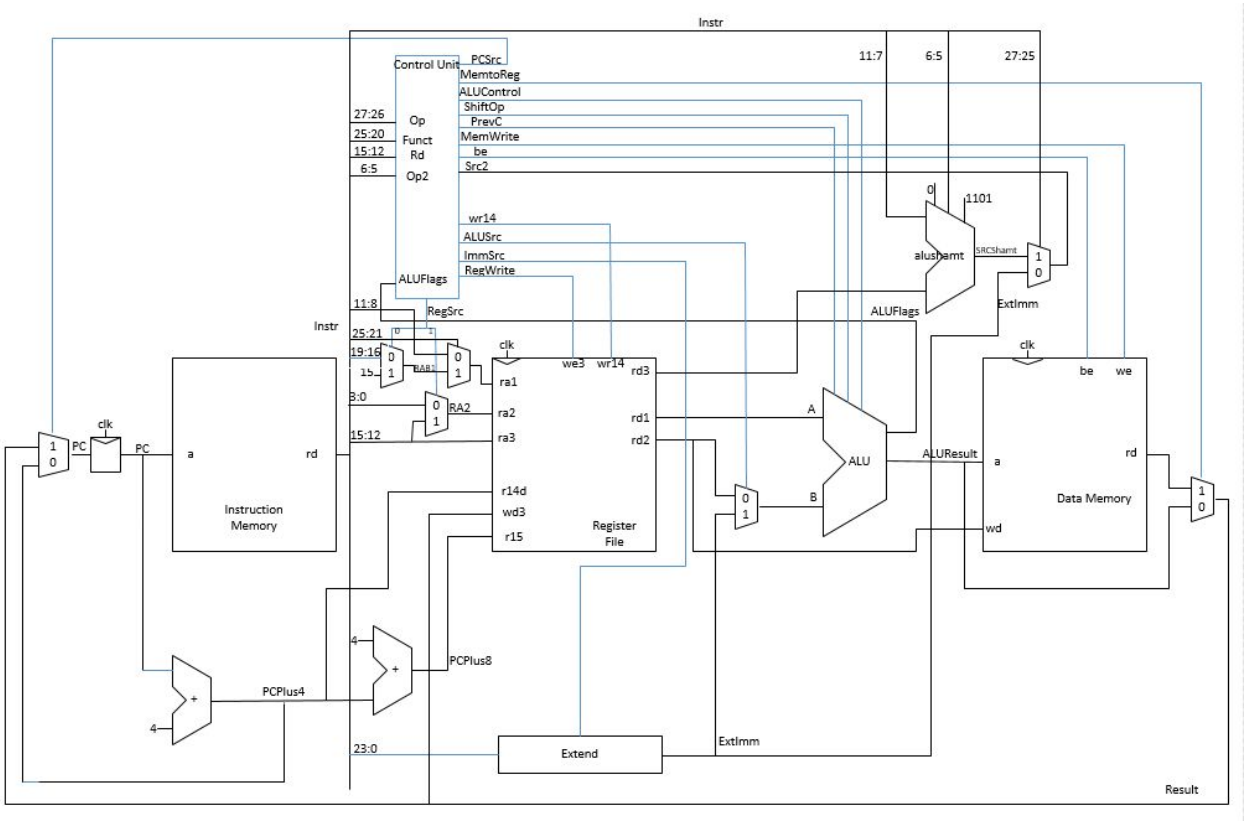
Single-cycle ARM Datapath and Control - Complete

Group ID: Kikei

Submission Date: 2/28/2017

Prepared by:
Jeffrey Han, 51999492
Aaron Liao, 90811748
Bryan Ou, 11074596
Kelvin Phan, 51197373

Block Diagram of Processor Design:



For our block design in this lab, we built upon what the last lab provided. One of the key differences in this design is that ALUControl was increased from two-bit to four-bit to accommodate for the increased amount of instructions. In addition, for these data-processing instructions we have added a new wire named ShiftOp, which determines which shift operation to perform. To perform these shift operations, we have included a new ALU with its own inputs and outputs, called alushamt. To handle memory operations, a new wire called be was added, to indicate byte enable. This is connected to an edited data memory which now consists of 4 arrays of 8x512 and is word-aligned. For the branch-link instruction, wire wr14 is used to indicate the register file to put PCPlus4 into R14. To perform this, we connected PCPlus4 from the first adder to the register file.

Design and TestBench Architecture:

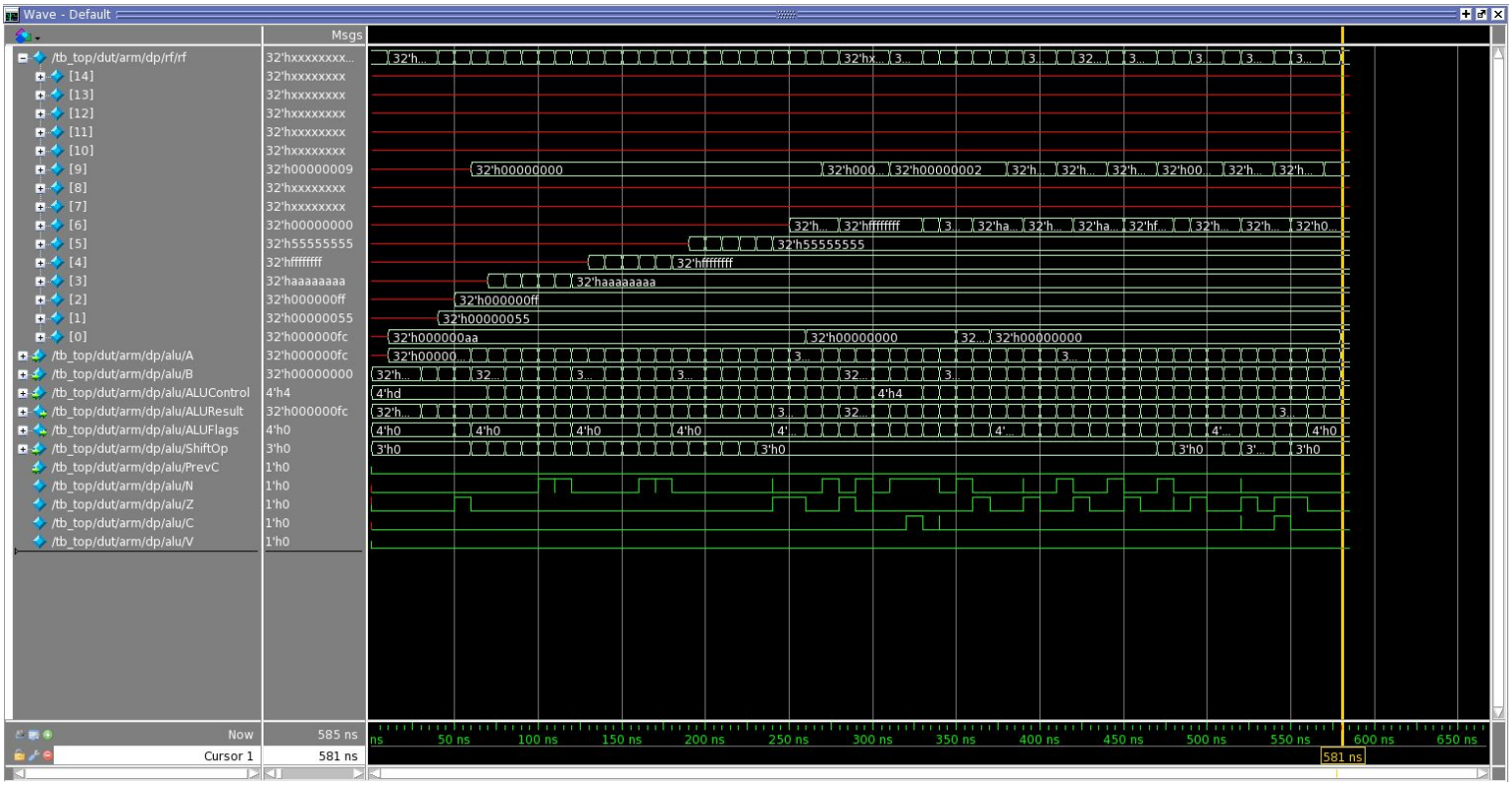
➔ ALU Test 1 (ALU_test_disassembly.txt):

- MobaXterm console with final register values **(R9 = 9 out of 9)**:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 19:08:07 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCIA
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECTI
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UND
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 000000fc
# 1 00000055
# 2 000000ff
# 3 aaaaaaaa
# 4 ffffffff
# 5 55555555
# 6 00000000
# 7 xxxxxxxx
# 8 xxxxxxxx
# 9 00000009
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 xxxxxxxx
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 19:08:08 on Feb 28,2017, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
zuma%
obaXterm by subscribing to the professional edition here:
```

- Questa Sim Results (9 out of 9 for Pass Counter in R9):



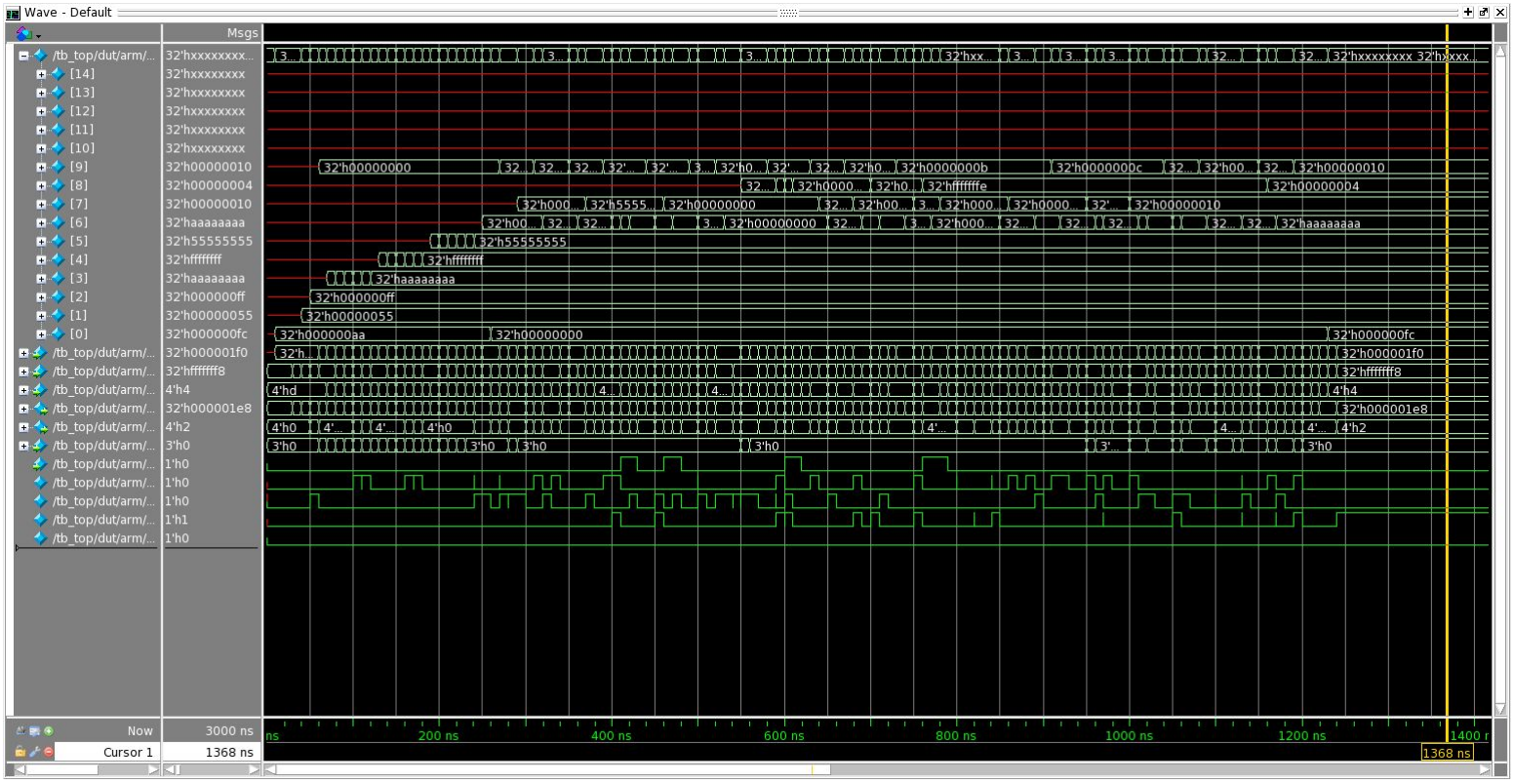
➔ **ALU Test 2 (ALU_test.s):**

- MobaXterm console with final register values **(R9 = 10 out of 10)**:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 19:23:54 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCI
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECT
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UN
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 000000fc
# 1 00000055
# 2 000000ff
# 3 aaaaaaaa
# 4 ffffffff
# 5 55555555
# 6 aaaaaaaa
# 7 00000010
# 8 00000004
# 9 00000010
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 xxxxxxxx
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 19:23:55 on Feb 28,2017, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
zuma%
obaXterm by subscribing to the professional edition here:
```

- Questa Sim Results (10 out of 10 for Pass Counter in R9):



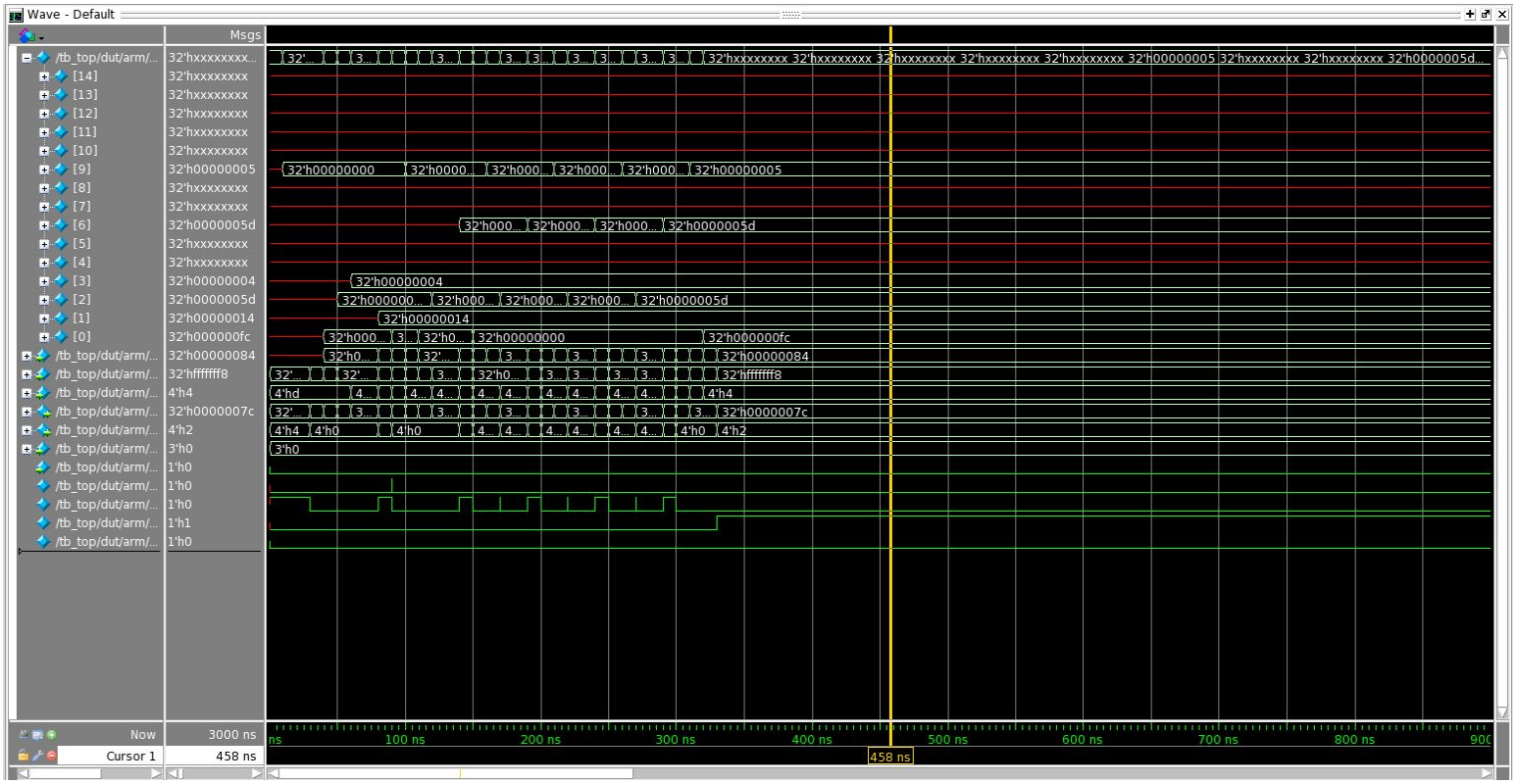
➔ **LDR-STR Test (ldr-str_test_disassembly.txt):**

- MobaXterm console with final register values **(R9 = 5 out of 5)**:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 19:54:04 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANC
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FRO
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SEC
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE U
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 000000fc
# 1 00000014
# 2 0000005d
# 3 00000004
# 4 xxxxxxxx
# 5 xxxxxxxx
# 6 0000005d
# 7 xxxxxxxx
# 8 xxxxxxxx
# 9 00000005
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 xxxxxxxx
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 19:54:05 on Feb 28,2017, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
zuma%
obaXterm by subscribing to the professional edition here:
```

- Questa Sim Results (5 out of 5 for Pass Counter in R9):



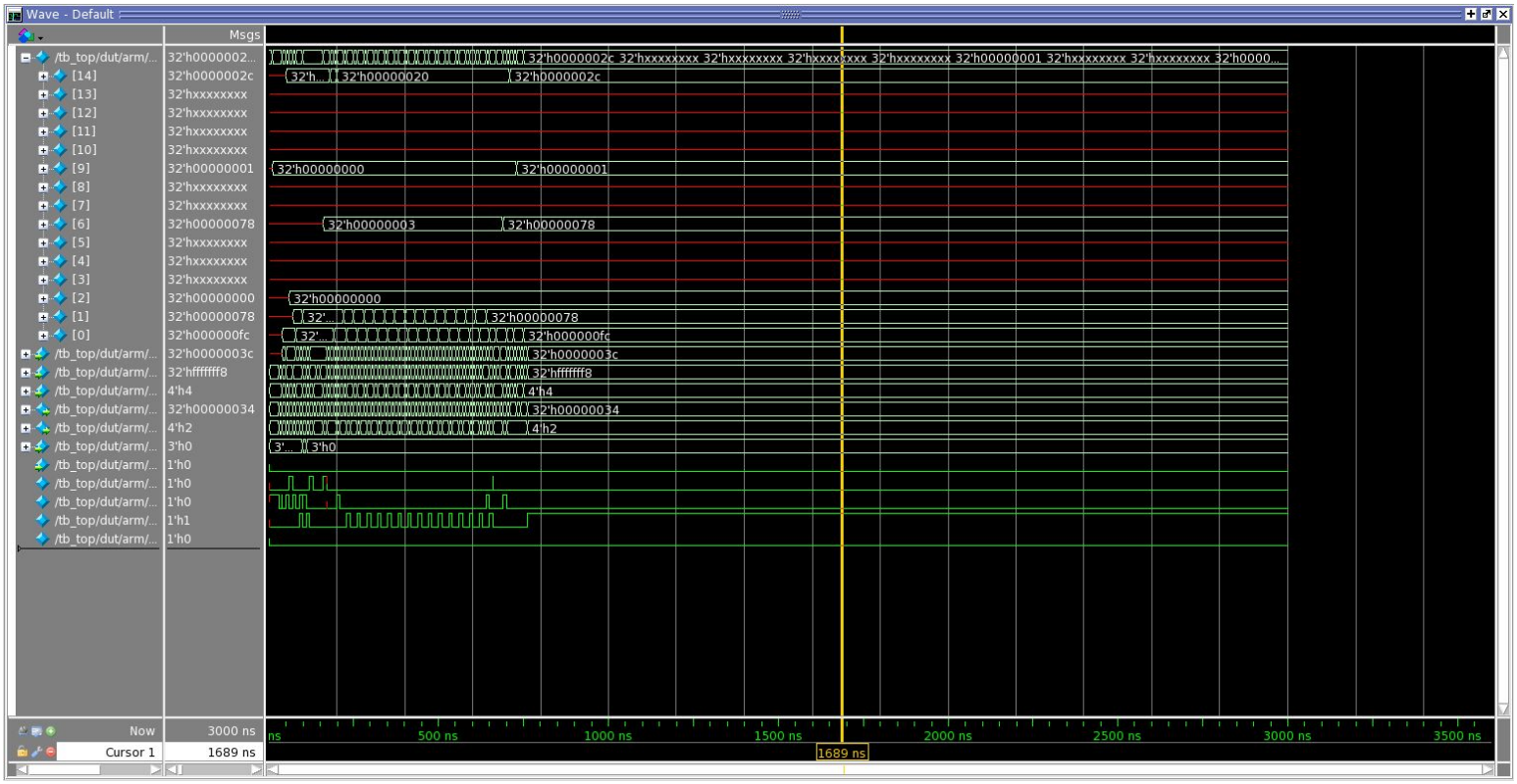
➔ **Regression Test (Regression_disassembly.txt):**

- MobaXterm console with final register values **(R9 = 1 out of 2)**:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 20:08:51 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCI
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECT
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UN
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 000000fc
# 1 00000078
# 2 00000000
# 3 xxxxxxxx
# 4 xxxxxxxx
# 5 xxxxxxxx
# 6 00000078
# 7 xxxxxxxx
# 8 xxxxxxxx
# 9 00000001
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 0000002c
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 20:08:51 on Feb 28,2017, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
zuma%
obaXterm by subscribing to the professional edition here:
```

- Questa Sim Results (1 out of 2 for Pass Counter in R9):



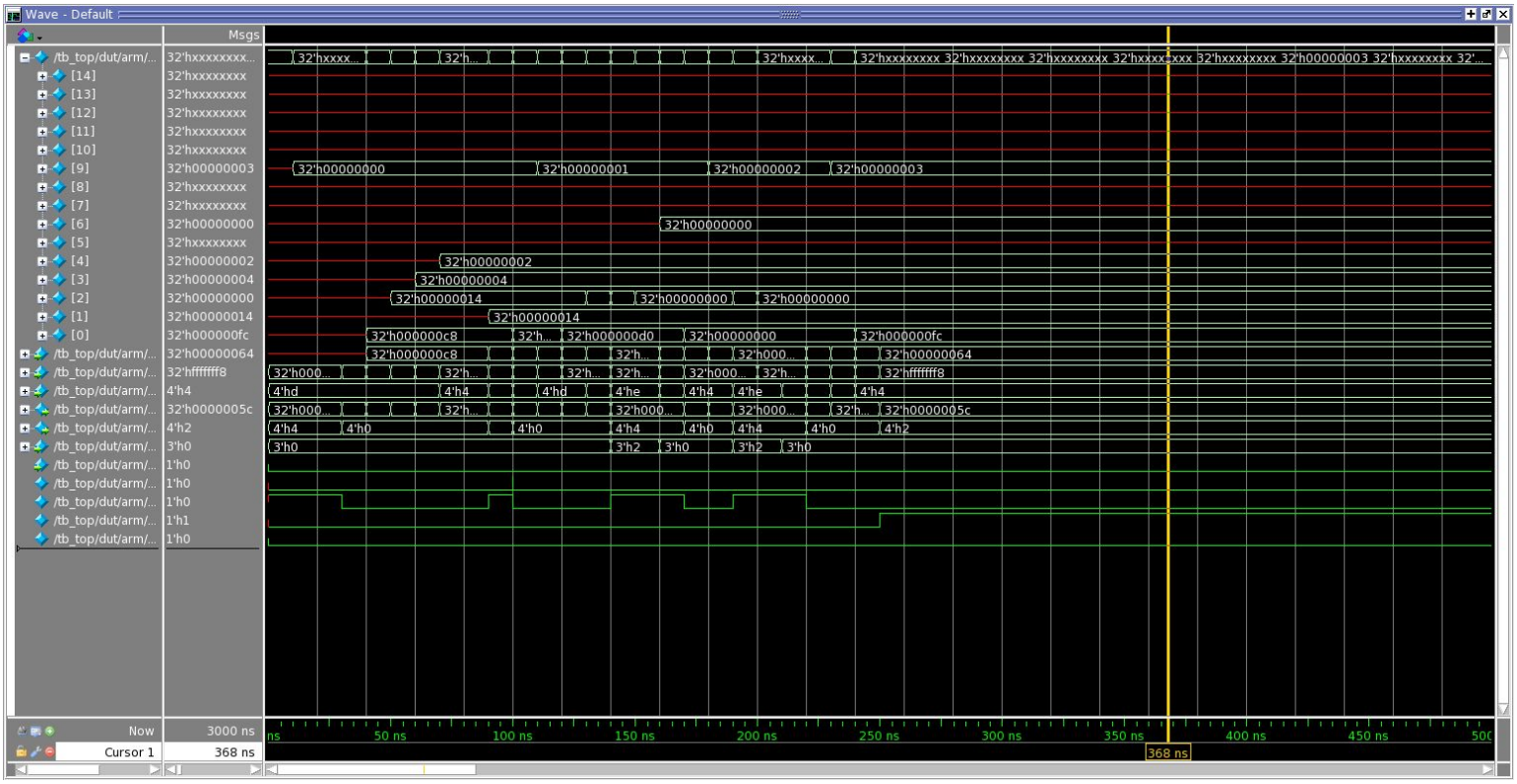
➔ **Bonus Credit Test (Bonus_credit_disassembly.txt):**

- MobaXterm console with final register values **(R9 = 3 out of 3)**:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 20:25:34 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCI
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECT
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UN
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 000000fc
# 1 00000014
# 2 00000000
# 3 00000004
# 4 00000002
# 5 xxxxxxxx
# 6 00000000
# 7 xxxxxxxx
# 8 xxxxxxxx
# 9 00000003
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 xxxxxxxx
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 20:25:35 on Feb 28,2017, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
zuma%
obaXterm by subscribing to the professional edition here: http://mobaxterm.mobatek.net
```

- Questa Sim Results (3 out of 3 for Pass Counter in R9):



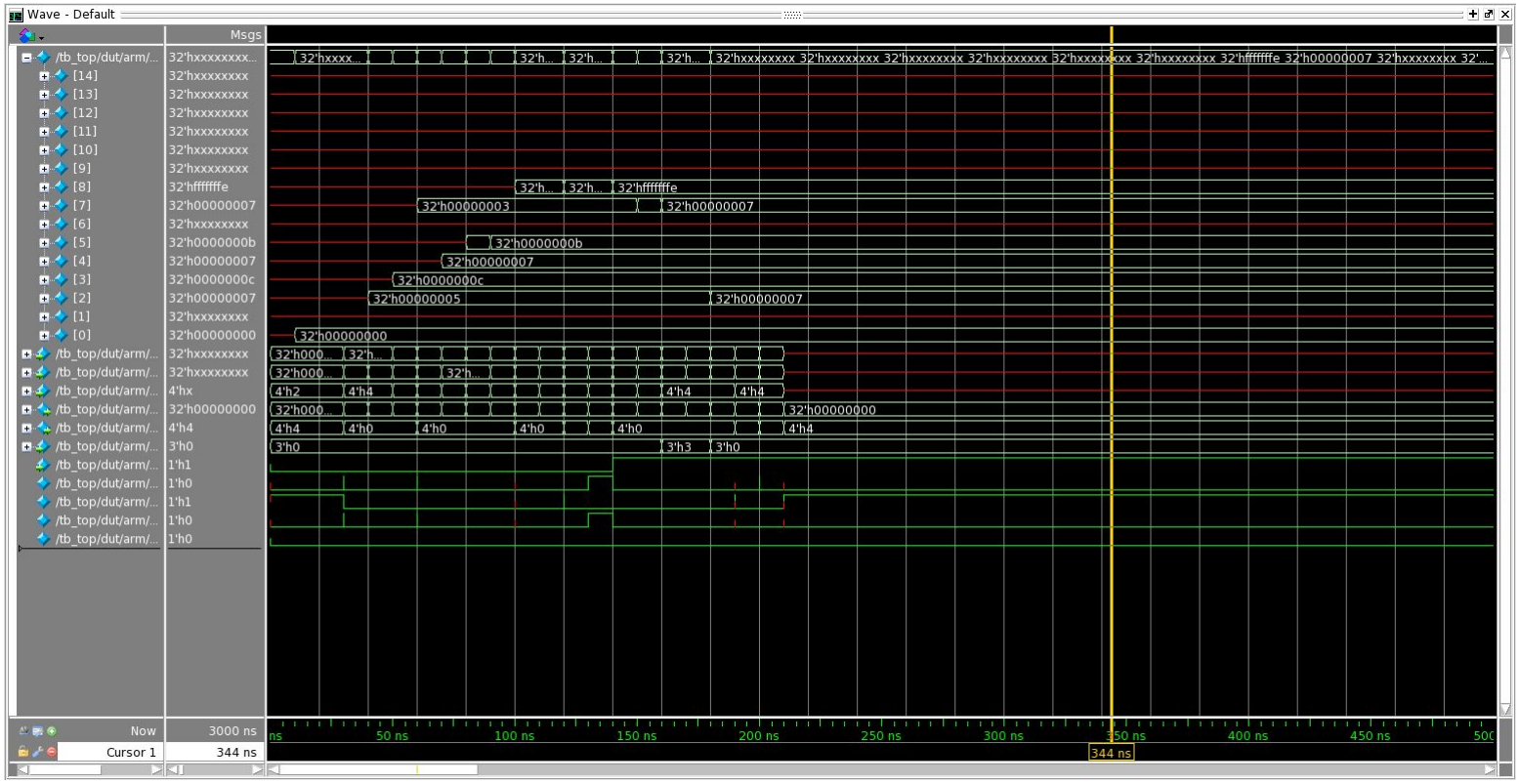
Simulated Results (with Sample Program, Figure 7.60):

➔ MobaXterm console with final register values:

```
2. zuma.eecs.uci.edu (oub)
# vsim -c tb_top_opt -do "sim/sim.do"
# Start time: 20:53:35 on Feb 28,2017
# //  Questa Sim-64
# //  Version 10.4c linux_x86_64 Jul 19 2015
# //
# //  Copyright 1991-2015 Mentor Graphics Corporation
# //  All Rights Reserved.
# //
# //  THIS WORK CONTAINS TRADE SECRET AND PROPRIETARY INFORMATION
# //  WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION OR ITS
# //  LICENSORS AND IS SUBJECT TO LICENSE TERMS.
# //  THIS DOCUMENT CONTAINS TRADE SECRETS AND COMMERCIAL OR FINANCI
# //  INFORMATION THAT ARE PRIVILEGED, CONFIDENTIAL, AND EXEMPT FROM
# //  DISCLOSURE UNDER THE FREEDOM OF INFORMATION ACT, 5 U.S.C. SECT
# //  FURTHERMORE, THIS INFORMATION IS PROHIBITED FROM DISCLOSURE UN
# //  THE TRADE SECRETS ACT, 18 U.S.C. SECTION 1905.
# //
# Loading sv_std.std
# Loading work.tb_top(fast)
# Loading work.top(fast)
# Loading work.arm(fast)
# Loading work.controller(fast)
# Loading work.decoder(fast)
# Loading work.condlogic(fast)
# Loading work.flopenr(fast)
# Loading work.condcheck(fast)
# Loading work.datapath(fast)
# Loading work.mux2(fast)
# Loading work.flopr(fast)
# Loading work.adder(fast)
# Loading work.mux2(fast__1)
# Loading work.regfile(fast)
# Loading work.extend(fast)
# Loading work.alu(fast)
# Loading work.imem(fast)
# Loading work.dmem(fast)
```

```
# do sim/sim.do
# waveform.wlf
# 0 00000000
# 1 xxxxxxxx
# 2 00000007
# 3 0000000c
# 4 00000007
# 5 0000000b
# 6 xxxxxxxx
# 7 00000007
# 8 fffffffe
# 9 xxxxxxxx
# 10 xxxxxxxx
# 11 xxxxxxxx
# 12 xxxxxxxx
# 13 xxxxxxxx
# 14 xxxxxxxx
# 15 xxxxxxxx
# ** Note: $finish    : /users/ugrad2/2015/spring/oub/EECS_112L/Lab2/verif/tb_top.sv(33)
#    Time: 3 us  Iteration: 1  Instance: /tb_top
# End time: 20:53:36 on Feb 28,2017, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
zuma%
MobaXterm by subscribing to the professional edition here: http://mobaxterm.mobatek.net
```

➔ Questa Sim Results:



Simulation Analysis:

- We can verify the functionality of of our processors design by comparing the waveforms we acquired with the given testbench values (Figure 7.60).
- From the testbench, R0 = 0, R2 = 5, R3 = 12, R7 = 3, R4 = 7, and R5 = 4 for initial values.
- Chronologically:
    - R5 changes to 11, which can be seen in Figure 1 at 100ns.
    - R8 is then set to 8, and since R8 changes to 5 at 120ns, it is apparent that the BEQ instruction was skipped.
    - The next branch to the “around” label is taken, as the value in R5 does not change.
    - In Figure 2, R7 changes to 12, then subsequently 7 at 150ns.
    - To verify LDR and STR, mem[96] is set to 7, and the value in R2 is then set equal to mem[96], resulting in R2 = 7.
    - R2 remains unchanged through the rest of the waveform, as the branch instruction to the “end” label is taken, skipping further ADD instructions.
- End register value results:
    - R0 = 0
    - R2 = 7
    - R3 = C = 12
    - R4 = 7
    - R5 = B = 11
    - R7 = 7
    - R8 = -2
- For most of the simulation our design performed the successfully. In all but the regression test, we had values within R9 that indicated out tests performed as expected. The only instance where this did not occur was in the regression test, notably the segment labeled “log”. In regression, we only had 1 out of 2 successful tests.

Synthesization Results/Analysis:

➔ MobaXterm console with Area, Timing, and Power results:

```
****************************************
Report : qor
Design : arm
Version: J-2014.09-SP4
Date   : Tue Feb 28 21:16:50 2017
****************************************


  Timing Path Group (none)
  -----------------------------------
  Levels of Logic:               43.00
  Critical Path Length:           2.64
  Critical Path Slack:          uninit
  Critical Path Clk Period:       2.00
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           8
  Hierarchical Port Count:         676
  Leaf Cell Count:                2399
  Buf/Inv Cell Count:              443
  Buf Cell Count:                    9
  Inv Cell Count:                  434
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:       2399
  Sequential Cell Count:             0
  Macro Count:                       0
  -----------------------------------
```

```
Area
-----------------------------------
Combinational Area:     5024.681049
Noncombinational Area:     0.000000
Buf/Inv Area:            577.415170
Total Buffer Area:            22.87
Total Inverter Area:         554.54
Macro/Black Box Area:      0.000000
Net Area:               1712.703257
-----------------------------------
Cell Area:              5024.681049
Design Area:            6737.384306


Design Rules
-----------------------------------
Total Number of Nets:          3007
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
-----------------------------------


Hostname: zuma.eecs.uci.edu

Compile CPU Statistics
---------------------------------------
Resource Sharing:                  4.12
Logic Optimization:                1.21
Mapping Optimization:              6.53
---------------------------------------
Overall Compile Time:             44.07
Overall Compile Wall Clock Time:  55.56

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

--------------------------------------------------------------------
```

```
46  ---------------------------------------------------------------------------------------
47                                          Switch   Int      Leak     Total
48  Hierarchy                               Power    Power    Power    Power    %
49  ---------------------------------------------------------------------------------------
50  arm                                      133.489  211.979 2.77e+09 3.12e+03 100.0
51    dp (datapath)                          133.068  208.697 2.75e+09 3.09e+03  99.1
52      alu (alu_1)                          122.799  191.221 2.47e+09 2.79e+03  89.4
53      alushamt (alu_0)                       4.096    8.354 8.45e+07   96.947   3.1
54      pcadd2 (adder_WIDTH32_1)                 N/A    2.818 7.23e+07   74.763   2.4
55      pcadd1 (adder_WIDTH32_0)               2.667    2.508 7.23e+07   77.495   2.5
56    c (controller)                           6.735    3.282 2.42e+07   34.203   1.1
57      cl (condlogic)                         2.003    3.282 2.42e+07   29.471   0.9
58        cc (condcheck)                       1.737    2.718 1.71e+07   21.587   0.7
59  1
```

➔ Final Results:

- Area (Design): 6737.3843
- Power (ARM Total): 3.12e3
- Frequency: 1.0 GHz