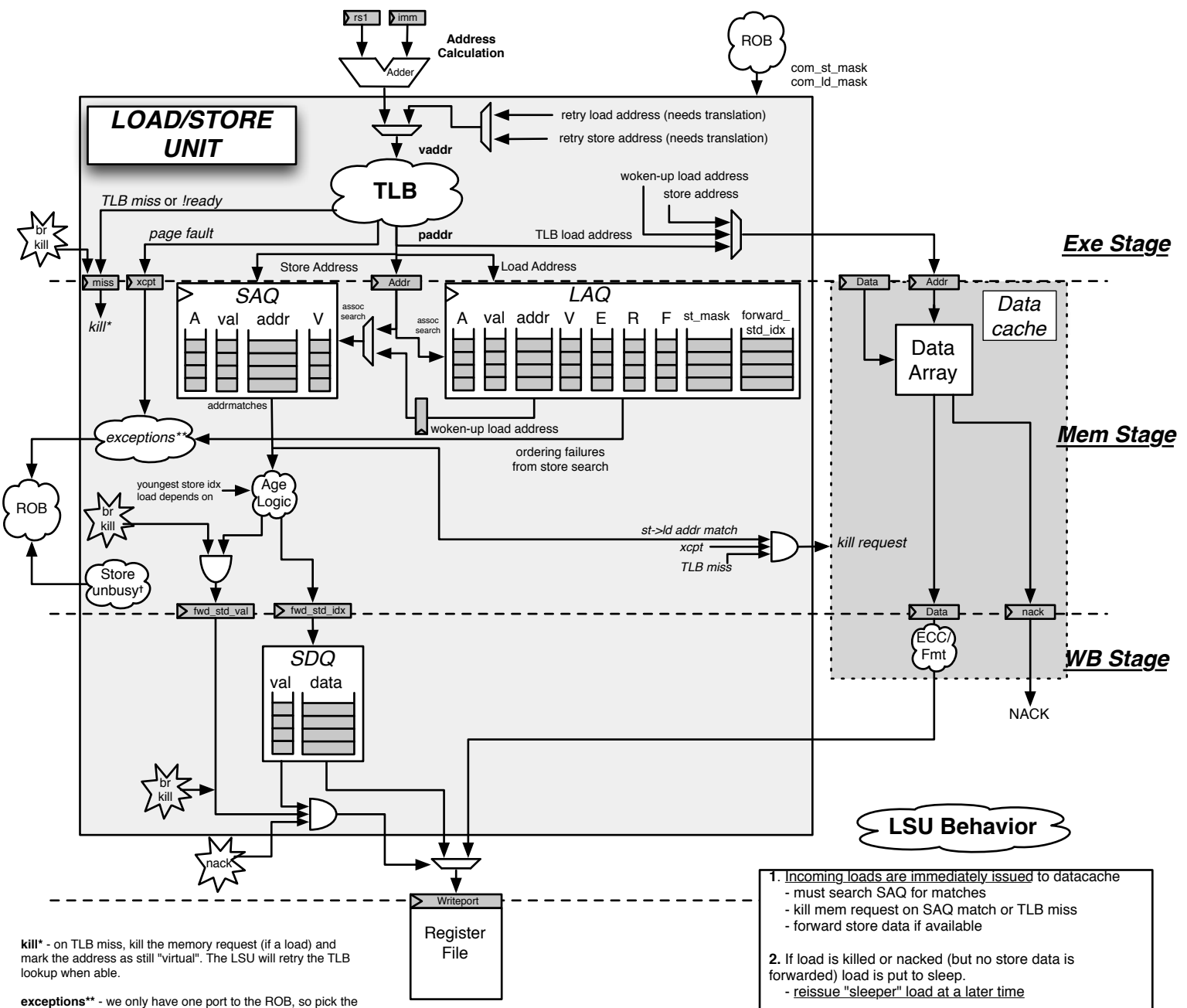

kill* - on TLB miss, kill the memory request (if a load) and mark the address as still "virtual". The LSU will retry the TLB lookup when able.

exceptions** - we only have one port to the ROB, so pick the oldest excepting instruction

store unbusy† - when a store-address enters the SAQ or a store-data enters the SDQ it checks if the other store half is present and if so, tells the ROB to unbusy the store.

LAQ information

address **val**id
entry **a**llocated
address is **v**irtual (translation retry required)
load **e**xecuted (sent to mem)
load **r**equesting wakeup
load **f**ailed (detected mem ordering failure)
bit **mask** of dependee stores
index of store the load got its data from (if any)

LSU Behavior

1. Incoming loads are immediately issued to datacache
- must search SAQ for matches
- kill mem request on SAQ match or TLB miss
- forward store data if available

2. If load is killed or nacked (but no store data is forwarded) load is put to sleep.
- reissue "sleeper" load at a later time

3. incoming store addresses...
- search LAQ for matches (ordering failures)
- failed loads require pipeline flush

4. issue stores to memory at commit

5. addresses requiring translations are re-issued on free cycles
- stores can't clear ROB busy-bit until valid translation