# COMPAL CONFIDENTIAL

MODEL NAME : VAQ10

PCB NO : LA-9771P

BOM P/N : 4319MF31L01(TPM HDMI LVDS)
4319MF31L02(TPM HDMI QHD)
4319MF31L03(DTP HDMI LVDS)
4319MF31L04(DTP HDMI QHD)

GPIO MAP:

# Diesel 15"

REV : 0.2 (X01)

2013.XX.XX

1@ : LVDS panel

2@ : eDP(QHD) panel

EMC@ : EMI/ESD/RF part

@ : Nopop Component

CONN@ : Connector Component

CXDP@,PXDP@ : Total debug Component (pop them until ST)

MB PCB

| Part Number | Description |
|---|---|
| DAA0006I000 | PCB 0MF LA-9771P REV0 MB |

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Title: Cover Sheet

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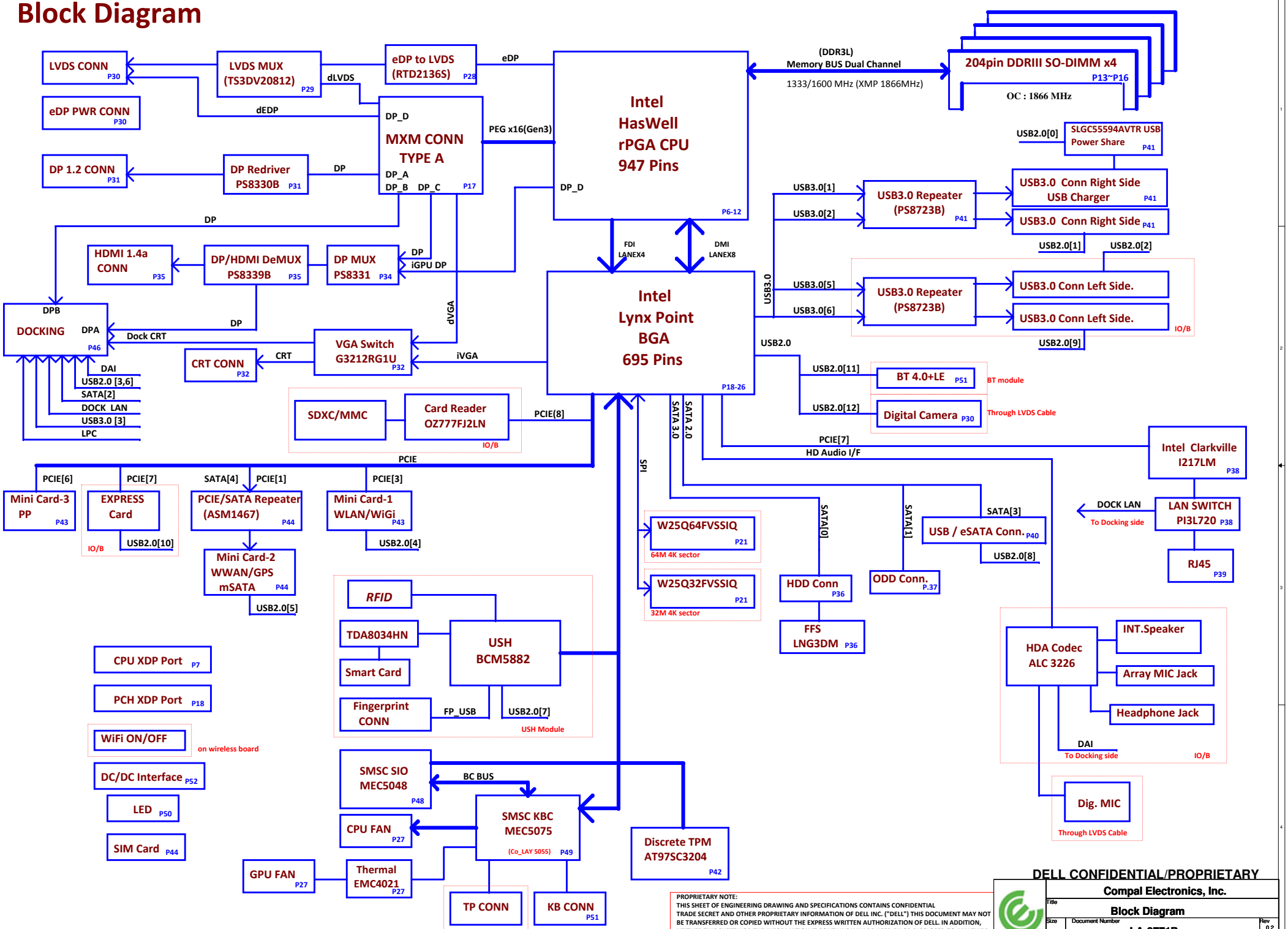
# Block Diagram





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## POWER STATES

| State \ Signal | SLP S3# | SLP S4# | SLP S5# | S4 STATE# | SLP M# | ALWAYS PLANE | M PLANE | SUS PLANE | RUN PLANE | CLOCKS |
|---|---|---|---|---|---|---|---|---|---|---|
| S0 (Full ON) / M0 | HIGH | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON | ON |
| S3 (Suspend to RAM) / M1 | LOW | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | OFF | OFF |
| S4 (Suspend to DISK) / M1 | LOW | LOW | HIGH | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S5 (SOFT OFF) / M1 | LOW | LOW | LOW | LOW | HIGH | ON | ON | OFF | OFF | OFF |
| S3 (Suspend to RAM) / M-OFF | LOW | HIGH | HIGH | HIGH | LOW | ON | OFF | ON | OFF | OFF |
| S4 (Suspend to DISK) / M-OFF | LOW | LOW | HIGH | LOW | LOW | ON | OFF | OFF | OFF | OFF |
| S5 (SOFT OFF) / M-OFF | LOW | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF | OFF |

## PM TABLE

| power plane / State | +5V_ALW<br>+3.3V_ALW2<br>+3.3V_ALW<br>+3.3V_ALW_PCH<br>+3.3V_RTC_LDO | +3.3V_SUS<br>+1.35V_MEM | +5V_RUN<br>+3.3V_RUN<br>+1.5V_RUN<br>+0.675V_DDR_VTT<br>+VCC_CORE<br>+1.05V_RUN | +3.3V_M<br>+1.05V_M | +3.3V_M<br>+1.05V_M<br>(M-OFF) |
|---|---|---|---|---|---|
| S0 | ON | ON | ON | ON | ON |
| S3 | ON | ON | OFF | ON | OFF |
| S5 S4/AC | ON | OFF | OFF | ON | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF | OFF | OFF |

## Stack up

| Layer No. | Name | Er | Material | Thickness (Material SPEC.) Unit : mil | Thickness (Actuality) Unit : mil |
|---|---|---|---|---|---|
| | | | SolderMask | IT-158 | 0.50 |
| | | | Add Plating | | 1.00 |
| 1 | Top | | Copper foil | 0.5oz | 0.65 |
| | | 3.7 | Prepreg | 1080 | 2.60 |
| 2 | GND1 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 3.91 |
| 3 | Sig 1 | | Copper foil | 1oz | 1.35 |
| | | 4.1 | Prepreg | 2116Mx2 | 8.26 |
| 4 | GND/PWR | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 3.91 |
| 5 | Sig 2 | | Copper foil | 1oz | 1.35 |
| | | 3.8 | Prepreg | 1080Hx2 | 4.80 |
| 6 | Sig 3 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 3.91 |
| 7 | GND/PWR | | Copper foil | 1oz | 1.35 |
| | | 4.1 | Prepreg | 2116Mx2 | 8.26 |
| 8 | Sig 4 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Core | 4mil | 3.91 |
| 9 | GND 3 | | Copper foil | 1oz | 1.35 |
| | | 3.7 | Prepreg | 1080 | 2.60 |
| 10 | Bottom | | Copper foil | 0.5oz | 0.65 |
| | | | Add Plating | | 1.00 |
| | | | SolderMask | | 0.50 |
| Overall Thickness (1.45mm ± 10%) | | | 57.09 | | 57.26000 |
| | | | | | 1.454404 |

| USB3.0 PORT | DESTINATION |
|---|---|
| 1 | JUSB1 (Ext Right Side) |
| 2 | JUSB2 (Ext Right Side) |
| 3 | Dock |
| 4 | NA(define PCIE_2) |
| 5 | IO/B- JUSB1(Ext Left Side) |
| 6 | IO/B- JUSB2(Ext Left Side) |

| | USB PORT# | DESTINATION |
|---|---|---|
| PCH | 0 | JUSB1 (Ext Right Side) |
| | 1 | JUSB2 (Ext Right Side) |
| | 2 | IO Board- JUSB1 (Ext Left Side) |
| | 3 | Docking USB3.0 |
| | 4 | WLAN/WIGIG |
| | 5 | WWAN/GPS/LTE/UWB/mSATA |
| | 6 | Docking USB 2.0 |
| | 7 | USH |
| | 8 | ESATA |
| | 9 | IO Board- JUSB2 (Ext Left Side) |
| | 10 | Express Card |
| | 11 | NA |
| | 12 | Carmera |
| | 13 | NA |

| | | |
|---|---|---|
| USH | 0 | BIO |
| | 1 | NA |

| SATA | DESTINATION |
|---|---|
| SATA 0 | HDD1 |
| SATA 1 | ODD |
| SATA 2 | Dock |
| SATA 3 | ESATA |
| SATA 4 | mSATA |
| SATA 5 | NA |

| PCI EXPRESS | DESTINATION |
|---|---|
| Lane 1 | mSATA/WWAN |
| Lane 2 | 10/100/1G LOM |
| Lane 3 | MINI CARD-2 (WLAN) |
| Lane 4 | NA |
| Lane 5 | NA |
| Lane 6 | NA |
| Lane 7 | EXPRESS CARD |
| Lane 8 | MMI(Card reader) |

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Title: Index and Config.

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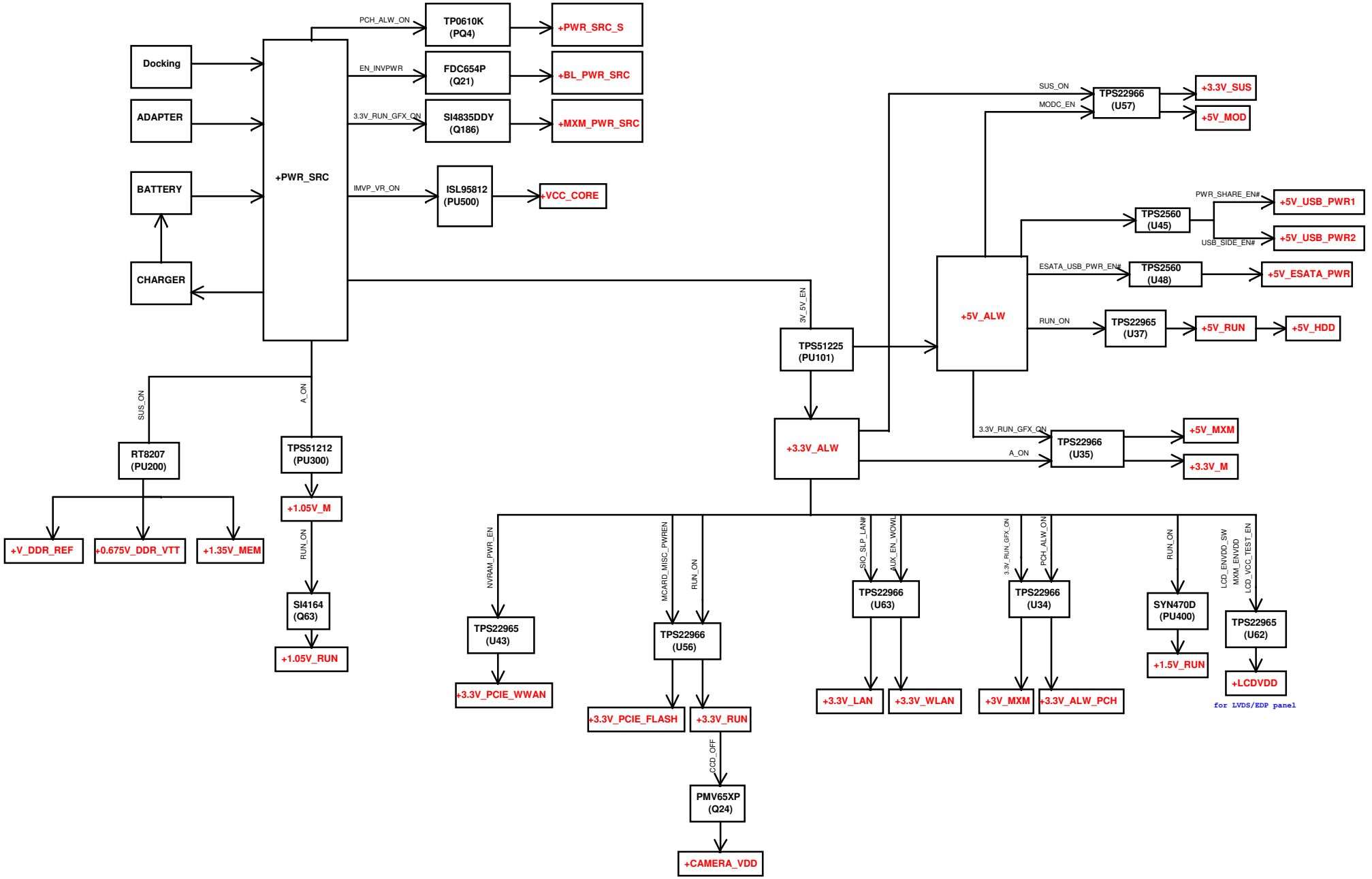


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Title: Power Rail

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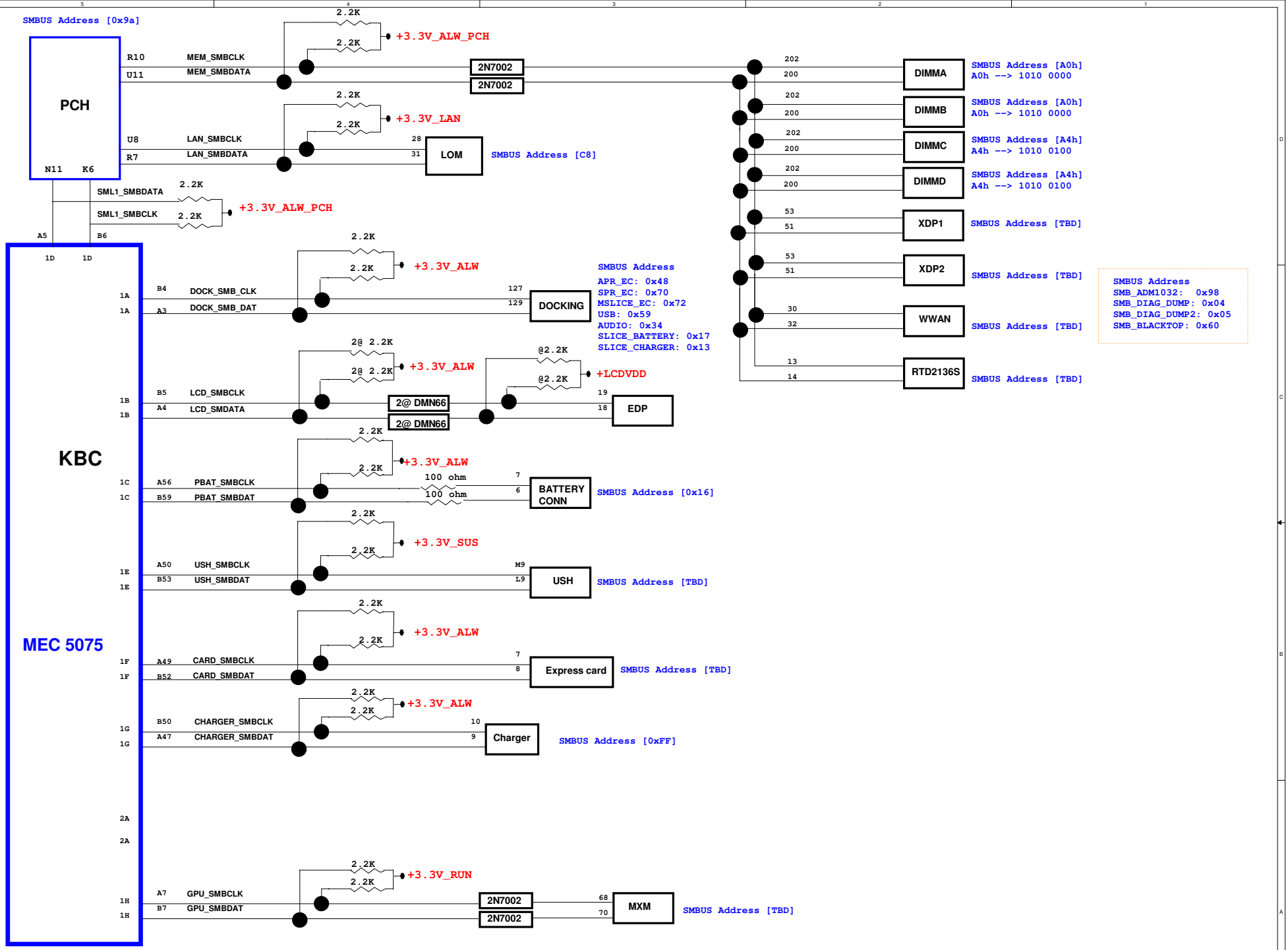


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Title: SMBUS Bolck Diagram

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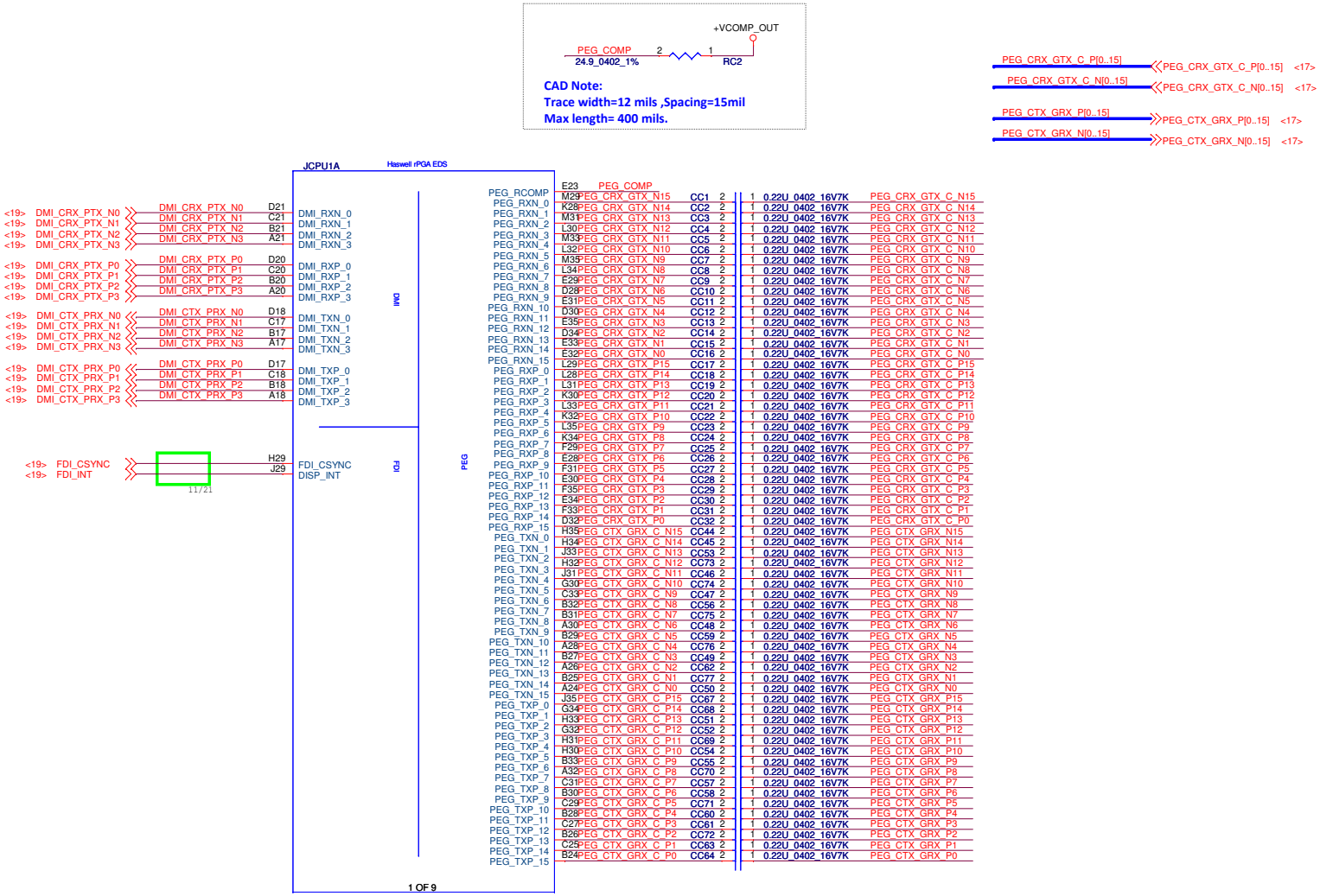


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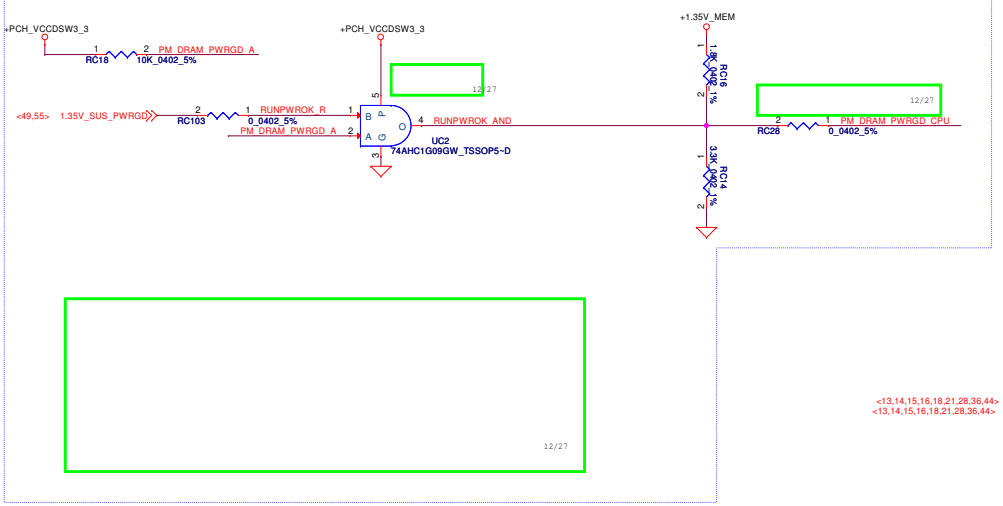
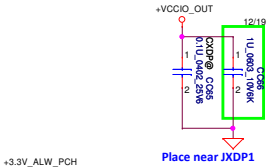
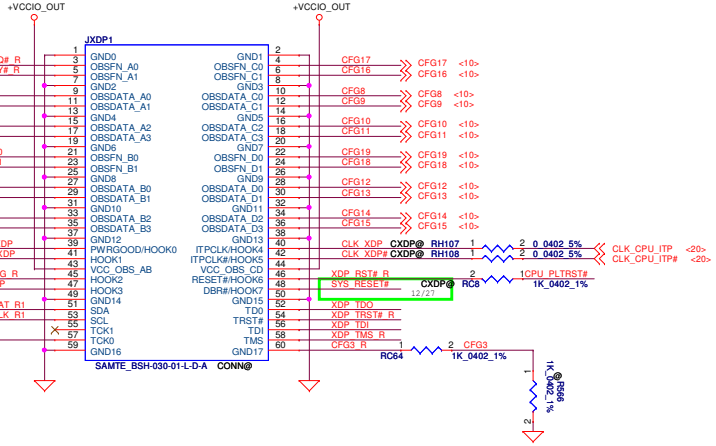
## SM_DRAMPWROK with DDR Power Gating Topology







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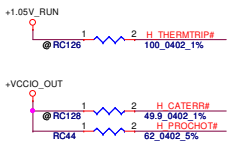
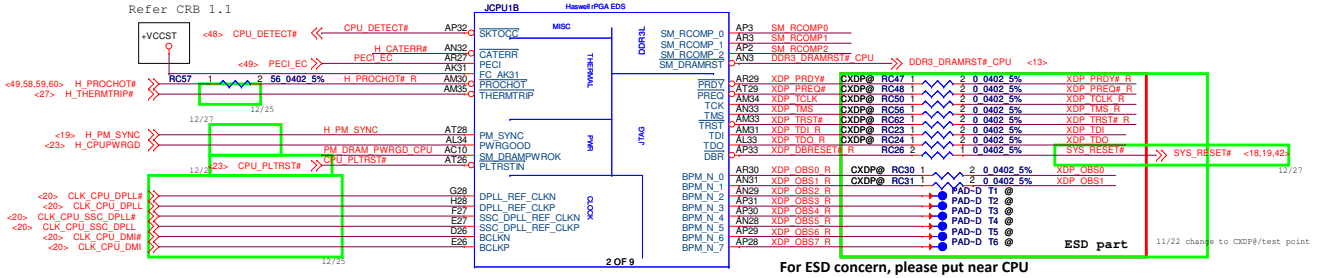
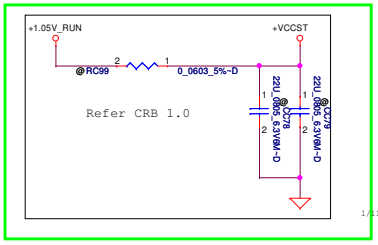
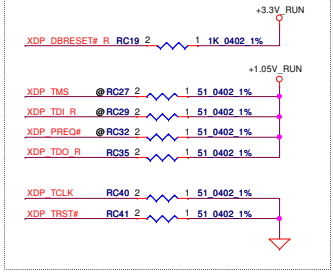


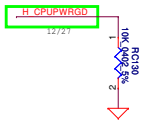




## PU/PD for JTAG signals

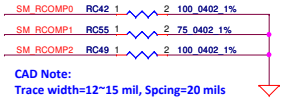



## Buffered reset to CPU




CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC25 & RC130

## DDR3 COMPENSATION SIGNALS




CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil

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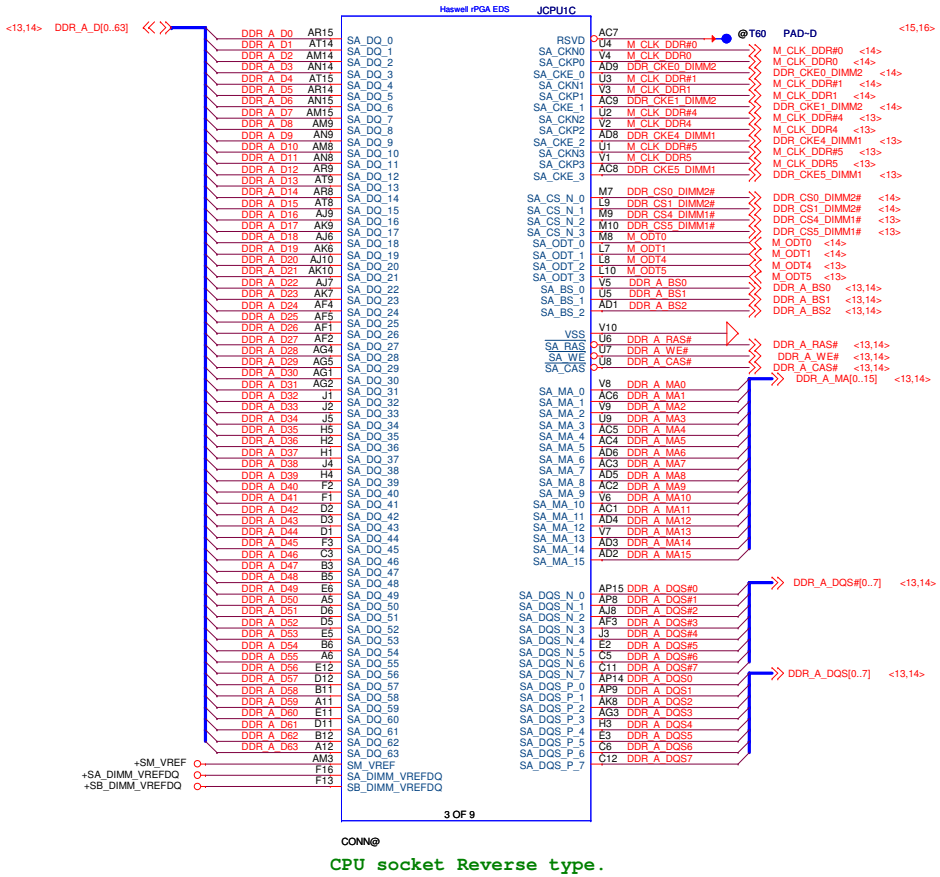

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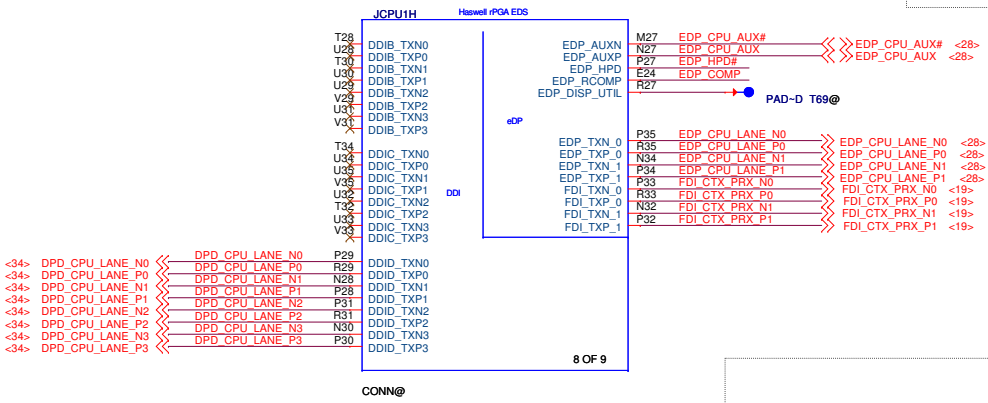
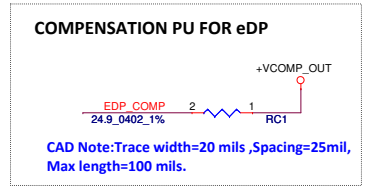
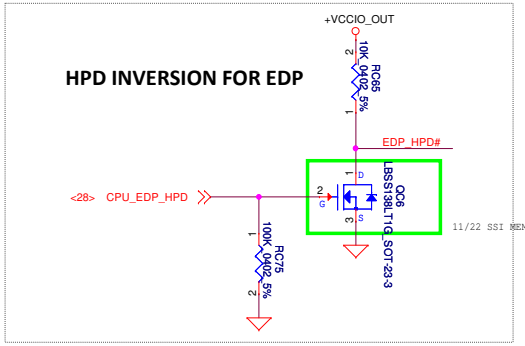



CPU socket Reverse type.

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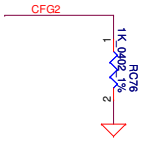
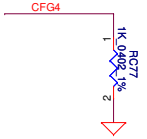
# CFG STRAPS for CPU



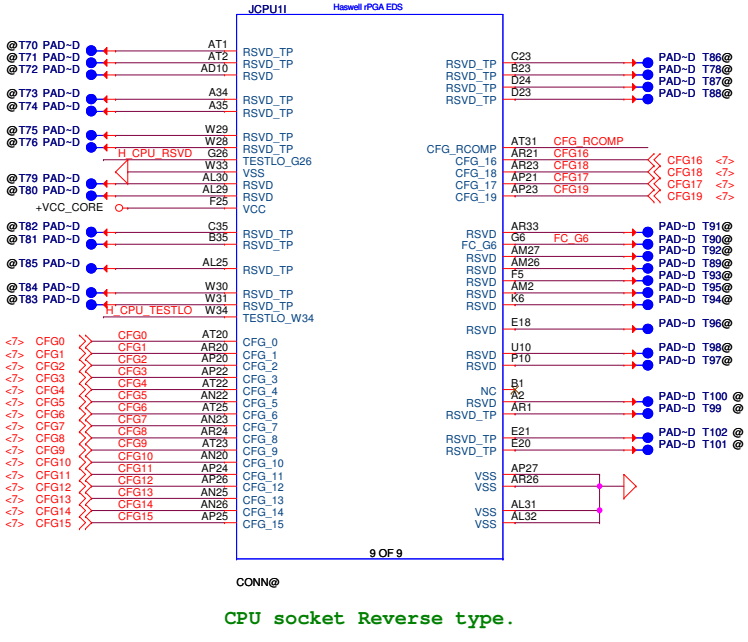

| PEG Static Lane Reversal - CFG2 is for the 16x | |
|---|---|
| CFG2 | 1:(Default) Normal Operation; Lane # definition matches socket pin map definition<br>0:Lane Reversed |



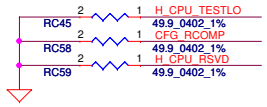

| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

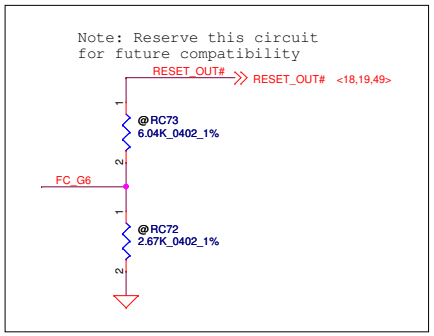
| PCIE Port Bifurcation Straps(PEG) | |
|---|---|
| CFG[6:5] | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled |

| PEG DEFER TRAINING | |
|---|---|
| CFG7 | 1: (Default) PEG Train immediately following xxRESETB de assertion<br>0: PEG Wait for BIOS for training |




CPU socket Reverse type.

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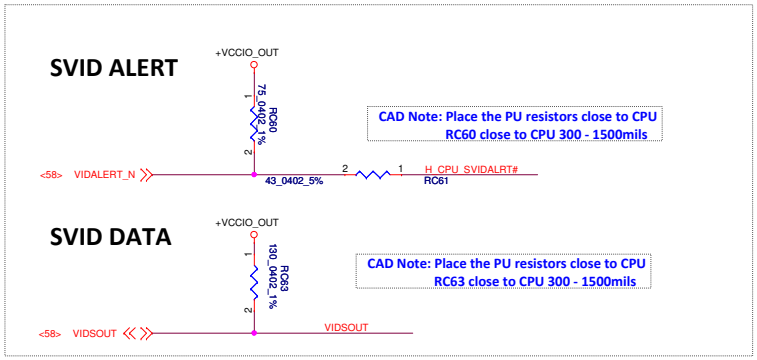


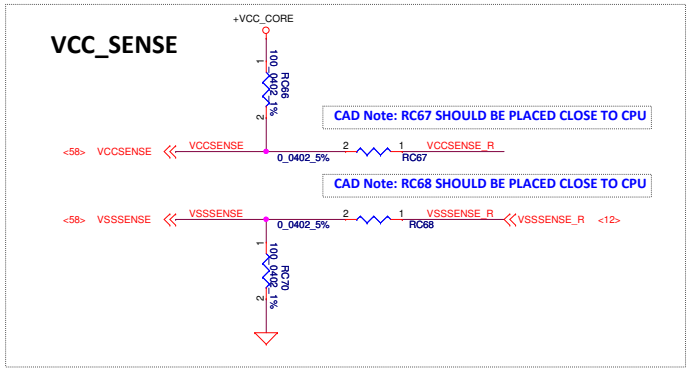


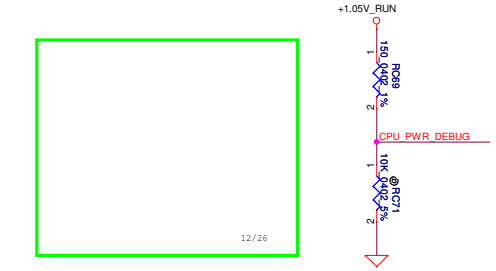


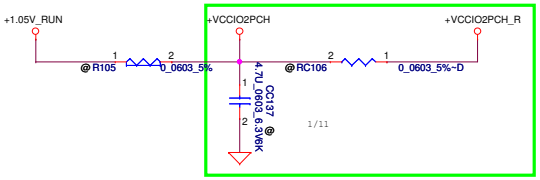


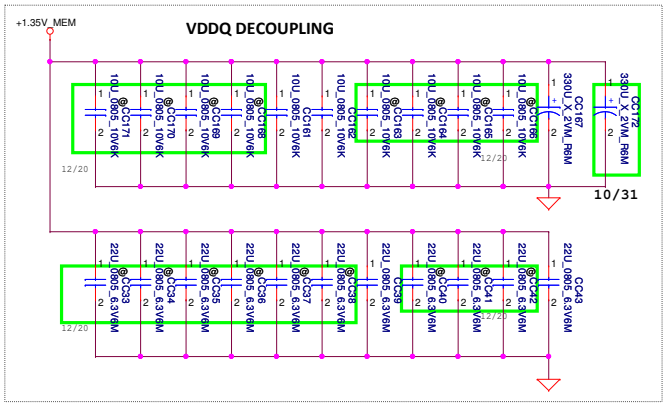


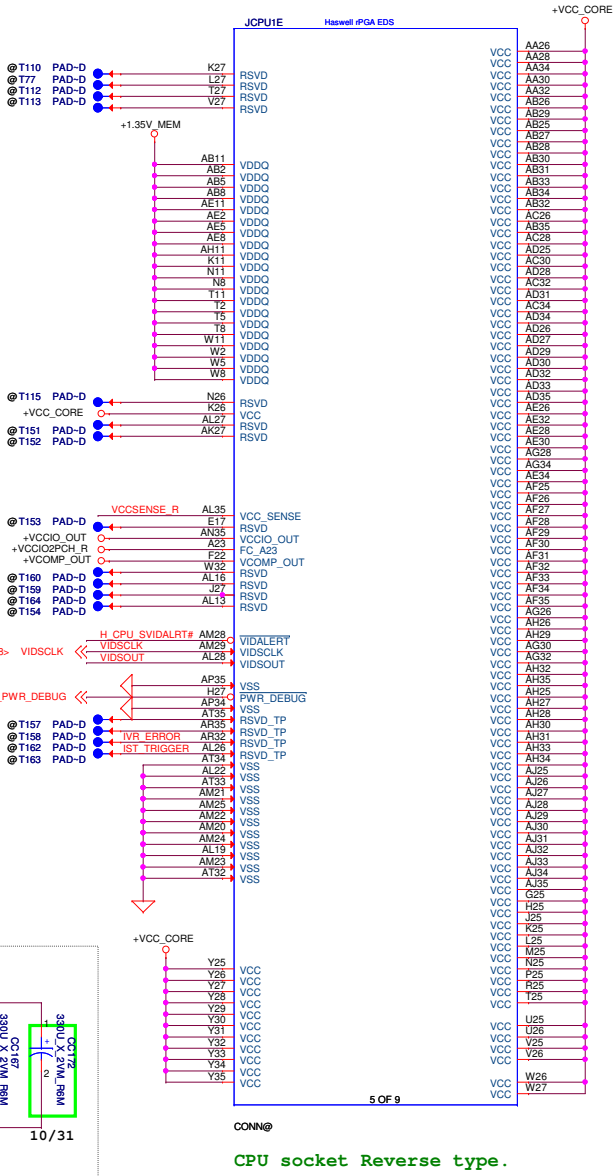


CPU socket Reverse type.

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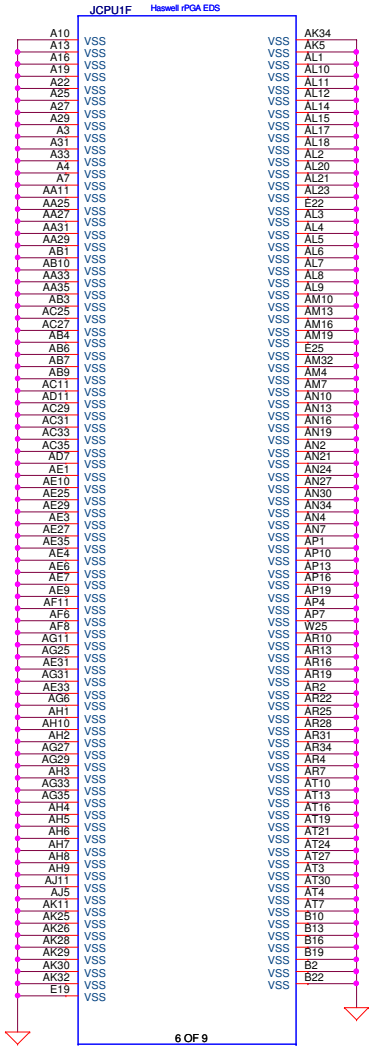
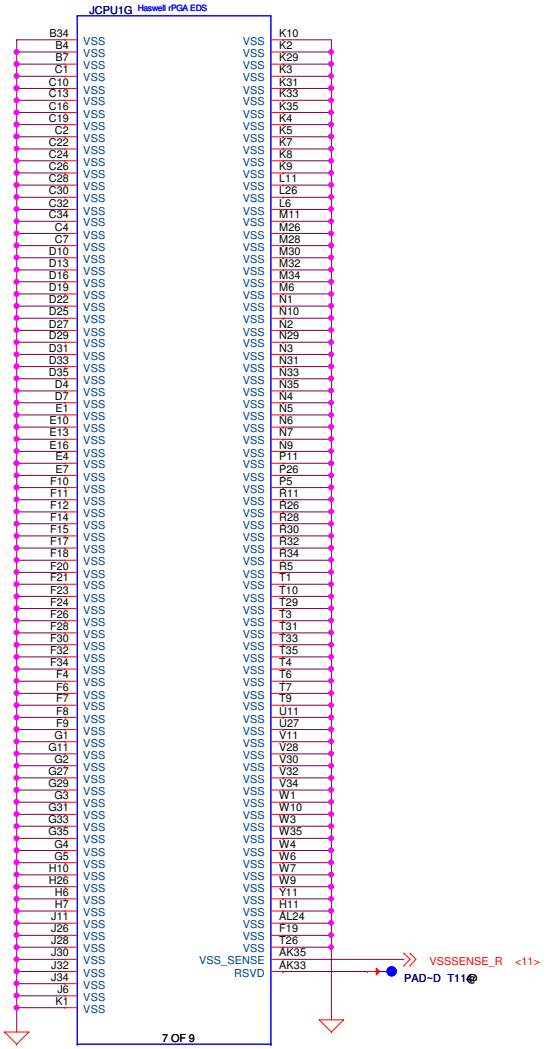
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: Haswell (6/7) | | |
| Size | Document Number: LA-9771P | Rev: 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 11 of 65 | |




CPU socket Reverse type.




CPU socket Reverse type.

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Title: Haswell (7/7)

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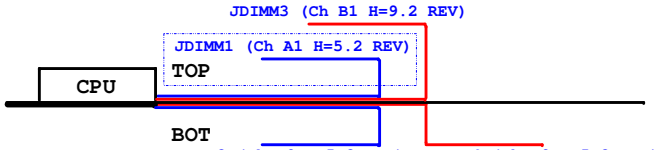
Date: Tuesday, January 15, 2013 | Sheet 12 of 65

# JDIMM1 REV Type H=5.2



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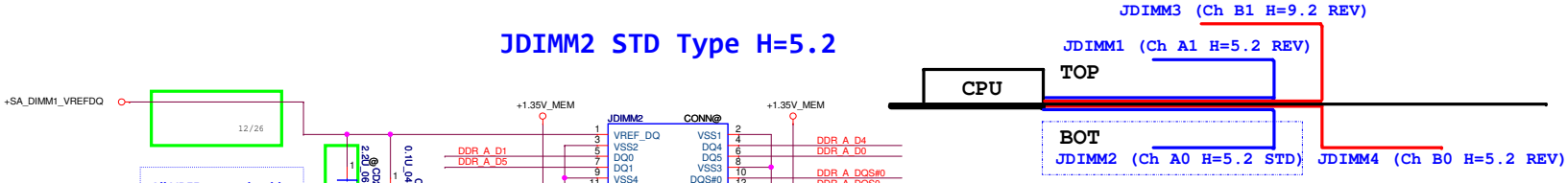
Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

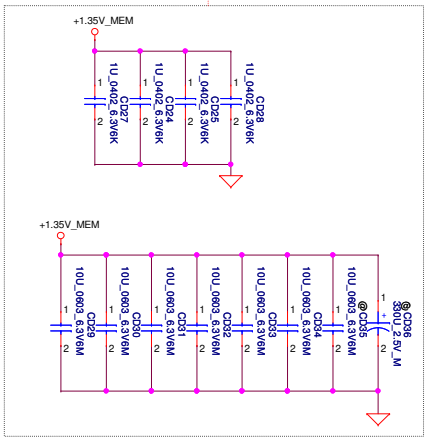
Size | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 13 of 65

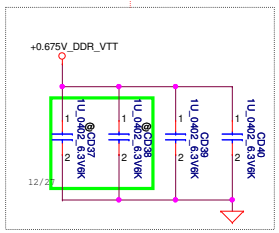
# JDIMM2 STD Type H=5.2




Layout Note:
Place near JDIMM2



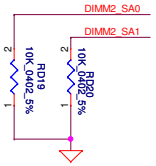

Layout Note:
Place near JDIMM2.Pin 203,204



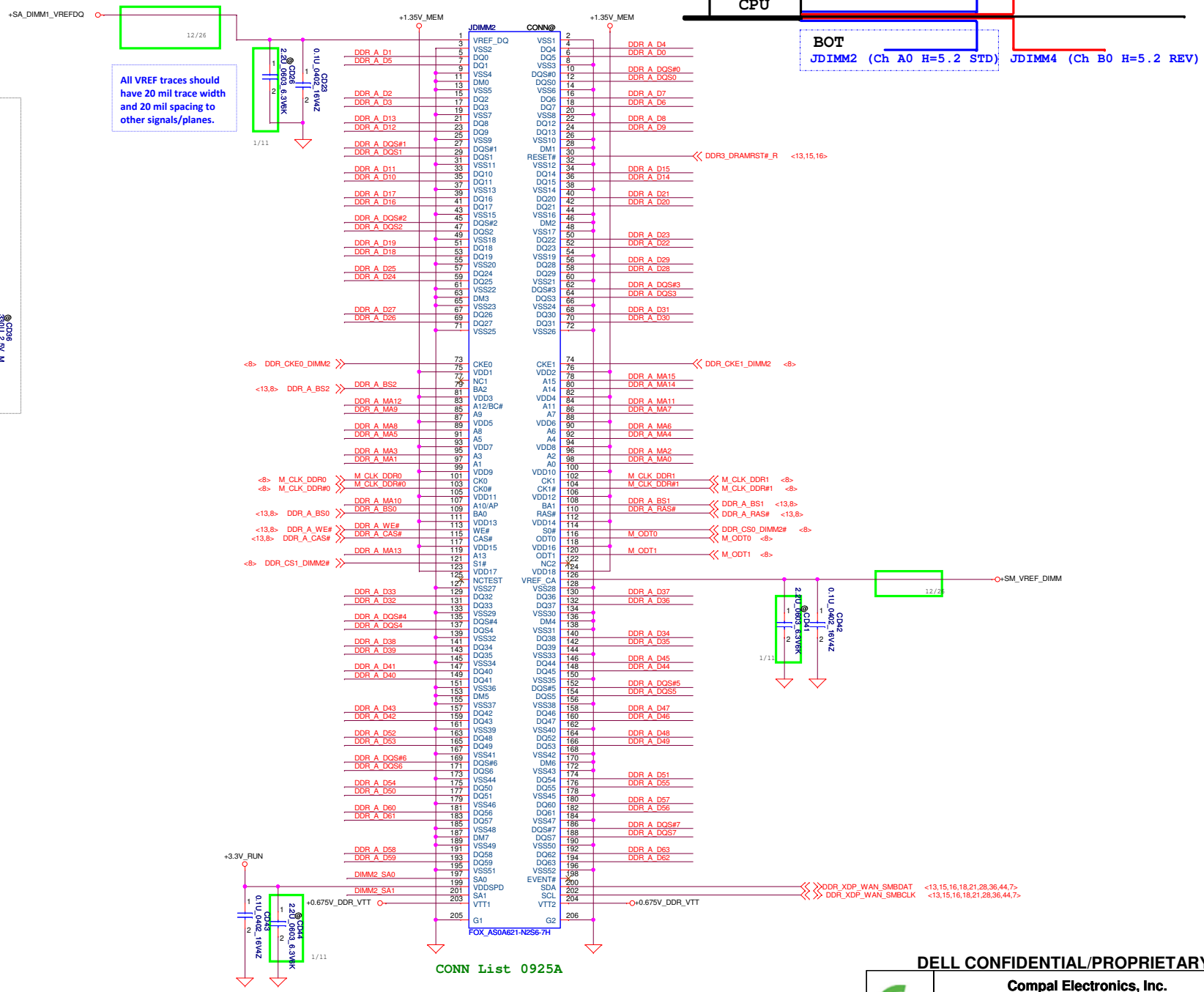

## DIMM Select

12/26

| SA0 | SA1 | |
|---|---|---|
| 1 | 0 | DIMM1 |
| 0 | 0 | DIMM2 |
| 1 | 1 | DIMM3 |
| 0 | 1 | DIMM4 |




All VREF traces should have 20 mil trace width and 20 mil spacing to other signals/planes.




CONN List 0925A

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Title: DDRIII-SODIMM SLOT2

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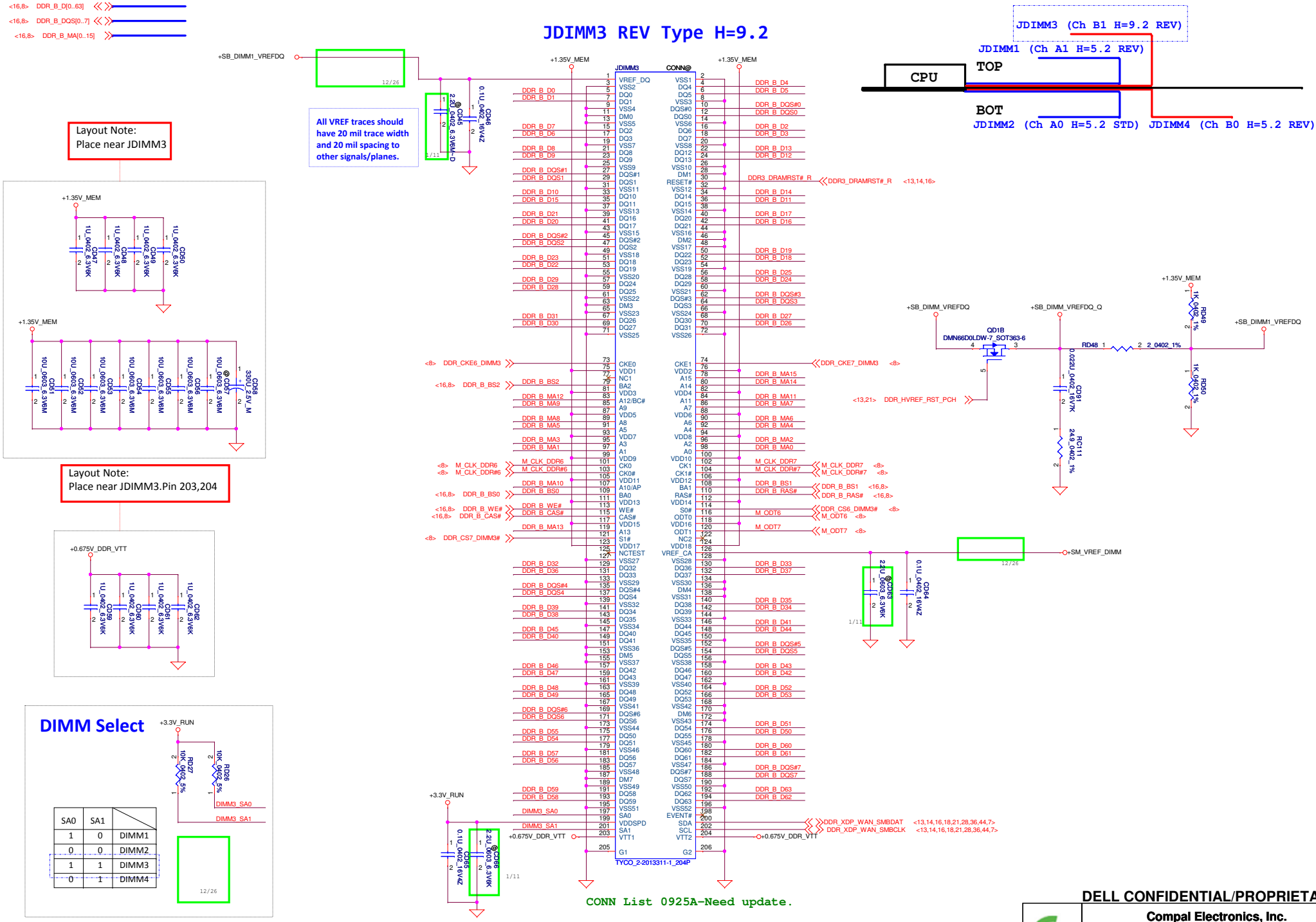
# JDIMM3 REV Type H=9.2





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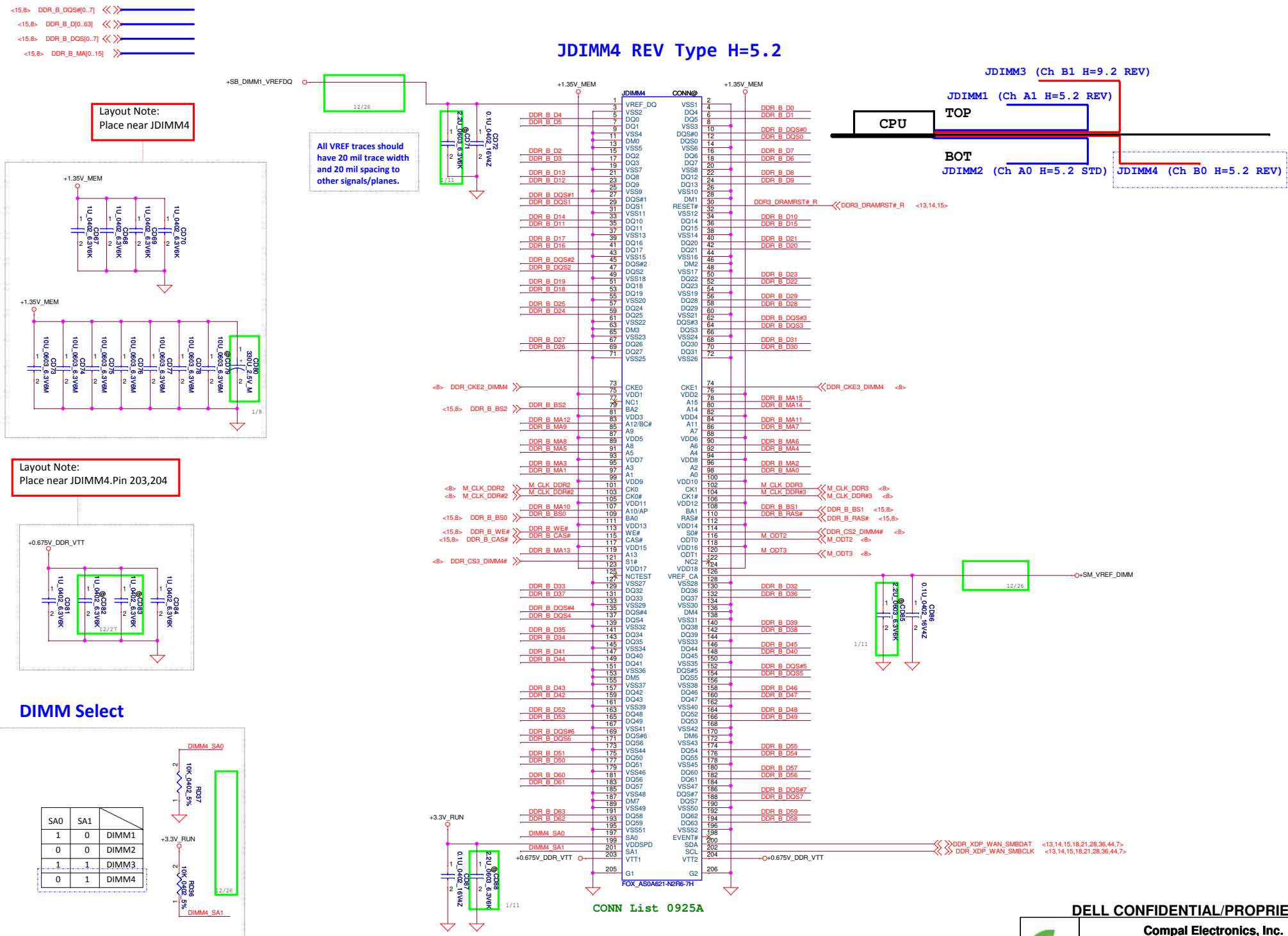
# JDIMM4 REV Type H=5.2

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Title: DDRIII-SODIMM SLOT4

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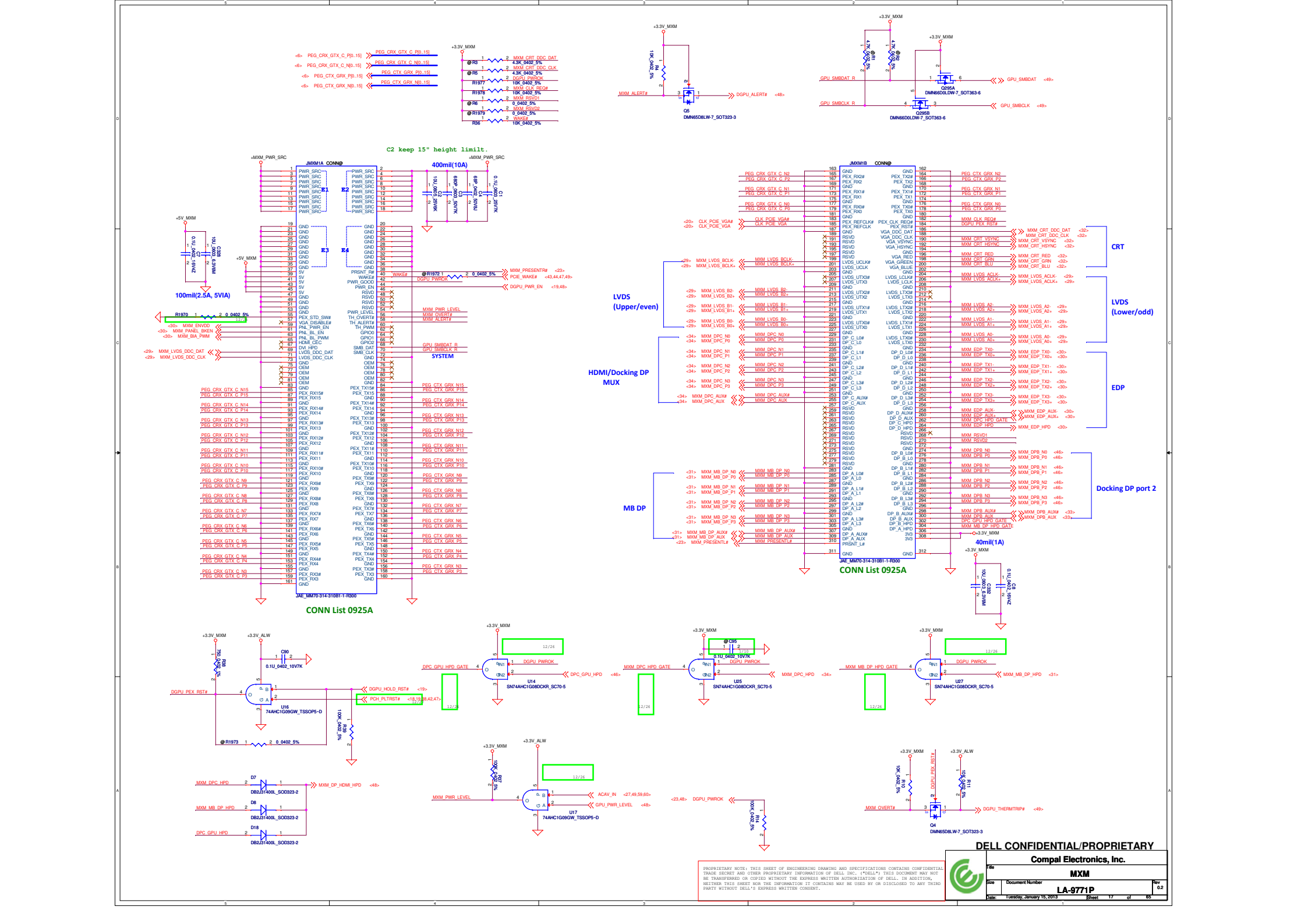
C2 keep 15" height limilt.
400mil(10A)
100mil(2.5A, 5VIA)
40mil(1A)
JMXM1A CONN@
JMXM1B CONN@
JAE_MM70-314-310B1-1-R300
CONN List 0925A
LVDS (Upper/even)
LVDS (Lower/odd)
HDMI/Docking DP MUX
MB DP
CRT
EDP
Docking DP port 2
SYSTEM
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MXM
LA-9771P
Tuesday, January 15, 2013
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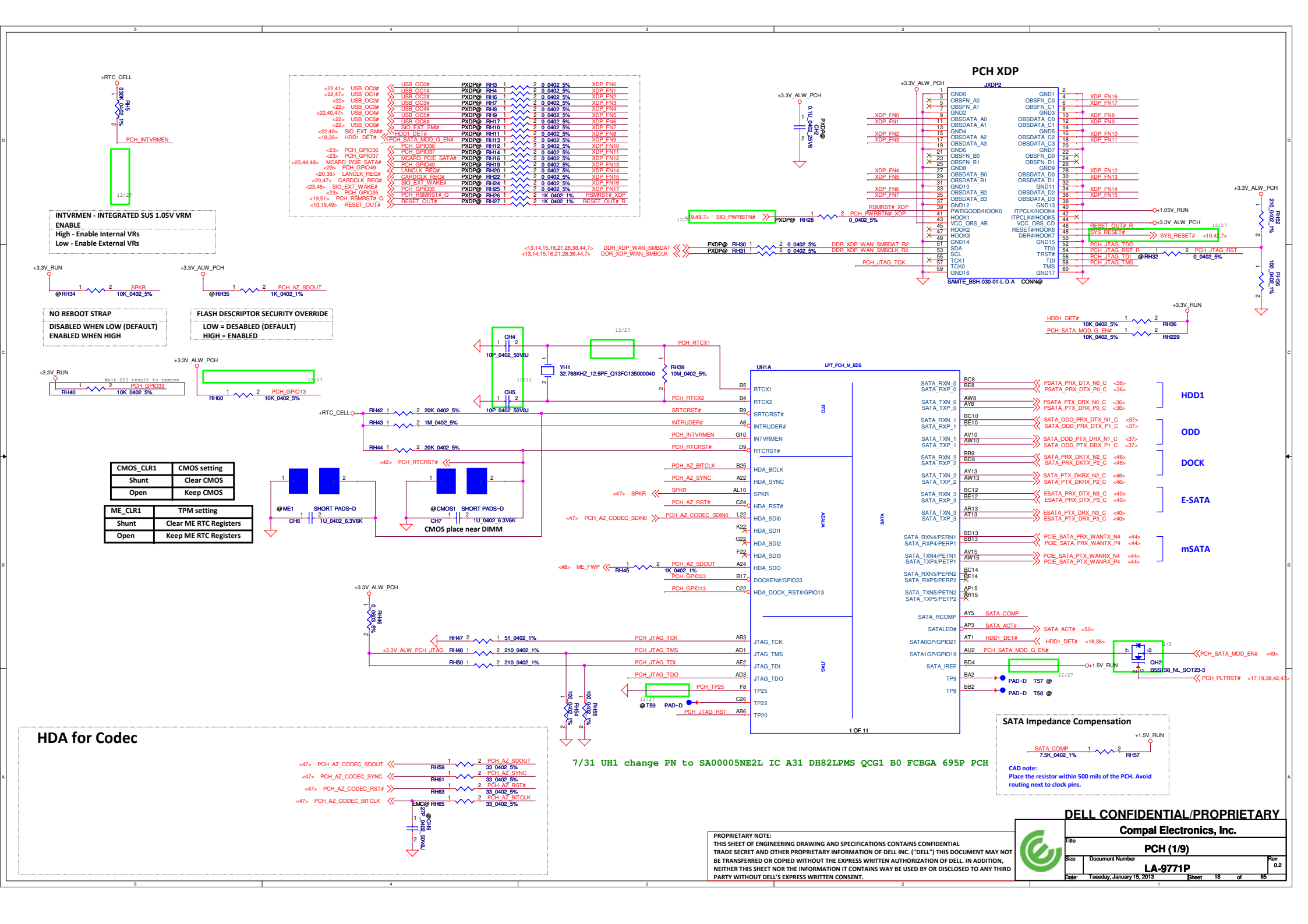
PCH XDP
JXDP2
SAMTE_BSH-030-01-L-D-A CONN@
INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs
NO REBOOT STRAP
DISABLED WHEN LOW (DEFAULT)
ENABLED WHEN HIGH
FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED
CMOS_CLR1 | CMOS setting
Shunt | Clear CMOS
Open | Keep CMOS
ME_CLR1 | TPM setting
Shunt | Clear ME RTC Registers
Open | Keep ME RTC Registers
CMOS place near DIMM
UH1A
LPT_PCH_M_EDS
HDD1
ODD
DOCK
E-SATA
mSATA
SATA Impedance Compensation
HDA for Codec
7/31 UH1 change PN to SA00005NE2L IC A31 DH82LPMS QCG1 B0 FCBGA 695P PCH
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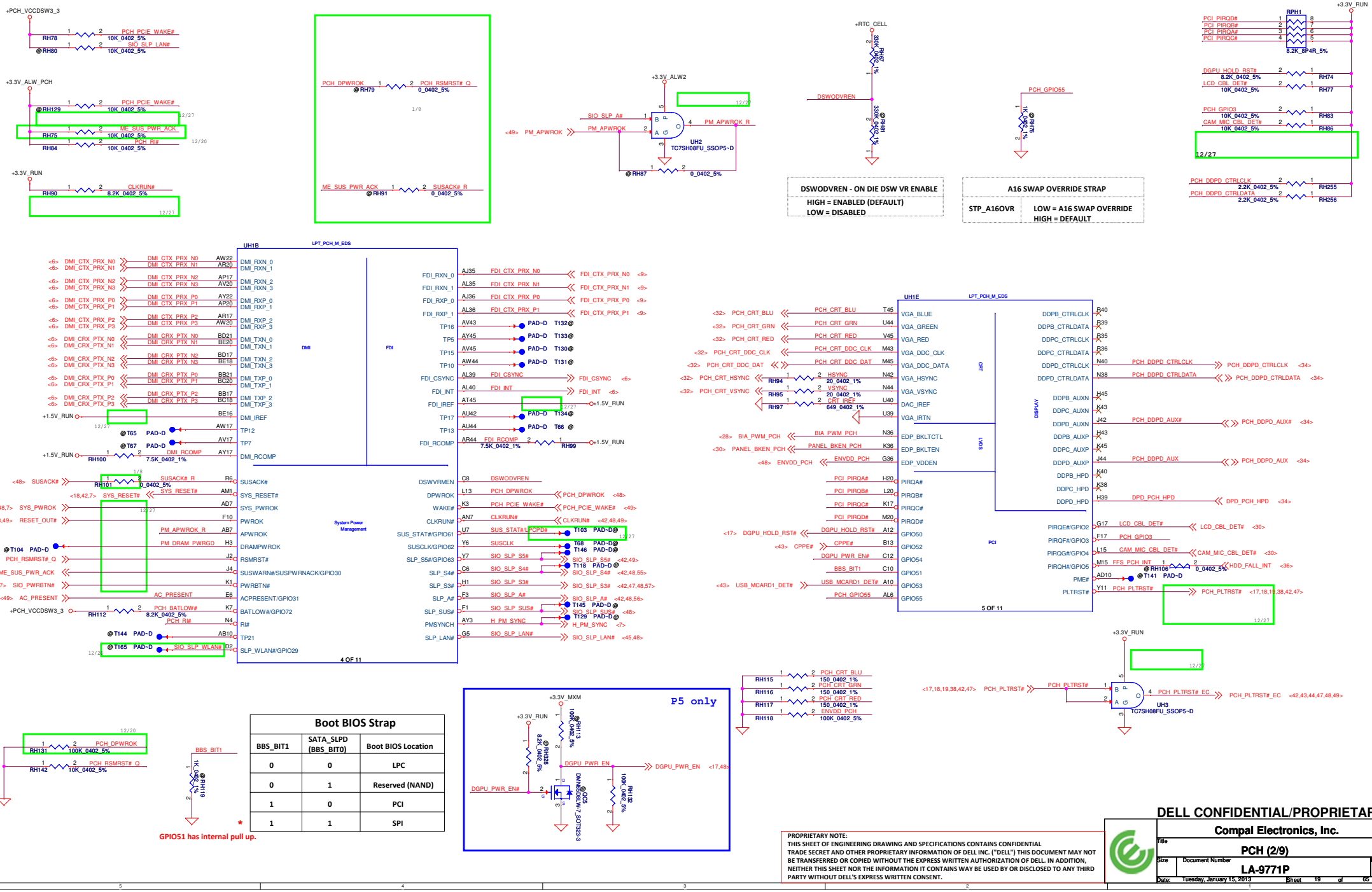
PCH (1/9)
LA-9771P
Tuesday, January 15, 2013


+PCH_VCCDSW3_3
RH78 10K_0402_5%
PCH_PCIE_WAKE#
@RH80 10K_0402_5%
SIO_SLP_LAN#
+3.3V_ALW_PCH
@RH129 10K_0402_5%
PCH_PCIE_WAKE#
RH75 10K_0402_5%
ME_SUS_PWR_ACK
RH84 10K_0402_5%
PCH_RI#
+3.3V_RUN
RH90 8.2K_0402_5%
CLKRUN#
PCH_DPWROK
@RH79 0_0402_5%
PCH_RSMRST#_Q
ME_SUS_PWR_ACK
@RH91 0_0402_5%
SUSACK#_R
+3.3V_ALW2
SIO_SLP_A#
PM_APWROK
<49> PM_APWROK
PM_APWROK_R
UH2
TC7SH08FU_SSOP5-D
@RH87 0_0402_5%
+RTC_CELL
RH27 330K_0402_1%
DSWODVREN
@RH181 330K_0402_1%
PCH_GPIO55
@RH178 1K_0402_1%
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
A16 SWAP OVERRIDE STRAP
STP_A16OVR
LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT
+3.3V_RUN
RPH1
PCI_PIRQD#
PCI_PIRQB#
PCI_PIRQA#
PCI_PIRQC#
8.2K_8P4R_5%
DGPU_HOLD_RST# 8.2K_0402_5% RH74
LCD_CBL_DET# 10K_0402_5% RH77
PCH_GPIO3 10K_0402_5% RH83
CAM_MIC_CBL_DET# 10K_0402_5% RH86
PCH_DDPD_CTRLCLK 2.2K_0402_5% RH255
PCH_DDPD_CTRLDATA 2.2K_0402_5% RH256
UH1B
LPT_PCH_M_EDS
DMI
FDI
System Power Management
4 OF 11
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_IREF
TP12
TP7
DMI_RCOMP
@RH100 7.5K_0402_1%
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
TP21
SLP_WLAN#/GPIO29
FDI_RXN_0
FDI_RXN_1
FDI_RXP_0
FDI_RXP_1
TP16
TP5
TP15
TP10
FDI_CSYNC
FDI_INT
FDI_IREF
TP17
TP13
FDI_RCOMP
7.5K_0402_1%
DSWVRMEN
DPWROK
WAKE#
CLKRUN#
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#
UH1E
LPT_PCH_M_EDS
CRT
LVDS
DISPLAY
PCI
5 OF 11
VGA_BLUE
VGA_GREEN
VGA_RED
VGA_DDC_CLK
VGA_DDC_DATA
VGA_HSYNC
VGA_VSYNC
DAC_IREF
VGA_IRTN
EDP_BKLTCTL
EDP_BKLTEN
EDP_VDDEN
PIRQA#
PIRQB#
PIRQC#
PIRQD#
GPIO50
GPIO52
GPIO54
GPIO51
GPIO53
GPIO55
DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPB_AUXN
DDPC_AUXN
DDPD_AUXN
DDPB_AUXP
DDPC_AUXP
DDPD_AUXP
DDPB_HPD
DDPC_HPD
DDPD_HPD
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
PME#
PLTRST#
PCH_CRT_BLU
PCH_CRT_GRN
PCH_CRT_RED
PCH_CRT_DDC_CLK
PCH_CRT_DDC_DAT
HSYNC 20_0402_1%
VSYNC 20_0402_1%
CRT_IREF 649_0402_1%
BIA_PWM_PCH
PANEL_BKEN_PCH
ENVDD_PCH
DGPU_HOLD_RST#
CPPE#
DGPU_PWR_EN#
BBS_BIT1
USB_MCARD1_DET#
PCH_GPIO55
PCH_DDPD_CTRLCLK
PCH_DDPD_CTRLDATA
PCH_DDPD_AUX#
PCH_DDPD_AUX
DPD_PCH_HPD
LCD_CBL_DET#
PCH_GPIO3
CAM_MIC_CBL_DET#
HDD_FALL_INT
@RH106 0_0402_5%
@T141 PAD-D
PCH_PLTRST#
SUSACK# R6
SYS_RESET# AM1
SYS_PWROK AD7
RESET_OUT# F10
PM_APWROK_R AB7
PM_DRAM_PWRGD H3
PCH_RSMRST#_Q J2
ME_SUS_PWR_ACK J4
SIO_PWRBTN# K1
AC_PRESENT E6
PCH_BATLOW# 8.2K_0402_5% K7
PCH_RI# N4
SIO_SLP_WLAN# D2
DSWODVREN C8
PCH_DPWROK L13
PCH_PCIE_WAKE# K3
CLKRUN# AN7
SUSCLK Y6
SIO_SLP_S5# Y7
SIO_SLP_S4# C6
SIO_SLP_S3# H1
SIO_SLP_A# F3
SIO_SLP_SUS# F1
H_PM_SYNC AY3
SIO_SLP_LAN# G5
PCH_CRT_BLU T45
PCH_CRT_GRN U44
PCH_CRT_RED V45
PCH_CRT_DDC_CLK M43
PCH_CRT_DDC_DAT M45
HSYNC N42
VSYNC N44
CRT_IREF U40
VGA_IRTN U39
BIA_PWM_PCH N36
PANEL_BKEN_PCH K36
ENVDD_PCH G36
PCI_PIRQA# H20
PCI_PIRQB# L20
PCI_PIRQC# K17
PCI_PIRQD# M20
DGPU_HOLD_RST# A12
CPPE# B13
DGPU_PWR_EN# C12
BBS_BIT1 C10
USB_MCARD1_DET# A10
PCH_GPIO55 AL6
PCH_DDPD_CTRLCLK R40
PCH_DDPD_CTRLDATA N38
PCH_DDPD_AUX# J42
PCH_DDPD_AUX J44
DPD_PCH_HPD H39
LCD_CBL_DET# G17
PCH_GPIO3 F17
CAM_MIC_CBL_DET# L15
HDD_FALL_INT M15
PCH_PLTRST# Y11
PCH_DPWROK
PCH_RSMRST#_Q
BBS_BIT1
1K_0402_1% @RH119
*
GPIO51 has internal pull up.
Boot BIOS Strap
BBS_BIT1
SATA_SLPD (BBS_BIT0)
Boot BIOS Location
0 0 LPC
0 1 Reserved (NAND)
1 0 PCI
1 1 SPI
P5 only
+3.3V_MXM
+3.3V_RUN
@RH828 8.2K_0402_5%
@RH113 100K_0402_5%
DGPU_PWR_EN
DGPU_PWR_EN#
@Q25 DMN66D0LW-7_SOT323-3
100K_0402_5% RH132
RH115 150_0402_1% PCH_CRT_BLU
RH116 150_0402_1% PCH_CRT_GRN
RH117 150_0402_1% PCH_CRT_RED
RH118 100K_0402_5% ENVDD_PCH
+3.3V_RUN
PCH_PLTRST#
UH3
TC7SH08FU_SSOP5-D
PCH_PLTRST# EC
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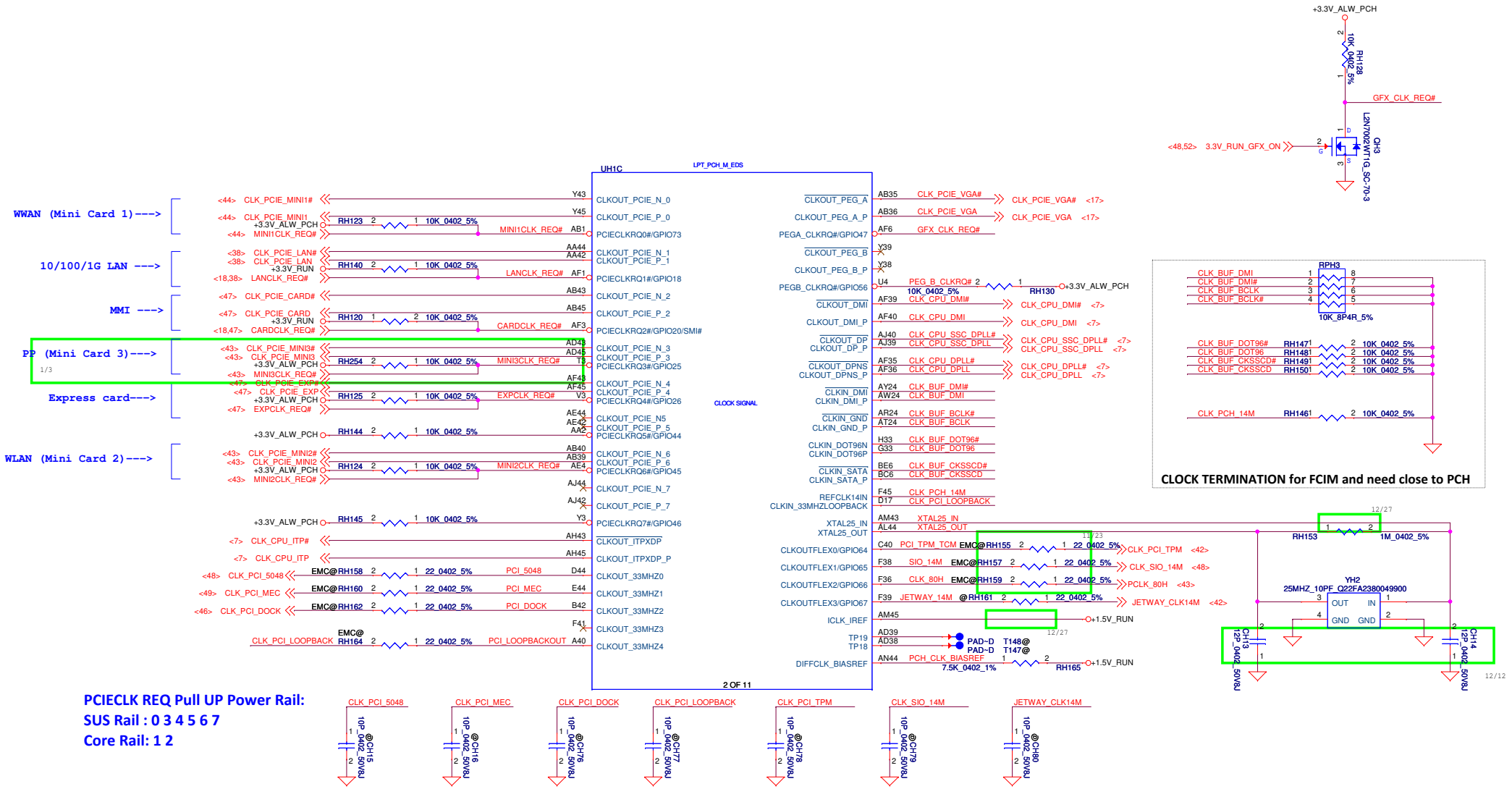
Title
PCH (2/9)
Size
Document Number
LA-9771P
Rev
0.2
Date: Tuesday, January 15, 2013
Sheet 19 of 65





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Title: PCH (3/9)

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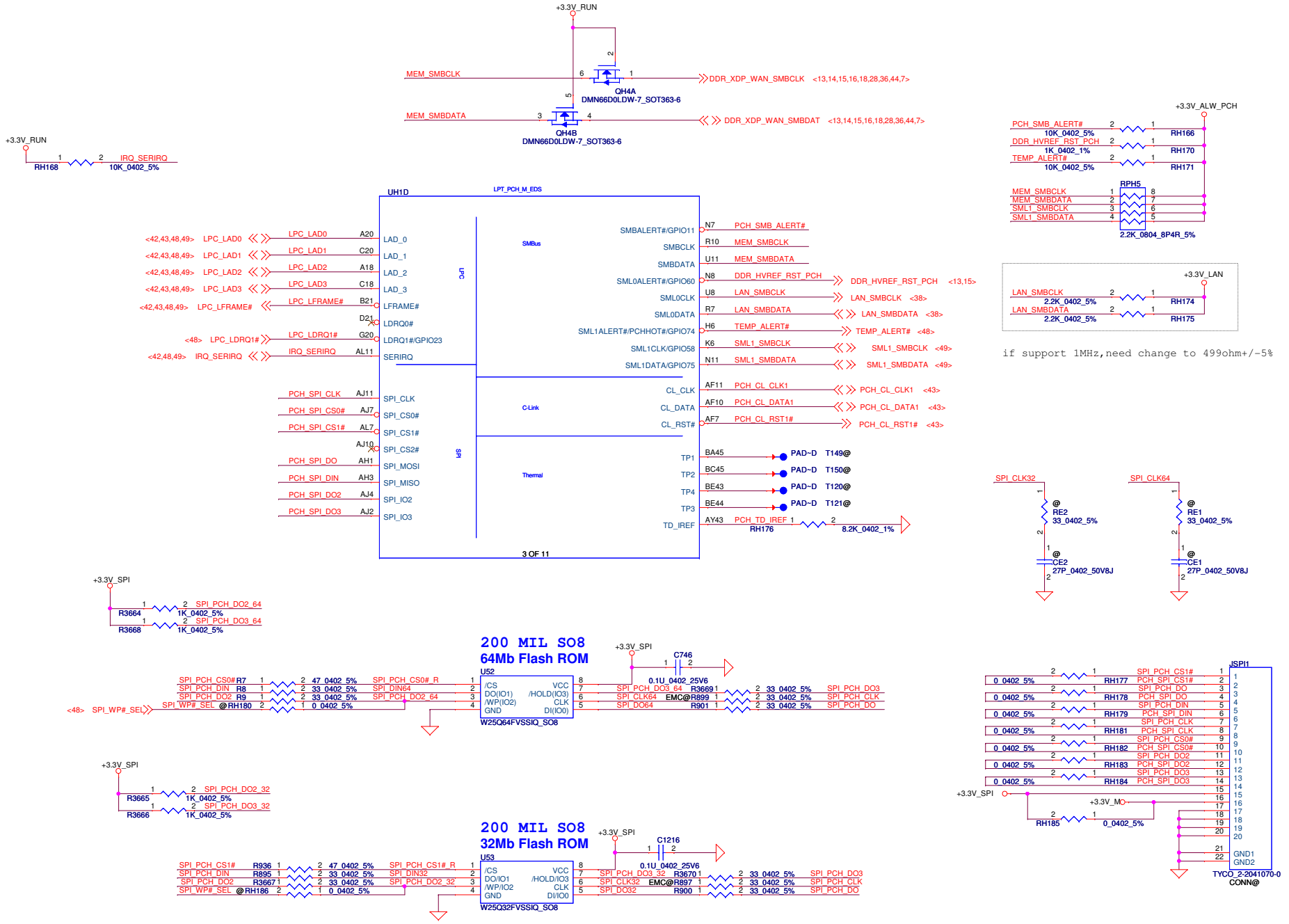
Date: Tuesday, January 15, 2013 | Sheet 20 of 65





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Title: PCH (4/9)

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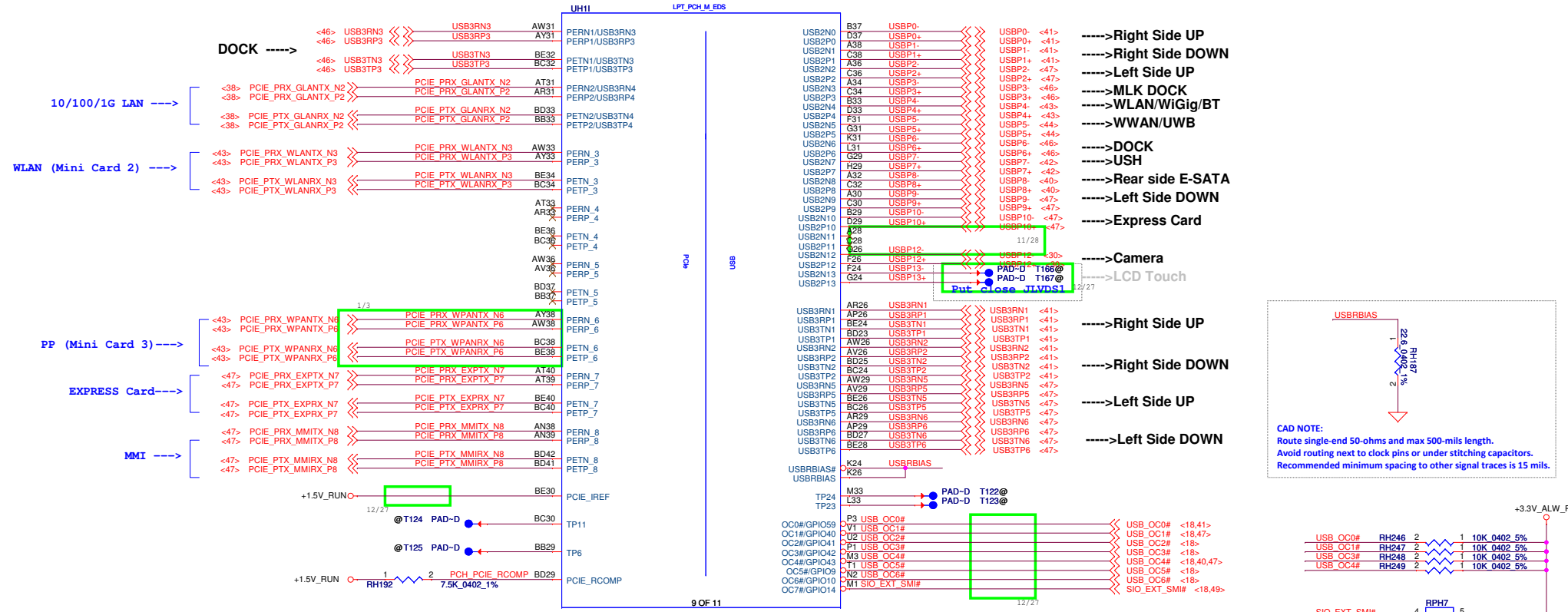


| Fixed Signals | | | | Muxed Signals | | Fixed Signals | | | | | | Muxed Signals | | Fixed Signals | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| USB3 1 | USB3 2 | USB3 5 | USB3 6 | PCIE 1 (00) | PCIE 2 (00) | PCIE 3 | PCIE 4 | PCIE 5 | PCIE 6 | PCIE 7 | PCIE 8 | SATA 4 (00) | SATA 5 (00) | SATA 0 | SATA 1 | SATA 2 | SATA 3 |
| | | | | USB3 3 (01) | USB3 4 (01) | | | | | | | PCIE 1 (01) | PCIE 2 (01) | | | | |


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Title: PCH (5/9)

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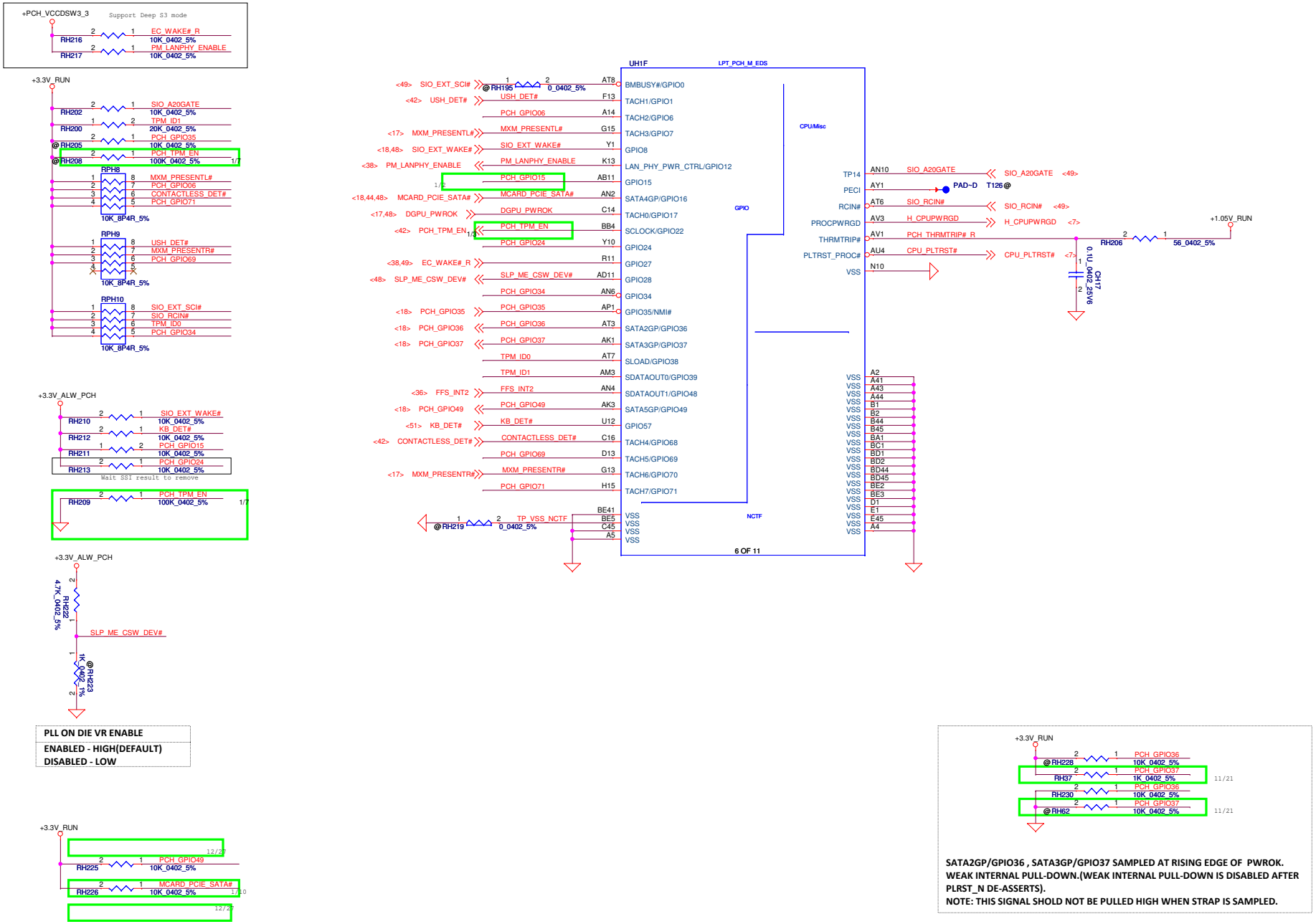


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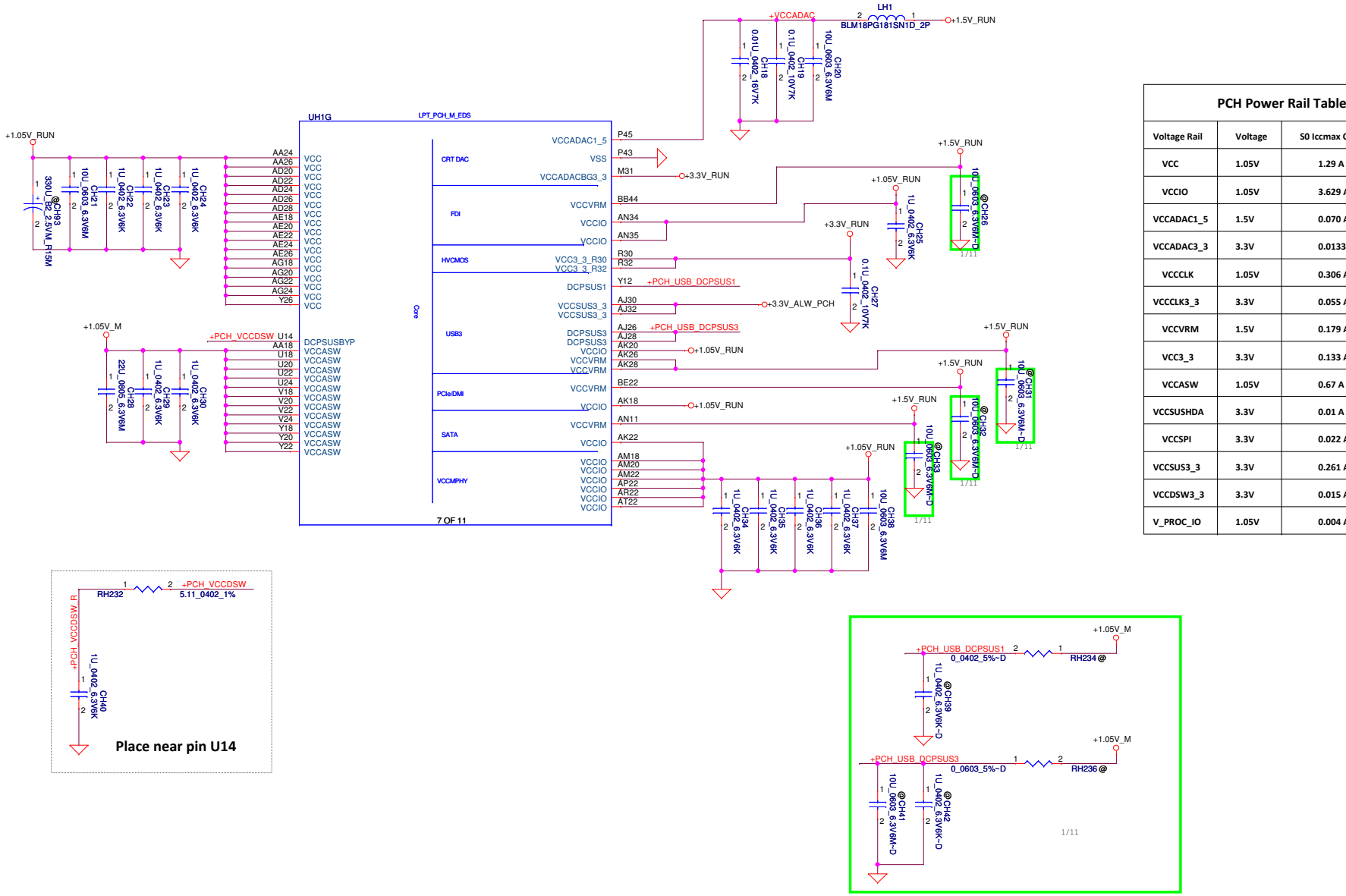
Title: PCH (6/9)

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 23 of 65




## PCH Power Rail Table

| Voltage Rail | Voltage | S0 Iccmax Current (A) |
|---|---|---|
| VCC | 1.05V | 1.29 A |
| VCCIO | 1.05V | 3.629 A |
| VCCADAC1_5 | 1.5V | 0.070 A |
| VCCADAC3_3 | 3.3V | 0.0133 A |
| VCCCLK | 1.05V | 0.306 A |
| VCCCLK3_3 | 3.3V | 0.055 A |
| VCCVRM | 1.5V | 0.179 A |
| VCC3_3 | 3.3V | 0.133 A |
| VCCASW | 1.05V | 0.67 A |
| VCCSUSHDA | 3.3V | 0.01 A |
| VCCSPI | 3.3V | 0.022 A |
| VCCSUS3_3 | 3.3V | 0.261 A |
| VCCDSW3_3 | 3.3V | 0.015 A |
| V_PROC_IO | 1.05V | 0.004 A |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Title: PCH (7/9)

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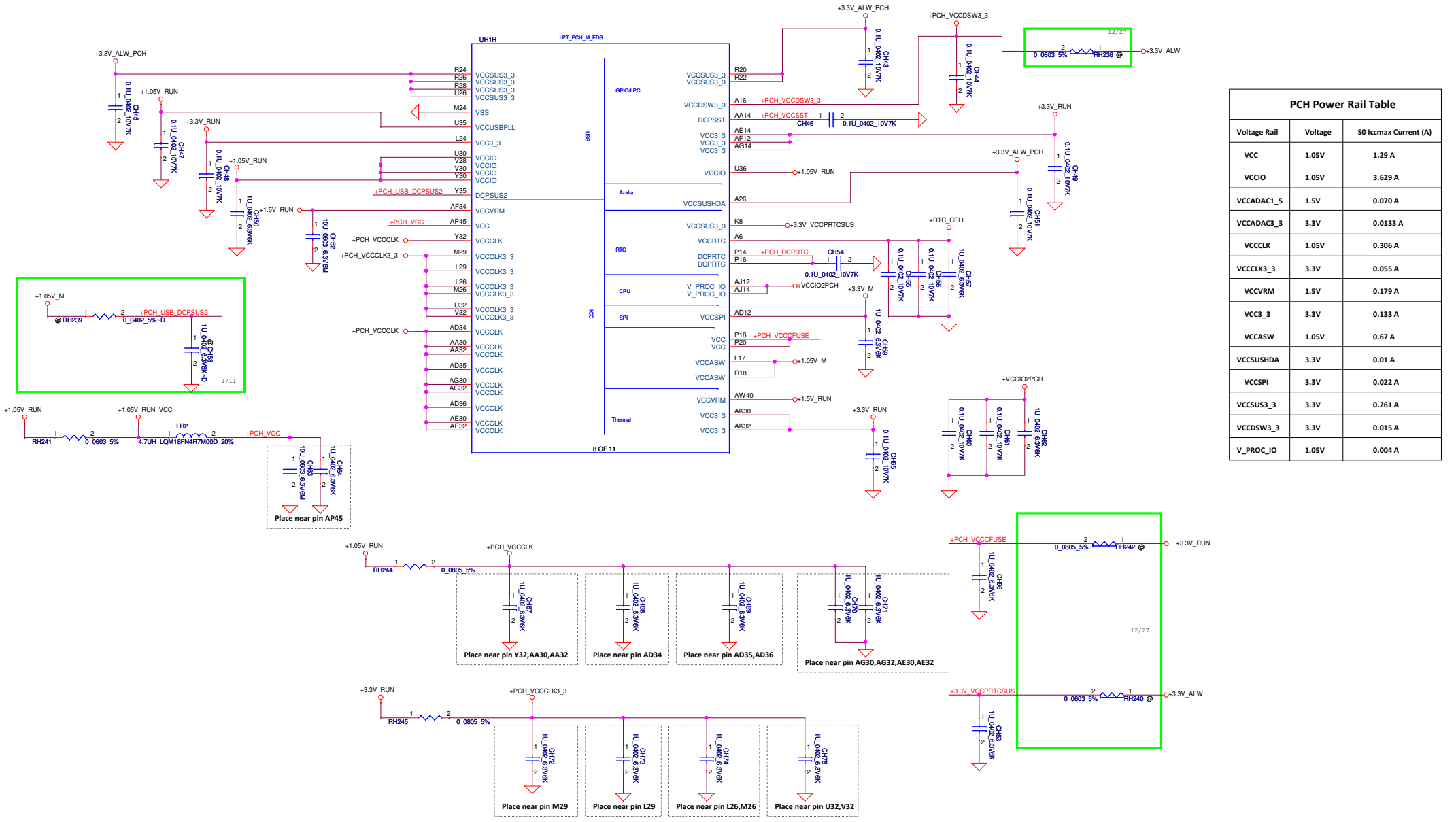
Date: Tuesday, January 15, 2013 | Sheet 24 of 65




## PCH Power Rail Table

| Voltage Rail | Voltage | S0 Iccmax Current (A) |
|---|---|---|
| VCC | 1.05V | 1.29 A |
| VCCIO | 1.05V | 3.629 A |
| VCCADAC1_5 | 1.5V | 0.070 A |
| VCCADAC3_3 | 3.3V | 0.0133 A |
| VCCCLK | 1.05V | 0.306 A |
| VCCCLK3_3 | 3.3V | 0.055 A |
| VCCVRM | 1.5V | 0.179 A |
| VCC3_3 | 3.3V | 0.133 A |
| VCCASW | 1.05V | 0.67 A |
| VCCSUSHDA | 3.3V | 0.01 A |
| VCCSPI | 3.3V | 0.022 A |
| VCCSUS3_3 | 3.3V | 0.261 A |
| VCCDSW3_3 | 1.05V | 0.015 A |
| V_PROC_IO | 1.05V | 0.004 A |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Title: PCH (8/9)

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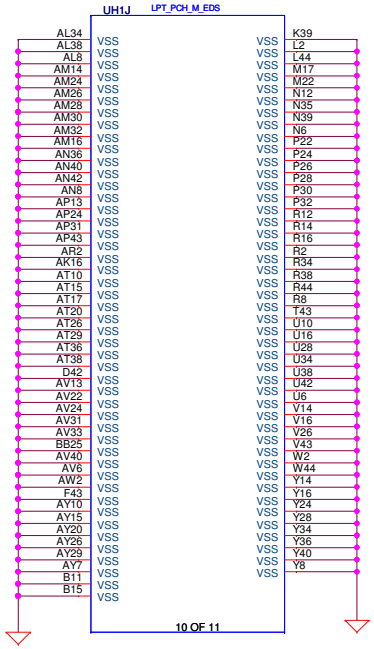
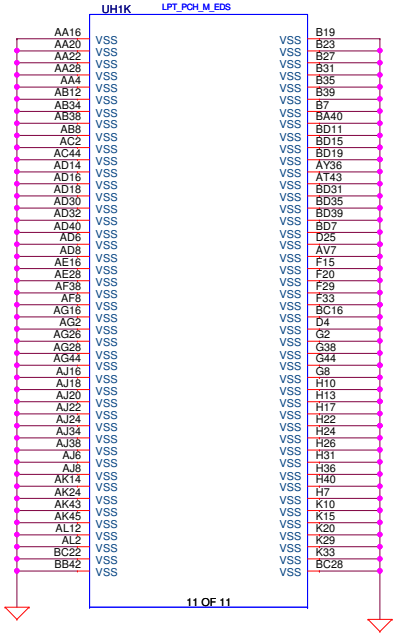
Date: Tuesday, January 15, 2013 | Sheet 25 of 65





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Compal Electronics, Inc.

Title: PCH (9/9)

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Date: Tuesday, January 15, 2013 | Sheet 26 of 65

Place Q26 under CPU
Place C339 close to the Q26

REM_DIODE1_P
@C339 100P_0402_50V8J
Q26 PMST3904_SOT323-3
REM_DIODE1_N

DP2/DN2 for SODIMM on Q17(TOP),
place Q17 close to SODIMM and C340 close to Q2

REM_DIODE2_P
@C340 100P_0402_50V8J
Q17 PMST3904_SOT323-3
REM_DIODE2_N

DP3/DN3 for Butterfly CHA on Q14(BOT),
place Q14 close to Butterfly CHA and C272 close to Q14

REM_DIODE3_P
@C272 100P_0402_50V8J
Q14 PMST3904_SOT323-3
REM_DIODE3_N

DP4/DN4 for Skin on Q15,
place Q15 close to Vcore VR choke and C288 close to Q15

REM_DIODE4_P
@C288 100P_0402_50V8J
Q15 PMST3904_SOT323-3
@C335 2200P_0402_50V7K
REM_DIODE4_N

REM_DIODE1_N ↔ REM_DIODE1_N <49>
REM_DIODE1_P ↔ REM_DIODE1_P <49>
REM_DIODE2_N ↔ REM_DIODE2_N <49>
REM_DIODE2_P ↔ REM_DIODE2_P <49>
REM_DIODE3_N ↔ REM_DIODE3_N <49>
REM_DIODE3_P ↔ REM_DIODE3_P <49>
REM_DIODE4_N ↔ REM_DIODE4_N <49>
REM_DIODE4_P ↔ REM_DIODE4_P <49>

Place Q16 under MXM(TOP side)
Place C273 close to the Q16

REM_DIODE1_P_4021
@C273 100P_0402_50V8J
Q16 PMST3904_SOT323-3
REM_DIODE1_N_4021

DP2/DN2 for MXM on Q27(BOT side),
place Q27 close to Butterfly CHB and C291 close to Q27

REM_DIODE2_P_4021
@C291 100P_0402_50V8J
Q27 PMST3904_SOT323-3
REM_DIODE2_N_4021

VCP_4021 — R430 10K_0402_5%

VSET_4021 — C319 0.1U_0402_25V6 — R424 1.33K_0402_1%

Rest=1.33k, Tp=93degree

+3.3V_RUN

FAN1_PWM — R407 10K_0402_5%
FAN2_PWM_D — R409 10K_0402_5%
FAN2_TACH_FB — R405 10K_0402_5%
FAN1_TACH_FB — R408 10K_0402_5%

## CPU FAN

+5V_RUN
<49> FAN1_PWM ↔ FAN1_PWM
<49> FAN1_TACH_FB ↔ FAN1_TACH_FB
C328 10U_0805_10V6K
C364 0.1U_0402_25V6
JFAN1 CONN@
GND1 GND2
ACES_50271-0040N-001
CONN List 0925A

+3.3V_ALW
R396 8.2K_0402_5%
THERMTRIP2# → THERMATRIP2# <49>
+VCCIO_OUT
R399 2.2K_0402_5%
Q28 PMST3904_SOT323-3
C327 0.1U_0402_25V6
<7> H_THERMTRIP#

## MXM FAN

+5V_RUN
FAN2_PWM — D90 RB751S40T1G_SOD523-2 — FAN2_PWM_D
FAN2_TACH_FB
C329 10U_0805_10V6K
C370 0.1U_0402_25V6
JFAN2 CONN@
GND1 GND2
ACES_50271-0040N-001
CONN List 0925A

+RTC_CELL
C287 0.1U_0402_25V6
POWER_SW# → U10 TC7SH08FU_SSOP5~D → DOCK_PWR_SW# <49>, POWER_SW_IN# <49>

U29 EMC4021-1-EZK-TR_QFN32_5X5~D

+3.3V_M — R402 10K_0402_5% — VDD_PWRGD
VDD_H, VDD_H, VDD_L, VDD_PWRGD
C271 2200P_0402_50V7K — REM_DIODE1_N_4021 / REM_DIODE1_P_4021 — DN1/THERM DP1/VREF_T
C315 2200P_0402_50V7K — REM_DIODE2_N_4021 / REM_DIODE2_P_4021 — DN2/DP4 DP2/DN4
N/C, N/C
R820 100K_0402_5% — VCP_4021 — VCP VIN
VSET_4021 — VSET
Test3
0 = 4021
1 = 4022
SMSC request
FAN2_TACH_FB — R420 10K_0402_5% — TACH/GPIO1
TEST3
FAN2_PWM — GPIO3/PWM/THERMTRIP_SIO
<49> PCH_PWRGD# — R410 1K_0402_1% — 3V_PWROK#
+RTC_CELL — C278 1U_0402_6.3V6K — RTC_PWR3V

THERMTRIP2# — R818 10K_0402_5% — +3.3V_M
N/C
SYS_SHDN# → THERM_STP# <54>
POWER_SW# — @R395 47K_0402_1% — +RTC_CELL
ACAVAIL_CLR / ATF_INT#/BC_IRQ# — BC_INT#_EMC4021 → ACAV_IN <17,49,59,60>, BC_INT#_EMC4021 <49>
FAN_OUT, FAN_OUT
SMCLK/BC_CLK / SMDATA/BC_DATA → BC_CLK_EMC4021 <49>, BC_DAT_EMC4021 <49>
VDD ADDR_MODE/XEN — +VCC_4021 — +ADDR_XEN — R394 4.7K_0402_5% — +VCC_4021
TEST1, TEST2, VSS — R418 10K_0402_5% SMSC request
+3.3V_M — R392 22_0402_5%
C318 0.1U_0402_25V6
C1198 1U_0402_6.3V6K

BC_INT#_EMC4021 — R426 10K_0402_5% — +3.3V_M

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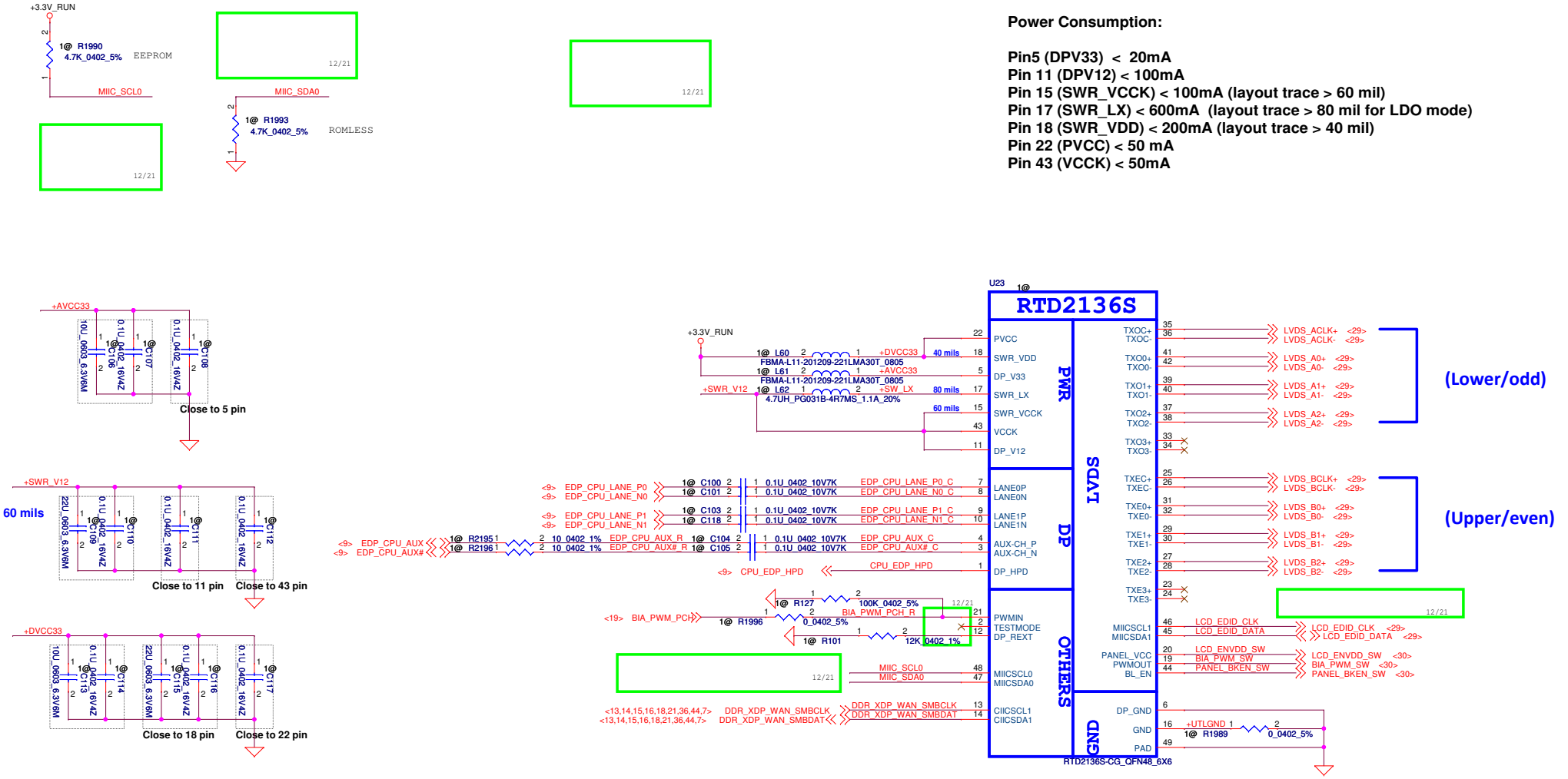
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | FAN control |
| Size | Document Number: LA-9771P |
| Rev | 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 27 of 65 |

**Power Consumption:**

**Pin5 (DPV33) < 20mA**
**Pin 11 (DPV12) < 100mA**
**Pin 15 (SWR_VCCK) < 100mA (layout trace > 60 mil)**
**Pin 17 (SWR_LX) < 600mA (layout trace > 80 mil for LDO mode)**
**Pin 18 (SWR_VDD) < 200mA (layout trace > 40 mil)**
**Pin 22 (PVCC) < 50 mA**
**Pin 43 (VCCK) < 50mA**




1009 change to SA000067100(RTD2136R)

* RTD2136R SA000067100 : Populate R1993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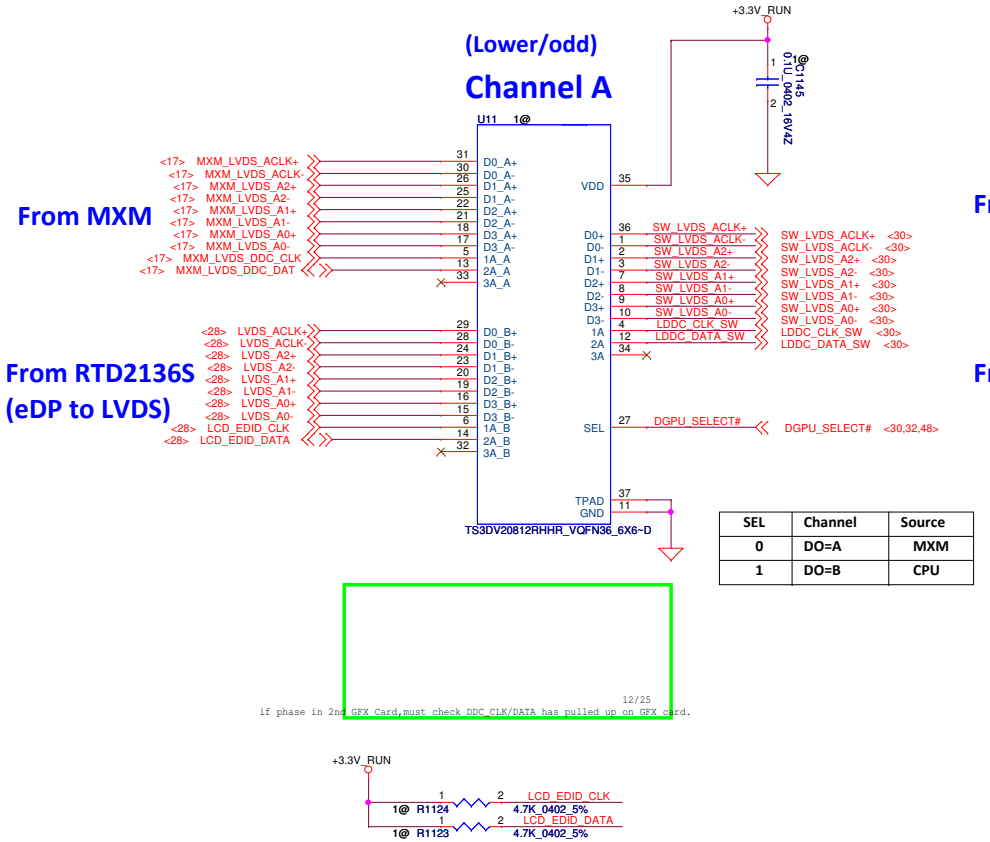
Compal Electronics, Inc.

Title: eDP to LVDS

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 28 of 65

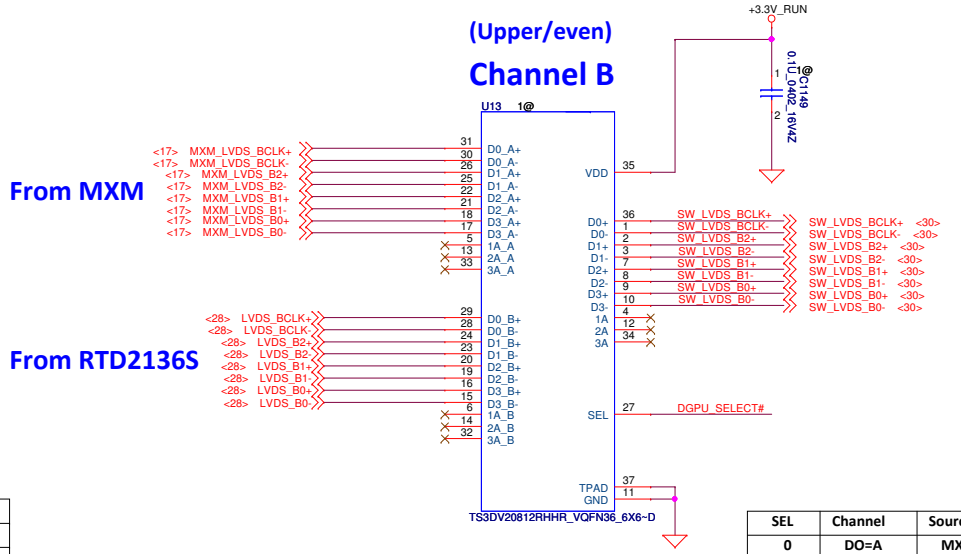



| SEL | Channel | Source |
|---|---|---|
| 0 | DO=A | MXM |
| 1 | DO=B | CPU |

12/25

if phase in 2nd GFX Card,must check DDC_CLK/DATA has pulled up on GFX card.




| SEL | Channel | Source |
|---|---|---|
| 0 | DO=A | MXM |
| 1 | DO=B | CPU |

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Compal Electronics, Inc.

Title: LVDS SW

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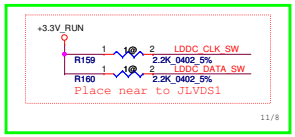
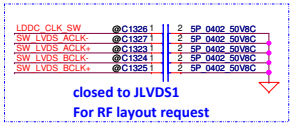
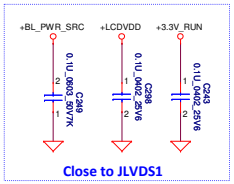
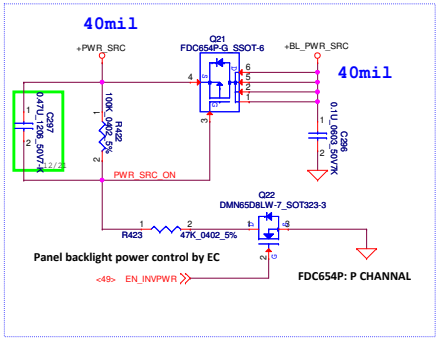
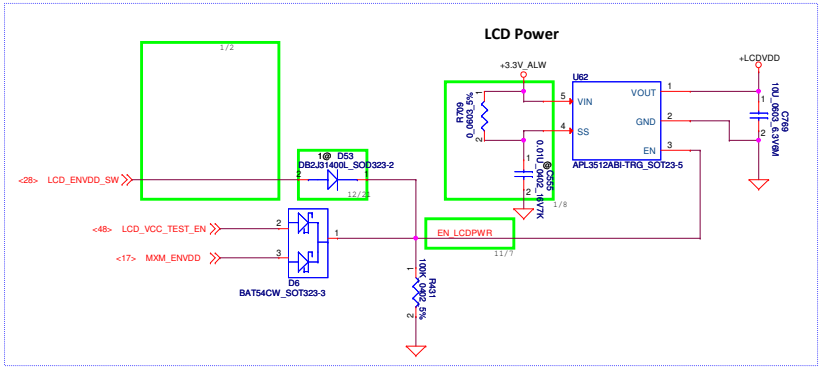
Date: Tuesday, January 15, 2013 | Sheet 29 of 65

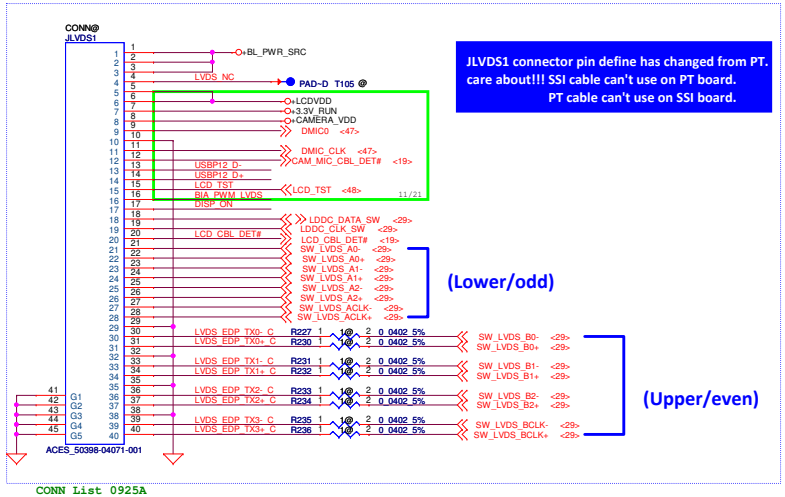


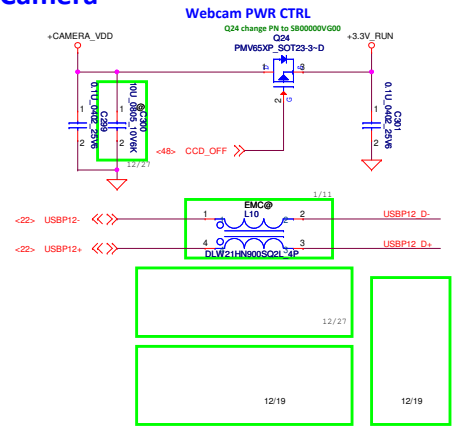



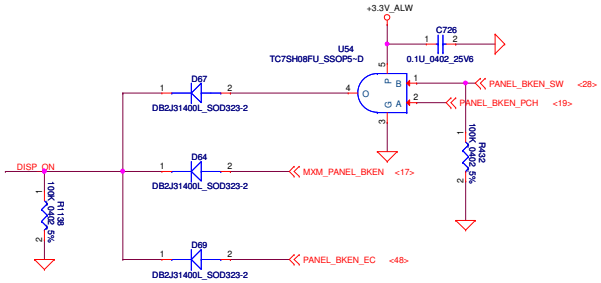



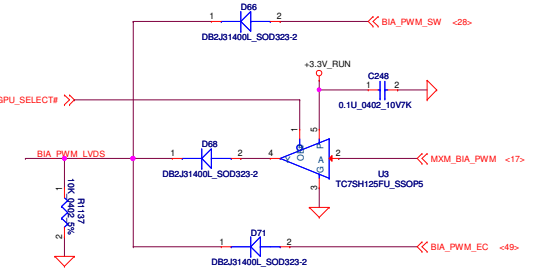

JLVDS1 connector pin define has changed from PT. care about!!! SSI cable can't use on PT board. PT cable can't use on SSI board.

CONN List 0925A

## Camera

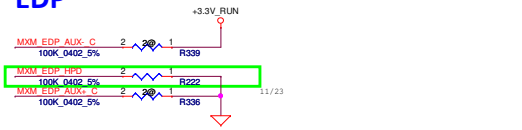


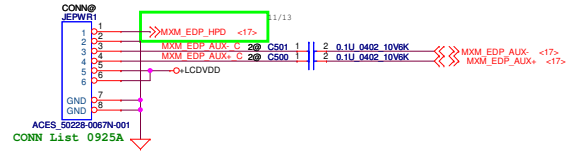



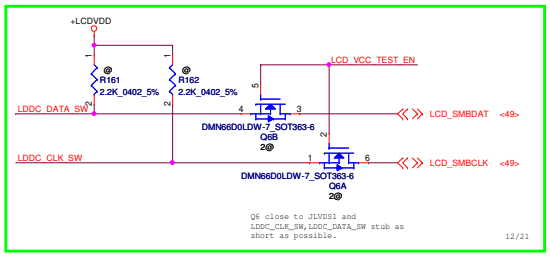

## EDP

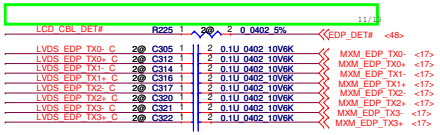
cable connect to GND for eDP panel supporting BIST pin




CONN List 0925A

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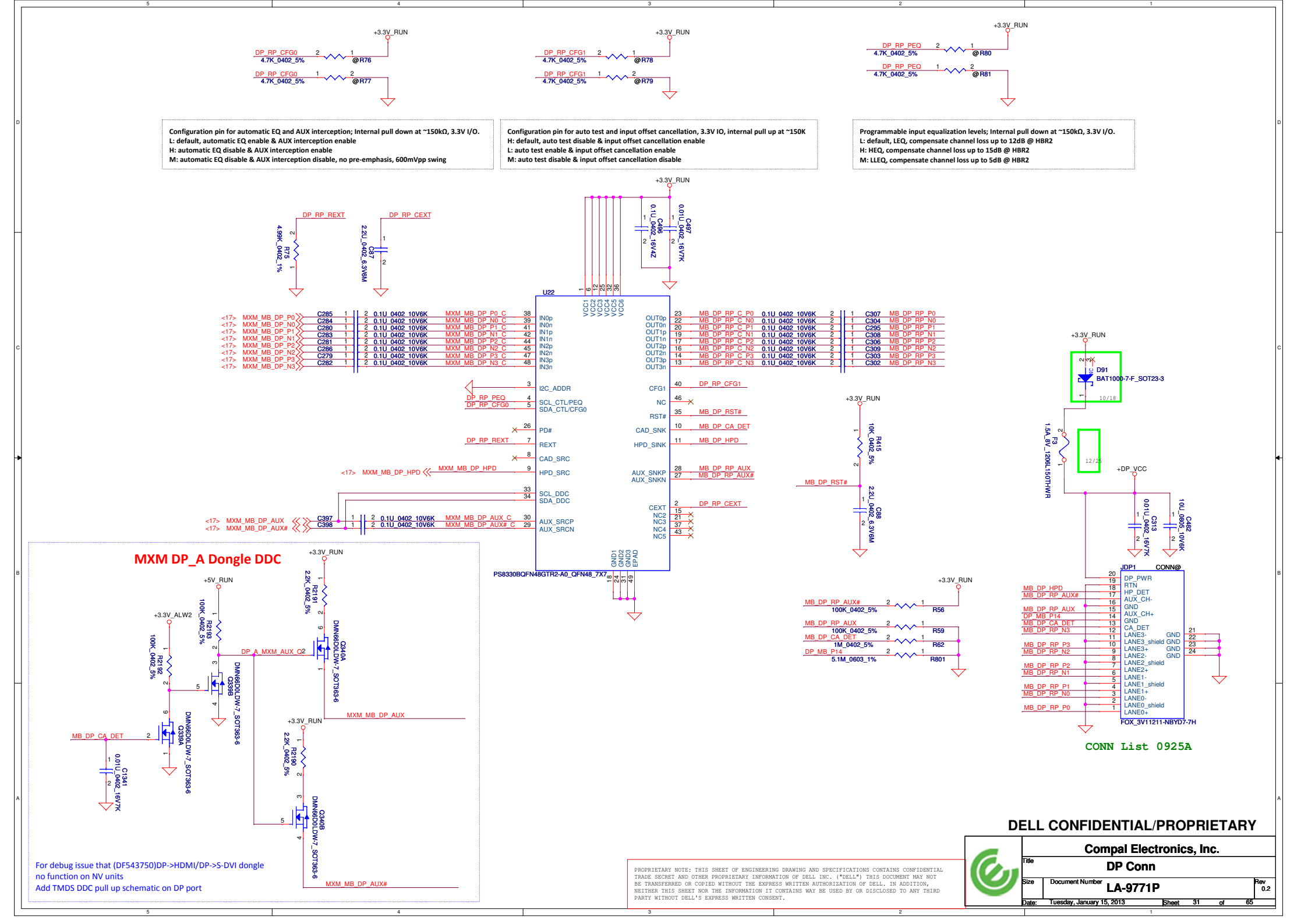
Compal Electronics, Inc.

Title: LVDS& CAM

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 30 of 65


+3.3V_RUN
DP_RP_CFG0
4.7K_0402_5%
@R76
@R77
DP_RP_CFG1
@R78
@R79
DP_RP_PEQ
@R80
@R81
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable
Programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2
DP_RP_REXT
DP_RP_CEXT
4.99K_0402_1%
R75
2.2U_0402_6.3V6M
C87
U22
PS8330BQFN48GTR2-A0_QFN48_7X7
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
0.1U_0402_16V4Z
C486
0.01U_0402_16V7K
C497
IN0p
IN0n
IN1p
IN1n
IN2p
IN2n
IN3p
IN3n
OUT0p
OUT0n
OUT1p
OUT1n
OUT2p
OUT2n
OUT3p
OUT3n
I2C_ADDR
SCL_CTL/PEQ
SDA_CTL/CFG0
PD#
REXT
CAD_SRC
HPD_SRC
SCL_DDC
SDA_DDC
AUX_SRCP
AUX_SRCN
CFG1
NC
RST#
CAD_SNK
HPD_SINK
AUX_SNKP
AUX_SNKN
CEXT
NC2
NC3
NC4
NC5
GND1
GND2
GND3
GND4
EPAD
0.1U_0402_10V6K
C285
C284
C280
C283
C281
C286
C279
C282
C397
C398
C307
C304
C295
C308
C306
C309
C303
C302
MB_DP_RP_C_P0
MB_DP_RP_C_N0
MB_DP_RP_C_P1
MB_DP_RP_C_N1
MB_DP_RP_C_P2
MB_DP_RP_C_N2
MB_DP_RP_C_P3
MB_DP_RP_C_N3
MB_DP_RST#
MB_DP_CA_DET
MB_DP_HPD
MB_DP_RP_AUX
MB_DP_RP_AUX#
DP_RP_CFG1
DP_RP_CEXT
R415
10K_0402_5%
C88
2.2U_0402_6.3V6M
D91
BAT1000-7-F_SOT23-3
F3
1.5A_8V_1206L150THWR
C313
0.01U_0402_16V7K
C482
10U_0805_10V6K
+DP_VCC
JDP1
CONN@
FOX_3V11211-NBYD7-7H
DP_PWR
RTN
HP_DET
AUX_CH-
GND
AUX_CH+
CA_DET
LANE3-
LANE3_shield
LANE3+
LANE2-
LANE2_shield
LANE2+
LANE1-
LANE1_shield
LANE1+
LANE0-
LANE0_shield
LANE0+
MB_DP_RP_P0
MB_DP_RP_N0
MB_DP_RP_P1
MB_DP_RP_N1
MB_DP_RP_P2
MB_DP_RP_N2
MB_DP_RP_P3
MB_DP_RP_N3
DP_MB_P14
100K_0402_5%
1M_0402_5%
5.1M_0603_1%
R56
R59
R62
R801
MXM DP_A Dongle DDC
+5V_RUN
+3.3V_ALW2
R2193
R2192
R2191
R2190
2.2K_0402_5%
DP_A_MXM_AUX_Q2
DMN66D0LDW-7_SOT363-6
Q339A
Q339B
Q340A
Q340B
MXM_MB_DP_AUX
MXM_MB_DP_AUX#
C1341
0.01U_0402_16V7K
For debug issue that (DF543750)DP->HDMI/DP->S-DVI dongle
no function on NV units
Add TMDS DDC pull up schematic on DP port
CONN List 0925A
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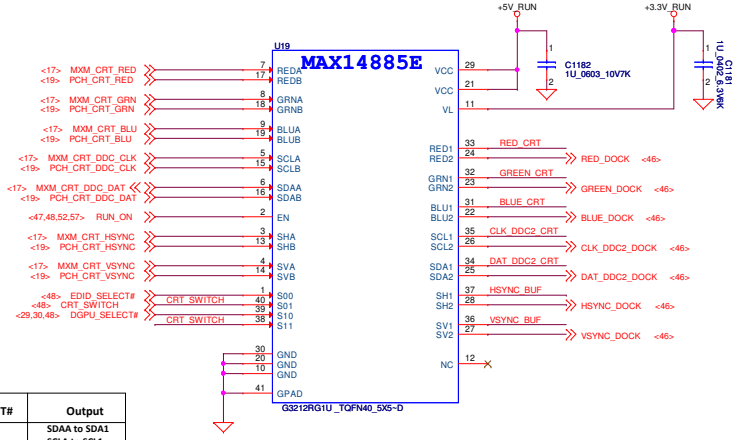
Compal Electronics, Inc.
Title
DP Conn
Size
Document Number
LA-9771P
Rev
0.2
Date:
Tuesday, January 15, 2013
Sheet
31
of
65

**Channel A --> MXM**

**Channel B --> PCH**

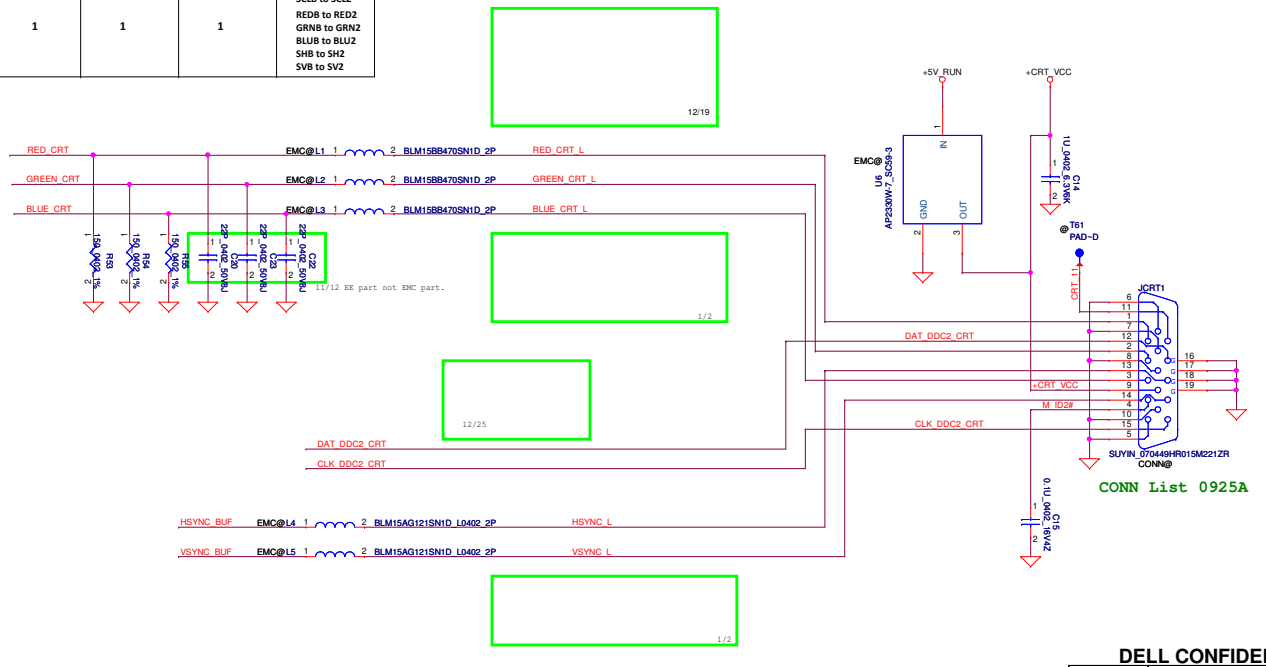



**Port 1 --> MB board CRT**

**Port 2 --> Docking Port RGB**

1009 need change symbol to G3212RG1U(SA00004IK00)

| | CRT_SWITCH | DGPU_SELECT# | EDID_SELECT# | Output |
|---|---|---|---|---|
| DSC mode output to MB VGA | 0 | 0 | 0 | SDAA to SDA1<br>SCLA to SCL1<br>REDA to RED1<br>GRNA to GRN1<br>BLUA to BLU1<br>SHA to SH1<br>SVA to SV1 |
| DSC mode output to docking VGA | 1 | 0 | 0 | SDAA to SDA2<br>SCLA to SCL2<br>REDA to RED2<br>GRNA to GRN2<br>BLUA to BLU2<br>SHA to SH2<br>SVA to SV2 |
| UMA mode output to MB VGA | 0 | 1 | 1 | SDAB to SDA1<br>SCLB to SCL1<br>REDB to RED1<br>GRNB to GRN1<br>BLUB to BLU1<br>SHB to SH1<br>SVB to SV1 |
| UMA mode output to docking VGA | 1 | 1 | 1 | SDAB to SDA2<br>SCLB to SCL2<br>REDB to RED2<br>GRNB to GRN2<br>BLUB to BLU2<br>SHB to SH2<br>SVB to SV2 |




CONN List 0925A

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Compal Electronics, Inc.

Title: VGA Conn

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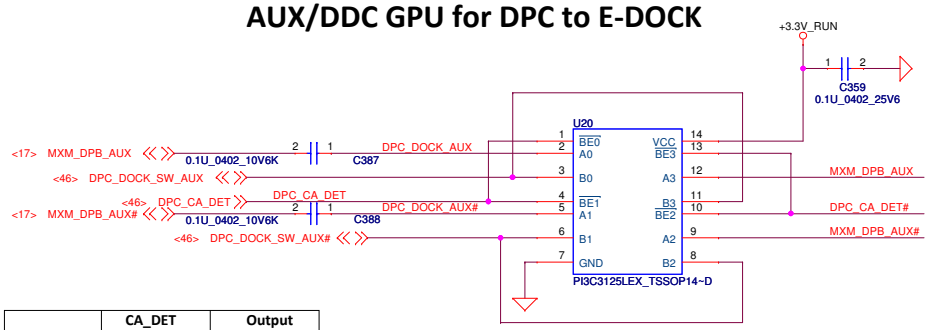
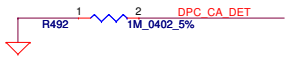
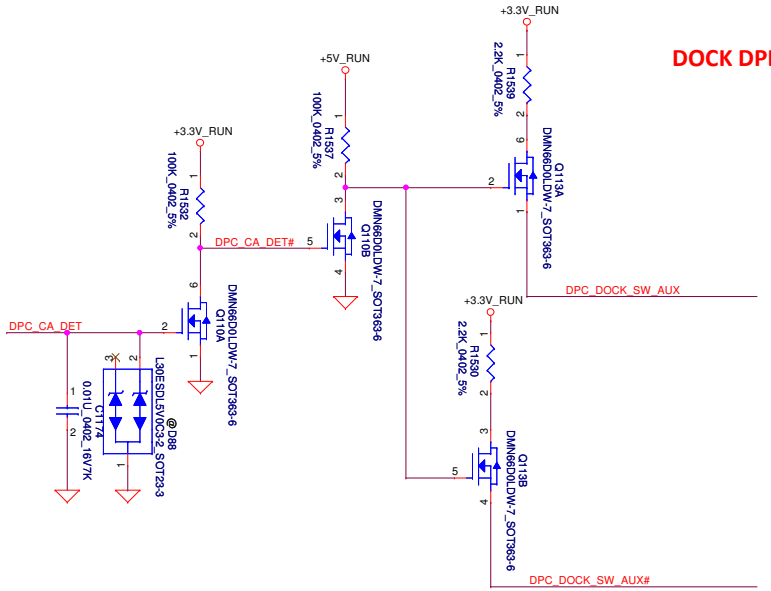
# AUX/DDC GPU for DPC to E-DOCK




| | CA_DET | Output |
|---|---|---|
| HDMI/DVI | 1 | A2=B2<br>A3=B3 |
| DP | 0 | A0=B0<br>A1=B1 |




# DOCK DPB(PORT2) DDC





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Compal Electronics, Inc.

Title: DP DDC SW

Size: | Document Number: LA-9771P | Rev: 0.2

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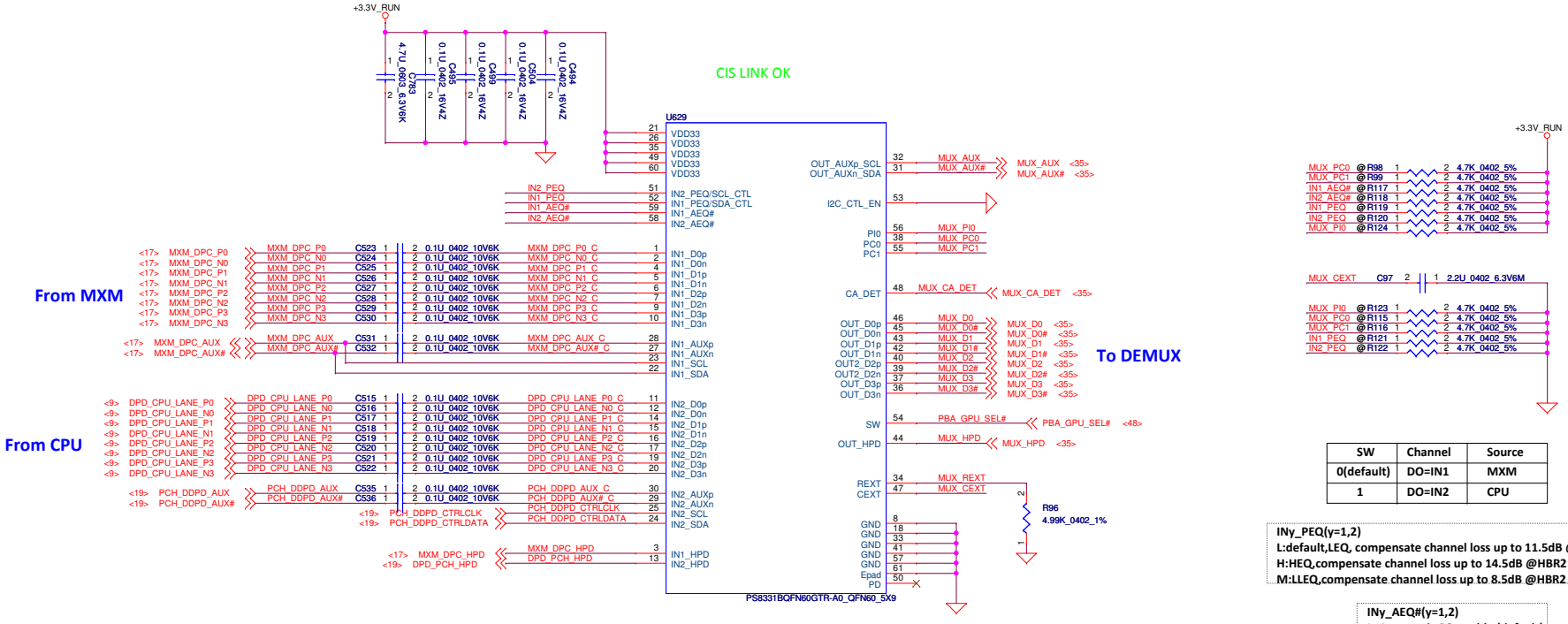



| SW | Channel | Source |
|---|---|---|
| 0(default) | DO=IN1 | MXM |
| 1 | DO=IN2 | CPU |

**INy_PEQ(y=1,2)**
L:default,LEQ, compensate channel loss up to 11.5dB @HBR2
H:HEQ,compensate channel loss up to 14.5dB @HBR2
M:LLEQ,compensate channel loss up to 8.5dB @HBR2

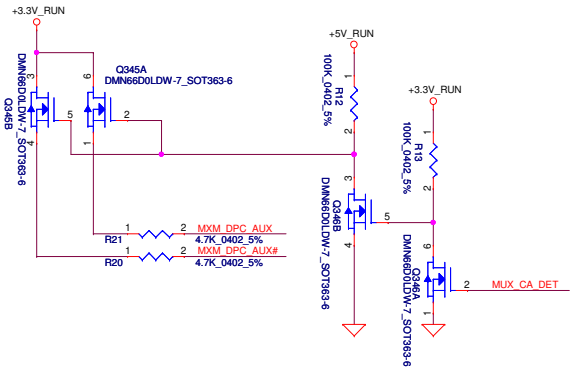
**INy_AEQ#(y=1,2)**
L: Automatic EQ enable (default)
H: Automatic EQ disable

**PI0**
L: Auto test disable & input offset cancellation enable (default)
H: Auto test enable & input offset cancellation enable
M: Auto test disable & input offset cancellation disable

**PC0**
L: AUX interception enable, driver configuration is set by link training (default)
H: AUX interception disable, driver output with fixed 800mV and 0dB
M: AUX interception disable, driver output with fixed 400mV and 0dB

**PC1**
L: default
H: Output swing +20%
M: Output swing -16.7%

## DOCK DPA(PORT1) DDC & HDMI DDC-before PS8331

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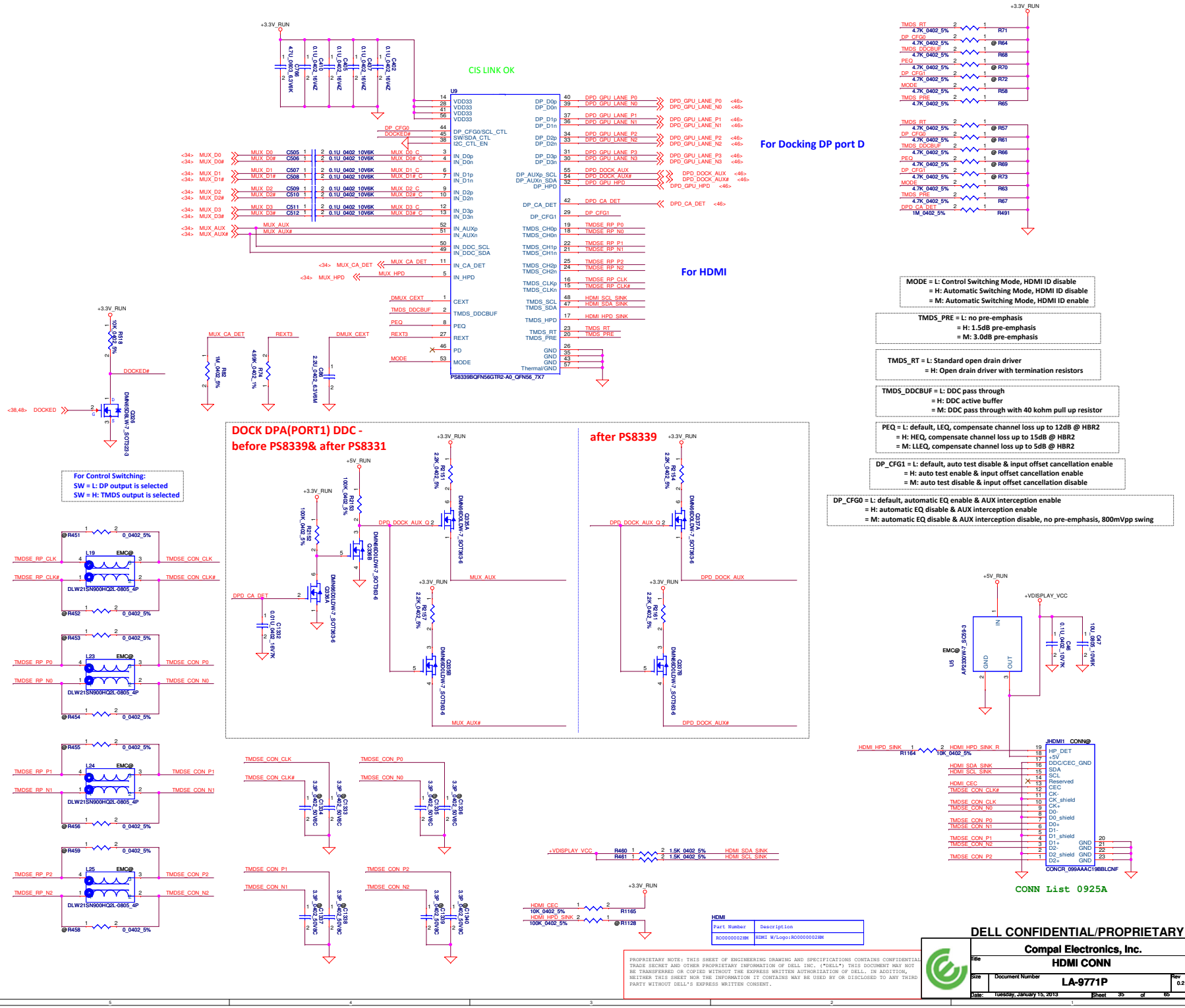
Compal Electronics, Inc.

Title: DP MUX

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 34 of 65


CIS LINK OK
For Docking DP port D
For HDMI
DOCK DPA(PORT1) DDC - before PS8339& after PS8331
after PS8339
For Control Switching:
SW = L: DP output is selected
SW = H: TMDS output is selected
MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable
TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis
TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors
TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor
PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2
DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable
DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
CONN List 0925A
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
HDMI CONN
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Tuesday, January 15, 2013
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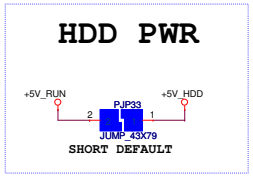


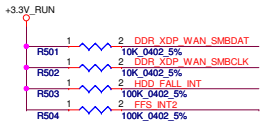


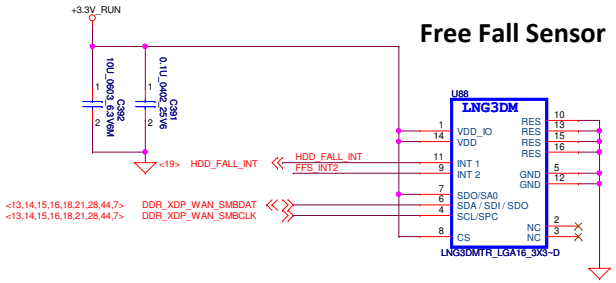


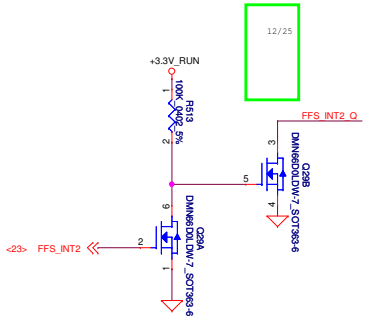


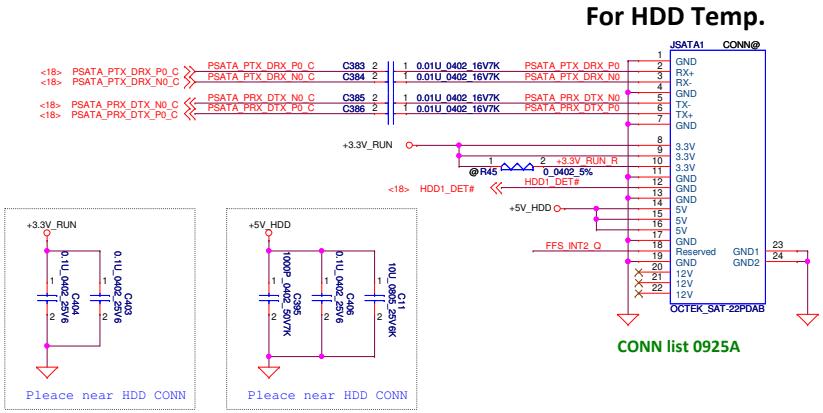


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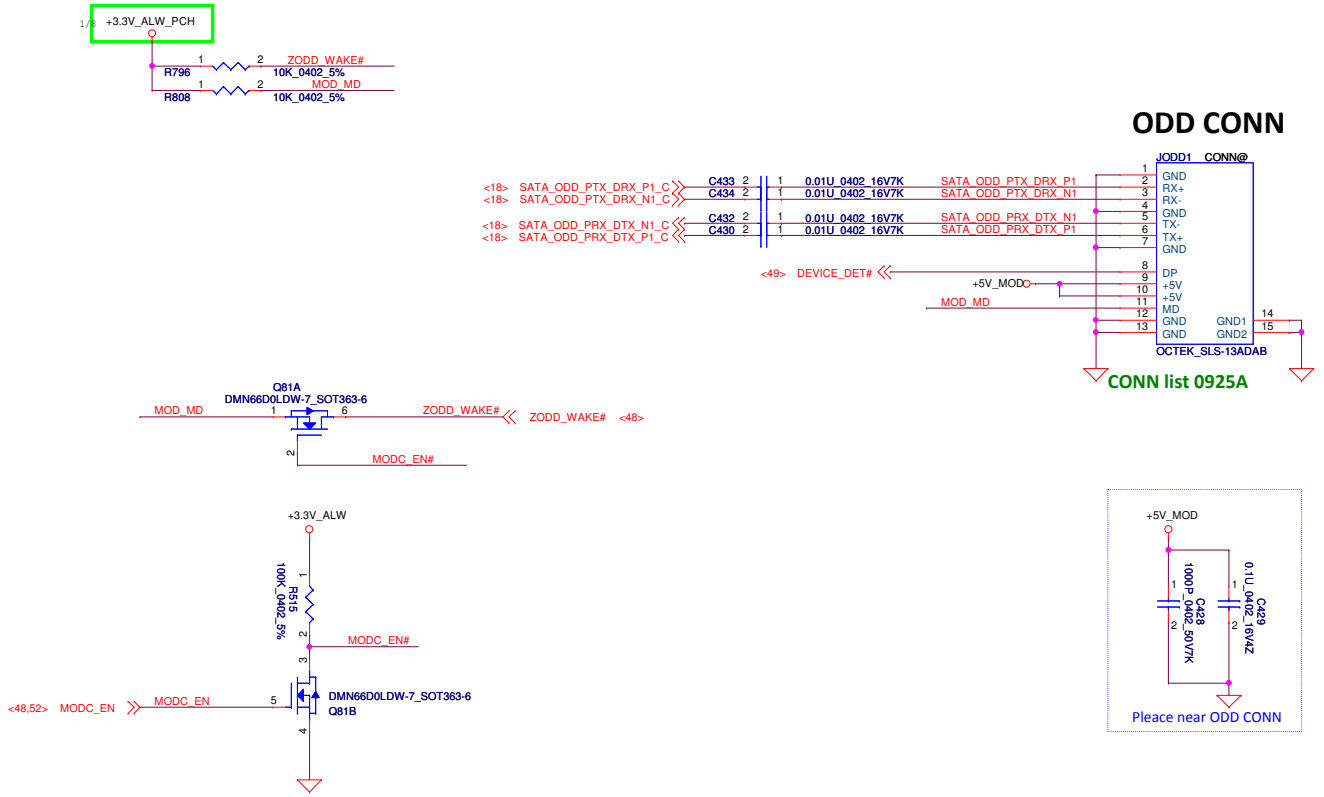
Compal Electronics, Inc.

Title: HDD CONN

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 36 of 65

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| | |
|---|---|
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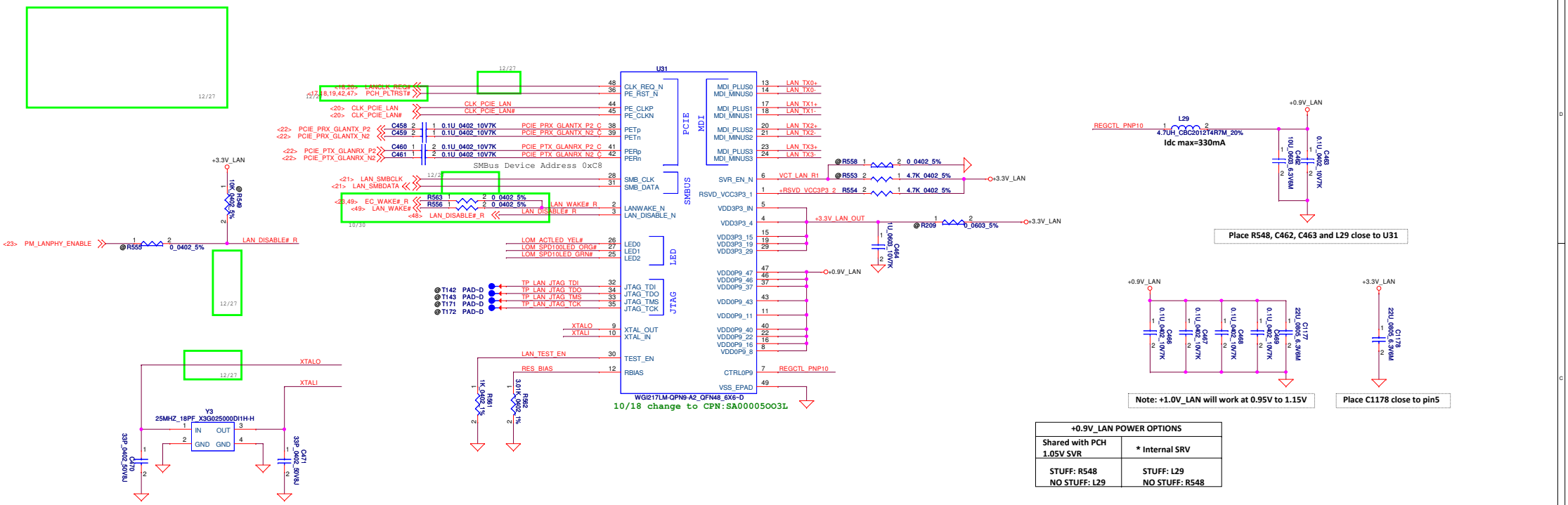
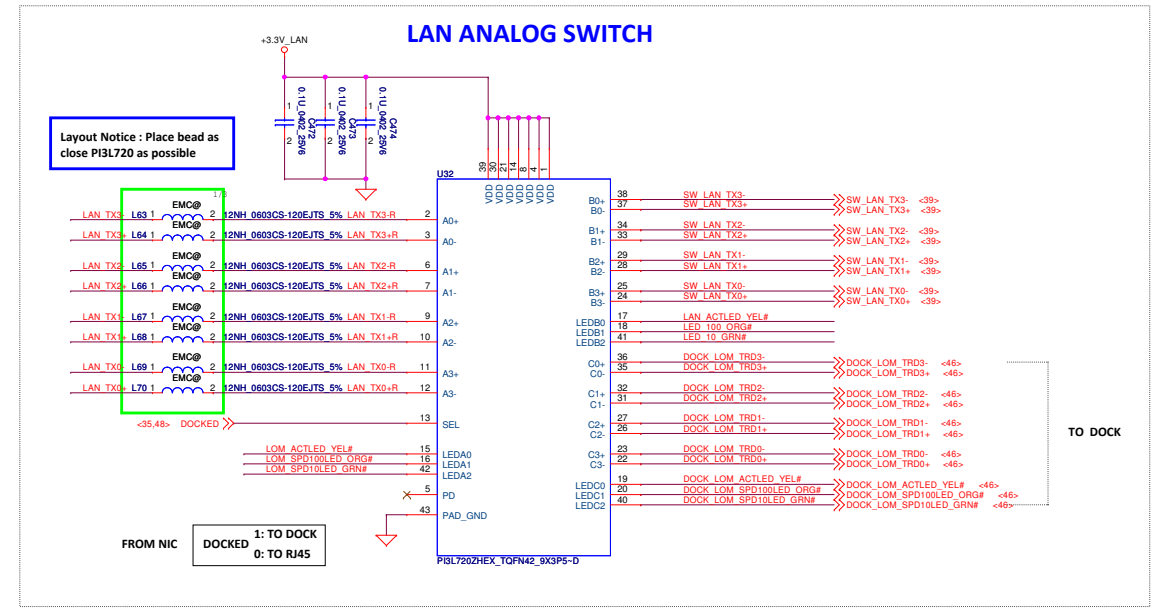
| Title | ODD CONN |
| Size | Document Number: LA-9771P |
| Rev | 0.2 |
| Date: | Tuesday, January 15, 2013 |
| Sheet | 37 of 65 |




| +0.9V_LAN POWER OPTIONS | |
|---|---|
| Shared with PCH 1.05V SVR | * Internal SRV |
| STUFF: R548<br>NO STUFF: L29 | STUFF: L29<br>NO STUFF: R548 |



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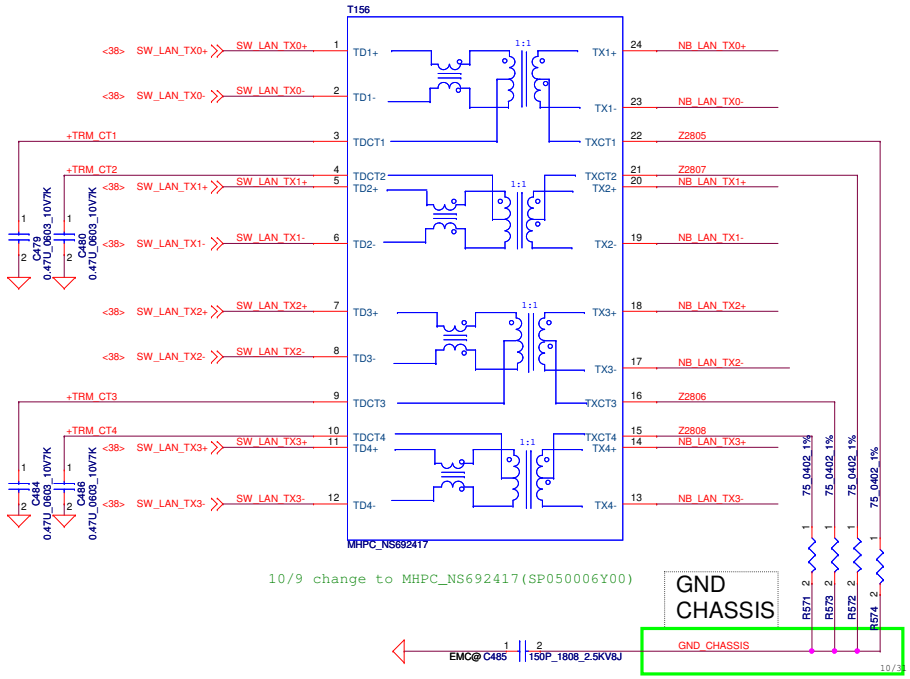
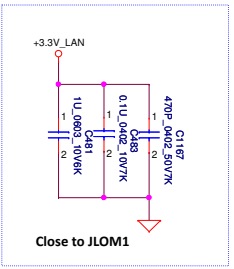
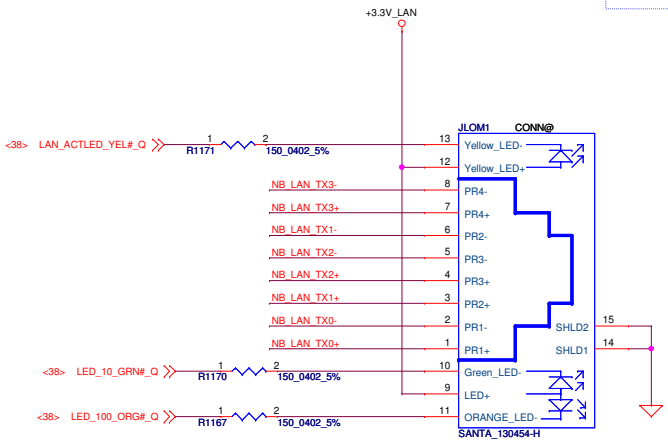
| | | |
|---|---|---|
| Title | LAN/LAN SW | |
| Size | Document Number LA-9771P | Rev 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 38 of 65 | |




+3.3V_LAN:20mils




CONN List 0925A

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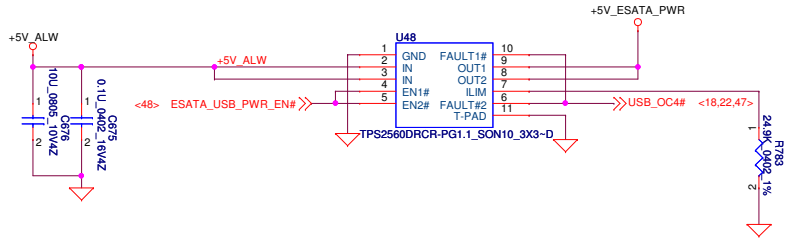
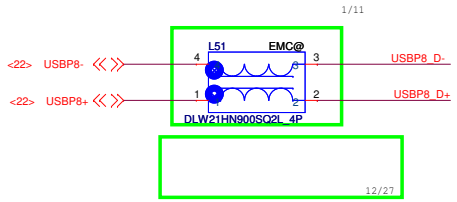
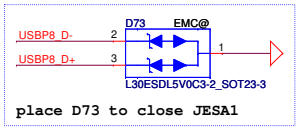
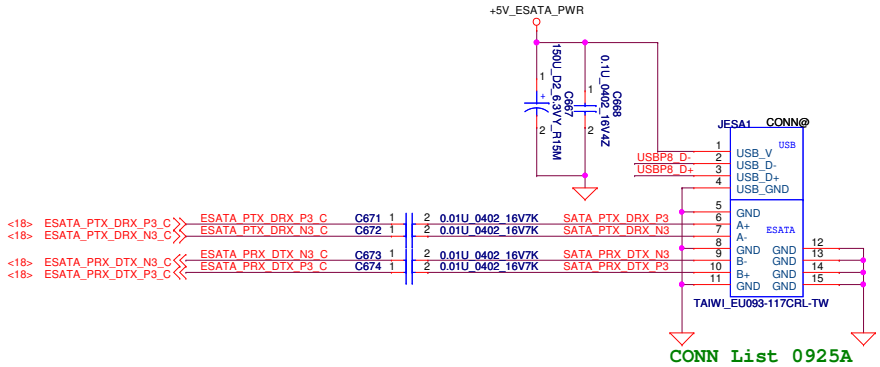
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: RJ45 | | |
| Size | Document Number: LA-9771P | Rev: 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 39 of 65 | |

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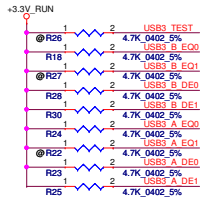
| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: ESATA | | |
| Size | Document Number: LA-9771P | Rev: 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 40 of 65 | |



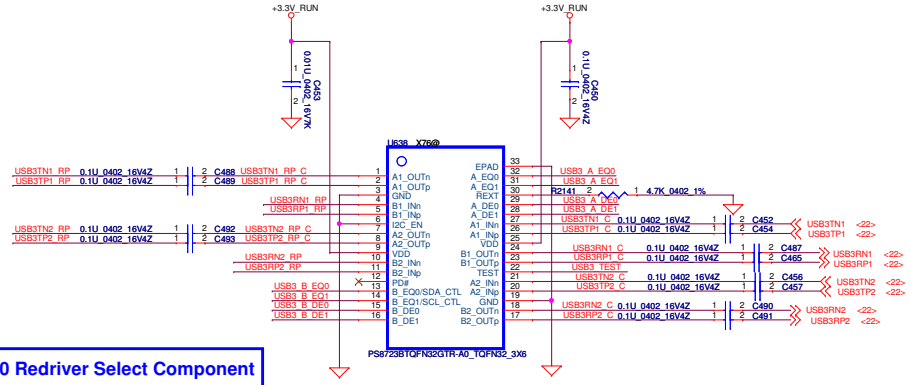

11/30

EQ : Equalizer control and program,
3.3V tolerant. Internally pulled down at ~150K ohm
[A_EQ1, A_EQ0] = [B_EQ1, B_EQ0]=
LL: program EQ for channel loss up to 9.5dB
LH: program EQ for channel loss up to 13dB
HL: program EQ for channel loss up to 4.5dB
HH: program EQ for channel loss up to 7.5dB

TEST : Chip test mode enable.
3.3V tolerant. Internally pulled down at ~150K ohm.
L: Normal operation (default)
H: Test mode enable
for compliance test, this pin should be pulled to high.

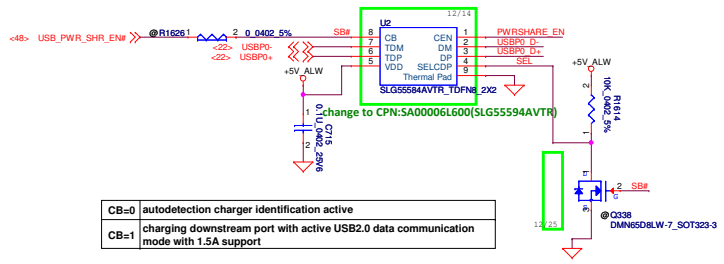
DE : Programmable output pre-emphasis level setting,
3.3V tolerant. Internally pulled down at ~150K ohm
[A_DE1, A_DE0] =[B_DE1, B_DE0]=
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

Pin 13 : B_EQ0 / SDA_CTL
Pin 14 : B_EQ1 / SCL_CTL
Pin 15 : B_DE0 / I2C_ADDR0
Pin 16 : B_DE1 / I2C_ADDR1
Pin28 : A_DE1 / NC
Pin29 : A_DE0 / NC
Pin31 : A_EQ1 / NC
Pin32 : A_EQ0 / NC




| USB3.0 Redriver Select Component | | |
|---|---|---|
| | X76(Main)<br>X76xxxxxxxx<br>PS8723B<br>SA000064P00 | X76(2nd)<br>X76xxxxxxxx<br>PTN36242LBS<br>SA000060K0L |
| U638 | V | V |
| R22 | | V |
| R27 | | V |

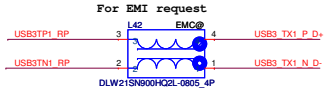
PD# : chip power down, active LOW, 3.3V tolerant, internally pulled up at ~ 150K ohm.



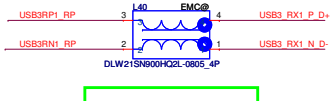

| CB | SELCDP | Function |
|---|---|---|
| 0 | X | DCP autodetect with mouse/keyboard wakeup |
| 1 | 0 | S0 charging with SDP only |
| 1 | 1 | S0 charging with CDP or SDP only (depending on external device) |

| | |
|---|---|
| CB=0 | autodetection charger identification active |
| CB=1 | charging downstream port with active USB2.0 data communication mode with 1.5A support |

For EMI request

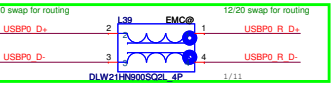



12/25




12/25

12/20 swap for routing

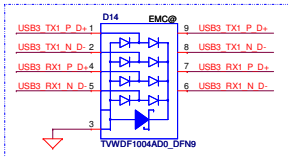



1/11

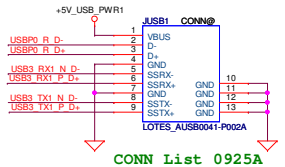
12/20 swap for routing

12/25

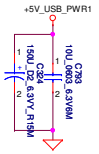
For ESD request

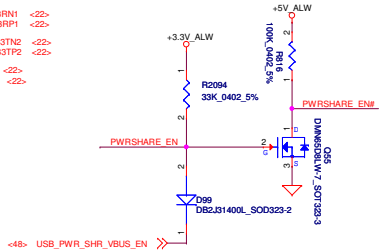


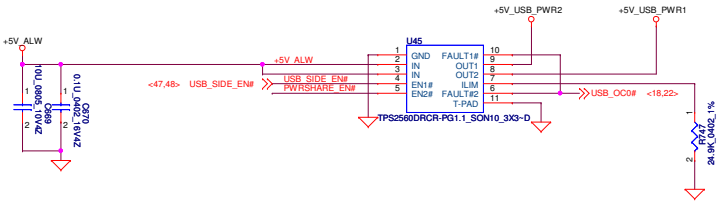

place D14,D15 to close JUSB1



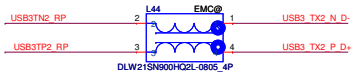

CONN List 0925A



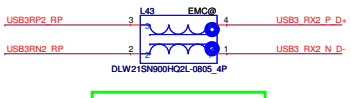



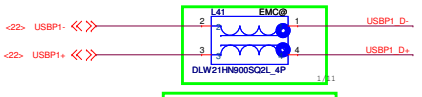

For EMI request




12/25



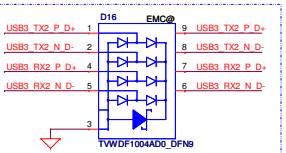

12/25



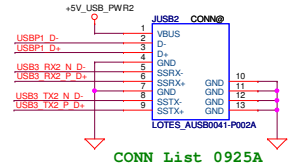

1/11

12/25

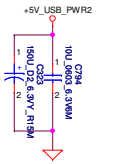
For ESD request




place D16,D17 to close JUSB2




CONN List 0925A

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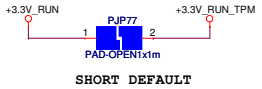
Compal Electronics, Inc.

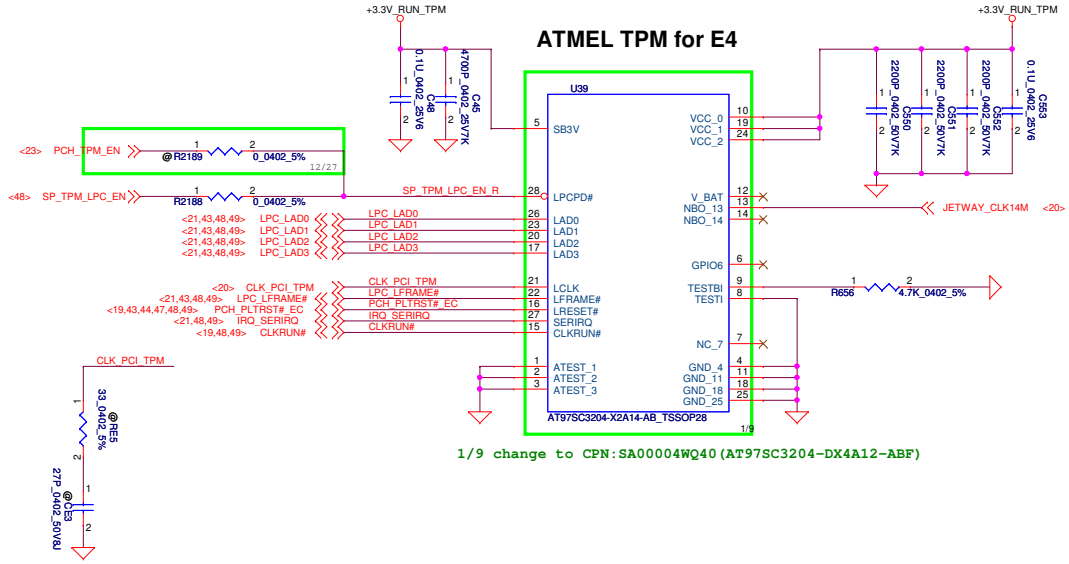
Title: USB3.0

Size: | Document Number: LA-9771P | Rev: 0.2

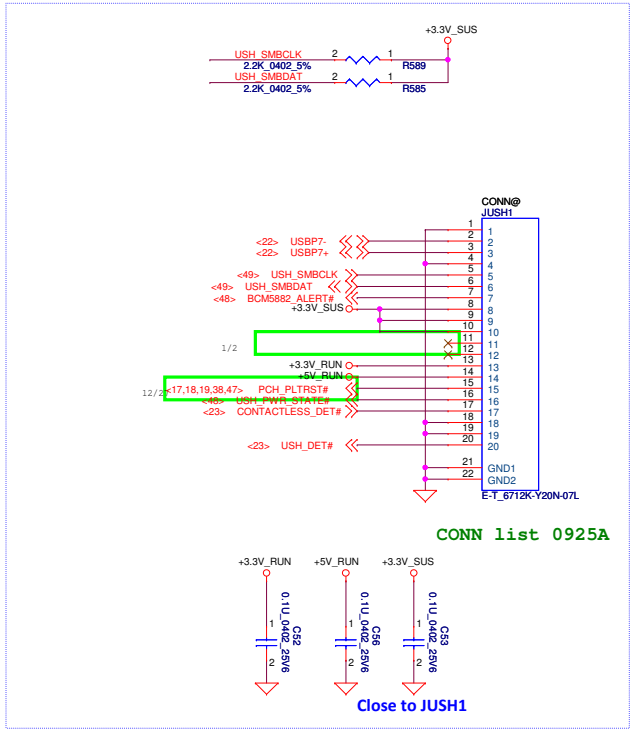
Date: Tuesday, January 15, 2013 | Sheet 41 of 65

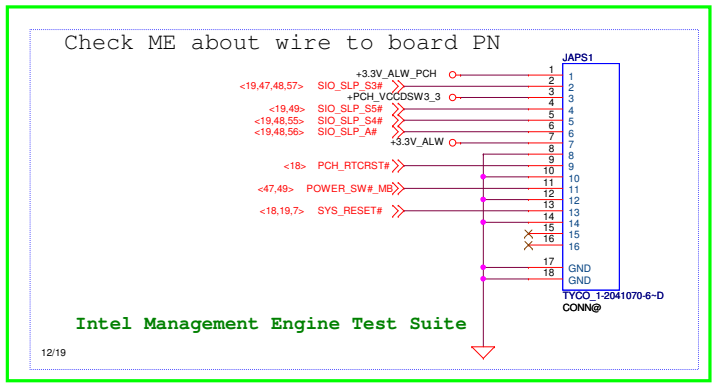



**SHORT DEFAULT**




1/9 change to CPN:SA00004WQ40(AT97SC3204-DX4A12-ABF)

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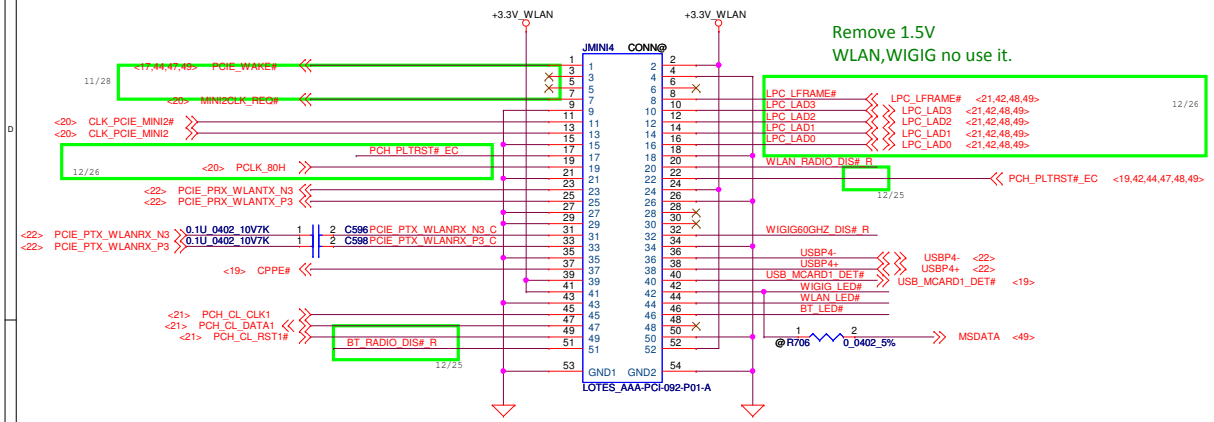
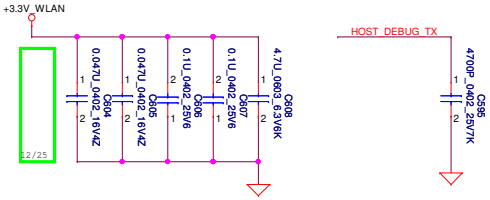
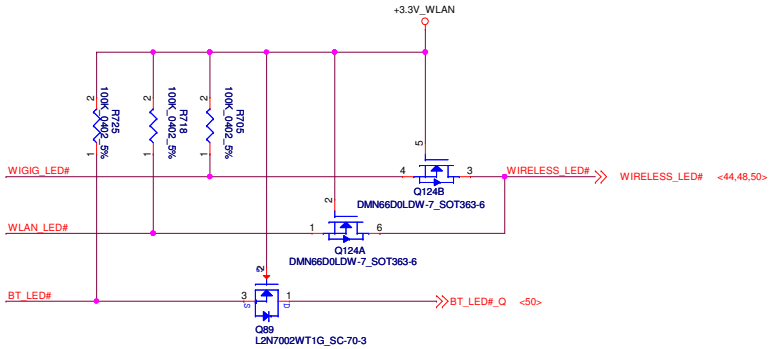
| Compal Electronics, Inc. | | |
| Title: TPM | | |
| Size | Document Number: LA-9771P | Rev: 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 42 of 65 | |

# Mini WLAN/WiGig H=4

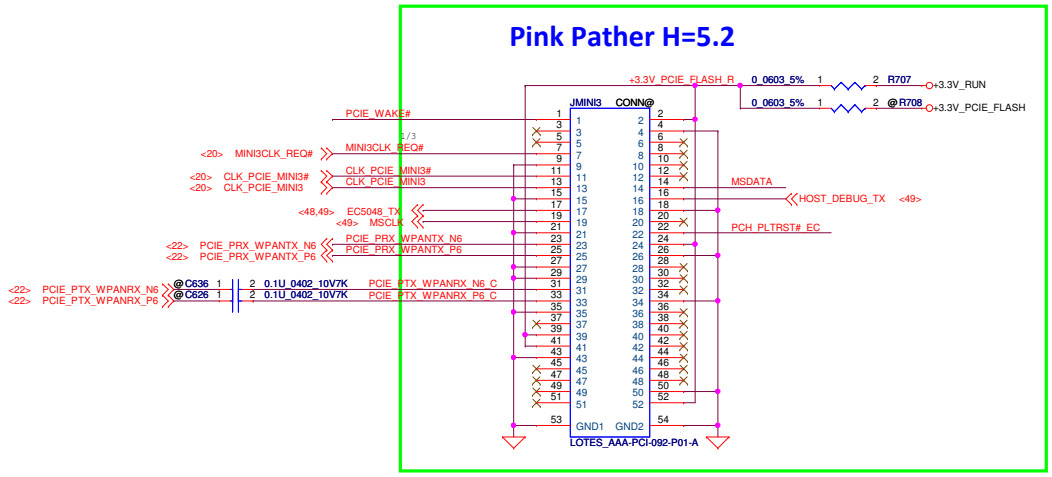


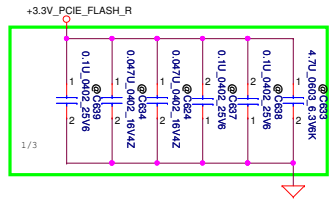

CONN List 0925A






# Pink Pather H=5.2




CONN List 0925A

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Compal Electronics, Inc.

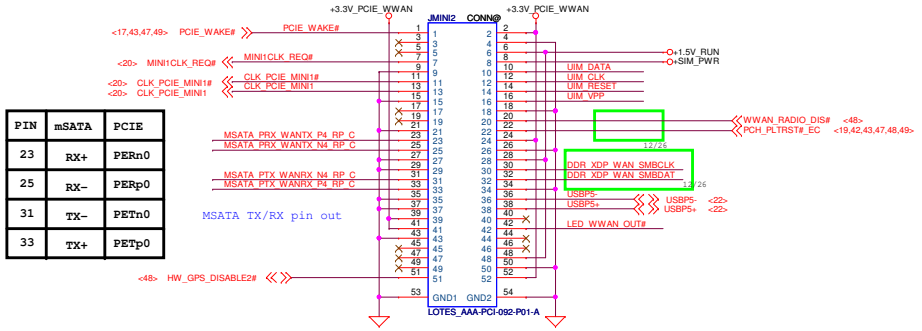
Title: Mini Card-1/2

Size: | Document Number: LA-9771P | Rev: 0.2

Date: Tuesday, January 15, 2013 | Sheet 43 of 65

## SIM Card Push-Push

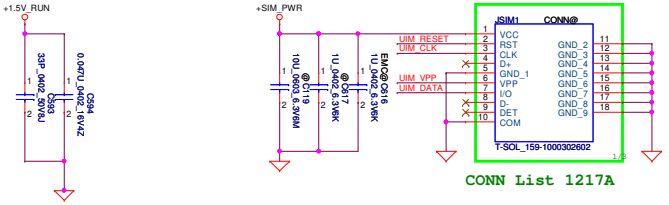
## Mini WWAN/GPS/LTE/mSATA



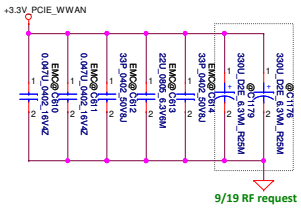

| PIN | mSATA | PCIE |
|---|---|---|
| 23 | RX+ | PERn0 |
| 25 | RX- | PERp0 |
| 31 | TX- | PETn0 |
| 33 | TX+ | PETp0 |

MSATA TX/RX pin out

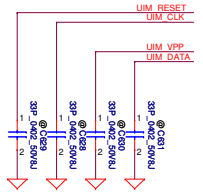
CONN List 0925A

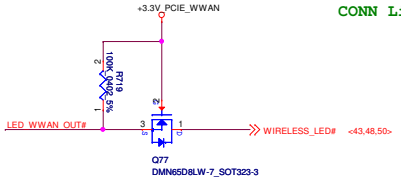


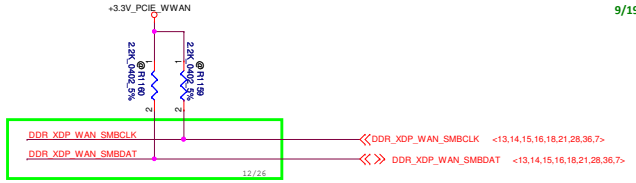

CONN List 1217A

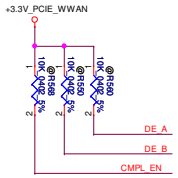



9/19 RF request



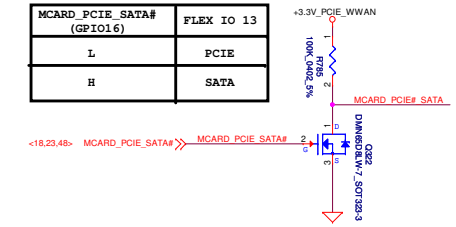



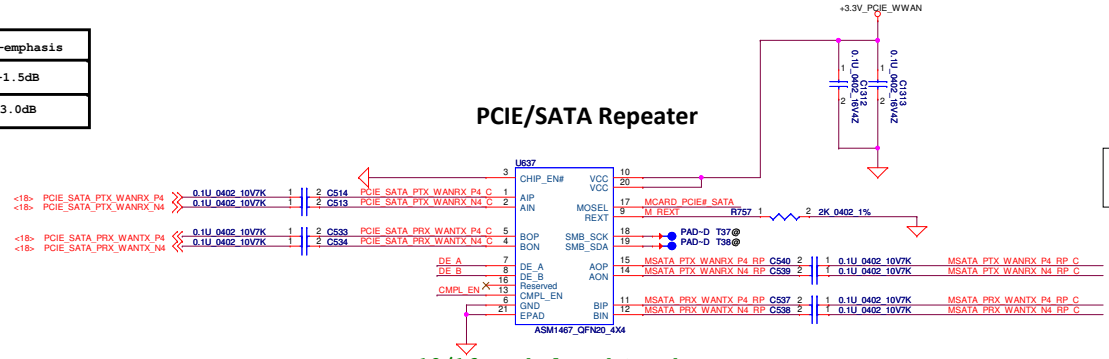

| CHIP_EN# | Funtion |
|---|---|
| 0 | Normal mode |
| 1 | power down mode |

| DE_A/DE_B | de-emphasis |
|---|---|
| 0(default) | +1.5dB |
| 1 | +3.0dB |

| MCARD_PCIE_SATA# (GPIO16) | FLEX IO 13 |
|---|---|
| L | PCIE |
| H | SATA |




## PCIE/SATA Repeater




10/16 symbol update ok.

MOSEL 1: PCIE redriver
0: SATA redriver

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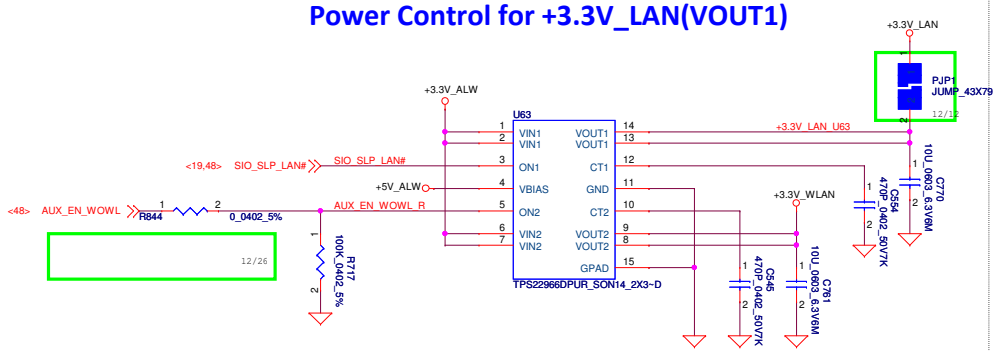
Compal Electronics, Inc.

Title: Mini Card-2/2

Size | Document Number: LA-9771P | Rev: 0.2

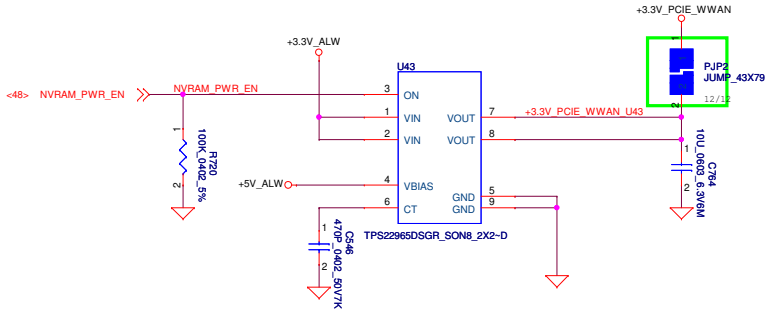
Date: Tuesday, January 15, 2013 | Sheet 44 of 65

## Power Control for +3.3V_LAN(VOUT1)

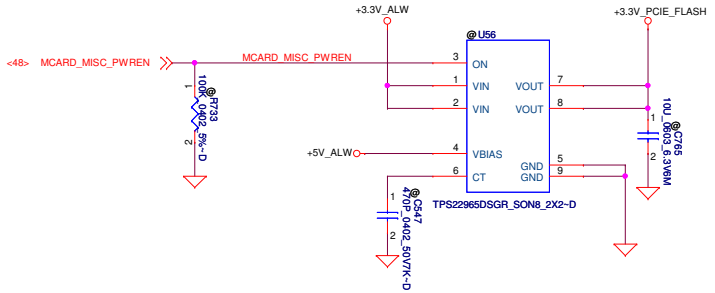



## Power Control for Mini card2(VOUT2)

## Power Control for Mini card1




## Power Control for Mini card3

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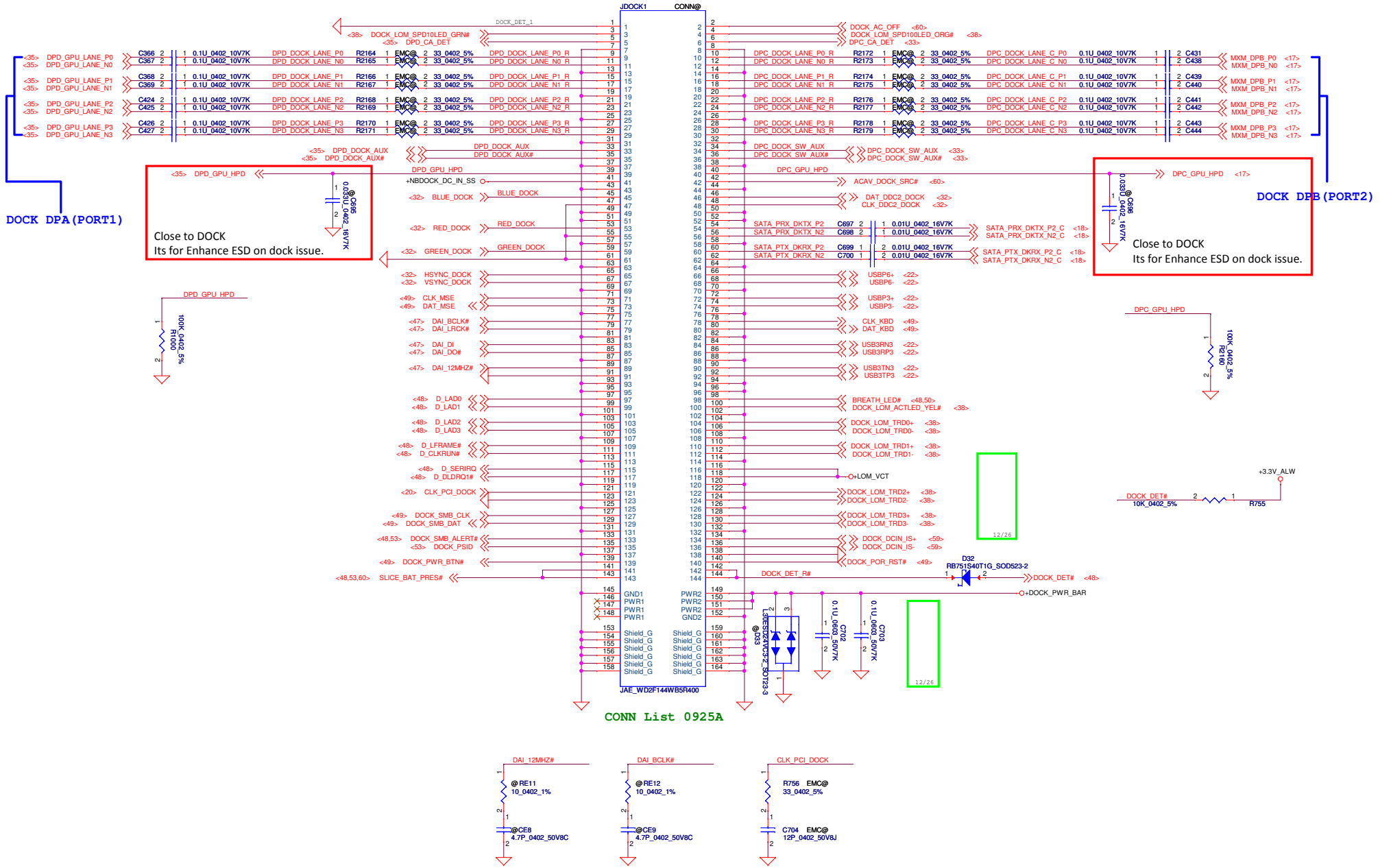
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | Mini Card PWR |
| Size / Document Number | LA-9771P |
| Rev | 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 45 of 65 |

EMI request add 33ohm for DOCK DVI signals.







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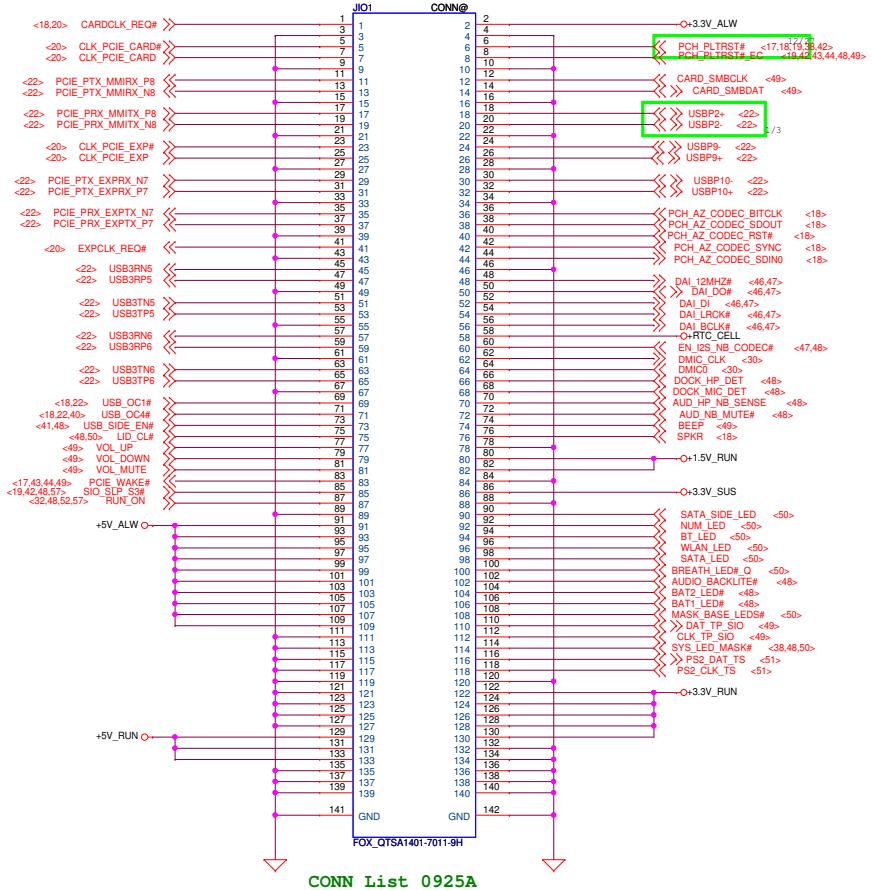
Compal Electronics, Inc.

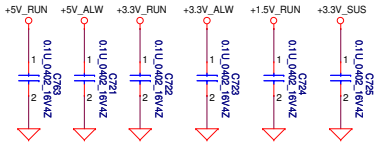
Title: Docking

Size: | Document Number: LA-9771P | Rev: 0.2

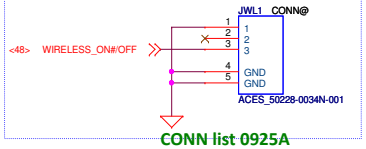
Date: Tuesday, January 15, 2013 | Sheet 46 of 65




CONN List 0925A

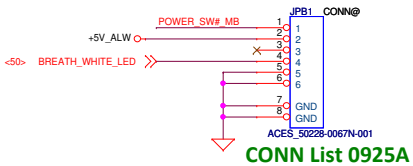



## WireLess ON/OFF CONN



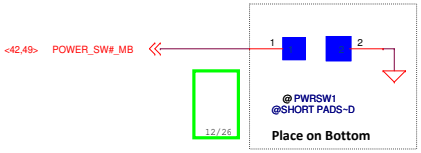

CONN list 0925A

## Power Button CONN




CONN List 0925A

## Power Switch for debug

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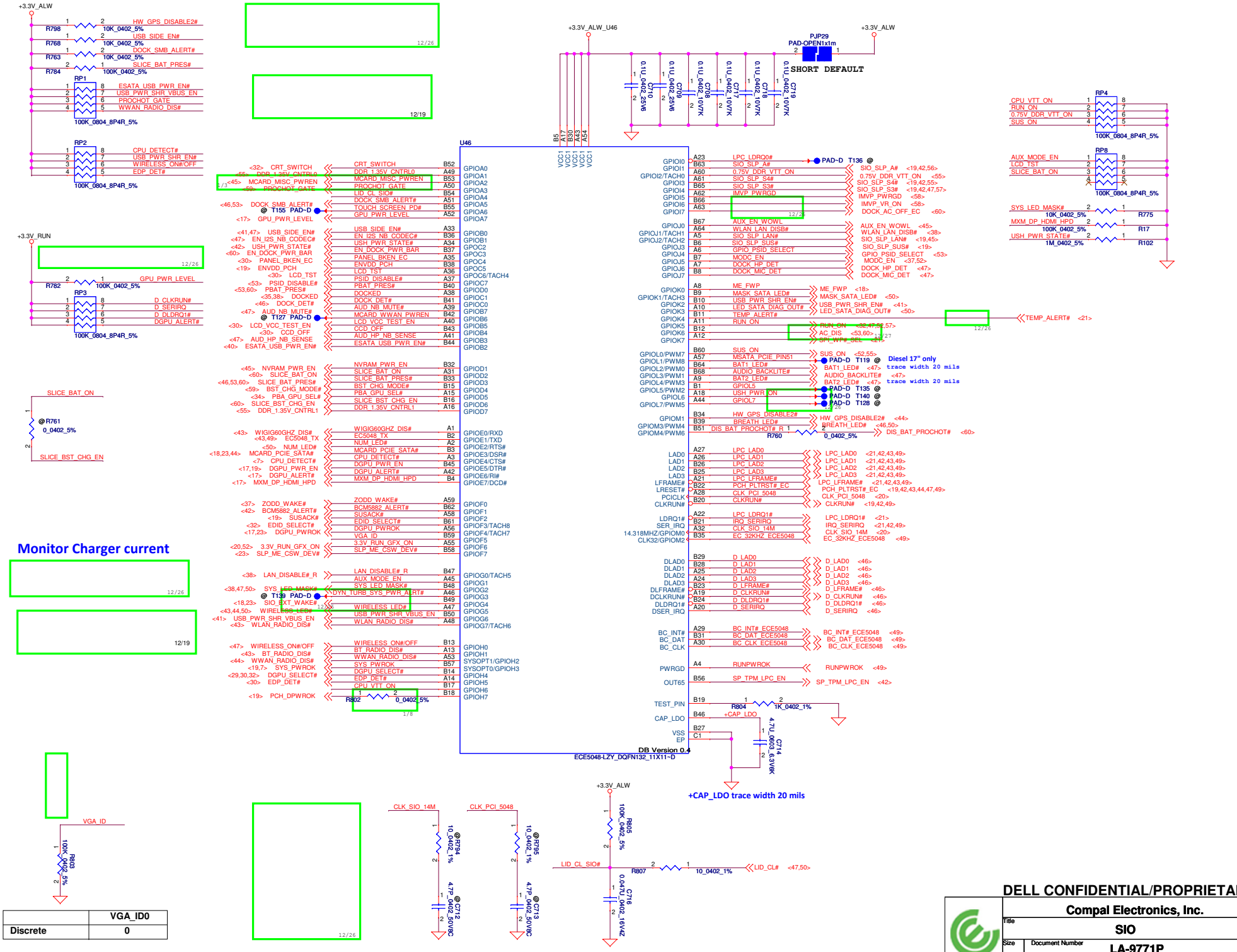
Compal Electronics, Inc.

| | | |
|---|---|---|
| Title | I/O board | |
| Size | Document Number LA-9771P | Rev 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 47 of 65 | |


+3.3V_ALW
HW_GPS_DISABLE2#
USB_SIDE_EN#
DOCK_SMB_ALERT#
SLICE_BAT_PRES#
ESATA_USB_PWR_EN#
USB_PWR_SHR_VBUS_EN
PROCHOT_GATE
WWAN_RADIO_DIS#
CPU_DETECT#
USB_PWR_SHR_EN#
WIRELESS_ON#/OFF
EDP_DET#
+3.3V_RUN
GPU_PWR_LEVEL
D_CLKRUN#
D_SERIRQ
D_DLDRQ1#
DGPU_ALERT#
SLICE_BAT_ON
SLICE_BST_CHG_EN
Monitor Charger current
VGA_ID
VGA_ID0
Discrete
0
+3.3V_ALW_U46
PJP29
PAD-OPEN1x1m
SHORT DEFAULT
U46
CRT_SWITCH
DDR_1.35V_CNTRL0
MCARD_MISC_PWREN
PROCHOT_GATE
LID_CL_SIO#
DOCK_SMB_ALERT#
TOUCH_SCREEN_PD#
GPU_PWR_LEVEL
USB_SIDE_EN#
EN_I2S_NB_CODEC#
USH_PWR_STATE#
EN_DOCK_PWR_BAR
PANEL_BKEN_EC
ENVDD_PCH
LCD_TST
PSID_DISABLE#
PBAT_PRES#
DOCKED
DOCK_DET#
AUD_NB_MUTE#
MCARD_WWAN_PWREN
LCD_VCC_TEST_EN
CCD_OFF
AUD_HP_NB_SENSE
ESATA_USB_PWR_EN#
NVRAM_PWR_EN
SLICE_BAT_ON
SLICE_BAT_PRES#
BST_CHG_MODE#
PBA_GPU_SEL#
SLICE_BST_CHG_EN
DDR_1.35V_CNTRL1
WIGIG60GHZ_DIS#
EC5048_TX
NUM_LED#
MCARD_PCIE_SATA#
CPU_DETECT#
DGPU_PWR_EN
DGPU_ALERT#
MXM_DP_HDMI_HPD
ZODD_WAKE#
BCM5882_ALERT#
SUSACK#
EDID_SELECT#
DGPU_PWROK
VGA_ID
3.3V_RUN_GFX_ON
SLP_ME_CSW_DEV#
LAN_DISABLE#_R
AUX_MODE_EN
SYS_LED_MASK#
DYN_TURB_SYS_PWR_ALRT#
SIO_EXT_WAKE#
WIRELESS_LED#
USB_PWR_SHR_VBUS_EN
WLAN_RADIO_DIS#
WIRELESS_ON#/OFF
BT_RADIO_DIS#
WWAN_RADIO_DIS#
SYS_PWROK
DGPU_SELECT#
EDP_DET#
CPU_VTT_ON
PCH_DPWROK
GPIOA0 GPIOA1 GPIOA2 GPIOA3 GPIOA4 GPIOA5 GPIOA6 GPIOA7
GPIOB0 GPIOB1 GPIOC2 GPOC3 GPOC4 GPOC5 GPOC6/TACH4 GPIOC7 GPIOD0 GPIOC1 GPIOC0 GPIOB7 GPIOB6 GPIOB5 GPIOB4 GPIOB3 GPIOB2
GPIOD1 GPIOD2 GPIOD3 GPIOD4 GPIOD5 GPIOD6 GPIOD7
GPIOE0/RXD GPIOE1/TXD GPIOE2/RTS# GPIOE3/DSR# GPIOE4/CTS# GPIOE5/DTR# GPIOE6/RI# GPIOE7/DCD#
GPIOF0 GPIOF1 GPIOF2 GPIOF3/TACH8 GPIOF4/TACH7 GPIOF5 GPIOF6 GPIOF7
GPIOG0/TACH5 GPIOG1 GPIOG2 GPIOG3 GPIOG4 GPIOG5 GPIOG6 GPIOG7/TACH6
GPIOH0 GPIOH1 SYSOPT1/GPIOH2 SYSOPT0/GPIOH3 GPIOH4 GPIOH5 GPIOH6 GPIOH7
GPIOI0 GPIOI1 GPIOI2/TACH0 GPIOI3 GPIOI4 GPIOI5 GPIOI6 GPIOI7
GPIOJ0 GPIOJ1/TACH1 GPIOJ2/TACH2 GPIOJ3 GPIOJ4 GPIOJ5 GPIOJ6 GPIOJ7
GPIOK0 GPIOK1/TACH3 GPIOK2 GPIOK3 GPIOK4 GPIOK5 GPIOK6 GPIOK7
GPIOL0/PWM7 GPIOL1/PWM8 GPIOL2/PWM0 GPIOL3/PWM1 GPIOL4/PWM3 GPIOL5/PWM2 GPIOL6 GPIOL7/PWM5
GPIOM1 GPIOM3/PWM4 GPIOM4/PWM6
LAD0 LAD1 LAD2 LAD3 LFRAME# LRESET# PCICLK CLKRUN#
LDRQ1# SER_IRQ 14.318MHZ/GPIOM0 CLK32/GPIOM2
DLAD0 DLAD1 DLAD2 DLAD3 DLFRAME# DCLKRUN# DLDRQ1# DSER_IRQ
BC_INT# BC_DAT BC_CLK
PWRGD OUT65
TEST_PIN CAP_LDO VSS EP
DB Version 0.4
ECE5048-LZY_DQFN132_11X11-D
+CAP_LDO trace width 20 mils
Diesel 17" only
trace width 20 mils
CPU_VTT_ON RUN_ON 0.75V_DDR_VTT_ON SUS_ON
AUX_MODE_EN LCD_TST SLICE_BAT_ON
SYS_LED_MASK# MXM_DP_HDMI_HPD USH_PWR_STATE#
CLK_SIO_14M CLK_PCI_5048
LID_CL_SIO#
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
SIO
LA-9771P
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Tuesday, January 15, 2013
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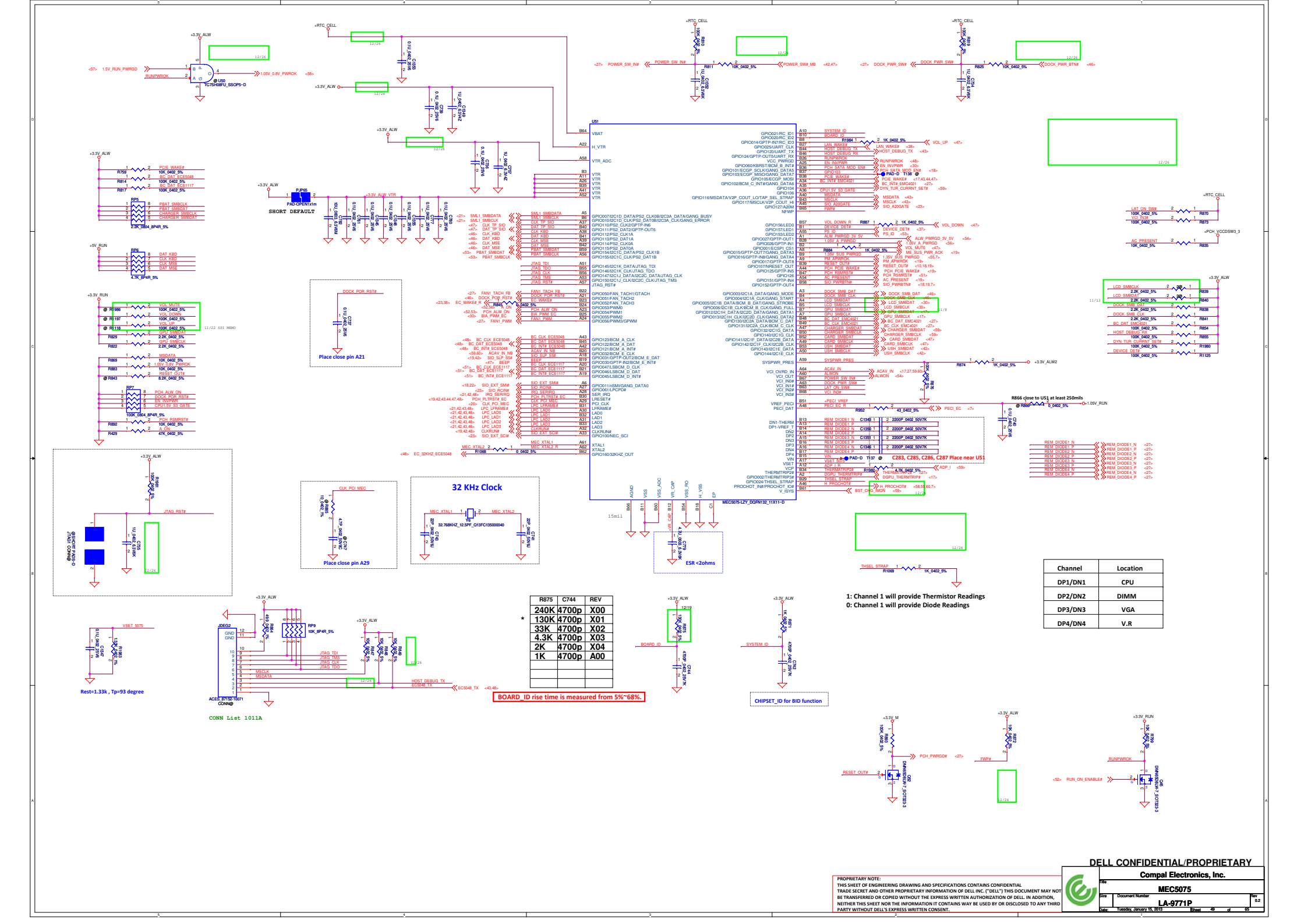


| R875 | C744 | REV |
|---|---|---|
| 240K | 4700p | X00 |
| 130K | 4700p | X01 |
| 33K | 4700p | X02 |
| 4.3K | 4700p | X03 |
| 2K | 4700p | X04 |
| 1K | 4700p | A00 |

| Channel | Location |
|---|---|
| DP1/DN1 | CPU |
| DP2/DN2 | DIMM |
| DP3/DN3 | VGA |
| DP4/DN4 | V.R |


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| | | |
|---|---|---|
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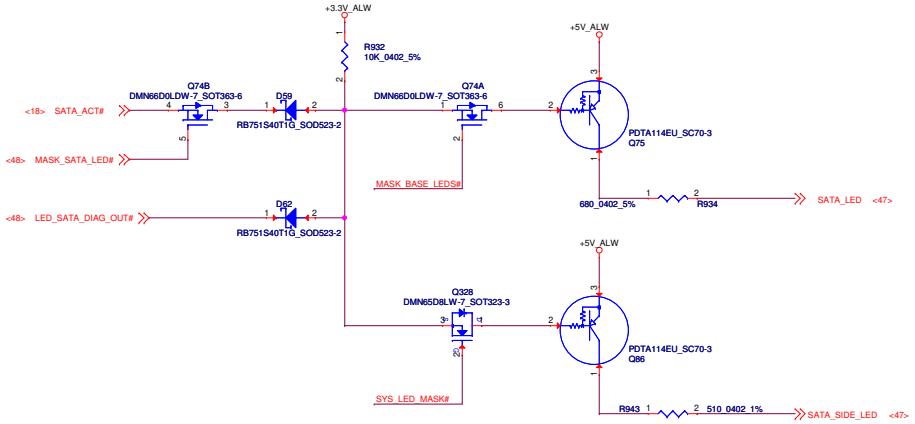
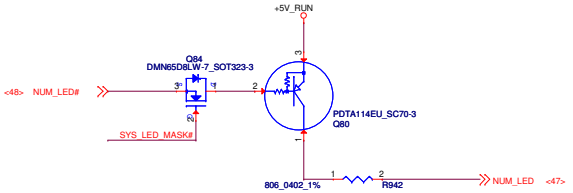
| Size | Document Number | Rev |
| | LA-9771P | 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 49 of 65 | |

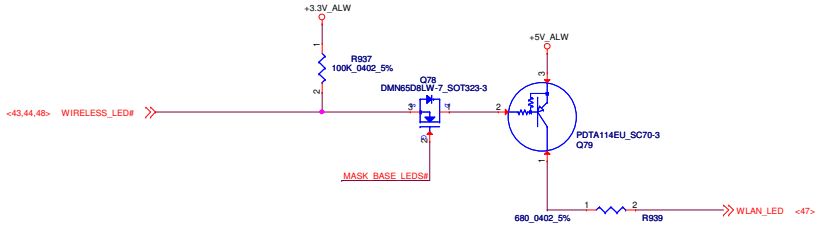
## HDD LED



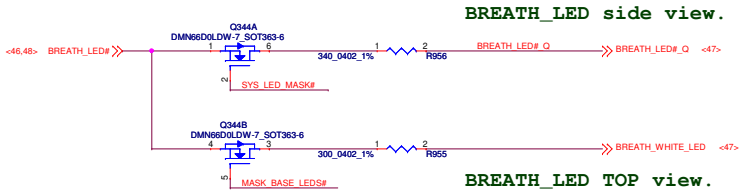

## NUM LED



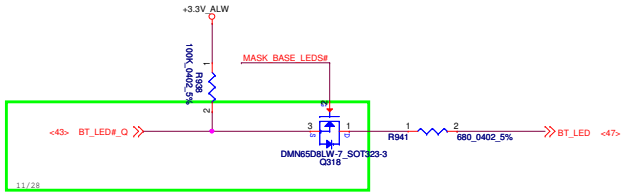

## WWAN/WLAN LED



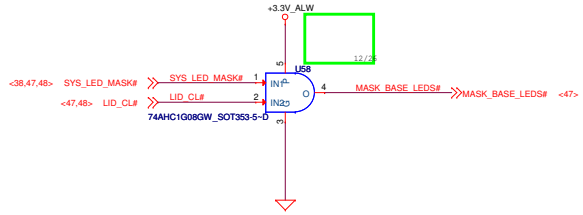

## Breath LED



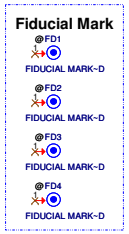

## BT LED

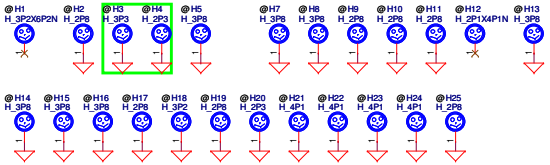



| LED Circuit Control Table | | |
|---|---|---|
| | SYS_LED_MASK# | LID_CL# |
| Mask All LEDs (Sniffer Function) | 0 | X |
| Mask Base MB LEDs (Lid Closed) | 1 | 0 |
| Do not Mask LEDs (Lid Opened) | 1 | 1 |




**Fiducial Mark**

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Title: PAD & Standoff & LED

Size | Document Number: LA-9771P | Rev: 0.2

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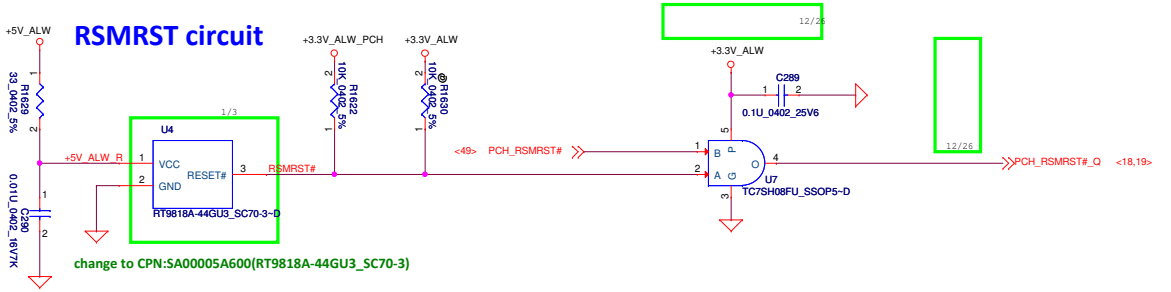
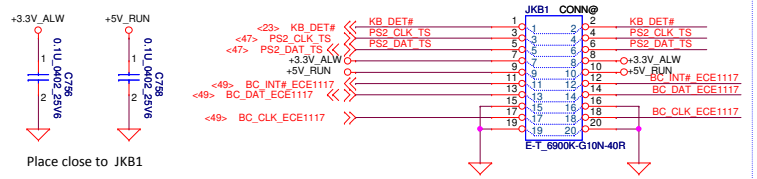
## RSMRST circuit




## BlueTooth

## Keyboard

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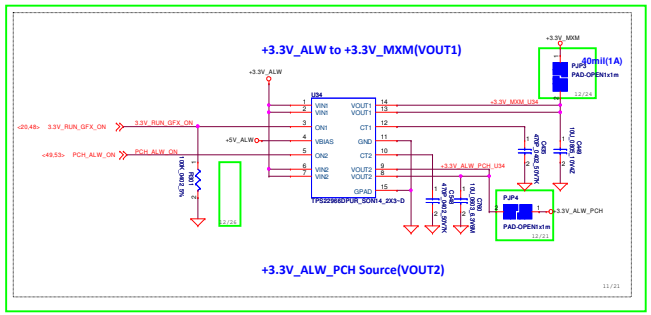
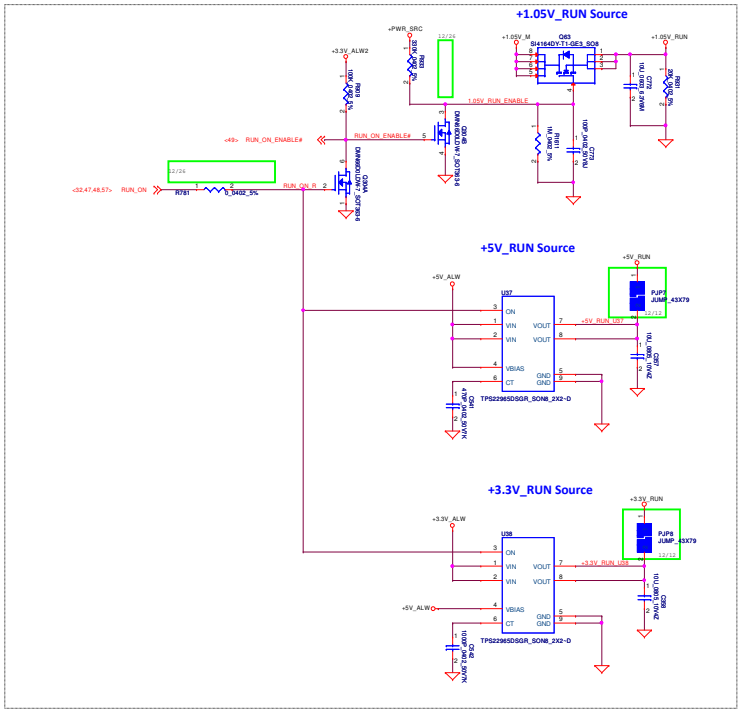
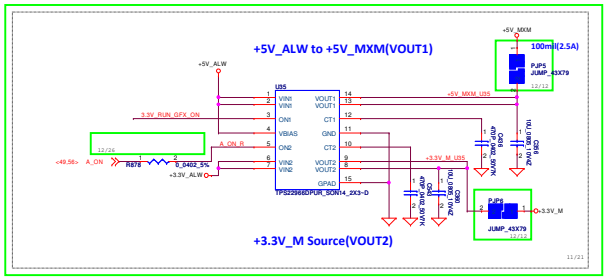
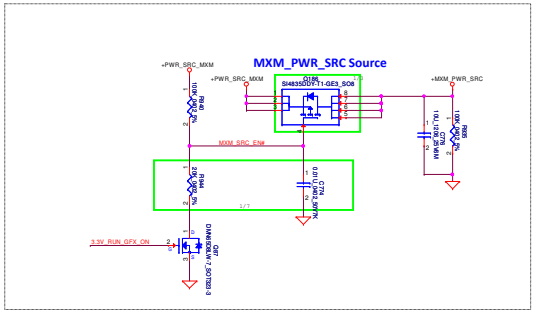
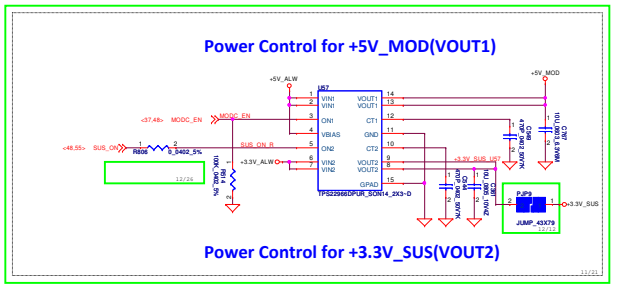
| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | Touch PAD/Int KB |
| Size | Document Number: LA-9771P |
| Rev | 0.2 |
| Date: Tuesday, January 15, 2013 | Sheet 51 of 65 |

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Compal Electronics, Inc.

Power Control

LA-9771P

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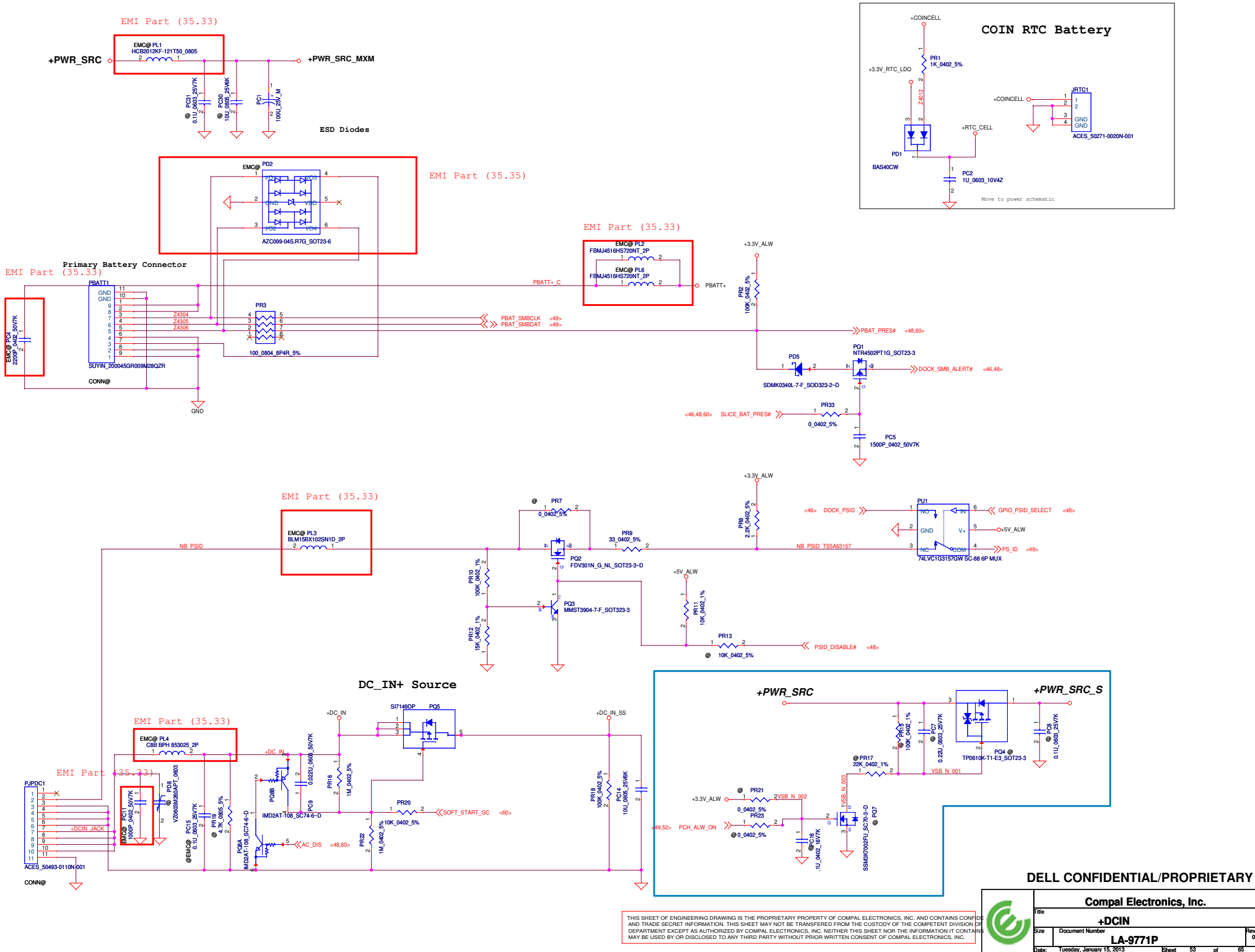
EMI Part (35.33)
+PWR_SRC
EMC@ PL1
HCB2012KF-121T50_0805
+PWR_SRC_MXM
PC31
0.1U_0603_25V7K
PC30
10U_0805_25V6K
PC1
100U_25V_M
ESD Diodes
EMI Part (35.35)
EMC@ PD2
AZC099-04S.R7G_SOT23-6
COIN RTC Battery
+COINCELL
PR1
1K_0402_5%
+3.3V_RTC_LDO
2.4K/2
JRTC1
ACES_50271-0020N-001
+RTC_CELL
PD1
BAS40CW
PC2
1U_0603_10V4Z
Move to power schematic
EMI Part (35.33)
Primary Battery Connector
EMI Part (35.33)
PBATT1
SUYIN_200045GR009M28QZR
CONN@
EMC@ PC4
2200P_0402_50V7K
PR3
100_0804_8P4R_5%
PBAT_SMBCLK
PBAT_SMBDAT
EMI Part (35.33)
EMC@ PL2
FBMJ4516HS720NT_2P
EMC@ PL6
FBMJ4516HS720NT_2P
PBATT+_C
PBATT+
+3.3V_ALW
PR2
100K_0402_5%
PBAT_PRES#
PD5
SDMK0340L-7-F_SOD323-2-D
PQ1
NTR4502PT1G_SOT23-3
DOCK_SMB_ALERT#
PR33
0_0402_5%
SLICE_BAT_PRES#
PC5
1500P_0402_50V7K
EMI Part (35.33)
EMC@ PL3
BLM15BX102SN1D_2P
NB_PSID
PR7
0_0402_5%
PR9
33_0402_5%
PQ2
FDV301N_G_NL_SOT23-3-D
PR10
100K_0402_1%
PR12
15K_0402_1%
PQ3
MMST3904-7-F_SOT323-3
+3.3V_ALW
PR8
2.2K_0402_5%
DOCK_PSID
PU1
74LVC1G3157GW SC-88 6P MUX
GPIO_PSID_SELECT
+5V_ALW
PS_ID
NB_PSID_TS5A63157
+5V_ALW
PR11
10K_0402_1%
PR13
10K_0402_5%
PSID_DISABLE#
DC_IN+ Source
EMI Part (35.33)
EMC@ PL4
C8B BPH 853025_2P
PJPDC1
ACES_50493-0110N-001
CONN@
+DCIN_JACK
EMC@ PC11
1000P_0402_50V7K
PD8
VZ0603M260APT_0603
PC15
0.1U_0603_25V7K
PR19
4.7K_0805_5%
PQ8A
IMD2AT-108_SC74-6-D
PQ8B
IMD2AT-108_SC74-6-D
+DC_IN
0.022U_0603_50V7K
PC9
PR16
1M_0402_5%
SI7149DP
PQ5
PR20
10K_0402_5%
SOFT_START_GC
PR22
1M_0402_5%
AC_DIS
+DC_IN_SS
PR18
100K_0402_5%
PC14
10U_0805_25V6K
+PWR_SRC
+PWR_SRC_S
PR17
22K_0402_1%
PR21
0_0402_5%
PR23
0_0402_5%
PC16
.1U_0402_16V7K
SSM6K7002FELJ_SC70-3-D
PQ7
PQ4
TP0610K-T1-E3_SOT23-3
VSB_N_001
VSB_N_002
PCH_ALW_ON
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Size
Document Number
LA-9771P
Rev
0.2
Date: Tuesday, January 15, 2013
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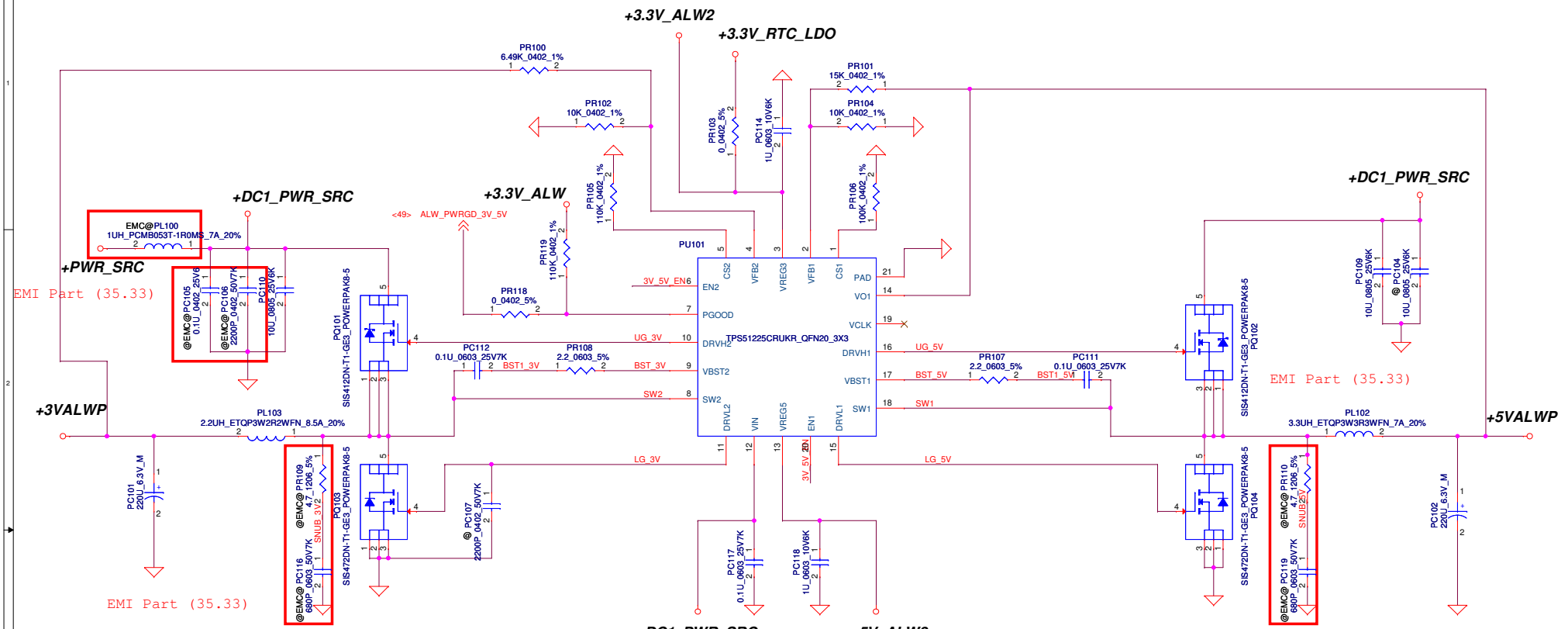
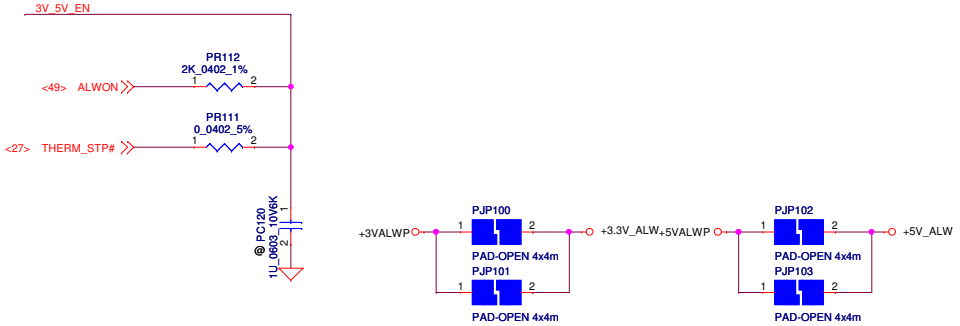



3VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 350kHz
TDC 6.1 A
Peak Current 8.7 A
OCP current 10.5 A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR Max:17mohm
Choke Ityp:8.3A / Isat:10.8A
Bulk cap ESR 15mohm




EMI Part (35.33)

5VALWP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 300kHz
TDC 6 A
Peak Current 8.5 A
OCP current 10.2 A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR Max:28mohm
Choke Ityp:6.6A / Isat:8.2A
Bulk cap ESR 15mohm

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
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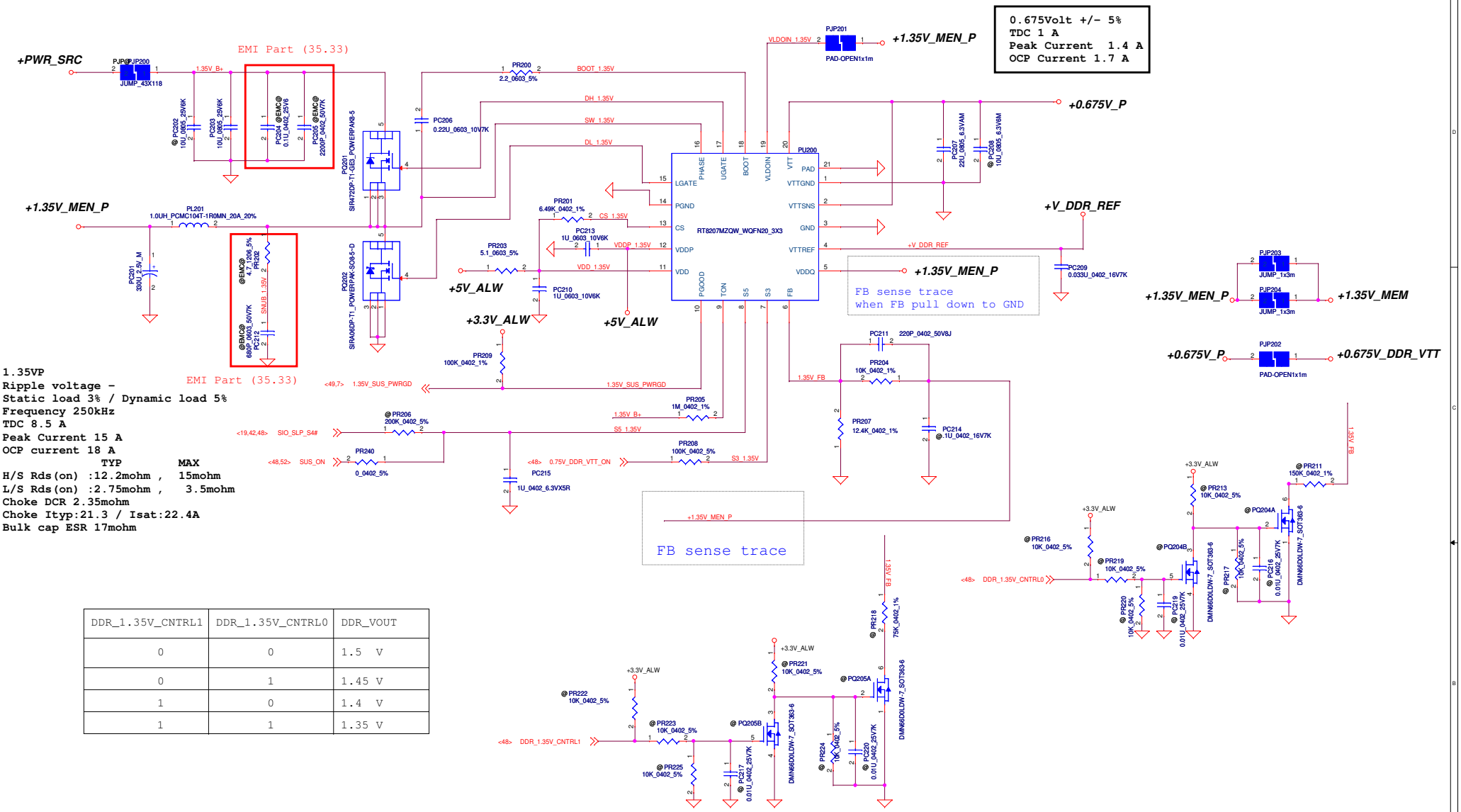
| | | | Date: Tuesday, January 15, 2013 Sheet 54 of 65 |




| DDR_1.35V_CNTRL1 | DDR_1.35V_CNTRL0 | DDR_VOUT |
|---|---|---|
| 0 | 0 | 1.5 V |
| 0 | 1 | 1.45 V |
| 1 | 0 | 1.4 V |
| 1 | 1 | 1.35 V |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 |

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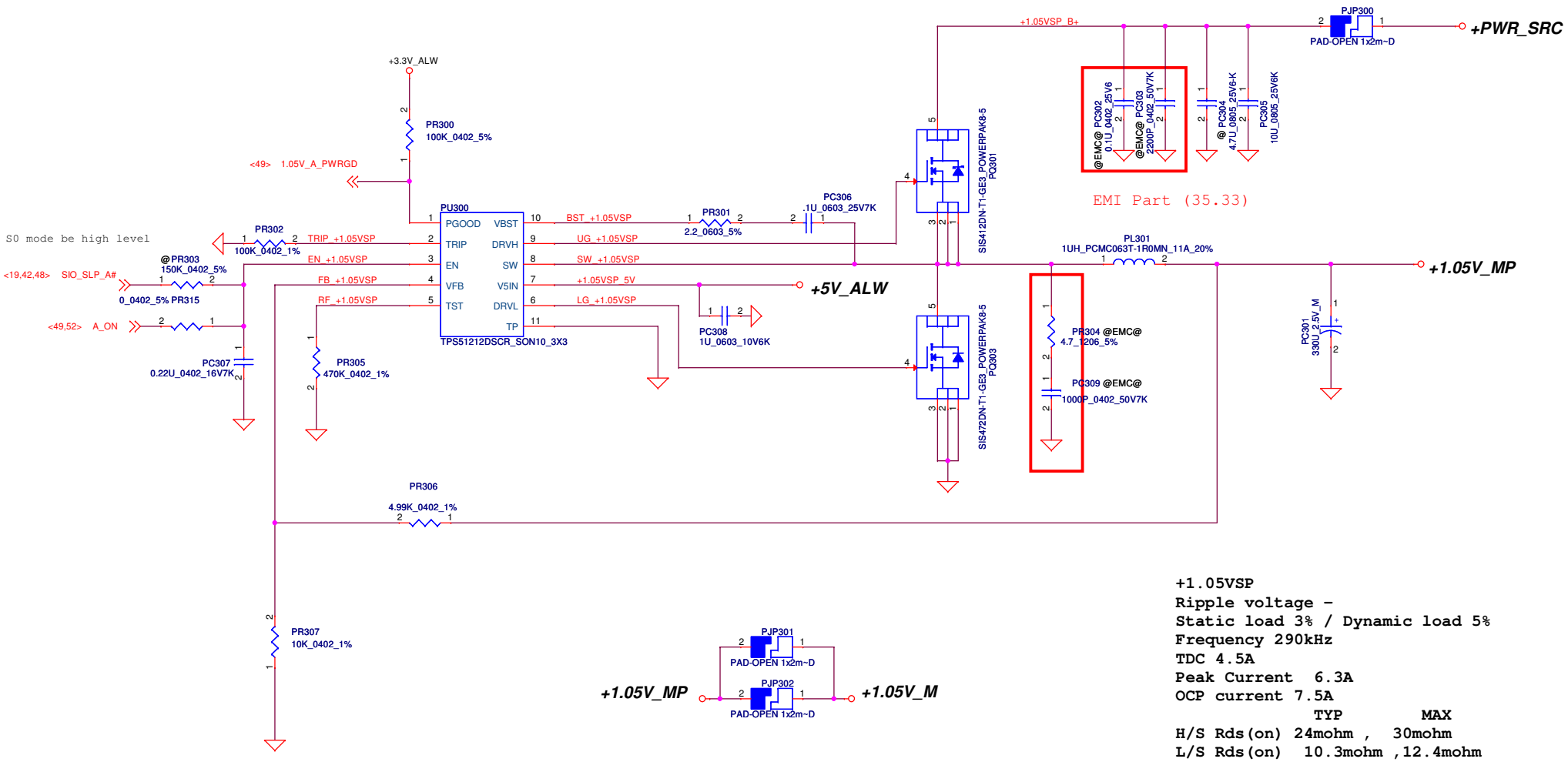
| Title | PWR-1.35VP/0.675VSP | | |
| Size | Document Number | | Rev |
| | LA-9771P | | 0.2 |
| Date: | Tuesday, January 15, 2013 | Sheet | 55 of 65 |




+1.05VSP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 4.5A
Peak Current 6.3A
OCP current 7.5A

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | 24mohm , | 30mohm |
| L/S Rds(on) | 10.3mohm , | 12.4mohm |

Choke DCR 11mohm
Choke Ityp:11A / Isat:14.5A
Bulk cap ESR 17mohm

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 |

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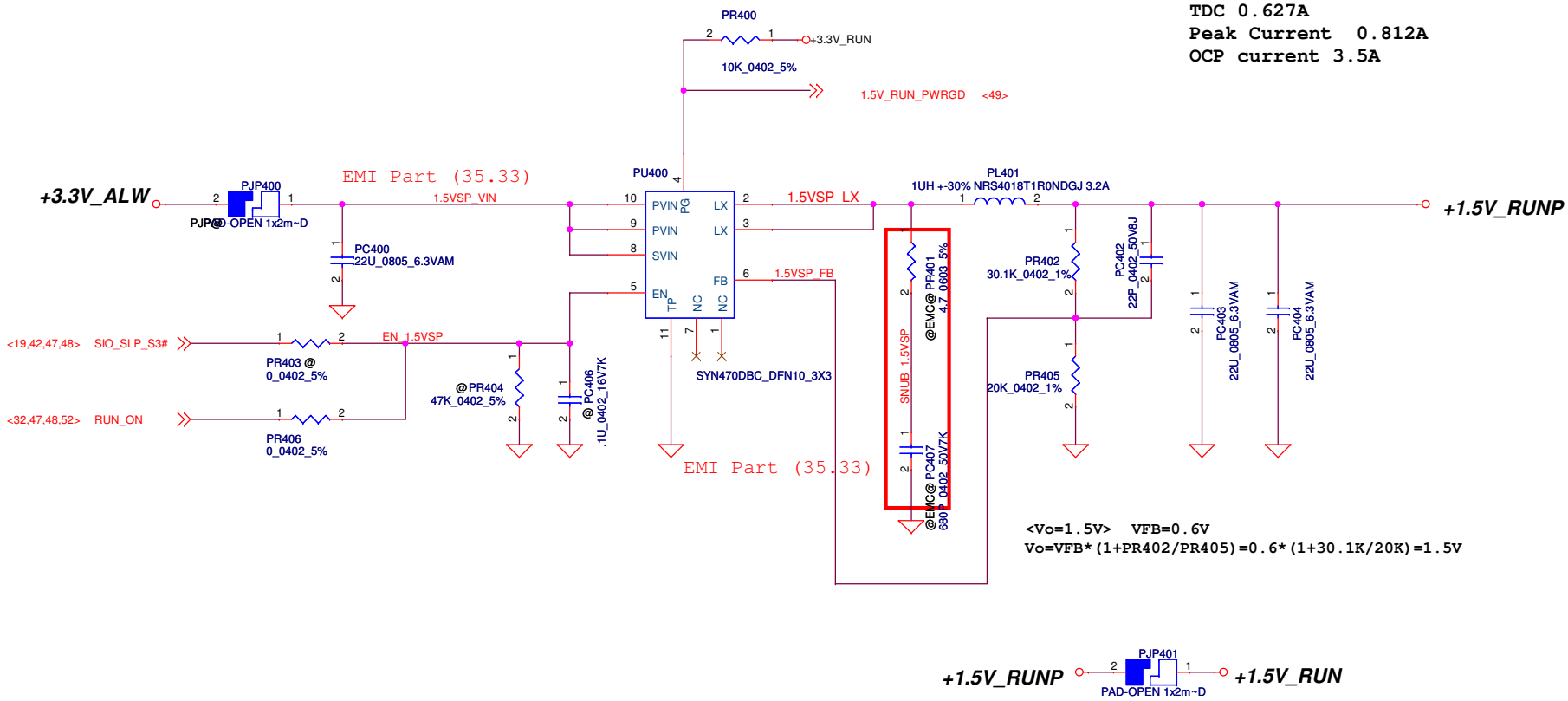
| | | | |
|---|---|---|---|
| Title | PWR-+1.05VSP | | |
| Size | Document Number | | Rev |
| | LA-9771P | | 0.2 |
| Date: | Tuesday, January 15, 2013 | Sheet | 56 of 65 |

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|---|---|---|
| Compal Electronics, Inc. | | |
| Title: PWR-1.5VSP | | |
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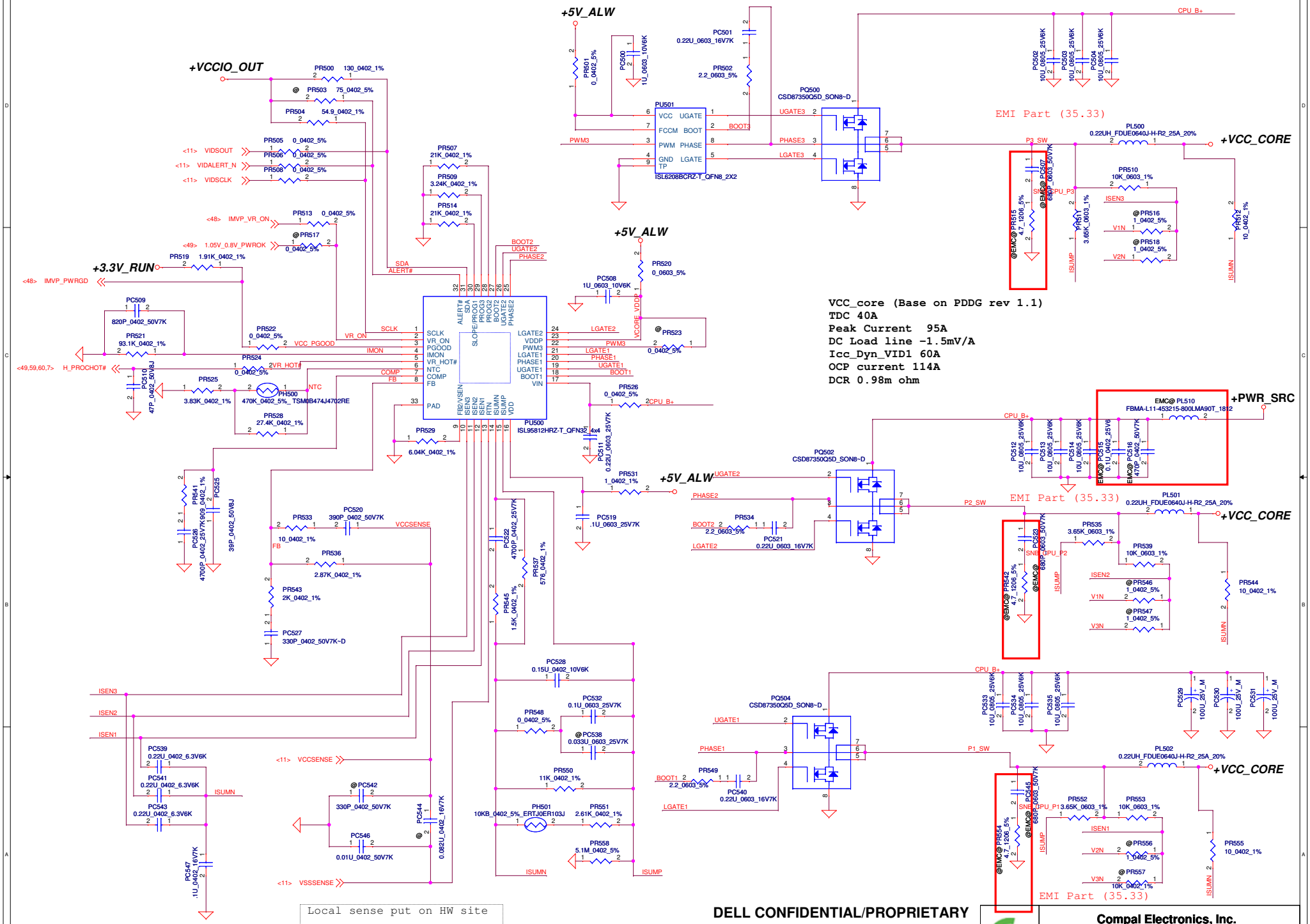
+5V_ALW
+VCCIO_OUT
+3.3V_RUN
PU501
ISL6208BCRZ-T_QFN8_2X2
PU500
ISL95812HRZ-T_QFN32_4x4
PQ500
PQ502
PQ504
CSD87350Q5D_SON8~D
EMI Part (35.33)
+VCC_CORE
+PWR_SRC
CPU_B+
VCC_core (Base on PDDG rev 1.1)
TDC 40A
Peak Current 95A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCP current 114A
DCR 0.98m ohm
Local sense put on HW site
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+VCC_CORE
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Iada=0~9.6A(180W)

ADP_I = 40 *Iadapter*Rsense

CC = 3.52A (Normal)

CV = 13.3V

EMI Part (35.33)

EMI Part (35.33)

EMI Part (35.33)

EMI Part (35.33)

VIN in detect limit
+SDC_IN=2.4V/82.5*(82.5+499)=16.9V

Current limit
Charger :8A Vilim=1.6V :
Max Boost Charger 12A Vilim=2.4V
6 Cell ( 2C )
9 Cell (1.3C )

Maximum charging current is 7.2A

| | DYN_TUR_CURRENT_SET# |
|---|---|
| 150W | High |
| 180W | Low |

Discrete current monitor circuit

sense adapter

Adapter Protection Circuit for Turbo Mode

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2012/01/17 | Deciphered Date | 2013/01/16 |

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Title: PWR-Charger

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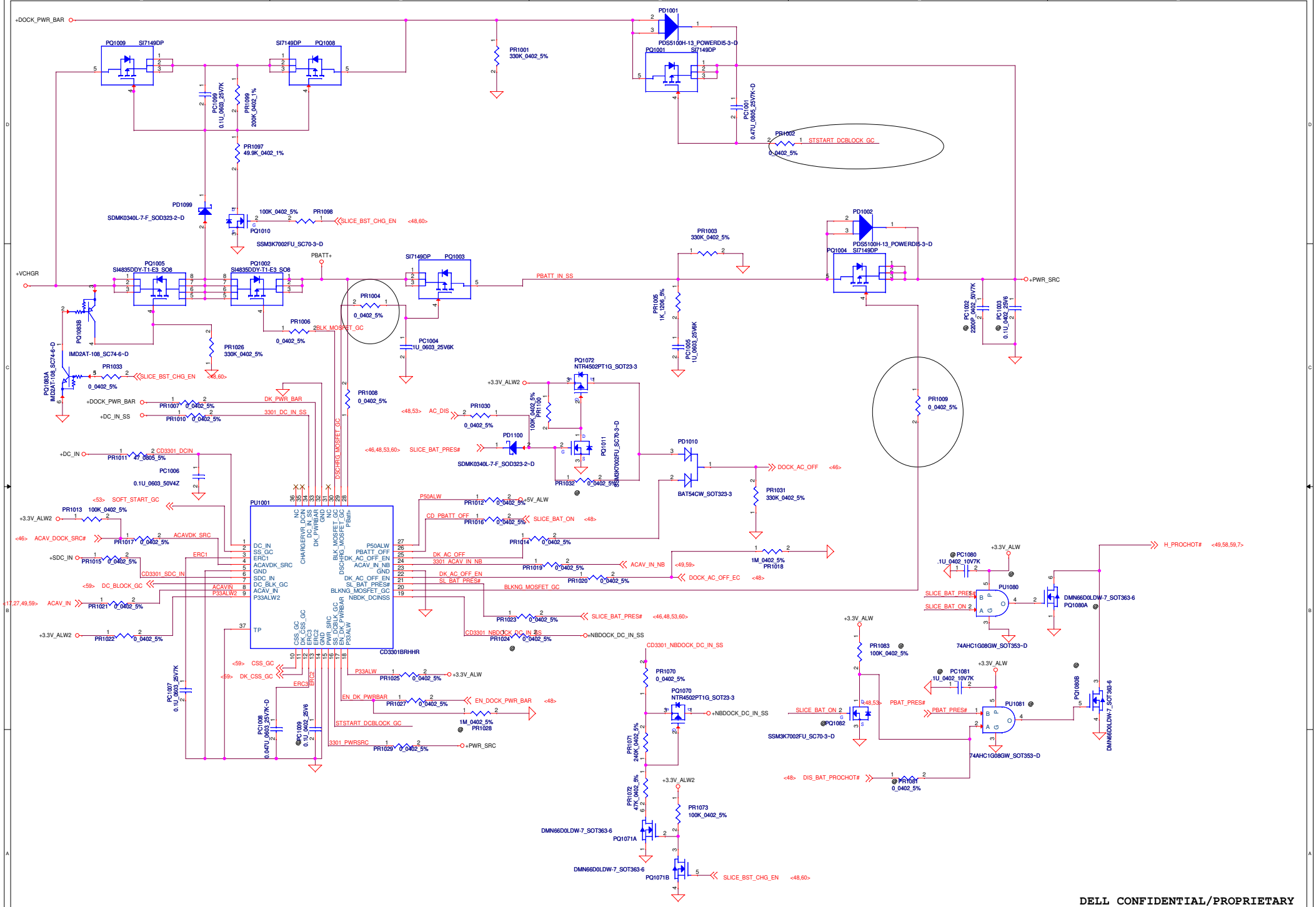
+DOCK_PWR_BAR
PQ1009 SI7149DP
SI7149DP PQ1008
PR1001 330K_0402_5%
PD1001
PDS5100H-13_POWERDI5-3~D
PQ1001 SI7149DP
PC1099 0.1U_0603_25V7K
PR1099 200K_0402_1%
PC1001 0.47U_0805_25V7K~D
PR1097 49.9K_0402_1%
PB1002
STSTART_DCBLOCK_GC
0_0402_5%
PD1099
SDMK0340L-7-F_SOD323-2~D
100K_0402_5%
PR1098
SLICE_BST_CHG_EN <48,60>
PQ1010
SSM3K7002FU_SC70-3~D
PBATT+
+VCHGR
PQ1005 SI4835DDY-T1-E3_SO8
PQ1002 SI4835DDY-T1-E3_SO8
SI7149DP PQ1003
PBATT_IN_SS
PR1003 330K_0402_5%
PD1002
PDS5100H-13_POWERDI5-3~D
PQ1004 SI7149DP
+PWR_SRC
PR1005 1K_1206_5%
PC1105 1U_0603_25V6K
PC1102 2200P_0402_50V7K
PC1103 0.1U_0402_25V6
PQ1083B IMD2AT-108_SC74-6~D
PR1026 330K_0402_5%
PR1033 0_0402_5%
PQ1083A IMD2AT-108_SC74-6~D
PR1004 0_0402_5%
PR1006 0_0402_5%
BLK_MOSFET_GC
PC1004 1U_0603_25V6K
PR1008 0_0402_5%
DSCHRG_MOSFET_GC
PR1009 0_0402_5%
PQ1072 NTR4502PT1G_SOT23-3
+3.3V_ALW2
PR1100 100K_0402_5%
PR1030 0_0402_5%
<48,53> AC_DIS
PD1100
SDMK0340L-7-F_SOD323-2~D
PQ1011 SSM3K7002FU_SC70-3~D
PR1032 0_0402_5%
PD1010
BAT54CW_SOT323-3
DOCK_AC_OFF <46>
PR1031 330K_0402_5%
<46,48,53,60> SLICE_BAT_PRES#
+DOCK_PWR_BAR
PR1007 0_0402_5%
DK_PWR_BAR
+DC_IN_SS
PR1010 0_0402_5%
3301_DC_IN_SS
+DC_IN
PR1011 47_0805_5%
CD3301_DCIN
PC1006 0.1U_0603_50V4Z
<53> SOFT_START_GC
PR1013 100K_0402_5%
+3.3V_ALW2
<46> ACAV_DOCK_SRC#
PR1017 0_0402_5%
ACAVDK_SRC
+SDC_IN
PR1015 0_0402_5%
ERC1
CD3301_SDC_IN
<59> DC_BLOCK_GC
<17,27,49,59> ACAV_IN
PR1021 0_0402_5%
+3.3V_ALW2
PR1022 0_0402_5%
PU1001
CD3301BRHHR
DC_IN
SS_GC
ERC1
ACAVDK_SRC
GND
SDC_IN
DC_BLK_GC
ACAV_IN
P33ALW2
CHARGERVR_DIN
DC_IN_SS
DK_PWRBAR
BLK_MOSFET_GC
DSCHRG_MOSFET_GC
PBatt+
P50ALW
PBATT_OFF
DK_AC_OFF_EN
ACAV_IN_NB
DK_AC_OFF_EN
SL_BAT_PRES#
BLKNG_MOSFET_GC
NBDK_DCINSS
CSS_GC
DK_CSS_GC
ERC2
EN_DK_PWRBAR
STSTART_DCBLOCK_GC
3301_PWRSRC
P33ALW
PR1012 0_0402_5%
+5V_ALW
P50ALW
CD_PBATT_OFF
PR1016 0_0402_5%
SLICE_BAT_ON <48>
PR1014 0_0402_5%
DK_AC_OFF
3301_ACAV_IN_NB
PR1019 0_0402_5%
ACAV_IN_NB <49,59>
DK_AC_OFF_EN
SL_BAT_PRES#
PR1020 0_0402_5%
DOCK_AC_OFF_EC <48>
BLKNG_MOSFET_GC
1M_0402_5%
PR1018
PR1023 0_0402_5%
SLICE_BAT_PRES# <46,48,53,60>
CD3301_NBDOCK_DC_IN_SS
PR1024 0_0402_5%
+NBDOCK_DC_IN_SS
PC1007 0.1U_0603_25V7K
PC1008 0.047U_0603_25V7K~D
PC1009 0.1U_0402_25V6
PR1025 0_0402_5%
+3.3V_ALW
EN_DOCK_PWR_BAR <48>
PR1027 0_0402_5%
1M_0402_5%
PR1028
PR1029 0_0402_5%
+PWR_SRC
CD3301_NBDOCK_DC_IN_SS
PR1070 0_0402_5%
PQ1070 NTR4502PT1G_SOT23-3
+NBDOCK_DC_IN_SS
PR1071 240K_0402_5%
PR1072 47K_0402_5%
PR1073 100K_0402_5%
DMN66D0LDW-7_SOT363-6
PQ1071A
PQ1071B
SLICE_BST_CHG_EN <48,60>
PR1083 @ 100K_0402_5%
PC1081 @ 1U_0402_10V7K
PQ1082 @
SSM3K7002FU_SC70-3~D
PBAT_PRES# <48,53>
PU1081 @
74AHC1G08GW_SOT353~D
PQ1080B @
DMN66D0LDW-7_SOT363-6
<48> DIS_BAT_PROCHOT#
PR1084 @ 0_0402_5%
PC1080 @ .1U_0402_10V7K
PU1080
74AHC1G08GW_SOT353~D
PQ1080A @
DMN66D0LDW-7_SOT363-6
H_PROCHOT# <49,58,59,7>
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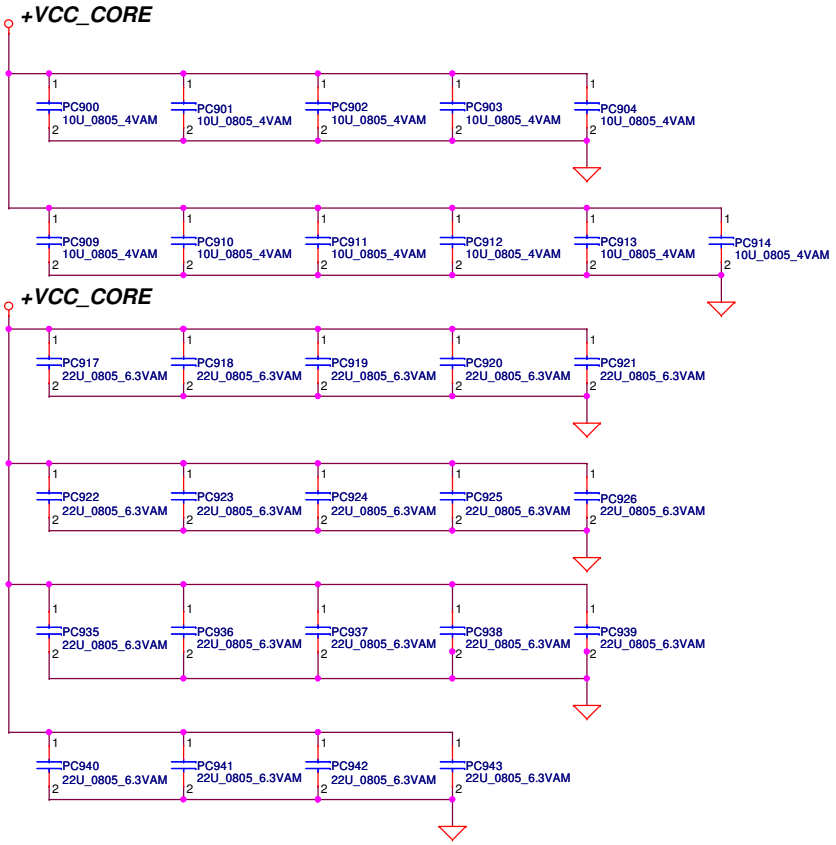
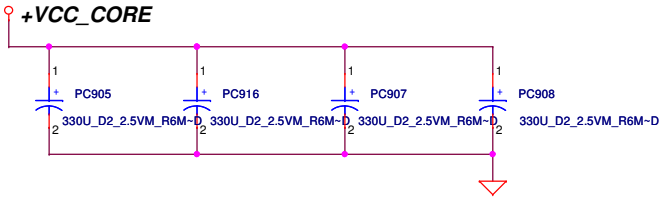
Based on PDDG rev 0.7 Table 5-1.

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Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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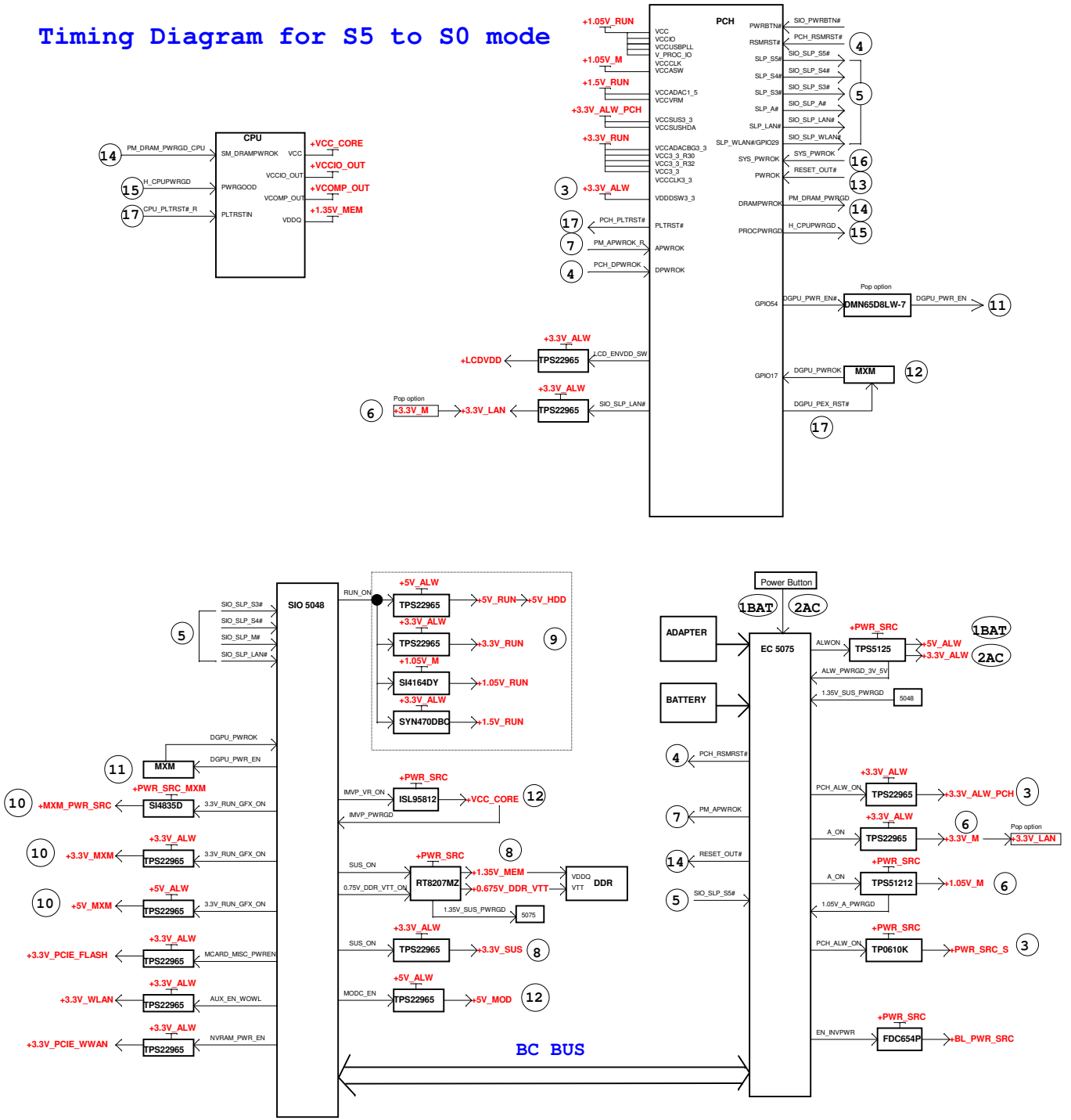
# Timing Diagram for S5 to S0 mode

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Power Sequence

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# Version Change List ( P. I. R. List )

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|---|---|---|---|---|---|---|---|
| 1 | 38 | HW | 10/30/2012 | DELL | Both EC_WAKE# and LAN_WAKE# to be connected to GPIO27 of PCH | pop R556. | X01(0.2) |
| 2 | 30 | HW | 11/21/2012 | compal | Q24,U46(ECE5048)burned out issue on SSI build IPQC test. | Change JLVDS1.5~JLVDS1.15 pin define. | X01(0.2) |
| 3 | 30,49 | HW | 11/21/2012 | compal | add BIST support(I2C solution) for QHD+ panel | add Q6,R161,R162. remove R239,R228.<br>change MXM_EDP_HPD to JEPWR1.1 and BS of R839,R840 to 2@. | X01(0.2) |
| 4 | 23 | HW | 11/21/2012 | compal | intel ME Crypto TLS ciperher suite with confidentiality. | pop RH37 and change to 1Kohm.de-pop RH62. | X01(0.2) |
| 5 | 45,52 | HW | 11/21/2012 | compal | component reduce plan-merge load sw from 1ch/1chip to 2ch/1chip. | merge (U63,U42);(U57,U41);(U34,U36);(U35,U40) depend on actual layout routing. | X01(0.2) |
| 6 | 9,50,49,13 14,15,16 | HW | 11/22/2012 | compal | SSI memo | change QC6 to SB00000QO00.<br>de-pop C778,R1986,R1197,R1118,CD80,CD22,CD44,CD66,CD88 | X01(0.2) |
| 7 | 22,42,43,50 51 | HW | 11/28/2012 | DELL | BT 4.0 USB module dropped for ARD REV1.2 | change Q318 to SOT323 package<br>remove R2207,R33,R34,R702,C600,R707,R724,R694,D28,C748,C754,C753,R904, R1133,R1134,JBT1 | X01(0.2) |
| ~~8~~ | ~~20,22,43,45 48~~ | ~~HW~~ | ~~11/28/2012~~ | ~~DELL~~ | ~~Pink Panther dropped for ARD REV1.2~~ | change JMINI3 PWR from +3.3V_PCIE_FLASH to +3.3V_RUN<br>remove C765,C547,R733,U56,C636,C626,C625,C635,C639,C634,C624,C637, C638,C633 | ~~X01(0.2)~~ |
| 9 | 30 | HW | 11/30/2012 | compal | PS8723B EQ table error | correct EQ table follow vendor suggestion.LL=9.5dB,LH=13dB,HL=4.5dB,HH=7.5dB. | X01(0.2) |
| 10 | 13,14,15,16 | HW | 12/11/2012 | INTEL | DDR Layout routing. | follow CRB DQ0~DQ63 distribution(DIMM1,DIMM3) and broardfile routing. DIMM2,DIMM4 depend on DIMM1,DIMM3 routing to define DQ0~DQ63. | X01(0.2) |
| 11 | 45,52 | HW | 12/12/2012 | compal | battery life measure. | add PJP1,PJP2,PJP5~PJP9(JUMP_43X79), PJP3,PJP4(JUMP_43X39) | X01(0.2) |
| 12 | 30 | HW | 12/12/2012 | compal | panel sequence(LCDVDD tr=T1,PWR_SRC tr= T12) | change C555 from 0.1uF to 0.01uF,C297 from 1000pF to 0.47uF. | X01(0.2) |
| 13 | 18,20 | HW | 12/12/2012 | compal | crystal EA | change CH4,CH5 from 18pF to 10pF;CH13,CH14 from 18pF to 12pF. | X01(0.2) |
| 14 | 41 | HW | 12/14/2012 | DELL | Charger current change to 1A. | change U2 to SLG55594AVTR(SA00006L600). | X01(0.2) |
| 15 | 42 | HW | 12/19/2012 | compal | APS pin define change for DG1.5 | change JAPS1.7 to POWER_SW#_MB,remove R19,R31,R29. | X01(0.2) |
| 16 | 7 | HW | 12/19/2012 | INTEL | VCCIO_OUT 6KHz noise in shark Bay 2-chip platform | change CC66 from 0.1uF to 1uF and pop it. | X01(0.2) |
| 17 | 49 | HW | 12/19/2012 | compal | Board ID | change R875 from 240Kohm to 130Kohm. | X01(0.2) |
| 18 | 30,32,48 | HW | 12/19/2012 | ESD | ESD EA | remove D87,D13,D10,D11,C749,C750. | X01(0.2) |
| 19 | 19,48 | HW | 12/20/2012 | compal | Deep Sleep feature support | pop R802,RH101,RH75,RH131;de-pop RH79,RH91. | X01(0.2) |
| 20 | 11,14 | HW | 12/20/2012 | compal | 1.35v decoupling cap reduce | de-pop CD34,CC36,CC35,CC40,CC169,CC166,CC165,CD36,CC38,CC33, CC42,CC37,CC41,CC163,CC170,CC171,CC168,CC164 | X01(0.2) |
| 21 | 41 | HW | 12/20/2012 | compal | Layout routing | Swap D15 D+,D-; L39 D+,D-. | X01(0.2) |
| 22 | 14,16,30,52 | HW | 1/7/2012 | compal | inrush current EA | add R944(20Kohm),change C774 from 2200P to 0.01U for +MXM_PWR_SRC.<br>de-pop CD37,CD38,CD82.CD83 for +0.675V_DDR_VTT.<br>de-pop C300 for +3.3V_RUN glith during turn on +CAMERA_VDD. | X01(0.2) |
| 23 | 48 | HW | 12/27/2012 | DELL | AC_DIS# polarity is inverted. | AC_DIS# signal change to AC_DIS,due to it's high active for "Peak Shift". | X01(0.2) |
| 24 | 23,42 | HW | 1/2/2013 | compal | USH/B drop O2 solution in X5. | remove netname"SMART_DET#". | X01(0.2) |

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|---|---|---|---|---|---|---|---|
| 25 | 18,51,52 | HW | 1/3/2013 | compal | replace X1 code component for LOAD BOM. | change U4 to SA00005A600,QH2 to SB501380020,Q186 to SB00000FF00. | X01(0.2) |
| 26 | 38 | HW | 1/3/2013 | compal | LAN EA. | change R570,R575~R581(0ohm) to L63~L70(12nH). | X01(0.2) |
| 27 | 20,22,43,45 48 | HW | 1/3/2013 | DELL | Add Pink Panther and reserve them. | add R707,R708,C765,C547,R733,U56,C636,C626,C639,C634,C624,C637,C638, C633 | X01(0.2) |
| 28 | 47 | HW | 1/3/2013 | compal | USBP0+/- layout routing. | swap USBP2+/- from JIO1.20/JIO1.18 to JIO1.18/JIO1.20. | X01(0.2) |
| 29 | 23,42 | HW | 1/7/2013 | compal | reserved routing SP_TPM_LPC_EN on PCH GPIO22 for GPIO MAP3.0 | add R2189,RH209,depop RH208,change netname PCH_GPIO22 to PCH_TPM_EN. | X01(0.2) |
| 30 | 44 | ME | 1/4/2013 | compal | connector List 1217A | change JSIM1 from T-SOL_159-1000302600 to T-SOL_159-1000302602 (SP011212271). | X01(0.2) |
| 31 | 43 | HW | 1/7/2013 | compal | modify netname and cap placement. | add +3.3V_PCIE_FLASH_R on R708.1 and change C639.1 net to +3.3V_PCIE_FLASH_R. | X01(0.2) |
| 32 | 50 | ME | 1/7/2013 | compal | screw hole change. | change H3 to 3P3,H4 to 2P3. | X01(0.2) |
| 33 | 13,16 | HW | 1/8/2013 | compal | DFX repair issue. | pop CD80,depop CD14. | X01(0.2) |
| 34 | 30 | HW | 1/8/2013 | compal | change main source circuit design for phase in LCDVDD PWR SW 2nd source. | add R709,depop C555. | X01(0.2) |
| 35 | 37 | HW | 1/8/2013 | compal | R796.1 PWR plane error. | change R796.1 PWR plane from +3.3V_ALW to +3.3V_ALW_PCH. | X01(0.2) |
| 36 | 19,48 | HW | 1/8/2013 | compal | reserve non-DS3 function circuit | add R802,RH101,RH79,RH91 | X01(0.2) |
| 37 | 42 | HW | 1/9/2013 | compal | TPM chip change version to DX4A12. | change U39 to SA00004WQ40(AT97SC3204-DX4A12-ABF). | X01(0.2) |
| 38 | 23 | BIOS | 1/10/2013 | compal | let EC set U46.B3(MCARD_PCIE_SATA#) as OD to save power same as Goliad/salado. | change RH226.2 from GND to pull up +3.3V_RUN | X01(0.2) |
| 39 | 30,40,41 | EMI | 1/11/2013 | compal | EMI request change USB2.0 choke. | change L10,L39,L41,L51 to DLW21HN900SQ2L(SM070001N00). | X01(0.2) |

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| Item | Page # | Title | Date | Request Owner | Issue Description | Solution Description | Rev. |
|---|---|---|---|---|---|---|---|
| 1 | 55 | PWR | 11/29/2012 | COMPAL | For 1.35V selector | Unpop PR225, PR224, PR218, PR220, PR217, PR211, PR222, PR223, PC217 PQ205, PR221, PC220, PR216, PR219, PC219, PQ204, PR213, PC216 | X01 |
| 2 | 54 | PWR | 11/29/2012 | COMPAL | For 3.3V OCP setting | Change PR105 to 90.9K | X01 |
| 3 | 57 | PWR | 11/29/2012 | COMPAL | For 1.5V output voltage setting | Change PR402 to 30.1K, PR405 to 20K | X01 |
| 4 | 54 | PWR | 11/29/2012 | COMPAL | For 3.3V/5V output voltage setting | Change PR102 and PR104 to 10K 1% | X01 |
| 5 | 58 | PWR | 11/29/2012 | COMPAL | Change better Vcore MOSFET | Change PQ500, PQ502, PQ504 to CSD87350Q5D | X01 |
| 6 | 53 | PWR | 12/11/2012 | COMPAL | Main source have x1 code | Change PQ1, PQ1070 to SB00000H500 | X01 |
| 7 | 53 | PWR | 12/11/2012 | COMPAL | Main source have x1 code | Change PU1 to SA00003DN00 | X01 |
| 8 | 59 | PWR | 12/11/2012 | COMPAL | For part count reduction | Combine PQ707, PQ708 to SB00000DH0L | X01 |
| 9 | 56 | PWR | 12/11/2012 | COMPAL | For part count reduction | Unpop PC304, change PC305 to SE00000QK00 | X01 |
| 10 | 55 | PWR | 12/11/2012 | COMPAL | For part count reduction | Unpop PC208, change PC207 to SE000008L80 | X01 |
| 11 | 55 | PWR | 12/20/2012 | COMPAL | Unite to same part number | Change PQ1, PQ1070 to SB000007900 | X01 |
| 12 | 58 | PWR | 12/20/2012 | COMPAL | For EMI test | Pop PC515 | X01 |
| 13 | 55 | PWR | 12/21/2012 | COMPAL | For cost down | Change PL201 to SH000004S00, PL701 to SH00000PO00 | X01 |
| 14 | 60 | PWR | 12/26/2012 | COMPAL | For Japan's Energy star | Add PQ1072, PQ1011, PD1010, PR1030, PD1100, PR1100, PR1031, PR1032 | X01 |
| 15 | 60 | PWR | 12/26/2012 | COMPAL | For boost charger behavior | Add PR1026, PQ1083 | X01 |
| 16 | 59 | PWR | 12/26/2012 | COMPAL | For current sense accuracy | Change PR706=33.2ohm, PR708=6.8ohm, PR713=12.1ohm, PR715=20ohm | X01 |
| 17 | 58 | PWR | 01/03/2013 | COMPAL | For Vcore compensation | Add PR558=5.1Mohm, PC509=820pF | X01 |
| 18 | 58 | PWR | 01/03/2013 | COMPAL | For EMI request | Pop PC516=470pF | X01 |
| 19 | 59 | PWR | 01/07/2013 | COMPAL | Unite to same part number | Change PD703 to SCS0340L010 | X01 |
| 20 | 53 | PWR | 01/07/2013 | COMPAL | Change to small size bead | Change PL3 to SM01000MB00 | X01 |
| 21 | 59 | PWR | 01/08/2013 | COMPAL | Refer to E5 | Change PR737.1 to +3.3V_ALW2 | X01 |

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