use these 2:
https://www.mouser.com/ProductDetail/Bourns/CAY16-911J4LF?qs=BOuw3wJAhvtHuJBTbQrYYQ%3D%3D
https://www.mouser.com/ProductDetail/Bourns/CAY16-4750F4LF?qs=NmEazmuVvbX6IRANgi73Gw%3D%3D

3.3 volt io

U1A
ICE40HX4K-TQ144

U1B
ICE40HX4K-TQ144

U1C
ICE40HX4K-TQ144

U1D
ICE40HX4K-TQ144

when the host tries to access
wait states

there are 4 clock signals to keep track of:
-ISA clock (1Mhz-16MHz)
-fpga clock (for memory access) (33Mhz-100MHz?)
-pixel clock (640x480) 25.175MHz
-1024 clock (for 1024x768) 65MHz

ideally it will be possible to enable the 640 clock or the 1024 clock
from software instead of having them botth run all the time

si5351 stuff

to vga port DAC

J9
Conn_01x09

according to math, I need something bigger

power supply for all the 3.3 volt devices

double check all power pins before routing anything

regular molex connector

U4

U5 LM3381 - the largest linear voltage regulator I know of
LM317_TO-220

R1=150
R2=300
R3=33
R1=300ohm
R2=600ohm

R2 330 ohms
R1 470+75 ohms
get 0.1% resistors
that gets you
3.3149393939393939394 volts +/- 0.009943182 volts

3.3 volt version

documentation says 5 volts will work U12
as input voltage for this AP7347DQ

U10
74LS245

U9
74LS245

U8
74LS245

U19
74ALVC164245

U18
74ALVC164245

isa bus steering

U15
74LS373

U14
74LS373

U13
74LS373

use these:
https://www.mouser.com/ProductDetail/Nexperia/74LVC573APW118?qs=me8TqzrmIYU4mlL%252B5pgpig%3D%3D

inputs

outputs

16 bit ISA bus. The LORD'S bus.

J6
Bus_ISA_16bit

important for speed

not needed on this device

the fpga has to control the address latches
because of the way it shares the address bus
to save fpga pins. Using BALE alone won't cut it

the fpga is fast enough it doesn't
need the extra delay in order to
address decode on time

no 3.3 volt rail

U11C
ADA4891-3

U11B
ADA4891-3

U11D
ADA4891-3

U11A
ADA4891-3

this needs at least a bypass capacitor

pull-up resistors

DB15_Female_HighDensity
J8

1.2 volt version

U2
AP7347DQ

I didn't see anything in the documentation talking about smd capacitors
so I'll just do the same exact thing I did with the xc2c128

documentation says 5 volts will work
as input voltage for this

external power input

J1
Conn_01x04

sysClock-PLL-Design-User-Guide says to do this.
to make inventory management easier, the only SMD
capacitors I use are 0.1uf and 1uF

you would not believe how much crap I have laying around as it is

seems that spi vcc needs to be 3.3 volts
https://github.com/OLIMEX/iCE40HX1K-EVB/blob/master/iCE40HX1K-EVB_Rev_B.pdf

capacitors for fpga

4148 diode seems to work the best. it doesn't like zener diodes though

note:
vccio is on the IO modules not this one

spi flash

U3

put next to spi rom

remember to put some decoupling capacitors near the rom
to make it more reliable

add a way to manually pull up or down the SS line.
The documentation says to do this "if not driven
by a processor" whatever that's supposed to mean

U1E
ICE40HX4K-TQ144

led is supposed to light up when finished programming

remove jumper for rom programming
add jumper and set to correct reset
logic level during in-system operation

for ice40 all pins are hi-Z with pullup enabled during FPGA reset and configuration
this means that if you know what you're doing you can make the fpga run your reset logic
instead of having your reset logic run the fpga

spi flash programmer port
J3
Conn_02x05_Odd_Even

these work perfectly with ice 40 fpgas

try it before putting this resistor on

si5351 clock module

J7
Conn_01x07

these ram chips have 10ns access times
its possible that it could access the ram at 24mhz or 48mhz
using ice40 internal oscillator. up to 42mb/s or 84mb/s respectively

either use the 256kb ones or the 512kb ones
640x480 8bpp will never need 1mb of ram so plan accordingly
6480x480 16bpp needs 614400 bytes of vram

the bandwidth between the fpga, the sram and the vga port will make
or break this entire design, although anything is better than a v9958

U6
CY7C1049G30
even byte

U7
CY7C1049G30
odd byte

derived from inverse of AV00

16 bit ice40 video card			
features: 1mb of high speed sram ice 40 fpga 16 bit color DAC resolutions of at least 640x480 16 bit isa compatibility			
Sheet: / File: fpga_videocard.kicad_sch			
Title:			
Size: A2	Date:		**Rev:**
KiCad E.D.A. 8.0.7			Id: 1/1