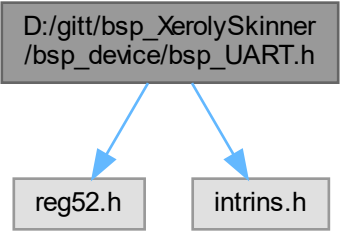


D:/gitt/bsp_XerolySkinner
/bsp_device/bsp_UART.h



```
graph TD; A["D:/gitt/bsp_XerolySkinner /bsp_device/bsp_UART.h"] --> B["reg52.h"]; A --> C["intrins.h"]
```

reg52.h

intrins.h