

LILYGO®

Sheet: /LoRa/
 File: LoRa.kicad_sch

Title: T-SimShield

Size: A4

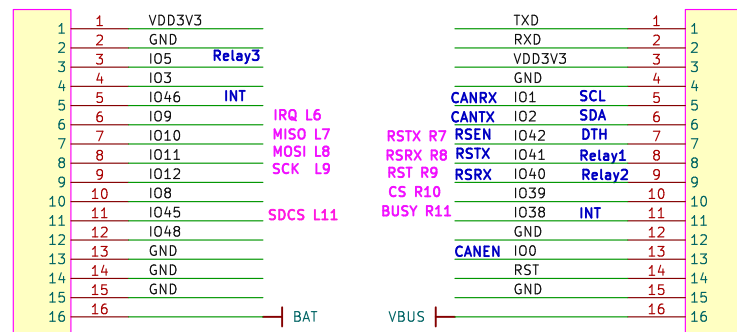
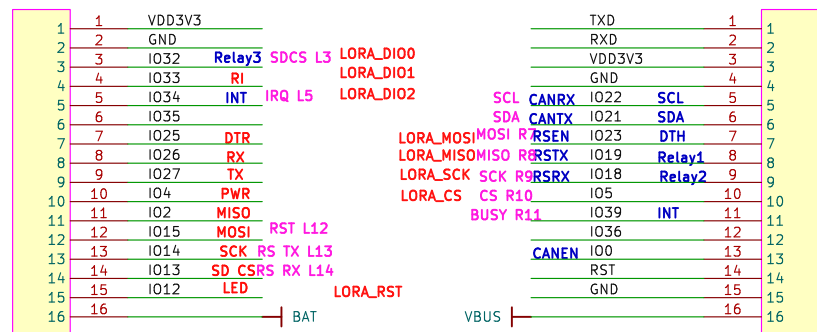
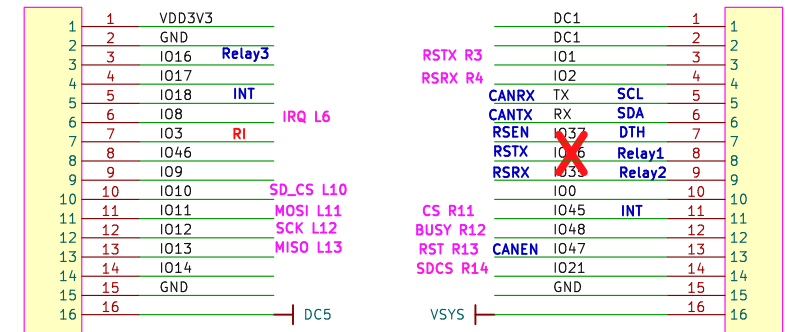
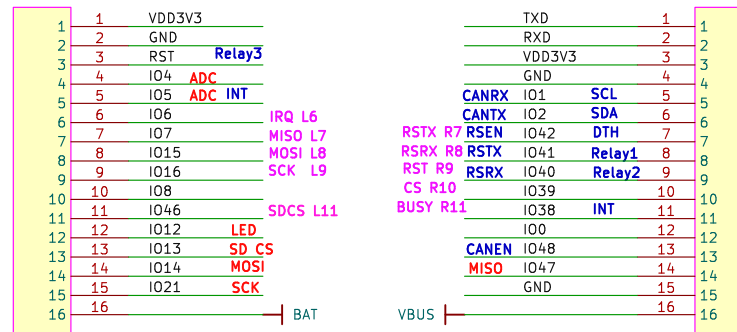
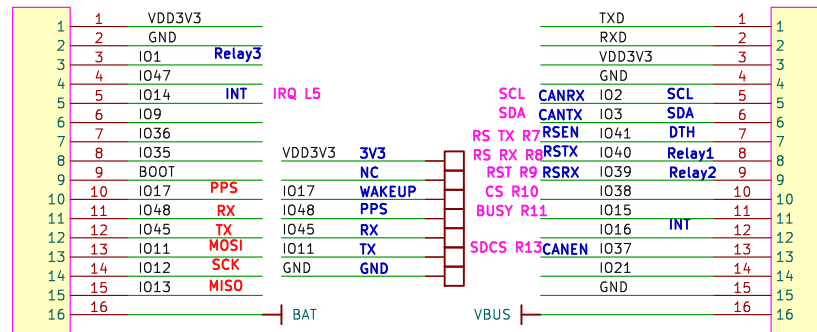
Date: 2025-08-09

Rev: V1.0

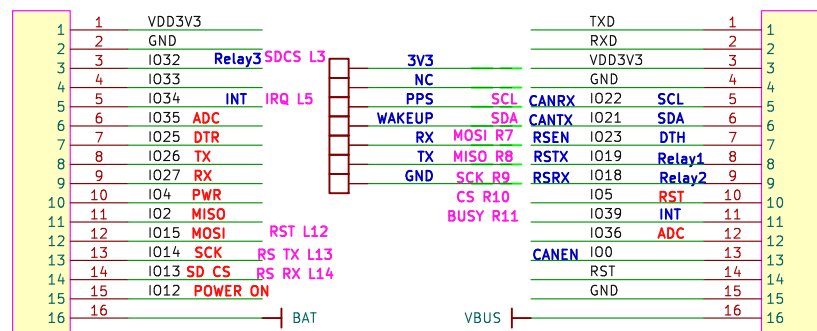
KiCad E.D.A. 8.0.6

RevAuthor: *Lewis He*

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The diagram shows the electrical connections for the CARD1 TF-SHORT module. A 3V3 power supply is connected to a decoupling network of capacitors C21 (10uF) and C22 (100nF) in parallel, which is connected to ground. The power supply is also connected to a 3-pin header. The header pins are connected to the module pins: Pin 1 (DAT2) is connected to SD_CS; Pin 2 (CS/DAT3) is connected to MOSI; Pin 3 (MOSI/CMD) is connected to SCK; Pin 4 (VDD) is connected to MISO; Pin 5 (SCK/CLK) is connected to GND; Pin 6 (VS5) is connected to GND; Pin 7 (MISO/DAT0) is connected to GND; Pin 8 (DAT1) is connected to GND. The module is labeled CARD1 TF-SHORT.



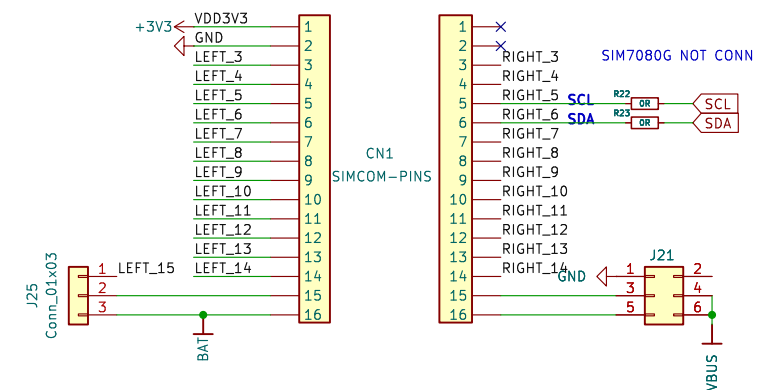
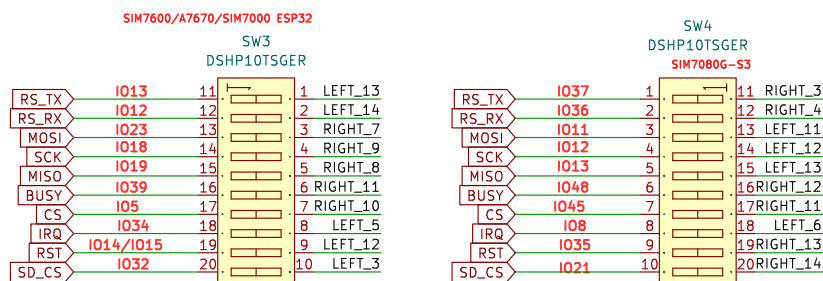
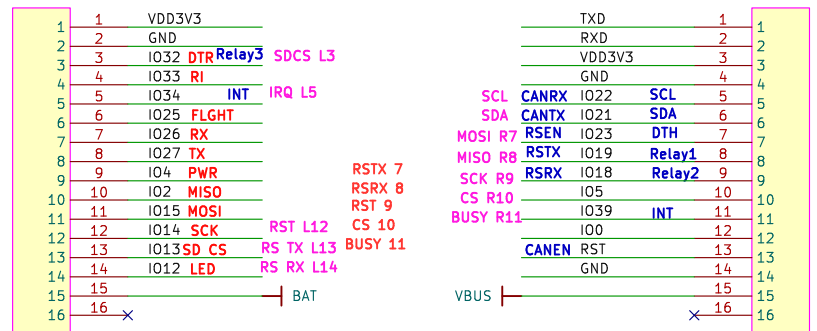
The diagram shows two parallel timing sequences for SW1 and SW2. Each sequence consists of a signal trace and a corresponding timing table.

SW1 Timing Table:

Signal	Value	Time (ns)	Event
RS_TX	I016	1	
RS_RX	I037	2	
MOSI	I011	3	
SCK	I012	4	
MISO	I013	5	
BUSY	I015	6	
BUSY	I038	7	
CS	I09	8	
IRQ	I039	9	
RST	I039	9	
SD_CS	I037	10	
RIGHT_7		11	
RIGHT_8		12	
LEFT_13		13	
LEFT_14		14	
LEFT_15		15	
RIGHT_11		16	
RIGHT_10		17	
LEFT_5		18	
RIGHT_9		19	
RIGHT_13		20	

SW2 Timing Table:

Signal	Value	Time (ns)	Event
RS_TX	I042	11	
RS_RX	I041	12	
MOSI	I015/I011	13	
SCK	I016/I012	14	
MISO	I07/I010	15	
BUSY	I038	16	
BUSY	I039	17	
CS	I06/I09	18	
IRQ	I040	19	
RST	I040	19	
SD_CS	I046/I015	20	
RIGHT_7		1	
RIGHT_8		2	
LEFT_8		3	
LEFT_9		4	
LEFT_7		5	
RIGHT_11		6	
RIGHT_10		7	
LEFT_6		8	
RIGHT_9		9	
LEFT_11		10	



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