XHSC 小华半导体 XIAOHUA SEMICONDUCTOR

HC32L110 Series

32-bit ARM® Cortex®-M0+ Microcontroller

Datasheet

Rev2.72 March 2025

Features

- 32MHz Cortex-M0+ 32-bit CPU platform
- HC32L110 series has a flexible power management system, ultra-low power performance
  - 0.5μA @ 3V Deep-sleep mode: all clocks off, power-on reset active, IO state retention, IO interrupt active, all registers, RAM and CPU data save state power consumption
  - 1.0μA @3V deep sleep mode + RTC working
  - 6μA @32.768kHz low-speed working mode: CPU and peripheral modules run, run programs from flash
  - 20μA/MHz@3V@16MHz sleep mode: CPU stops working, peripheral modules run, and main clock runs
  - 120μA/MHz@3V@16MHz working mode: CPU and peripheral modules run, and programs run from Flash
  - 4μs ultra-low power consumption wake-up time, making mode switching more flexible and efficient, and system response more agile
  - The above characteristics are typical values at room temperature. For specific electrical characteristics and power consumption characteristics, refer to the [Electrical characteristics] chapter
- 16K/32K bytes Flash memory, with erase and write protection function
- 2K/ 4K bytes RAM memory with parity check to enhance system stability
- General I/O pins (16IO/20pin, 12IO/16pin)
- Clock, crystal
  - External high-speed crystal oscillator 8 ~ 32MHz
  - External low-speed crystal 32.768KHz
  - Internal high-speed clock 4/8/16/22.12/24MHz
  - Internal low-speed clock 32.8/38.4KHz
  - Hardware supports internal and external clock calibration and monitoring
- Timer/counter
  - 3 general-purpose 16 -bit timer / counters
  - 3 high-performance 16-bit timers/counters, support PWM complementary, dead zone protection function
  - 1 low-power 16 -bit timer / counter
  - 1 programmable 16 -bit timer / counter, support capture compare, PWM output
  - 1 20 -bit programmable counting watchdog circuit, built-in dedicated ultra-low power RC -OSC to provide WDT counting
- Communication Interface
  - UART0-UART1 standard communication interface
  - LPUART supports ultra-low power communication interface using low-speed clock
  - SPI standard communication interface
  - I^2C standard communication interface
- Buzzer frequency generator, support complementary output
- Hardware perpetual calendar RTC module
- Hardware CRC-16 module
- Unique 10 -byte ID number
- 12-bit 1Msps sampling high-speed and high-precision SARADC, built-in op amp, can measure external weak signals
- 2 -way voltage comparator VC with integrated 6 -bit DAC and programmable reference input
- Integrated low voltage detector LVD, configurable 16-level comparison level, can monitor port voltage and power supply voltage
- Embedded debug solution that provides a full-featured real-time debugger
- Working temperature: -40 ~ 85 ℃
- Working voltage: 1.8 ~ 5.5V
- Package form: QFN20, TSSOP20, TSSOP16, CSP16

Support Model:

HC32L110C6UA	HC32L110C6PA
HC32L110C4UA	HC32L110C4PA
HC32L110B6PA	HC32L110B4PA
HC32L110B6YA	-

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1 Introduction

The HC32L110 series is an ultra-low power consumption, Low Pin Count, wide voltage operating range MCU designed to extend battery life in portable measurement systems. Integrating 12-bit 1Msps high-precision SARADC and integrating rich communication peripherals such as comparator, multi-channel UART, SPI, I2C, etc., it has the characteristics of high integration, high anti-interference, high reliability and ultra-low power consumption. The core of this product adopts the Cortex-M0+ core, cooperates with mature Keil & IAR debugging and development software, supports C language, assembly language, and assembly instructions.

Ultra-low power MCU typical applications

- Sensor applications, IoT applications;
- Smart transportation, smart city, smart home;
- Fire alarm probes, smart door locks, wireless monitoring and other smart sensor applications;
- All kinds of portable devices that are battery-powered and power-hungry.

32-bit CORTEX M0+ core

The ARM® Cortex®-M0+ processor is derived from Cortex-M0 and includes a 32-bit RISC processor with a computing power of 0.95 Dhrystone MIPS/MHz. At the same time, a number of new designs have been added to improve debugging and tracing capabilities, reduce the number of each instruction cycle (IPC) and improve the two-stage pipeline for Flash access, and incorporate energy-saving and consumption-reducing technologies. The Cortex-M0+ processor fully supports the integrated Keil & IAR debugger.

Cortex-M0+ includes a hardware debugging circuit that supports 2-pin SWD debugging interface.

ARM Cortex-M0+ features:

Instruction Set	Thumb / Thumb-2
Assembly line	2-stage assembly line
Performance efficiency	2.46 CoreMark / MHz
Performance efficiency	0.95 DMIPS / MHz in Dhrystone
Interrupt	32 fast interrupts
Interrupt priority	Configurable 4-level interrupt priority
Enhanced instruction	Single-cycle 32-bit multiplier
Debugging	Serial-wire debug port, supports 4 hard interrupts (break points) and 2 watch points (watch points)

16K/32K Byte Flash

The built-in fully integrated Flash controller does not require external high voltage input, and the high voltage is generated by the fully built-in circuit for programming. Support ISP, IAP, ICP functions.

2K/4K Byte RAM

According to different ultra-low power modes selected by customers, RAM data will be retained. With hardware parity bit, in case the data is accidentally damaged, when the data is read, the hardware circuit will immediately generate an interrupt to ensure the reliability of the system.

Clock system

A high-precision internal clock RCH with a configurable frequency of 4-24MHz. Under the configuration of 16MHz, the wake-up time from low power consumption mode to working mode is 4μs, and the frequency deviation within the full voltage and full temperature range is small, and it is not necessary to connect an expensive high-frequency crystal.

An external crystal oscillator XTH with a frequency of 8-32MHz.

An external crystal oscillator XTL with a frequency of 32.768KHz mainly provides the RTC real-time clock.

An internal clock RCL with a frequency of 32.8/38.4KHz.

Operating mode

1) Active Mode: CPU running, peripheral function modules running.
2) Sleep Mode: The CPU stops running, and the peripheral function modules run.
3) Deep sleep mode: The CPU stops running, the high-speed clock stops running, and the low-power function modules run.

Real Time Clock RTC

RTC (Real Time Counter) is a register that supports BCD data. It uses a 32,768Hz crystal oscillator as its clock to realize the perpetual calendar function. The interrupt cycle can be configured as year/month/day/hour/minute/second. 24/12 hour time mode, the hardware automatically corrects leap years. With accuracy compensation function, the highest accuracy is 0.96ppm. Internal temperature sensor or external temperature sensor can be used for accuracy compensation, software +1/-1 can be used to adjust year/month/day/hour/minute/second, and the minimum adjustable accuracy is 1 second.

The RTC calendar recorder used to indicate the time and date will not clear the retained value when the MCU is reset due to external factors. It is the best choice for measuring equipment and meters that require a permanent high-precision real-time clock.

Port controller GPIO

It can provide up to 16 GPIO ports, some of which are multiplexed with analog ports. Each port is controlled by an independent control register bit. Supports edge-triggered interrupts and level-triggered interrupts, and can wake up the MCU to working mode from various ultra-low power consumption modes. Support Push-Pull CMOS push-pull output, Open-Drain open-drain output. Built-in pull-up resistor, pull-down resistor, with Schmitt trigger input filter function. The output drive capability is configurable, and the maximum current drive capability is 12mA. 16 general-purpose IOs can support external asynchronous interrupts.

Interrupt Controller NVIC

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs; it has four interrupt priority levels, can handle complex logic, and can perform real-time control and interrupt processing.

The 32 interrupt entry vector addresses are:

Interrupt vector number	Interrupt source
[0]	GPIO_P0
[1]	GPIO_P1
[2]	GPIO_P2
[3]	GPIO_P3
[4]	-
[5]	-
[6]	UART0
[7]	UART1
[8]	LPUART
[9]	-
[10]	SPI
[11]	-
[12]	I^2C
[13]	-
[14]	Timer0
[15]	Timer1
[16]	Timer2
[17]	LPTimer
[18]	Timer4
[19]	Timer5
[20]	Timer6
[21]	PCA
[22]	WDT
[23]	RTC
[24]	ADC
[25]	-
[26]	VC0
[27]	VC1
[28]	LVD
[29]	-
[30]	RAM FLASH fault
[31]	Clock trim

Reset controller RESET

This product has 7 reset signal sources, each reset signal can make the CPU run again, most of the registers will be reset, and the program counter PC will be reset to point to 00000000.

	Reset source
[0]	Power-on brown-out reset POR BOR
[1]	External Reset Pin reset
[2]	WDT reset
[3]	PCA reset
[4]	Cortex-M0+ LOCKUP hardware reset
[5]	Cortex-M0+ SYSRESETREQ software reset
[6]	LVD reset

Timer TIM

		Bit width	Prescaler	Counting direction	PWM	capture	Complementary output
Basic timer	Timer0	16/32	1/2/4/8/16 32/64/256	Up count	No	No	No
	Timer1	16/32	1/2/4/8/16/ 32/64/256	Up count	No	No	No
	Timer2	16/32	1/2/4/8/16/ 32/64/256	Up count	No	No	No
Low power timer	LPTimer	16	无	Up count	No	No	No
Programmable counting array	PCA	16	2/4/8/16/32	Up count	5	5	无
Advanced timer	Timer4	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	Timer5	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1
	Timer6	16	1/2/4/8/16/ 64/256/1024	Up count/ Count down/ Up and down count	2	2	1

The basic timer contains three timers Timer0/1/2. Timer0/1/2 have exactly the same function. Timer0/1/2 is a synchronous timer/counter, which can be used as a 16-bit timer/counter with automatic reloading function, or as a 32-bit timer/counter without reloading function. Timer0/1/2 can count external pulses or implement system timing.

The low-power timer is an asynchronous 16-bit timer/counter, which can still time/count through the internal low-speed RC or external low-speed crystal oscillator after the system clock is turned off. Wake up the system in low-power mode through interrupts.

PCA (Programmable Counter Array) supports up to 5 16-bit capture/compare modules. The timer/counter can be used as a common clock count/event counter capture/compare function. Each

module of PCA can be independently programmed to provide input capture, output comparison or pulse width modulation. In addition, module 4 has an additional watchdog timer mode.

Timer4/5/6 which contains three timers. Timer4/5/6 are high-performance counters with the same function, which can be used to count and generate different forms of clock waveforms. One timer can generate a complementary pair of PWM or independent 2- way PWM output, which can capture external input for pulse width or period Measurement.

The basic functions and characteristics of the advanced timer are shown in the table:

Waveform mode	Sawtooth wave, triangular wave
Basic functions	• Direction of increments and decrements
	• Software synchronization
	• Hardware synchronization
	• Cache function
	• Orthogonal coding count
	• General PWM output
	• Protection mechanism
	• AOS related actions
Interrupt type	Count comparison match interrupt
	Count cycle match interrupt
	Dead time error interrupt
	Short-circuit monitoring interrupt

Watchdog WDT

WDT (Watch Dog Timer) is a configurable 20-bit timer that provides reset in the case of MCU abnormality; built-in 10K low-speed clock input is used as the counter clock. In debug mode, you can choose to pause or continue to run; WDT can only be restarted by writing a specific sequence.

Universal synchronous asynchronous transceiver UART0~UART1, LPUART

2- way Universal Asynchronous Receiver/Transmitter (Universal Asynchronous Receiver/Transmitter)

Basic functions of universal UART:

- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- Support 1 Bit stop bit
- Four different transmission modes
- Multi-machine communication

- Hardware address recognition

1 low power consumption mode can work asynchronous transceiver (Low Power Universal Asynchronous Receiver/Transmitter)

Basic functions of LPUART:

- Transmission clock SCLK (SCLK can choose XTL, RCL and PCLK)
- Send and receive data in system low power mode
- Half-duplex and full-duplex transmission
- 8/9-Bit transmission data length
- Hardware parity
- Support 1 Bit stop bit
- Four different transmission modes
- Multi-machine communication
- Hardware address recognition

Serial Peripheral Interface SPI

1 synchronous serial interface (Serial Peripheral Interface), supporting master-slave mode.

Basic characteristics of SPI:

- Can be configured as master or slave through programming
- Four-wire transmission mode, full duplex communication
- Host mode 7 kinds of baud rate configurable
- The maximum frequency division factor of the host mode is PCLK/2, and the maximum communication rate is 16M bps
- The maximum frequency division factor of slave mode is PCLK/8, and the maximum communication rate is 4M bps
- Configurable serial clock polarity and phase
- Support interrupt
- 8-bit data transmission, first transmit high bit and then low bit

I^2C bus

1 channel I^2C, using serial synchronous clock, can realize data transmission between devices at different rates.

Basic characteristics of I2C:

- Support four working modes of master sending/receiving and slave sending/receiving
- Support standard (100Kbps) / fast (400Kbps) / high speed (1Mbps) three working rates

- Support 7-bit addressing function
- Support noise filtering function
- Support broadcast address
- Support interrupt status query function

Buzzer

Three basic timers and one low-power timer function alternately output to provide a programmable drive frequency for the buzzer. The buzzer port can provide 12mA sink current, complementary output, no additional transistor is needed.

Clock calibration circuit module CLKTRIM

The built-in clock calibration circuit can calibrate the internal RC clock through an external precise crystal oscillator clock, and can also use the internal RC clock to check whether the external crystal oscillator clock is working properly.

Basic features of clock calibration:

- Calibration mode
- Monitoring mode
- 32-bit reference clock counter can be loaded with initial value
- 32-bit clock counter to be calibrated with configurable overflow value
- 6 reference clock sources
- 4 clock sources to be calibrated
- Support interrupt mode

Device electronic signature

Each chip has a unique 10-byte device identification number before leaving the factory, including wafer lot information and chip coordinate information. ID address 0x0010_0E74-0x0010_0E7F

Cyclic Redundancy Check (CRC)

Complies with the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239.

Analog-to-digital converter ADC

A 12-bit successive approximation analog-to-digital converter with monotonous and no missing codes, when working under a 24MHz ADC clock, the sampling rate reaches 1Msps. The reference voltage can be selected from the on-chip precision voltage (1.5V or 2.5V) or from an external input

or power supply voltage. 11 input channels, including 9 external pin inputs, 1 internal temperature sensor voltage and 1 1/3 supply voltage. Built-in configurable input signal amplifier to detect weak signals.

Basic characteristics of SAR ADC:

- 12-bit conversion accuracy;
- 1Msps conversion speed;
- 11 input channels, including 9 external pin inputs, 1 internal temperature sensor voltage and 1 VCC/3 voltage;
- 4 reference sources: VCC voltage, ExRef pin, built-in 1.5V reference voltage, built-in 2.5V reference voltage;
- ADC voltage input range: 0~Vref;
- 3 conversion modes: single conversion, sequential scan continuous conversion, continuous conversion accumulation;
- Input channel voltage threshold monitoring;
- Software can configure ADC conversion rate;
- Built-in signal amplifier, can convert high impedance signal;
- Support on-chip peripherals to automatically trigger ADC conversion, effectively reducing chip power consumption and improving real-time conversion.

Analog Voltage Comparator VC

Chip pin voltage monitoring / comparison circuit. 8 configurable positive/negative external input channels; 4 internal input channels, including 1 internal temperature sensor voltage, 1 built-in BGR 2.5V reference voltage, 1 64-order resistor Partial pressure. VC output can be used for basic timer, low power timer, advanced timer and programmable count array PCA capture, gating, external count clock. An asynchronous interrupt can be generated according to the rising/falling edge to wake up the MCU from the low-power mode. Configurable software anti-shake function.

Low voltage detector LVD

Detect the chip power supply voltage or chip pin voltage. 16-shift voltage monitoring values (1.8 - 3.3V). An asynchronous interrupt or reset can be generated based on the rising/falling edge. With hardware hysteresis circuit and configurable software anti-shake function.

LVD basic characteristics:

- 4 -channel monitoring sources, VCC, PC13, PB08, PB07;
- 16-stage threshold voltage, 1.8-3.3V optional;
- 8 trigger conditions, combinations of high level, rising edge and falling edge;

- 2 trigger results, reset and interrupt;
- 8-stage filter configuration to prevent false triggering;
- With hysteresis function, strong anti-interference.

Embedded debugging system

Embedded debugging solution, providing a full-featured real-time debugger, with standard mature Keil/IAR and other debugging and development software. Support 4 hard breakpoints and multiple soft breakpoints.

Programming mode

Support one programming mode: offline programming.

Support two programming protocols: ISP protocol, SWD protocol.

ISP protocol programming interface: P35, P36 or P27, P31.

SWD protocol programming interface: P27, P31.

When the chip receives the ISP programming command within a few milliseconds time window after the reset is completed, the chip works in the ISP programming mode, and the programmer can be used to program the FLASH.

When the chip does not receive the ISP programming instruction within a few milliseconds time window after the reset is completed, the chip works in the user mode, and the chip executes the program code in the FLASH.

Note:

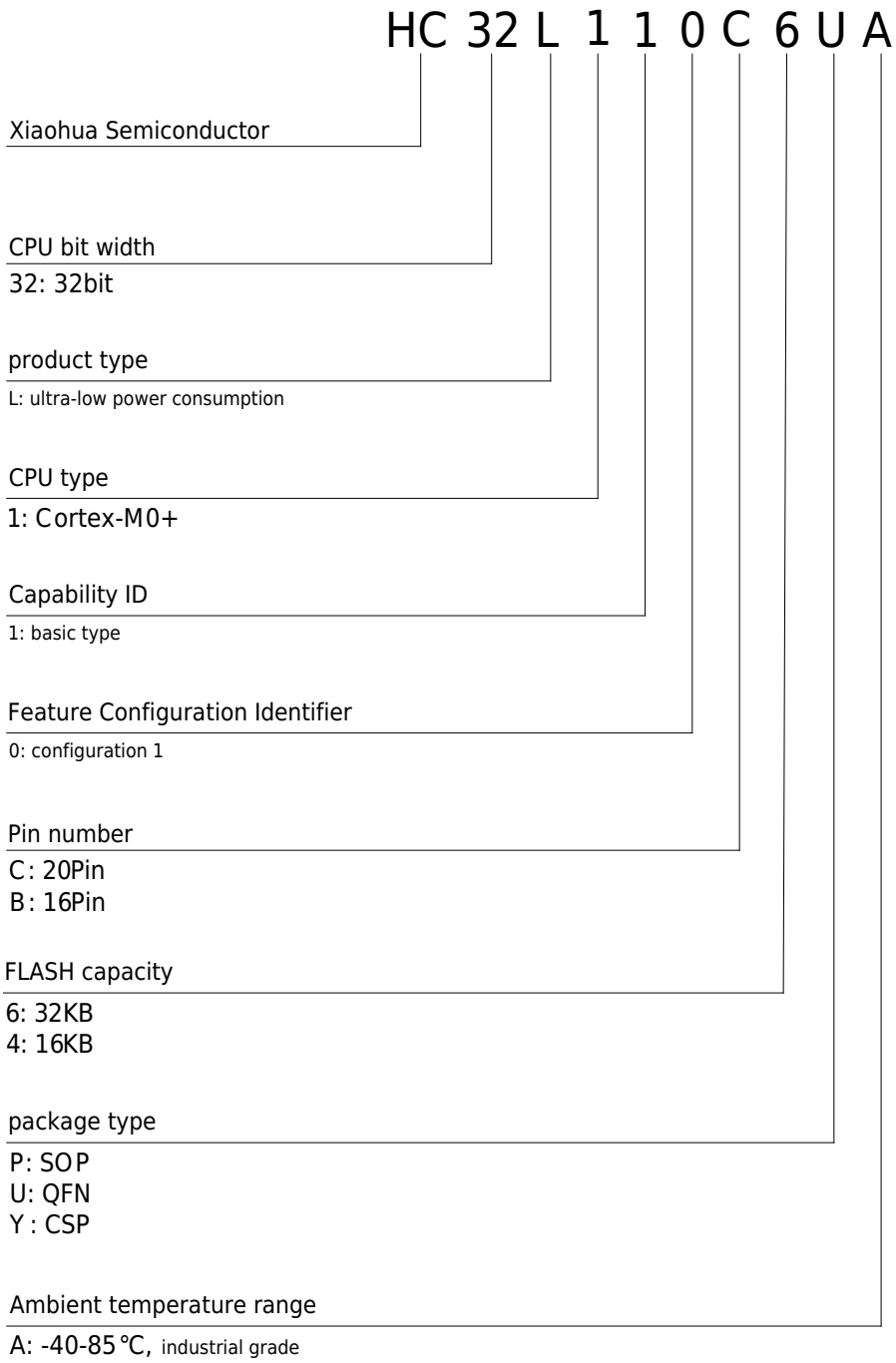
– It is recommended to reserve P35 and P36 as the ISP programming interface; if you need to use P27 and P31 as the ISP programming interface, please refer to PCN: PCN20200304-1_HC32L110HC32F003HC32F005 to increase the programming speed.

High security

Encrypted embedded debugging solution, providing a full-featured real-time debugger.

2 Product lineup

2.1 Product name

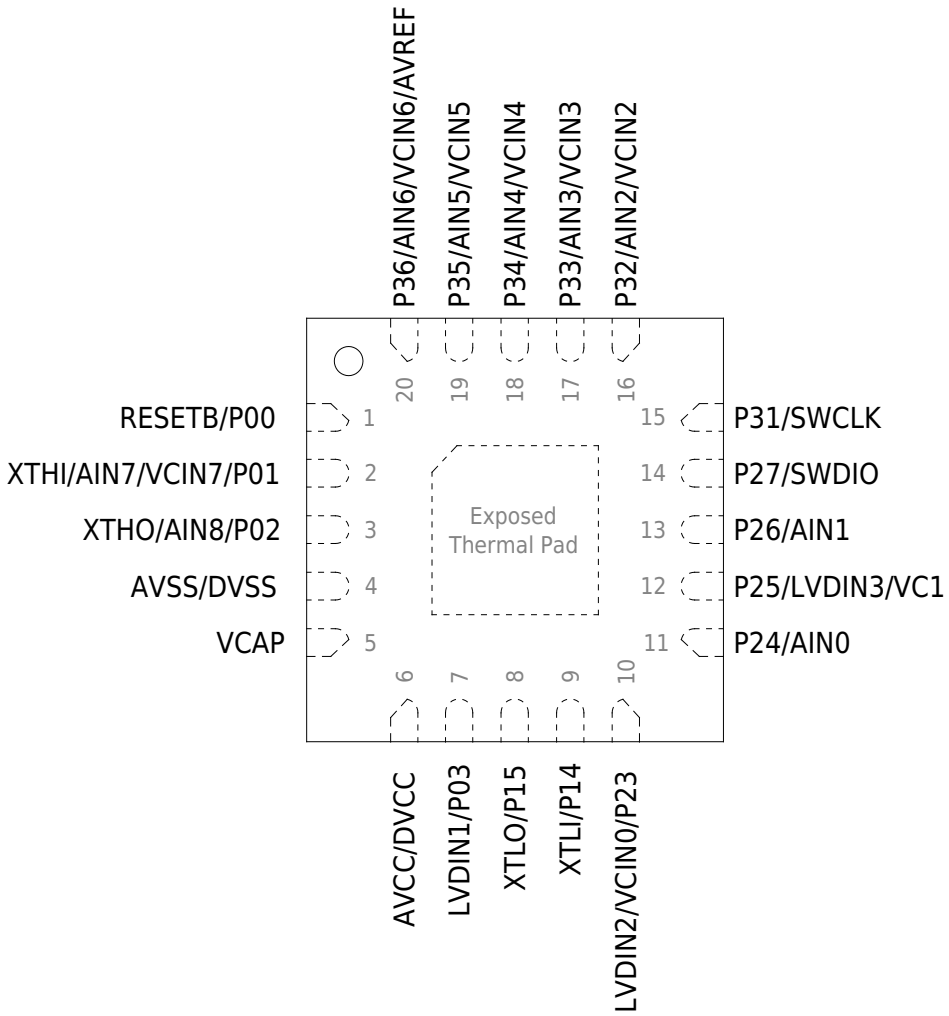


2.2 Function

Product name		HC32L110C6UA / HC32L110C6PA HC32L110C4UA / HC32L110C4PA	HC32L110B4PA / HC32L110B6PA HC32L110B6YA
Pin number		20	16
GPIO pin number		16	12
CPU	Kernel	Cortex M0+	
	Frequency	32MHz	
Supply voltage range		1.8 ~5.5V	
Single / dual power supply		Single power supply	
Temperature range		-40 ~ 85℃	
Debug function		SWD debug interface	
Unique identification code		Support	
Communication Interface		UART0/1 LPUART SPI I^{2}C	
Timer		General-purpose timer TIM0/1/2 Low Power Timer LPTIM Advanced timer TIM4/5/6	
12-bit A/D converter		9ch	6ch
Analog voltage comparator		VC0/1	
Real Time Clock		1	
Port interrupt		16	12
Low voltage detection reset / interrupt		1	
Clock	Internal high-speed oscillator	RCH 4/8/16/22.12/24MHz	
	Internal low-speed oscillator	RCL 32.8/38.4KHz	
	External high-speed crystal oscillator	8~32MHz	
	External Low Speed Crystal Oscillator	32.768kHz	
Buzzer		Max 4ch	
FLASH security protection		Support	
RAM parity		Support	

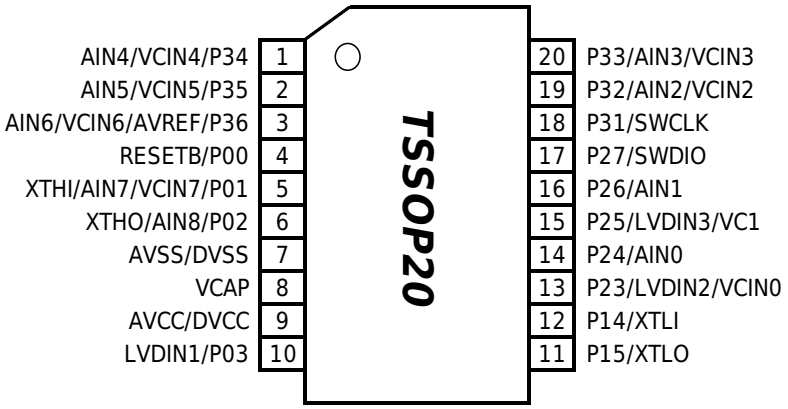
3 Pin configuration

HC32L110C6UA / HC32L110C4UA

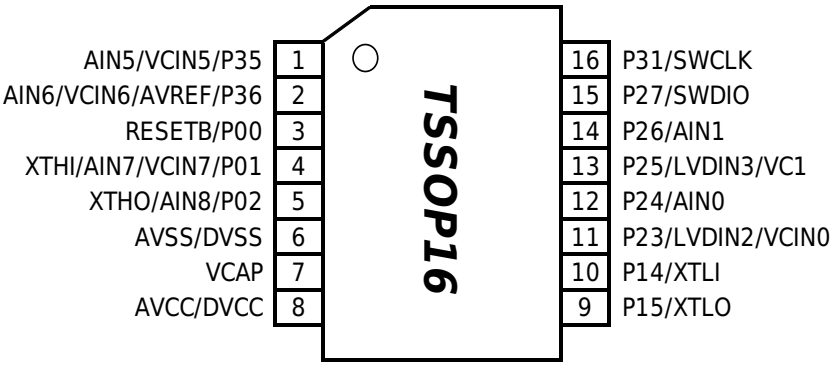


Note: Exposed Thermal Pad needs to be connected to DVSS.

HC32L110C6PA / HC32L110C4PA



HC32L110B4PA / HC32L110B6PA



Note: In the application, it is necessary to set the unleaded IO pin of the package relative to TSSOP20 as an input and enable the pull-up.

HC32L110B6YA

CSP16 TOP VIEW

Note:

- In the application, it is necessary to set the unleaded IO pin of the package relative to TSSOP20 as an input and enable the pull-up.
- A1 is Pin 1.

4 Pin function description

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
1	4	3	B2	RESETB P00	RESETB	Reset input port, low effective, chip reset
					GPIO	P00 digital input
2	5	4	B3	P01	GPIO	P01 General purpose digital input / output pin
					UART0_RXD	UART0 RXD
					I2C_SDA	I2C data
					UART1_TXD	UART1 TXD
					TIM0_TOG	Timer0 flip output
					TIM5_CHB	Timer5 capture input / comparison output B
					SPI_SCK	SPI clock
					TIM2_EXT	Timer2 external clock
					AIN7/VC7	Analog input
					XTHI	External XTH crystal clock enter
3	6	5	A4	P02	GPIO	P02 General purpose digital input / output pin
					UART0_TXD	UART0 TXD
					I2C_SCL	I2C Clock
					UART1_RXD	UART1 RXD
					TIM0_TOGN	Timer0 flips the inverted output
					TIM6_CHA	Timer6 capture input / comparison output A
					SPI_CS	SPI CS
					TIM2_GATE	Timer2 Gating
					AIN8	Analog input
					XTHO	External XTH crystal clock output
4	7	6	B4	AVSS/DVSS	GND	Chip ground
5	8	7	C3	Vcap	Power	LDO core power supply output (only for internal circuit use, connect a 4.7uF capacitor)
6	9	8	C4	AVCC/DVCC	Power	Chip power supply 1.8v~5.5v
7	10	Note	Note	P03	GPIO	P03 General purpose digital input / output pin
					PCA_CH3	PCA capture input / comparison output 3
					SPI_CS	SPI CS
					TIM6_CHB	Timer6 capture input / comparison output B
					LPTIM_EXT	LPTimer external clock input
					RTC_1HZ	RTC 1Hz output
					PCA_ECI	PCA external clock input

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					VC0_OUT	VC0 output
					LVDIN1	Analog input
8	11	9	D2	P15	GPIO	P15 General purpose digital input / output pin
					I2C_SDA	I2C data
					TIM2_TOG	Timer2 toggle output
					TIM4_CHB	Timer4 capture input / compare output B
					LPTIM_GATE	LPTimer Gating
					SPI_SCK	SPI clock
					UART0_RXD	UART0 RXD
					LVD_OUT	LVD Output
					XTLO	External XTL crystal oscillator clock output
9	12	10	D1	P14	GPIO	P14 General purpose digital input / output pin
					I2C_SCL	I2C Clock
					TIM2_TOGN	Timer2 flips the inverted output
					ECI	PCA external clock input
					ADC_RDY	ADC ready
					SPI_CS	SPI CS
					UART0_TXD	UART0 TXD
					XTLI	External XTL crystal oscillator clock input
10	13	11	C2	P23	GPIO	P23 General purpose digital input / output pin
					TIM6_CHA	Timer6 capture input / comparison output A
					TIM4_CHB	Timer4 capture input / compare output B
					TIM4_CHA	Timer4 capture input / comparison output A
					PCA_CH0	PCA capture input / comparison output 0
					SPI_MISO	SPI module host input and slave output data signal
					UART1_TXD	UART1 TXD
					IR_OUT	38K carrier output
					LVDIN2/VC0	Analog input
11	14	12	C1	P24	GPIO	P24 General purpose digital input / output pin
					TIM4_CHB	Timer4 capture input / compare output B
					TIM5_CHB	Timer5 capture input / comparison output B
					HCLK_OUT	HCLK Output
					PCA_CH1	PCA capture input / comparison output 1
					SPI_MOSI	SPI module master output slave input data signal

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					UART1_RXD	UART1 RXD
					VC1_OUT	VC1 output
					AIN0	Analog input
12	15	13	B1	P25	GPIO	P25 General purpose digital input / output pin
					SPI_SCK	SPI clock
					PCA_CH0	PCA capture input / comparison output 0
					TIM5_CHA	Timer5 capture input / comparison output A
					LVD_OUT	LVD Output
					LPUART_RXD	LPUART RXD
					I^2C_SDA	I^2C data
					TIM1_GATE	Timer1 Gating
					LVDIN3/VC1	Analog input
13	16	14	A1	P26	GPIO	P26 General purpose digital input / output pin
					SPI_MOSI	SPI module master output slave input data signal
					TIM4_CHA	Timer4 capture input / comparison output A
					TIM5_CHB	Timer5 capture input / comparison output B
					PCA_CH2	PCA capture input / comparison output 2
					LPUART_TXD	LPUART TXD
					I^2C_SCL	I^2C Clock
					TIM1_EXT	Timer1 clock input
					AIN1	Analog input
14	17	15	D3	P27	GPIO	P27 General purpose digital input / output pin
					SPI_MISO	SPI module host input and slave output data signal
					TIM5_CHA	Timer5 capture input / comparison output A
					TIM6_CHA	Timer6 capture input / comparison output A
					PCA_CH3	PCA capture input / comparison output 3
					UART0_RXD	UART0 RXD
					RCH_OUT	24M oscillation output
					XTH_OUT	32M oscillation output
					SWDIO	SWDIO
15	18	16	D4	P31	GPIO	P31 General purpose digital input / output pin
					TIM3_TOG	Timer3 toggle output
					PCA_ECI	PCA external clock
					PCLK_OUT	PCLK Output

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
					VC0OUT	VC0 output
					UART0_TXD	UART0 TXD
					RCL_OUT	RCL oscillator output
					HCLK_OUT	HCLK Output
					SWCLK	SWCLK
16	19	Note	Note	P32	GPIO	P32 General purpose digital input / output pin
					TIM3_TOGN	LPTimer flips reversed output
					PCA_CH2	PCA capture input / comparison output 2
					TIM6_CHB	Timer6 capture input/compare output B
					VC1OUT	VC1 output
					UART1_TXD	UART1 TXD
					PCA_CH4	PCA capture input / comparison output 4
					RTC_1HX	RTC1HZ output
					AIN2/VC2	Analog input
17	20	Note	Note	P33	GPIO	P33 General purpose digital input / output pin
					LPUART_RXD	LPUART RXD
					PCA_CH1	PCA capture input / comparison output 1
					TIM5_CHB	Timer5 capture input / comparison output B
					PCA_ECI	PCA external clock
					UART1_RXD	UART1 RXD
					XTL_OUT	32K oscillation output
					TIM1_TOGN	Timer1 flips reverse output
					AIN3/VC3	Analog input
18	1	Note	Note	P34	GPIO	P34 General purpose digital input / output pin
					PCA_CH0	PCA capture input / comparison output 0
					LPUART_TXD	LPUART TXD
					TIM5_CHA	Timer5 capture input / comparison output A
					TIM0_EXT	Timer0 clock input
					TIM4_CHA	Timer4 capture input / comparison output A
					RTC_1HZ	RTC1HZ output
					TIM1_TOG	Timer1 toggle output
					AIN4/VC4	Analog input
19	2	1	A2	P35	GPIO	P35 General purpose digital input / output pin
					UART1_TXD	UART1 TXD
					TIM6_CHB	Timer6 capture input/compare

Pin No. QFN20	Pin No. TSSOP20	Pin No. TSSOP16	Pin No. CSP16	Pin Name	Pin Type	Description
						output B
					UART0_TXD	UART0 TXD
					TIM0_GATE	Timer0 Gating
					TIM4_CHB	Timer4 capture input / compare output B
					SPI_MISO	SPI module host input and slave output data signal
					I^2C_SDA	I^2C data
					AIN5/VC5	Analog input
20	3	2	A3	P36	GPIO	P36 General purpose digital input / output pin
					UART1_RXD	UART1 RXD
					TIM6_CHA	Timer6 capture input / comparison output A
					UART0_RXD	UART0 RXD
					PCA_CH4	PCA capture input / comparison output 4
					TIM5_CHA	Timer5 capture input / comparison output A
					SPI_MOSI	SPI module master output slave input data signal
					I^2C_SCL	I^2C Clock
					AIN6/VC6/ AVREF	Analog input

Note: It is necessary to set the unleaded IO pin of the package to TSSOP20 as input and enable pull-up.

5 Block diagram

Functional module

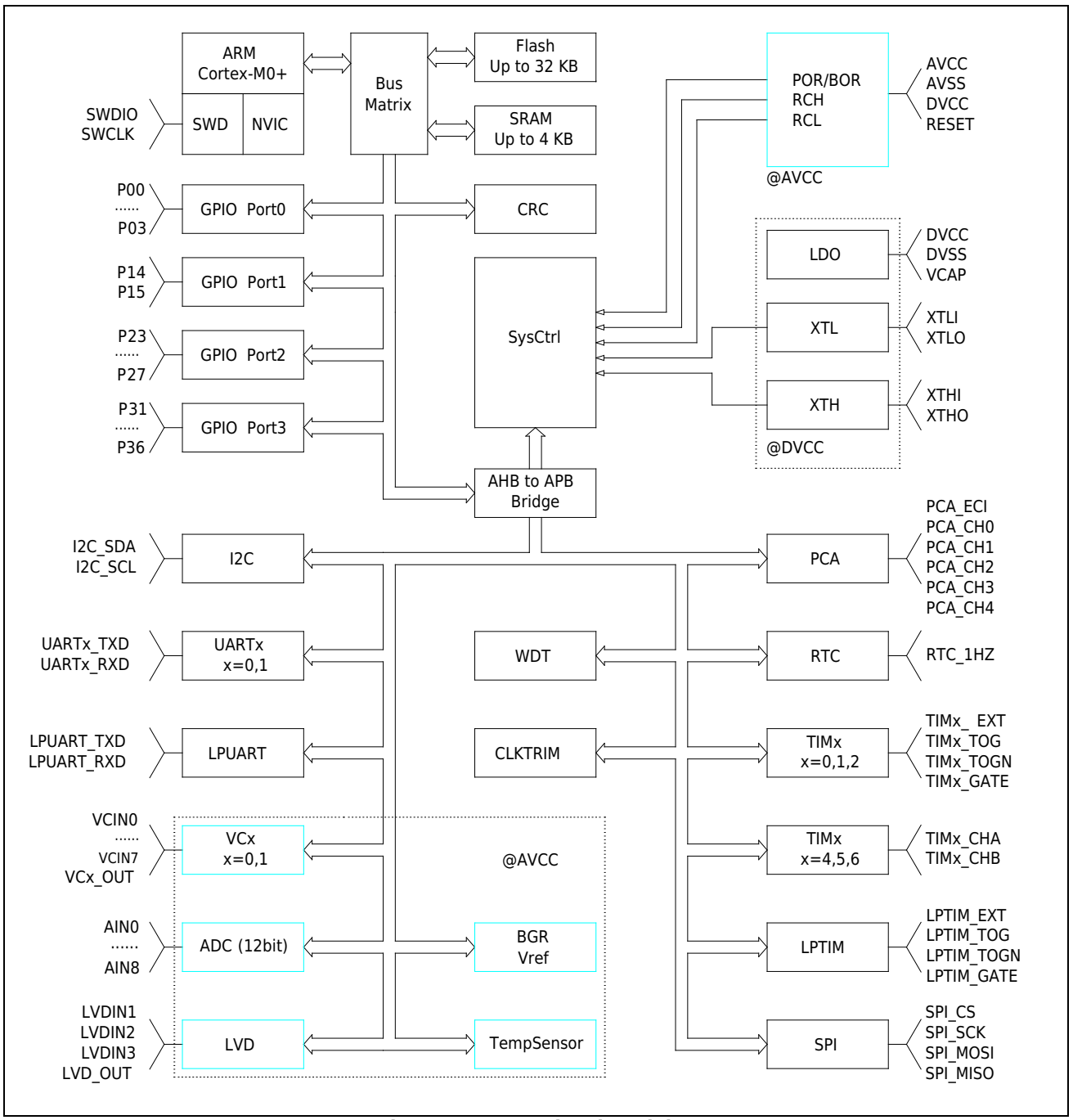
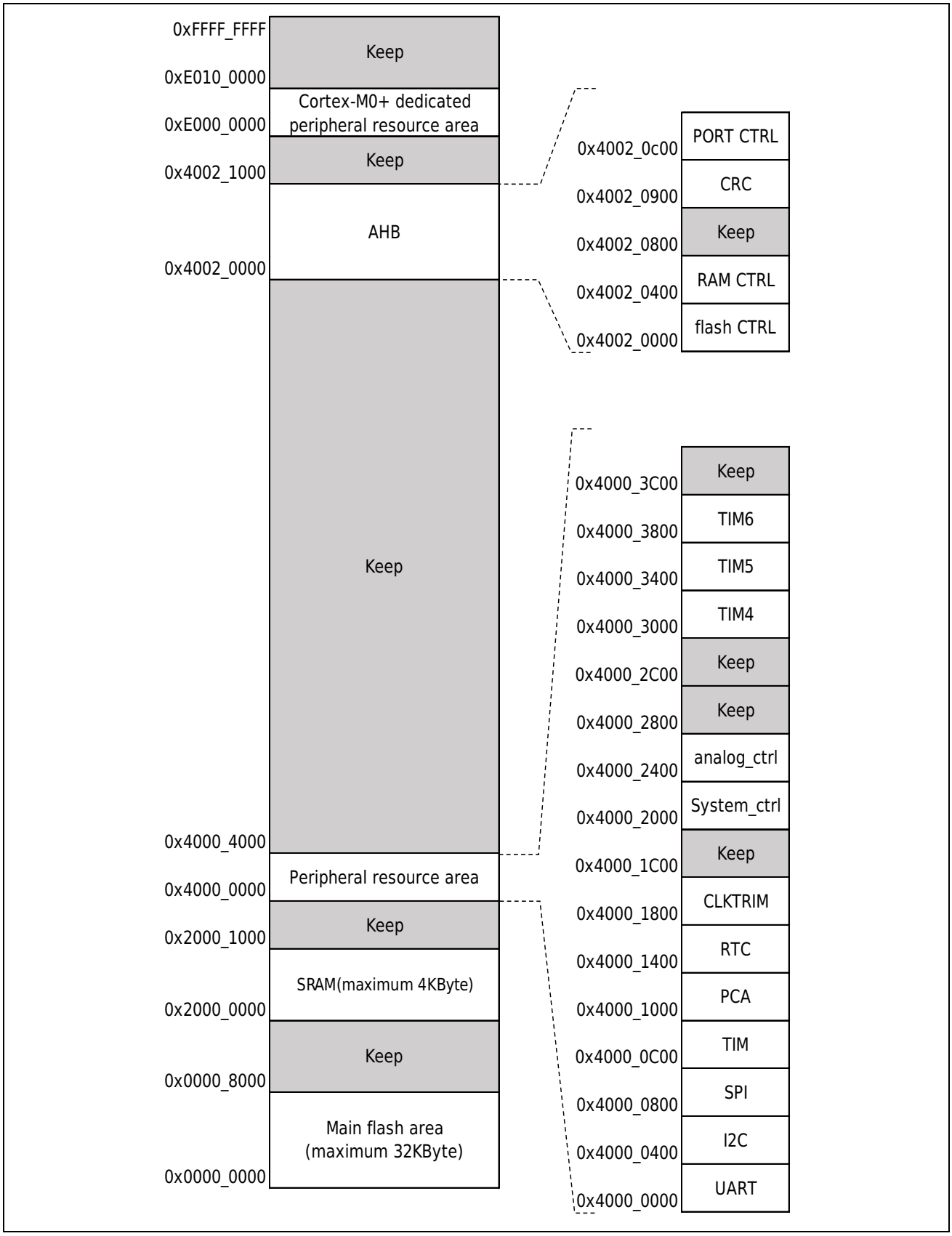
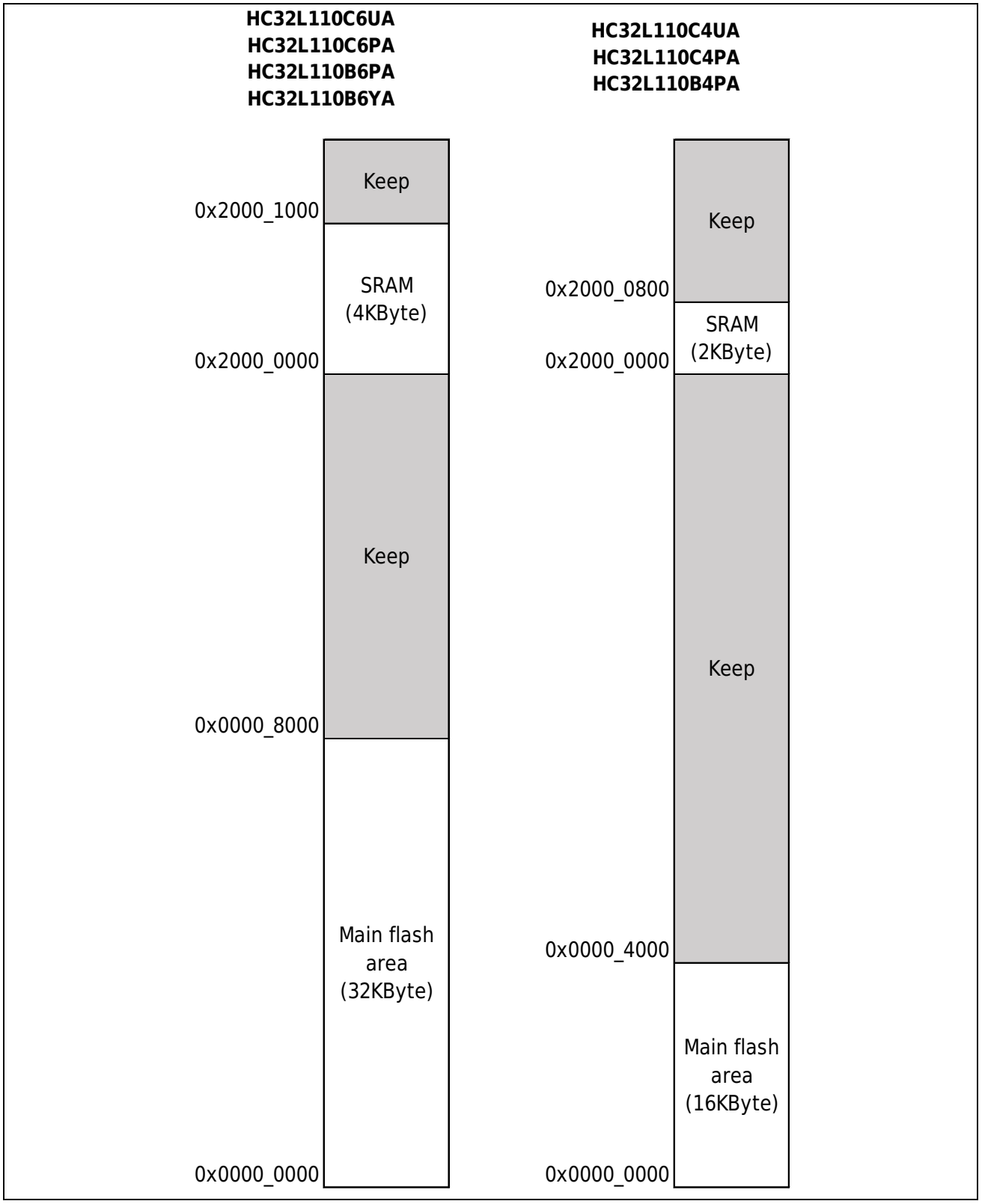


Figure 5-1 Functional modules

6 Storage area map




HC32L110C6UA
HC32L110C6PA
HC32L110B6PA
HC32L110B6YA
Keep
0x2000_1000
SRAM
(4KByte)
0x2000_0000
Keep
0x0000_8000
Main flash
area
(32KByte)
0x0000_0000
HC32L110C4UA
HC32L110C4PA
HC32L110B4PA
Keep
0x2000_0800
SRAM
(2KByte)
0x2000_0000
Keep
0x0000_4000
Main flash
area
(16KByte)
0x0000_0000

7 Electrical characteristics

7.1 Test Conditions

All voltages are referenced to VSS unless otherwise noted.

7.1.1 Minimum and maximum values

Unless otherwise specified, all minimum and maximum values will be in the worst environment through the test performed on 100% of the products in the production line at ambient temperature T_A=25℃ and T_A=$T_A$max ($T_A$max matches the selected temperature range) Guaranteed over temperature, supply voltage, and clock frequency.

The notes at the bottom of each table indicate data obtained through comprehensive evaluation, design simulation and/or process characteristics, and will not be tested on the production line; on the basis of comprehensive evaluation, the minimum and maximum values are after sample testing. Take the average value and add or subtract three times the standard distribution (mean ± 3Σ).

7.1.2 Typical value

Unless otherwise specified, typical data is based on T_A=25℃ and VCC=3.3V (1.8V ≤ VCC ≤ 5.5V voltage range). These data are only used for design guidance and not tested.

The typical ADC accuracy value is obtained by sampling a standard batch and testing under all temperature ranges. The error of 95% of the products is less than or equal to the given value (average ± 2Σ).

7.2 Absolute maximum ratings

If the load on the device exceeds the value given in the "Absolute Maximum Ratings" list, it may cause permanent damage to the device. This only gives the maximum load that can be withstood, and does not mean that the functional operation of the device under this condition is correct. Long-term operation of the device under the maximum condition will affect the reliability of the device.

Table 7-1 Voltage Characteristics

Symbol	Description	Minimum Value	Maximum Value	Unit
VCC – VSS	External main supply voltage (includes AVCC and DVCC)(1)	-0.3	5.5	V
V_{IN}	Input voltage on other pins(2)	VSS-0.3	VCC + 0.3	V
| ΔVCCx |	Voltage difference between different power supply pins		50	mV
| VSSx – VSS |	Voltage difference between different ground pins		50	mV
V_{ESD}(HBM)	ESD electrostatic discharge voltage (human body model)	Refer to absolute maximum electrical parameters		V

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.

2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

Table 7-2 Voltage Characteristics

Symbol	Description	Max (1)	Unit
I_{VCC}	The total current (supply current) through the DVCC/AVCC power cord (1)	300	mA
I_{VSS}	The total current through the VSS ground wire (outflow current) (1)	300	mA
I_{IO}	Output sink current on any I/O and control pin	25	mA
	Output current on any I/O and control pin	-25	mA
$I_{INJ(PIN)}$(2) (3)	Injection current of RESETB pin	+/-5	mA
	Injection current of XTHI pin of XTH and XTLI pin of XTL	+/-5	mA
	Injection current of other pins (4)	+/-5	mA
$\sum I_{INJ(PIN)}$ (2)	Total injection current on all I/O and control pins (4)	+/-25	mA

1. All power (DVCC, AVCC) and ground (DVSS, AVSS) pins must always be connected to an external power supply within the allowable range.
2. $I_{INJ(PIN)}$ must not exceed its limit, which means that V_{IN} does not exceed its maximum value. If it cannot be guaranteed that V_{IN} does not exceed its maximum value, it is also necessary to ensure that the external limit $I_{INJ(PIN)}$ does not exceed its maximum value. When $V_{IN}>V_{CC}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.
3. The reverse injection current will interfere with the analog performance of the device.
4. When several I/O ports have injection current at the same time, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute value of the forward injection current and the reverse injection current. This result is based on the characteristics of the maximum $\Sigma I_{INJ(PIN)}$ on the 4 I/O ports of the device.

Table 7-3 temperature characteristics

Symbol	Description	Numerical Value	Unit
T_{STG}	Storage temperature range	-65 ~ + 150	℃
T_J	Maximum junction temperature	105	℃

7.3 Operating conditions

7.3.1 General working conditions

Table 7-4 General Operating Conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
f_{HCLK}	Internal AHB clock frequency		0	32	MHz
f_{PCLK}	Internal APB clock frequency		0	32	MHz
DVCC	Working voltage of digital part		1.8	5.5	V
AVCC(1)	Analog part working voltage	Must be the same as DVCC(2)	1.8	5.5	V
P_D	Power dissipation T_A=85℃	TSSOP20		283	mW
T_A	Ambient temperature	Maximum power consumption	-40	85	℃
		Low power consumption (3)	-40	105	℃
T_J	Junction temperature range		-40	105	℃

1. When using an ADC, see ADC Electrical Specifications.
2. It is recommended to use the same power supply for DVCC and AVCC, allowing a maximum of 300mV difference between DVCC and AVCC during power-up and normal operation.
3. In a state of lower power dissipation, as long as T_J does not exceed T_{Jmax}, T_A can be extended to this range.

7.3.2 Working conditions at power-up and power-down

Table 7-5 Power-up and power-down operating conditions

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{Vcc}	VCC rising rate		0	5	V/μs
t_{Vcc}	VCC falling rate		0	5	V/μs

7.3.3 Embedded reset and LVD module features

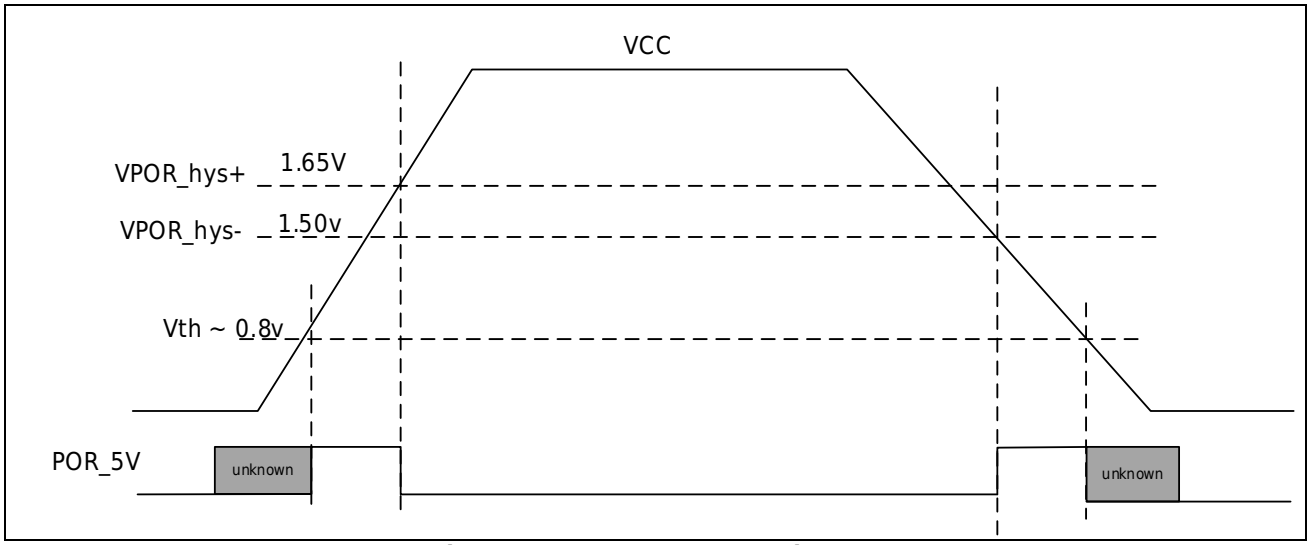


Figure 7-1 POR/Brown Out Diagram

1. Guaranteed by design, not tested in production.

Table 7-6 POR/Brown Out

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vpor	POR release voltage (power-on process) BOR detection voltage (power-down process)		1.45	1.50	1.65	V

Table 7-7 LVD module characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vex	External input voltage range		0		VCC	V
Vlevel	Detection threshold	LVD_CR.VTDS=0000 LVD_CR.VTDS =0001 LVD_CR.VTDS =0010 LVD_CR.VTDS =0011 LVD_CR.VTDS =0100 LVD_CR.VTDS=0101 LVD_CR.VTDS=0110 LVD_CR.VTDS=0111 LVD_CR.VTDS=1000 LVD_CR.VTDS=1001 LVD_CR.VTDS=1010 LVD_CR.VTDS=1011 LVD_CR.VTDS=1100 LVD_CR.VTDS=1101 LVD_CR.VTDS=1110 LVD_CR.VTDS=1111		1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.6 2.7 2.8 2.9 3.0 3.1 3.2 3.3		V
Icomp	Power consumption			0.12		μA
Tresponse	Response time			80		μs
Tsetup	Establishment time			400		μs
Vhyste	Hysteresis voltage			40		mV
Tfilter	Filter time	LVD_debounce = 000 LVD_debounce = 001 LVD_debounce = 010 LVD_debounce = 011 LVD_debounce = 100 LVD_debounce = 101 LVD_debounce = 110 LVD_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.4 Built-in reference voltage

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{REF25}	Internal 2.5V Reference Voltage	Room temperature 25°C 3.3V	2.475	2.5	2.525	V
V_{REF25}	Internal 2.5V Reference Voltage	-40~85°C 2.8~5.5V	2.438	2.5	2.563	V[1]
V_{REF15}	Internal 1.5V Reference Voltage	Room temperature 25°C 3.3V	1.485	1.5	1.515	V
V_{REF15}	Internal 1.5V Reference Voltage	-40~85°C 1.8~5.5V	1.463	1.5	1.538	V[1]
T_{coeff}	Internal 2.5V 1.5V temperature coefficient	-40~85°C			120	ppm/°C

1. The data is based on the assessment results and is not tested in production.

7.3.5 Operating Current Characteristics

Current consumption is a comprehensive index of multiple parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, I/O pin flip rate, and program in memory The location in and executed code, etc.

The microcontroller is in the following conditions:

- All I/O pins are in input mode and connected to a static level-VCC or VSS (no load).
- All peripherals are turned off, unless otherwise specified.
- The access time of the flash memory is adjusted to the frequency of f_{HCLK} (0 wait cycle for 0~24MHz, 1 wait cycle for 24~48MHz).
- When the peripheral is turned on: $f_{PCLK} = f_{HCLK}$.

Table 7-8 Operating Current Characteristics

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (Run in RAM)	All peripherals clock OFF, Run While(1) in RAM.	V_{CAP}=1.55V V_{CC}=3.3V	RCH clock source	4M	220		μA
				8M	400		
				16M	740		
				24M	1080		
				32M	1400		
I_{DD} (Run CoreMark)	All peripherals clock OFF, Run CoreMark in Flash.	V_{CAP} =1.55V V_{CC}=3.3V	RCH clock source	4M	670		μA
				8M	1300		
				16M	2380		
				24M	3410		
				32M (Flash Wait= 1)	3530		
IDD (Run mode)	All peripherals clock ON, Run while(1) in Flash	V_{CAP} =1.55V V_{CC}=1.8-5.5V	RCH clock source	4M	700	880	μA
				8M	1350	1600	
				16M	2500	3000	
				24M	3600	4300	
	All peripheral clock OFF, Run while(1) in Flash	V_{CAP} =1.55V V_{CC}=1.8-5.5V	RCH clock source	4M	550	750	
				8M	1050	1300	
				16M	1900	2400	
				24M	2700	3300	
				32M (Flash Wait= 1)	2850	3000	
IDD (Sleep mode)	All peripheral clock ON	V_{CAP} =1.55V V_{CC}=1.8-5.5V	RCH clock source	4M	260	280	μA
				8M	500	520	
				16M	950	970	
				24M	1400	1420	
	All	V_{CAP} =1.55V	RCH	4M	110	125	

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
	peripheral clock OFF	V_{CC}=1.8-5.5V	clock source	8M	190	210	
				16M	330	360	
				24M	470	500	
				32M	580	610	
IDD (LP Run)	All peripherals clock ON, Run while(1) in Flash	V_{CAP} =1.55V V_{CC}=1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = −40 to 25°C	7	9	µA
				T_A = 50 °C	7.3	9.2	
				T_A = 85 °C	8.9	11.3	
	All peripherals clock OFF, Run while(1) in Flash	V_{CAP} =1.55V V_{CC}=1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = −40 to 25°C	6	8	
				T_A = 50 °C	6.1	8.2	
				T_A = 85 °C	7.7	10.1	
IDD (LP Sleep)	All peripherals clock ON	V_{CAP} =1.55V V_{CC}=1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = −40 to 25°C	3.3	3.5	µA
				T_A = 50 °C	3.6	3.8	
				T_A = 85 °C	5.4	5.8	
	All peripherals clock OFF except LPTimer and RTC	V_{CAP} =1.55V V_{CC}=1.8-5.5V	XTL 32.768kHz (Driver = 1)	T_A = −40 to 25°C	2.2	2.4	
				T_A = 50 °C	2.5	2.6	
				T_A = 85 °C	4.2	4.6	
IDD (DeepSleep)	All peripherals clock OFF except RTC、WDT、LPTimer	V_{CAP} =1.55V V_{CC}=1.8-5.5V		T_A = −40 to 25°C	1.5	1.65	µA
				T_A = 50 °C	1.85	2.2	
				T_A = 85 °C	3.5	4.2	
	All peripherals clock OFF except WDT	V_{CAP} =1.55V V_{CC}=1.8-5.5V		T_A = −40 to 25°C	1.2	1.3	
				T_A = 50 °C	1.5	1.8	
				T_A = 85 °C	3.1	3.7	
	All peripherals clock OFF except LPTimer	V_{CAP} =1.55V V_{CC}=1.8-5.5V		T_A = −40 to 25°C	0.9	1	
				T_A = 50 °C	1.1	1.3	
				T_A = 85 °C	2.6	3	
	All peripherals clock OFF except RTC	V_{CAP} =1.55V V_{CC}=1.8-5.5V		T_A = −40 to 25°C	1.0	1.1	
				T_A = 50 °C	1.2	1.5	
				T_A = 85 °C	2.6	3.4	
	All peripherals clock OFF	V_{CAP} =1.55V V_{CC}=1.8-5.5V		T_A = −40 to 25°C	0.42	0.6	
				T_A = 50 °C	0.75	0.95	
				T_A = 85 °C	2.2	2.7	

1. If there are no other specified conditions, the value of this Typ is measured at 25℃& V_{CC} = 3.3V.
2. If there are no other specified conditions, the value of Max is the maximum value in the range of V_{CC} = 1.8-5.5 & Temperature = N40 – 85℃.
3. The data is based on the assessment results and is not tested in production.

7.3.6 Time to wake up from low power mode

The wake-up time is measured during the wake-up phase of the RCH oscillator. The clock source used when waking up depends on the current operating mode:

- Sleep mode: clock source is RCH oscillator
- RCH oscillator when entering deep sleep

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
T_{wu}	Sleep mode wake-up time			1.8		μs
	Deep sleep wake-up time	F_{MCLK} = 4MHz		9.0		μs
		F_{MCLK} = 8MHz		6.0		μs
		F_{MCLK} = 16MHz		5.0		μs
		F_{MCLK} = 24MHz		4.0		μs

1. The wake-up time is measured from the start of the wake-up event to the user program reading the first instruction.

7.3.7 External timer characteristic

External input high-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Fxth_ext	User external clock frequency (1)		0	8	32	MHz
V_{XTHH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTHL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTH)}$	Rise time (1)				20	ns
$T_{f(XTH)}$	Falling time (1)				20	ns
$T_{w(XTH)}$	Enter high or low time (1)		16			ns
$C_{in(XTH)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		40		60	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

External input low-speed clock

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Fxtl_ext	User external clock frequency (1)		0	32.768	1000	kHz
V_{XTLH}	Input pin high level voltage		0.7VCC		VCC	V
V_{XTLL}	Input pin low voltage		VSS		0.3VCC	V
$T_{r(XTL)}$	Rise time (1)				50	ns
$T_{f(XTL)}$	Falling time (1)				50	ns
$T_{w(XTL)}$	Enter high or low time (1)		450			ns
$C_{in(XTL)}$	Input capacitive reactance (1)			5		pF
Duty	Duty ratio		30		70	%
I_L	Input leakage current				±1	μA

1. Guaranteed by design, not tested in production.

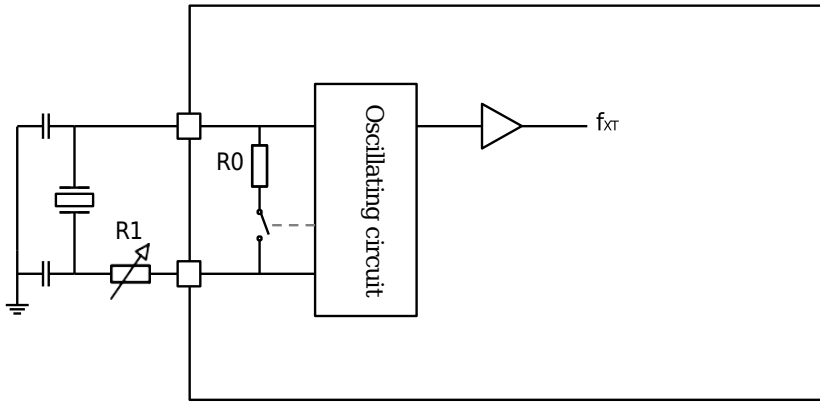
High-speed external clock XTH

The high-speed external clock (XTH) can be generated using a 8-32MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	8	-	32	MHz
ESR_{CLK}	Supported crystal oscillator ESR range	32MHz	-	-	60	Ω
		24MHz	-	-	80	
		16MHz	-	-	100	
		8MHz	-	-	120	
C_{LX} (3)	Load capacitance	Configure as required by the crystal manufacturer.	4	12	20	pF
Duty	Duty ratio	-	40	50	60	%
I_{dd} (4)	Current	XTH_CR[3:0]=0b1111	-	1000	-	μA
		XTH_CR[3:0]=0b1110	-	600	-	
		XTH_CR[3:0]=0b1010	-	370	-	
		XTH_CR[3:0]=0b0110	-	300	-	
		XTH_CR[3:0]=0b0010	-	160	-	
g_m	transconductance	XTH_CR[3:0]=0b1111	-	11.75	-	mA/V
		XTH_CR[3:0]=0b1110（32MHz，24MHz recommended value）	-	6.34	-	
		XTH_CR[3:0]=0b1101	-	4.38	-	
		XTH_CR[3:0]=0b1100	-	3.38	-	
		XTH_CR[3:0]=0b1011	-	7.41	-	
		XTH_CR[3:0]=0b1010（16MHz recommended value）	-	4.01	-	
		XTH_CR[3:0]=0b1001	-	2.77	-	
		XTH_CR[3:0]=0b1000	-	2.14	-	
		XTH_CR[3:0]=0b0111	-	5.59	-	
		XTH_CR[3:0]=0b0110（12MHz recommended value）	-	3.01	-	
		XTH_CR[3:0]=0b0101	-	2.08	-	

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
g_m	transconductance	XTH_CR[3:0]=0b0100	-	1.60	-	mA/V
		XTH_CR[3:0]=0b0011	-	2.50	-	
		XTH_CR[3:0]=0b0010（8MHz recommended value）	-	1.30	-	
		XTH_CR[3:0]=0b0001	-	0.93	-	
		XTH_CR[3:0]=0b0000	-	0.72	-	
T_{start}(5)	Start time	32MHz，CL=16pF @ XTH_CR[3:0]=0b1110	-	500	-	μs
		8MHz，CL=16pF @ XTH_CR[3:0]=0b0010	-	2	-	ms

1. The characteristic parameters of the resonator are provided by the crystal/ceramic resonator manufacturer.
2. According to comprehensive evaluation, it is not tested in production.
3. CLX refers to the two pin load capacitors CL1 and CL2of XTAL. For CL1 and CL2, it is recommended to use high-quality ceramic capacitors designed for high-frequency applications and select crystals or resonators that meet the requirements. Usually, CL1and CL2have the same parameters. Crystal manufacturers typically provide the parameters of load capacitance in a serial combination of CL1and CL2. When selecting CL1and CL2, the frequency and ESR parameters of the crystal oscillator should be taken into account, and the capacitance impedance of the PCB and MCU pins should be taken into account.
4. The current varies with the choice of frequency and driving capability. The higher the frequency, the stronger the driving ability, and the greater the current consumption..
5. Tstart is the startup time, which is measured from the software enabling XTH until a stable oscillation of 32MHz/8MHz is obtained. This value was measured using a standard crystal resonator with XTH_CR [5:4]=0b10 setting, and it may vary greatly depending on the crystal manufacturer and model.



Note：

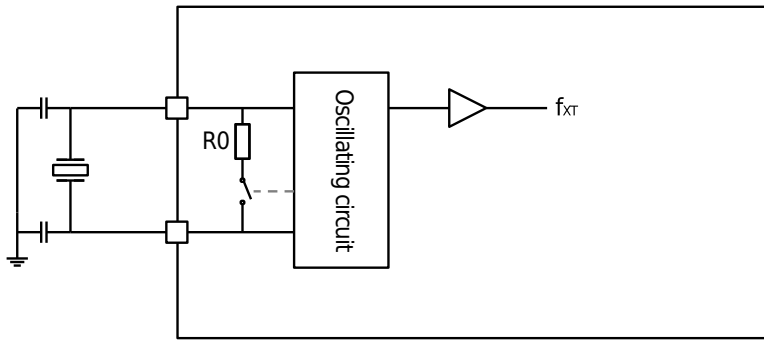
- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
- *If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.*
- *The chip has integrated feedback resistor R0.*
- *Damping resistor R1 is optional, and the value of the resistance depends on the crystal characteristics, with a default value of 0 Ω。*

Low-speed external clock XTL

The low-speed external clock (XTH) can be generated using a 32.768MHz crystal/ceramic resonator oscillator. The information given in this section is based on the results obtained through comprehensive characteristic evaluation using the typical external components listed in the table below. In the application, the resonator and load capacitor must be as close as possible to the oscillator pin to reduce output distortion and settling time at startup. For detailed parameters (frequency, packaging, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
F_{CLK}	Oscillation frequency	-	-	32.768	-	kHz
ESR_{CLK}	Supported crystal oscillator ESR range	-	-	-	60	kΩ
C_{Lx} (2)	Load capacitance	Configure as required by the crystal manufacturer.	8	12	20	pF
DC_{ACLK}	Duty ratio	-	30	50	70	%
I_{dd} (3)	Current	XTL_CR[3:0]=0b1111	-	1330	-	nA
		XTL_CR[3:0]=0b1011	-	1230	-	
		XTL_CR[3:0]=0b0111	-	1140	-	
		XTL_CR[3:0]=0b0011	-	1050	-	
		XTL_CR[3:0]=0b1110	-	630	-	
		XTL_CR[3:0]=0b1010 (recommended value)	-	580	-	
		XTL_CR[3:0]=0b0110	-	530	-	
		XTL_CR[3:0]=0b0010	-	490	-	
g_m	transconductance	XTL_CR[3:0]=0b1111	-	14.64	-	μA/V
		XTL_CR[3:0]=0b1011	-	13.17	-	
		XTL_CR[3:0]=0b0111	-	11.67	-	
		XTL_CR[3:0]=0b0011	-	10.15	-	
		XTL_CR[3:0]=0b1110	-	7.37	-	
		XTL_CR[3:0]=0b1010 (recommended value)	-	6.62	-	
		XTL_CR[3:0]=0b0110	-	5.87	-	
		XTL_CR[3:0]=0b0010	-	5.10	-	
T_{start} (4)	Start time	ESR=30kΩ C_L=12pF XTL_CR[3:0]=0b1010	-	2000	-	ms

1. Based on comprehensive evaluation, it is determined that testing will not be conducted during production。
2. CLX refers to the load capacitance of the two pins of XTAL. Users suggest selecting the capacitance value of this capacitor according to the requirements of the crystal manufacturer.
   If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.
   Example: When the crystal manufacturer provides a load capacitance of 8pF for the crystal, the capacitance value of the matching capacitor should be 16pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 15pF or 12pF.
   When the crystal manufacturer provides a matching capacitance of 12pF for the crystal, the capacitance value of the matching capacitance should be 12pF. Considering the distributed capacitance between PCB and MCU pins, it is recommended to choose matching capacitors with capacitance values of 10pF or 8pF.
3. Choosing a high-quality oscillator with a smaller ESR value (such as MSIV-TIN32.768kHz) can optimize current consumption by adjusting the XTL_CR [3:0] setting. The current consumption is proportional to the transconductance gm) provided by the circuit.
4. Tstart is the startup time, which is measured from the software enabling XTL until a stable 32768Hz oscillation is obtained. This value was measured using a standard crystal resonator with XTL_CR [3:0]=0b1010 and XTL_CR [5:4]=0b11 settings, and it may vary greatly depending on the crystal manufacturer and model



Note：

- *It is recommended to configure the matching capacitance of the crystal according to the requirements of the crystal manufacturer's technical manual.*
- *If the crystal manufacturer provides the capacitance value of the load capacitor, the capacitance value of the matching capacitor should be twice the capacitance value of the load capacitor provided by the crystal manufacturer. If the crystal manufacturer provides the capacitance value of the matching capacitor, then the capacitance value of the matching capacitor provided by the crystal manufacturer can be directly used.*
- *The chip has integrated feedback resistor R0.*

7.3.8 Internal timer characteristics

Internal RCH oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCH oscillator accuracy	User trimming step for given VCC and TA conditions		0.25		%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C	-3.5		+3.5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-2.0		+2.0	%
F_{CLK}	Oscillation frequency		4.0	4.0 8.0 16.0 22.12 24.0	24.0	MHz
I_{CLK}	Power consumption	F_{MCLK} = 4MHz		80		µA
		F_{MCLK} = 8MHz		100		µA
		F_{MCLK} = 16MHz		120		µA
		F_{MCLK} = 24MHz		140		µA
DC_{CLK}	Duty Cycle (1)		45	50	55	%

1. Resulted from comprehensive evaluation, not tested in production.

Internal RCL oscillator

Symbol	Papameter	Conditions	Min	Typ	Max	Unit
Dev	RCL oscillator accuracy	User trimming step for given VCC and TA conditions		0.5		%
		VCC = 1.8 ~ 5.5V T_{AMB} = -40 ~ 85°C	-5		+5	%
		VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-3		+3	%
F_{CLK}	Oscillation frequency			38.4 32.768		kHz
T_{CLK}	Start time			150		µs
DC_{CLK}	Duty Cycle (1)		25	50	75	%
I_{CLK}	Power consumption			0.25		µA

1. Resulted from comprehensive evaluation, not tested in production.

Internal low-speed clock 10k oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V	Operation voltage	-	1.8		5.5	V
Dev	Oscillator accuracy (1)	VCC = 1.8 ~ 5.5V T_{AMB} = -20 ~ 50°C	-50	-	50	%
F_{CLK}	Oscillation frequency	VCC=3.3v T_{AMB} = 25°C		10		KHz

1. Resulted from comprehensive evaluation, not tested in production.

7.3.9 Memory Characteristics

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
ECFLASH	Erase times	Regulator voltage=1.5V, T_{AMB} = 25℃	20			kcycles
RETFLASH	Data retention period	T_{AMB} = 85℃, after 20 kcycles	20			Years
Tw_prog	Programming time		6		7.5	μs
Tp_erase	Page erase time		4		5	ms
Tm_erase	Whole chip erase time		30		40	ms

7.3.10 EFT Characteristic

A chip reset can restore the system to normal operation.

Symbol	Level/Type
EFT to IO (IEC61000-4-4)	Class:4(B)
EFT to Power (IEC61000-4-4)	Class:4(B)

Software recommendations

The software process must include control to deal with program runaway, such as:

- Corrupted program counter
- Unexpected reset
- Critical data is destroyed (control registers, etc.)

During the EFT test, interference that exceeds the application requirements can be directly applied to the chip power supply or IO. When an unexpected action is detected, the software part is strengthened to prevent unrecoverable errors.

7.3.11 ESD Characteristic

Using specific measurement methods, the chip is subjected to strength testing to determine its electrical sensitivity performance.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$VESD_{HBM}$	ESD @ Human Body Mode			4		KV
$VESD_{CDM}$	ESD @ Charge Device Mode			1		KV
$VESD_{MM}$	ESD @ machine Mode			200		V
Ilatchup	Latch up current			200		mA

7.3.12 Port characteristics

Output characteristics——ports

Table 7-9 Port output characteristics

Symbol	Parameter	Conditions	Min	Max	Uuit
V_{OH}	High level output voltage Source Current	Sourcing 4 Ma, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 6 Ma, VCC = 3.3 V (see Note 2)	VCC-0.6		V
V_{OL}	Low level output voltage Sink Current	Sinking 4 Ma, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 6 Ma, VCC = 3.3 V (see Note 2)		VSS+0.6	V
V_{OHD}	High level output voltage Double source Current	Sourcing 8 Ma, VCC = 3.3 V (see Note 1)	VCC-0.25		V
		Sourcing 12 Ma, VCC = 3.3V (see Note 2)	VCC-0.6		V
V_{OLD}	Low level output voltage Double Sink Current	Sinking 8 Ma, VCC = 3.3 V (see Note 1)		VSS+0.25	V
		Sinking 12 Ma, VCC = 3.3 V (see Note 2)		VSS+0.6	V

NOTES:

1. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 40 Ma to satisfy the maximum specified voltage drop.
2. The maximum total current, IOH(max) and IOL(max), for all outputs combined, should not exceed 100 Ma to satisfy the maximum specified voltage drop.

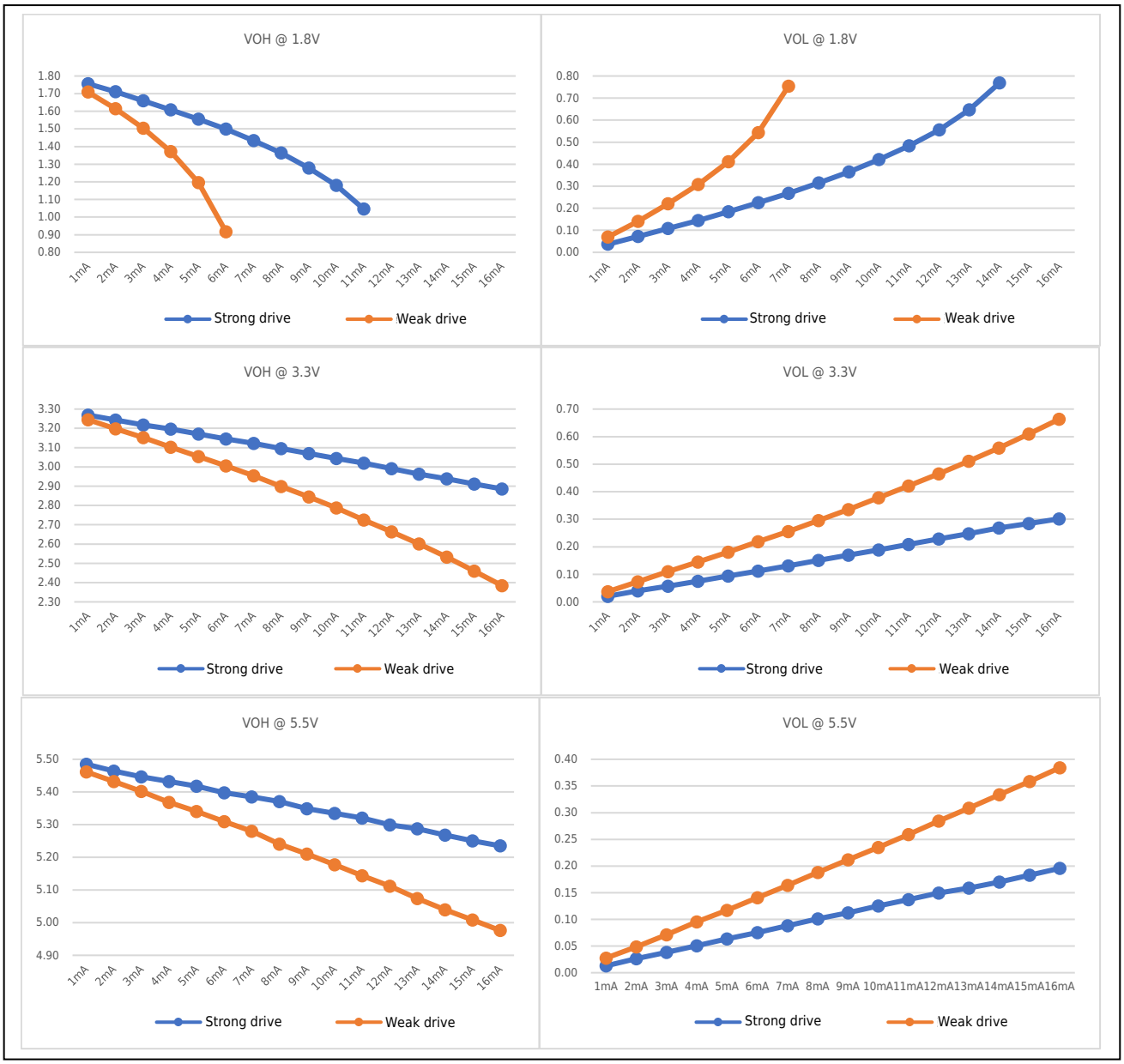


Figure 7-2 VOH/VOL measured curve of output port

Input Characteristics - Ports P0, P1, P2, P3

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{IH}	Positive-going input threshold voltage	VCC=1.8V	0.7VCC			V
		VCC=3.3V	0.7VCC			V
		VCC=5.5V	0.7VCC			V
V_{IL}	Negative-going input threshold voltage	VCC=1.8V			0.3VCC	V
		VCC=3.3V			0.3VCC	V
		VCC=5.5V			0.3VCC	V
$V_{hys(1)}$	Input voltage hysteresis (V_{IH} – V_{IL})	VCC=1.8V		0.3		V
		VCC=3.3V		0.4		V
		VCC=5.5V		0.6		V
$R_{pullhigh}$	Pullup resistor	Pullup enabled VCC=3.3V		80		kΩ
$R_{pulllow}$	Pulldown resistor	Pulldown enabled VCC=3.3V		40		kΩ
C_{input}	Input capacitance			5		pF

1. Resulted from comprehensive evaluation, not tested in production.

Port external input sampling requirements——Timer Gate/Timer Clock

Symbol	Papameter	Conditions	VCC	Min	Max	Uuit
t(int)	External interrupt timing	External trigger signal for the interrupt flag (see Note 1)	1.8V	30		ns
			3.3V	30		ns
			5.5V	30		ns
t(cap)	Timer capture timing	Timer4/5/6 capture pulse width Fsystem = 4MHz	1.8V	0.5		μs
			3.3V	0.5		μs
			5.5V	0.5		μs
t(clk)	Timer clock frequency applied to pin	Timer0/1/2/4/5/6 external clock input Fsystem = 4MHz	1.8V		PCLK/2	MHz
			3.3V		PCLK/2	MHz
			5.5V		PCLK/2	MHz
t(pca)	PCA clock frequency applied to pin	PCA external clock input Fsystem = 4MHz	1.8V		PCLK/8	MHz
			3.3V		PCLK/8	MHz
			5.5V		PCLK/8	MHz

NOTE:

1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.

Port leakage characteristics - P0, P1, P2, P3

Symbol	Papameter	Conditions	VCC	Max	Unit
$I_{lkg(Px.y)}$	Leakage current	$V_{(Px.y)}$ (see Note 1,2)	1.8 V/3.6 V	±50	nA

NOTES:

1. The leakage current is measured with VSS or VCC applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

7.3.13 RESETB pin characteristics

The RESETB pin input driver uses CMOS technology, which is connected with a pull-up resistor that cannot be disconnected.

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
$V_{IL(RESETB)}$ (1)	Input low level voltage		-0.3		0.3VCC	V V
$V_{IH(RESETB)}$	Input high level voltage		0.7VCC		VCC+0.3	V
$V_{hys(RESETB)}$	Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistance	VIN = VSS		80		kΩ
$T_{F(RESETB)}$ (1)	Input filter pulse				2	μs
$T_{NF(RESETB)}$ (1)	Input unfiltered pulse		10			μs

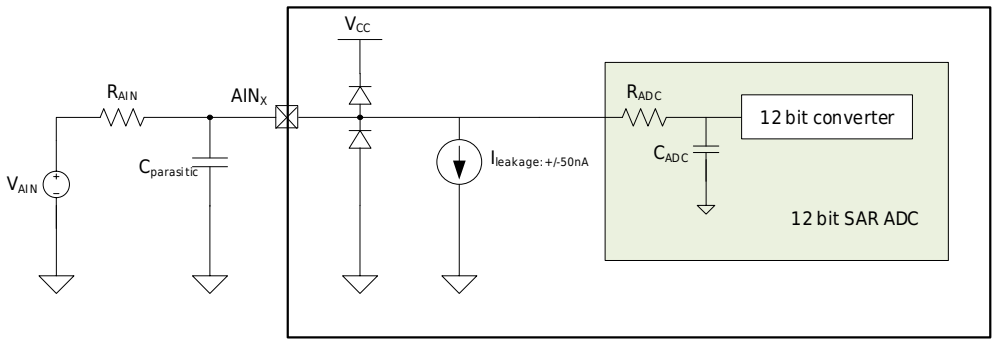
1. Guaranteed by design, not tested in production.

7.3.14 ADC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
V_{ADCIN}	Input voltage range	Single ended	0		$V_{ADCREFIN}$	V
$V_{ADCREFIN}$	Input range of external reference voltage	Single ended	0		VCC	V
$DEV_{VCC/3}$	VCC/3 accuracy			3		%
I_{ADC1}	Active current including reference generator and buffer	200Ksps		2		mA
I_{ADC2}	Active current without reference generator and buffer	1Msps		0.5		mA
C_{ADCIN}	ADC input capacitance			16	19.2	pF
R_{ADC}(1)	ADC sampling switch impedance			1.5		kΩ
R_{AIN}(1)	ADC external input resistor(2)				100	kΩ
F_{ADCCLK}	ADC clock Frequency				24M	Hz
$T_{ADCSTART}$	Startup time of reference generator and ADC core			30		μs
$T_{ADCCONV}$	Conversion time		20	24	28	cycles
ENOB	Effective Bits	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=EXREF		10.3		Bit
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		10.3		Bit
		200Ksps@VCC>=1.8V REF=internal 1.5V		9.4		Bit
		200Ksps@VCC>=2.8V REF=internal 2.5V		9.4		Bit
SNR	Signal to Noise Ratio	1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V		68.2		dB

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
		200Ksps@VCC>=1.8V REF=EXREF				
		1Msps@VCC>=2.7V 500Ksps@VCC>=2.4V 200Ksps@VCC>=1.8V REF=VCC		68.2		dB
		200Ksps@VCC>=1.8V REF=internal 1.5V		60		dB
		200Ksps@VCC>=2.8V REF=internal 2.5V		60		dB
DNL(1)	Differential non-linearity	200KSps; VREF=EXREF/VCC	-1		1	LSB
INL(1)	Integral non-linearity	200KSps; VREF=EXREF/VCC	-3		3	LSB
E_o	Offset error			0		LSB
E_g	Gain error			0		LSB

1. Guaranteed by design, not tested in production.
2. The typical application of ADC is shown in the figure below:



Under the condition of 0.5LSB sampling error accuracy requirement, the calculation formula of external input impedance is as follows:

$$R_{AIN} = \frac{M}{F_{ADC} * C_{ADC} * (N + 1) * \ln(2)} - R_{ADC}$$

Among them F_{ADC} is the ADC clock frequency, the register ADC_CR0<3:2> can set the relationship between it and PCLK, as shown in the following table:

The following table shows the ADC clock frequency F_{ADC} Relationship with PCLK frequency division ratio:

ADC_CR0<3:2>	N
00	1
01	2
10	4
11	8

M is the number of sampling periods, which is set by the register ADC_CR0<13:12>.

The following table shows the relationship between sampling time t_{sa} and ADC clock frequency F_{ADC}:

ADC_CR0<13:12>	**M**
00	4
01	6
10	8
11	12

The following table shows the relationship between ADC clock frequency F_{ADC} and external resistance R_{AIN} (M=12, under the condition of sampling error 0.5LSB):

R_{AIN} (kΩ)	**F_{ADC}(kHz)**
10	5600
30	2100
50	1300
80	820
100	660
120	550
150	450

For the above typical applications, you should pay attention to:

- Minimize the ADC input port AIN_X parasitic capacitance $C_{PARACITIC}$;
- In addition to considering R_{AIN} the value, if the internal resistance of the signal source V_{AIN} is large, it also needs to be considered.

7.3.15 VC Characteristic

Symbol	Parameter	Conditions	Minimum Value	Typical Value	Maximum Value	Unit
Vin	Input voltage range		0		5.5	V
Vincom	Input common mode range		0		VCC-0.2	V
Voffset	Input offset	Room temperature 25°C 3.3V	-10		+10	mV
Icomp	Comparator's current	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		0.3 1.2 10 20		μA
Tresponse	Comparator's response time when one input cross another	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Tsetup	Comparator's setup time when ENABLE. Input signals unchanged.	VCx_BIAS_SEL=00 VCx_BIAS_SEL=01 VCx_BIAS_SEL=10 VCx_BIAS_SEL=11		20 5 1 0.2		μs
Twarmup	From main bandgap enable to Temp sensor voltage、ADC internal 1.5V, 2.5V reference stable			20		μs
Tfilter	Digital filter time	VC_debounce = 000 VC_debounce = 001 VC_debounce = 010 VC_debounce = 011 VC_debounce = 100 VC_debounce = 101 VC_debounce = 110 VC_debounce = 111		7 14 28 112 450 1800 7200 28800		μs

7.3.16 TIM timer features

For details on the characteristics of the input and output multiplex function pins (output compare, input capture, external clock, PWM output), see the table below.

Table 7-10 Advanced Timer (ADVTIM) Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=32MHz	31.3		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=32MHz	0	16	MHz
Res_{Tim}	Timer resolution			16	位
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=32MHz	0.0313	2051	μs
T_{MAX_COUNT}	Maximum possible count			67108864	t_{TIMCLK}
		f_{TIMCLK}=32MHz		2.1	s

1. Guaranteed by design, not tested in production.

Table 7-11 Basic Timer Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=32MHz	31.3		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=32MHz	0	16	MHz
Res_{Tim}	Timer resolution	reload count		16	位
		free count		32	位
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=32MHz	0.0313	2051	μs
T_{MAX_COUNT}	Maximum possible count (reload mode)			16777216	t_{TIMCLK}
		f_{TIMCLK}=32MHz		524.3	ms

1. Guaranteed by design, not tested in production.

Table 7-12 PCA Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=32MHz	31.3		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=32MHz	0	16	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=32MHz	0.0313	2051	μs
T_{MAX_COUNT}	Maximum possible count			2097152	t_{TIMCLK}
		f_{TIMCLK}=32MHz		65.54	ms

1. Guaranteed by design, not tested in production.

Table 7-13 Low Power Timer Features

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	Timer to distinguish time		1		t_{TIMCLK}
		f_{TIMCLK}=32MHz	31.3		ns
f_{ext}	External clock frequency		0	$f_{TIMCLK/2}$	MHz
		f_{TIMCLK}=32MHz	0	16	MHz
Res_{Tim}	Timer resolution			16	Bit
$T_{counter}$	When the internal clock is selected, the 16-bit counter clock cycle		1	65536	t_{TIMCLK}
		f_{TIMCLK}=32MHz	0.0313	2051	μs
T_{MAX_COUNT}	Maximum possible count			65536	t_{TIMCLK}
		f_{TIMCLK}=32MHz		2.05	ms

1. Guaranteed by design, not tested in production.

Table 7-14 WDT Characteristics

Symbol	Parameter	Conditions	Minimum Value	Maximum Value	Unit
t_{res}	WDT overflow time	f_{WDTCLK}=10kHz	1.6	52000	ms

1. Guaranteed by design, not tested in production.

7.3.17 Communication Interface

I2C features

I2C interface characteristics are as follows:

Table 7-15 I2C Interface Characteristics

Symbol	Parameter	Standard mode (100K)		Fast mode (400K)		High speed mode (1M)		Unit
		Minimum Value	Maximum Value	Minimum Value	Maximum Value	Minimum Value	Maximum Value	
t_{SCLL}	SCL clock low time	4.7		1.25		0.5		μs
t_{SCLH}	SCL clock high time	4.0		0.6		0.26		μs
$t_{SU.SDA}$	SDA establishment time	250		100		50		ns
$t_{HD.SDA}$	SDA hold time	0		0		0		μs
$t_{HD.STA}$	Start condition hold time	2.5		0.625		0.25		μs
$t_{SU.STA}$	Repeated start condition establishment time	2.5		0.6		0.25		μs
$t_{SU.STO}$	Stop condition establishment time	0.25		0.25		0.25		μs
t_{BUF}	Bus idle (stop condition to start condition)	4.7		1.3		0.5		μs

1. Guaranteed by design, not tested in production.

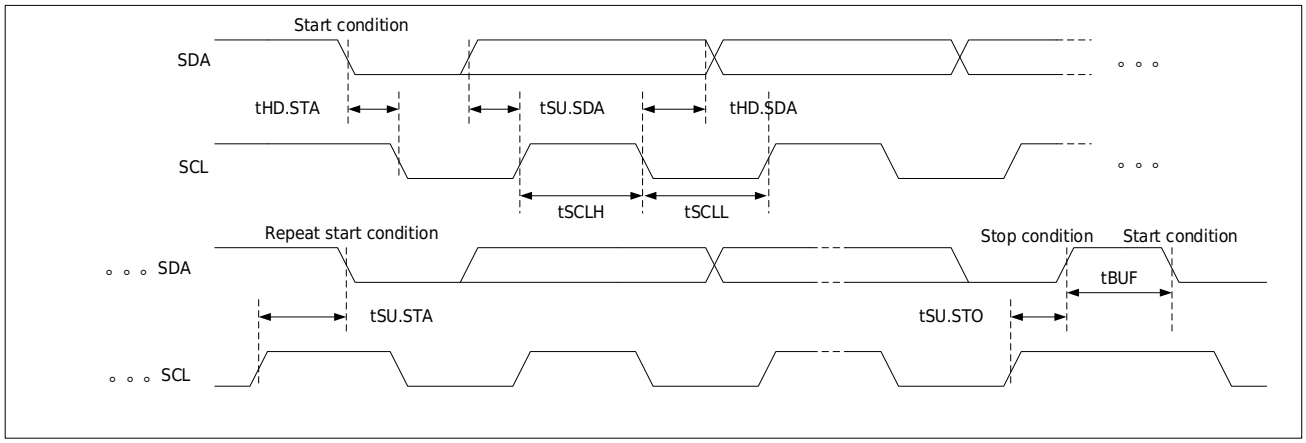


Figure 7-3 I2C Interface Timing

SPI features

Table 7-16 SPI Interface Features(1)(2)

Symbol	Parameter	Conditions	Minimum value	Maximum Value	Unit
$t_{c(SCK)}$	Serial clock period(3)	Host Transmit Mode f_{PCLK} = 32MHz	62.5	-	ns
		Host Receive Mode f_{PCLK} = 32MHz	160	-	ns
		Slave Transmit Mode f_{PCLK} = 32MHz	160	-	ns
		Slave Receive Mode f_{PCLK} = 32MHz	84	-	ns
$t_{w(SCKH)}$	High level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{w(SCKL)}$	Low level time of serial clock	Host mode	0.45 × $t_{c(SCK)}$	-	ns
		Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{su(SSN)}$	Setup time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{h(SSN)}$	Hold time selected by slave	Slave mode	0.45 × $t_{c(SCK)}$	-	ns
$t_{v(MO)}$	Effective time of host data output	-	-	3	ns
$t_{h(MO)}$	Hold time of host data output	-	2	-	ns
$t_{v(SO)}$	Effective time of slave data output	-	-	1.5*T_{pclk}+20	ns
$t_{h(SO)}$	Hold time of slave data output	-	0.5*T_{pclk}+10	-	ns
$t_{su(MI)}$	Setup time of host data input	-	10	-	ns
$t_{h(MI)}$	Hold time of host data input	-	2	-	ns
$t_{su(SI)}$	Setup time of slave data input	-	10	-	ns
$t_{h(SI)}$	Hold time of slave data input	-	2	-	ns

1. Guaranteed by design and not tested in production.
2. The data is based on the condition of VCC = 3.0V.
3. The maximum prescaler factor in host mode is PCLK/2, and in slave mode, it is PCLK/4.

The waveform and timing parameters of the SPI interface signal are as follows:

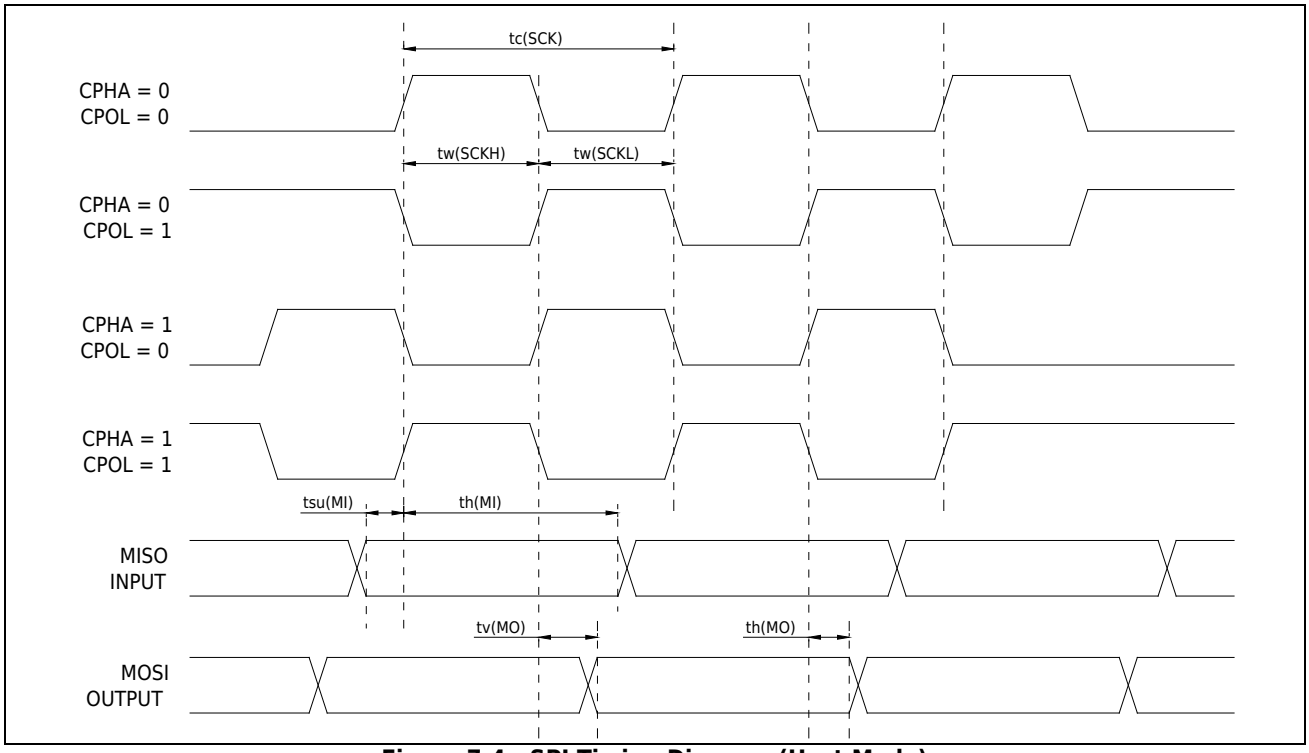


Figure 7-4 SPI Timing Diagram (Host Mode)

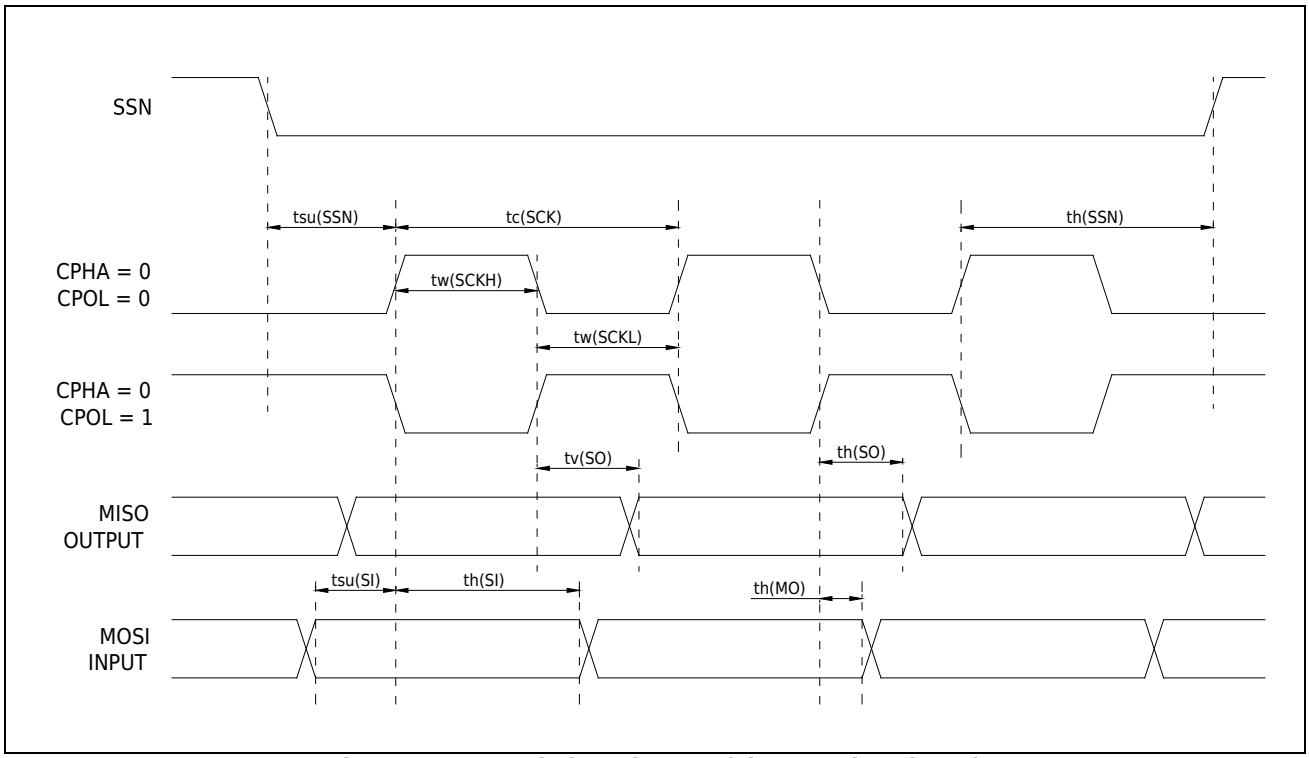


Figure 7-5 SPI Timing Diagram (slave mode cpha=0)

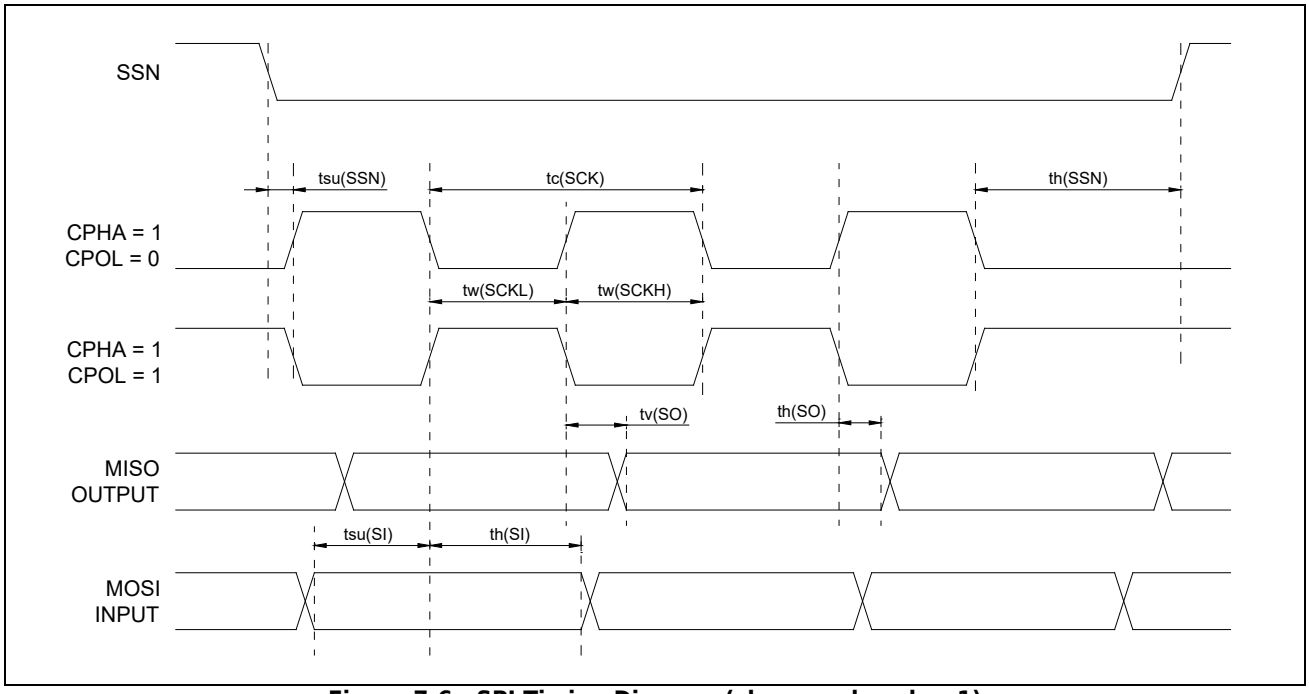
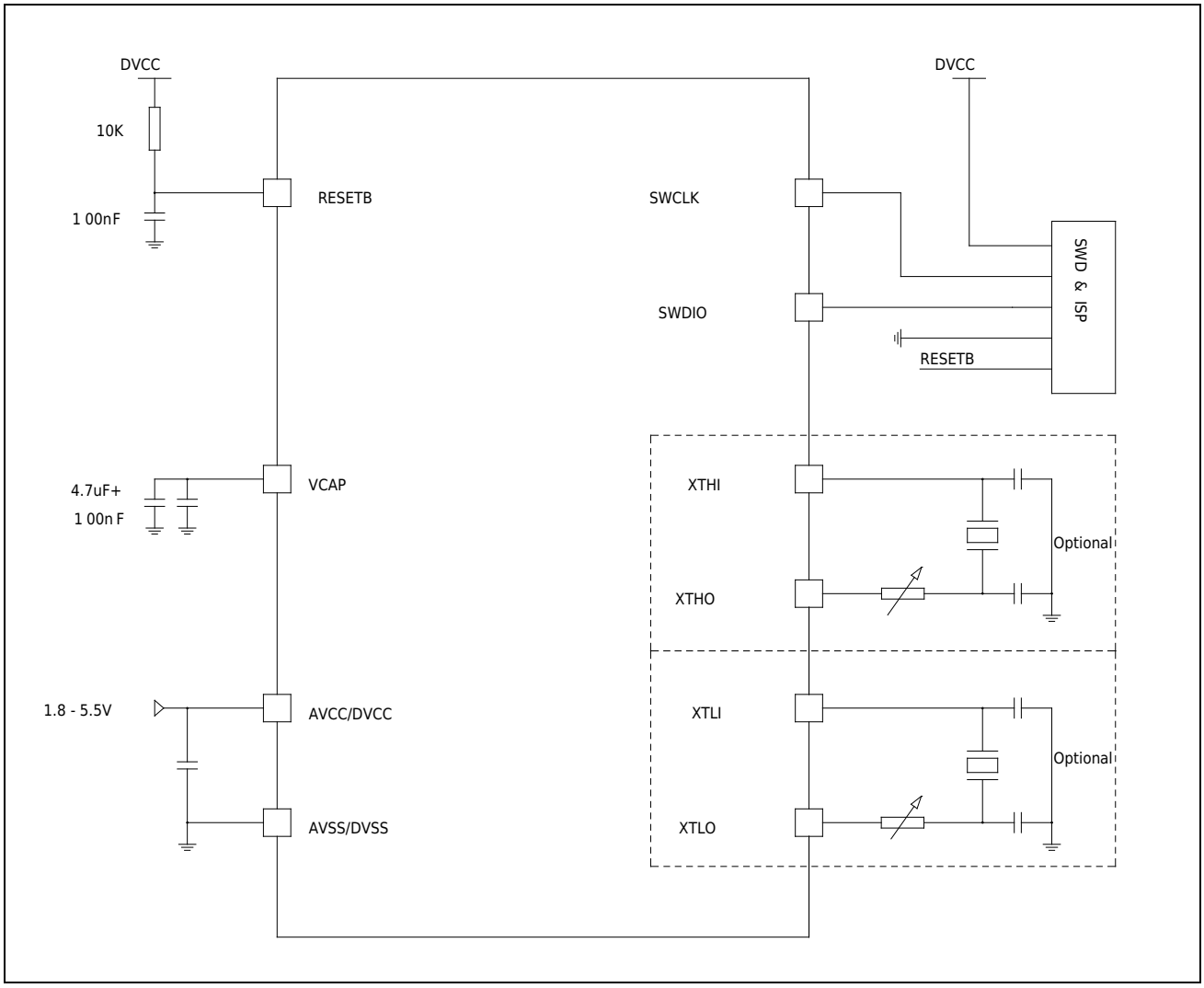


Figure 7-6 SPI Timing Diagram (slave mode cpha=1)

8 Typical application circuit diagram



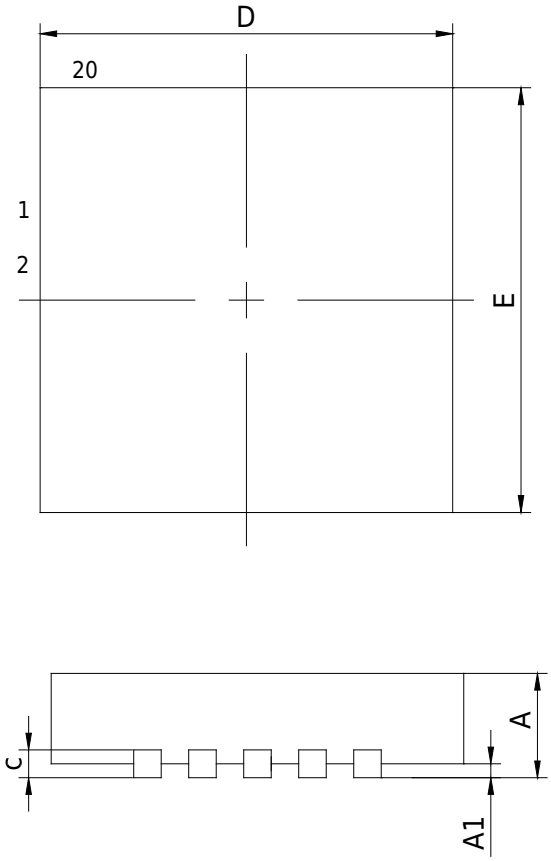
Note:

– Each power supply needs a decoupling capacitor, which should be as close as possible to the corresponding power supply pin.

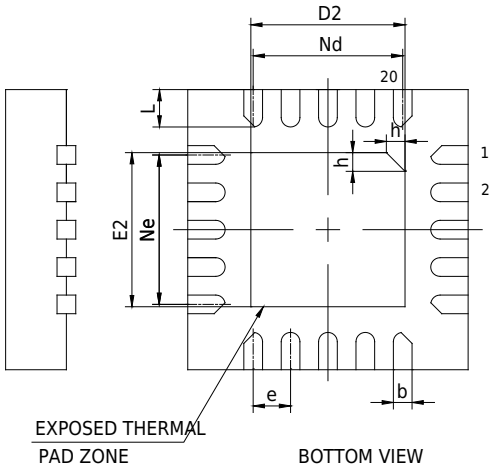
9 Package information

9.1 Packaging Size

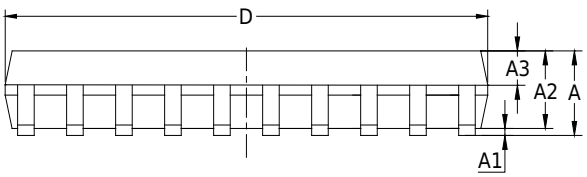
QFN20 packaging

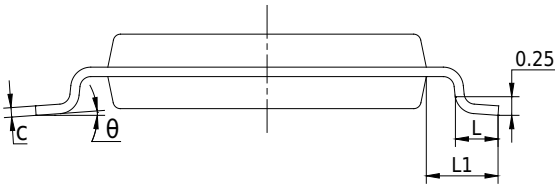


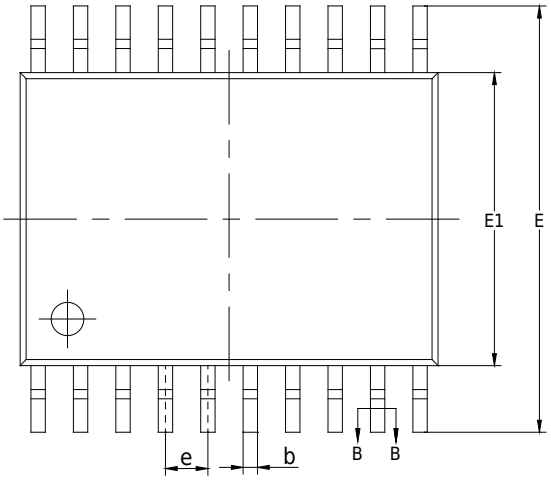
Symbol	QFN20 (3x3) millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F carrier size (Mil)	75 x 75		

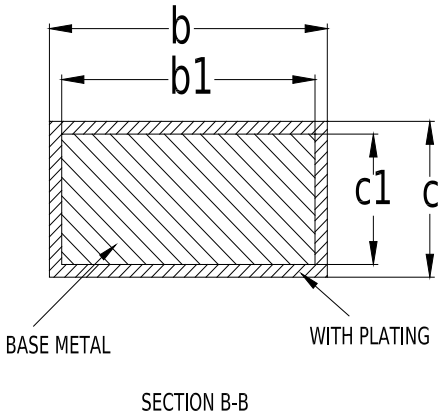


TSSOP20 packaging









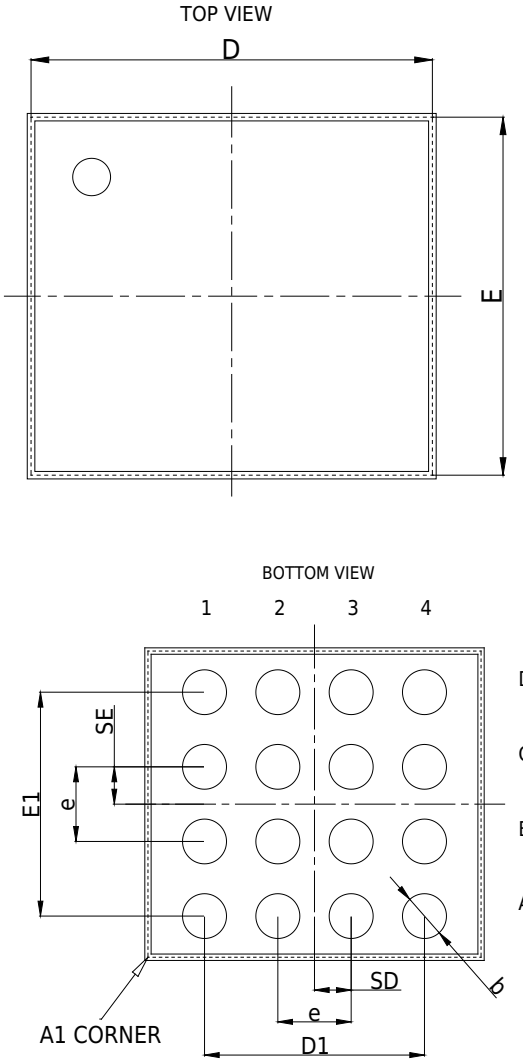
SECTION B-B

Symbol	TSSOP20 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	--	8°

NOTE:

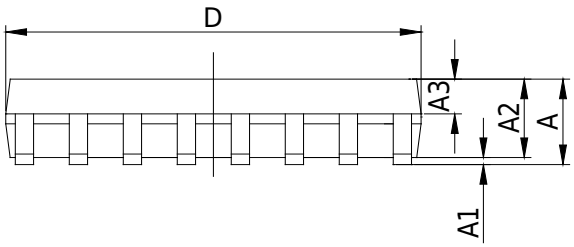
Dimensions “D” and “E1” do not include mold flash.

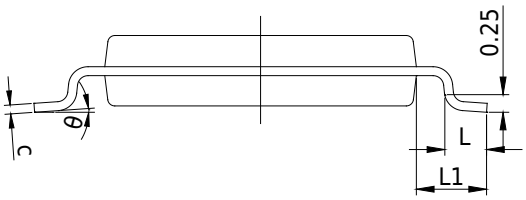
CSP16 packaging

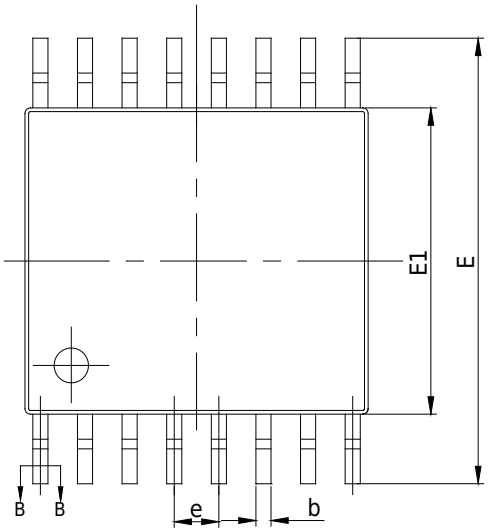


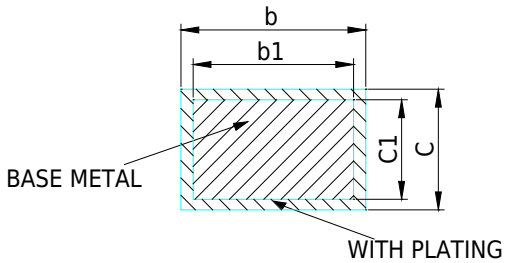
Symbol	CSP16 millimeter		
	Min	Nom	Max
A	0.496	0.533	0.57
A1	0.148	0.168	0.188
A2	0.037	0.04	0.043
b	0.18	0.21	0.24
S	0.3115	0.325	0.3385
D	1.565	1.59	1.615
E	1.411	1.436	1.461
e	0.35BSC		
D1	1.05BSC		
E1	1.05BSC		
SD	0.175		
SE	0.175		
n	16		

TSSOP16 packaging









SECTION B-B

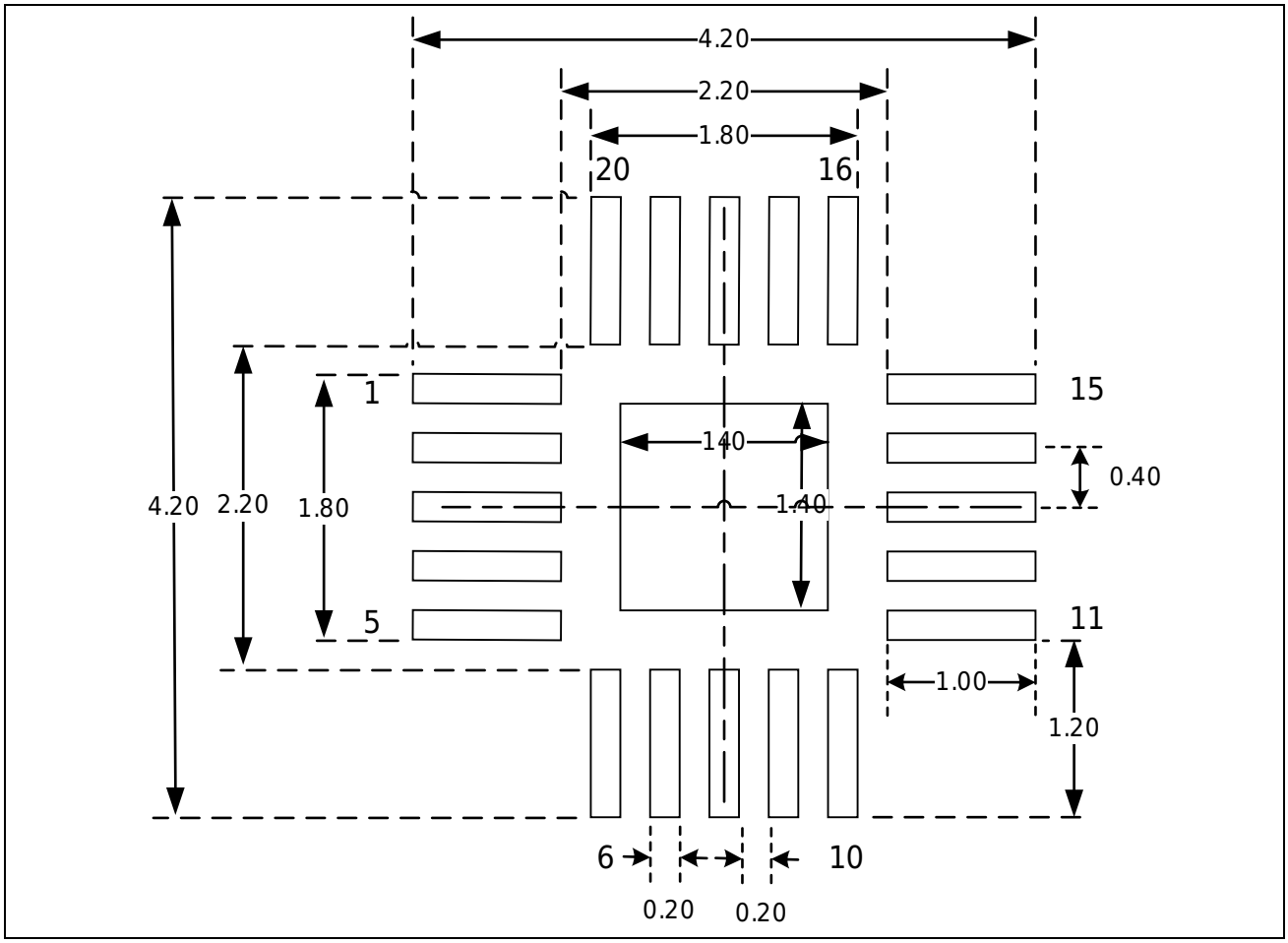
Symbol	TSSOP16 millimeter		
	Min	Nom	Max
A	--	--	1.20
A1	0.05	--	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	--	0.28
b1	0.19	0.22	0.25
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	--	8°

NOTE:

Dimensions “D” and “E1” do not include mold flash.

9.2 Schematic diagram of pad

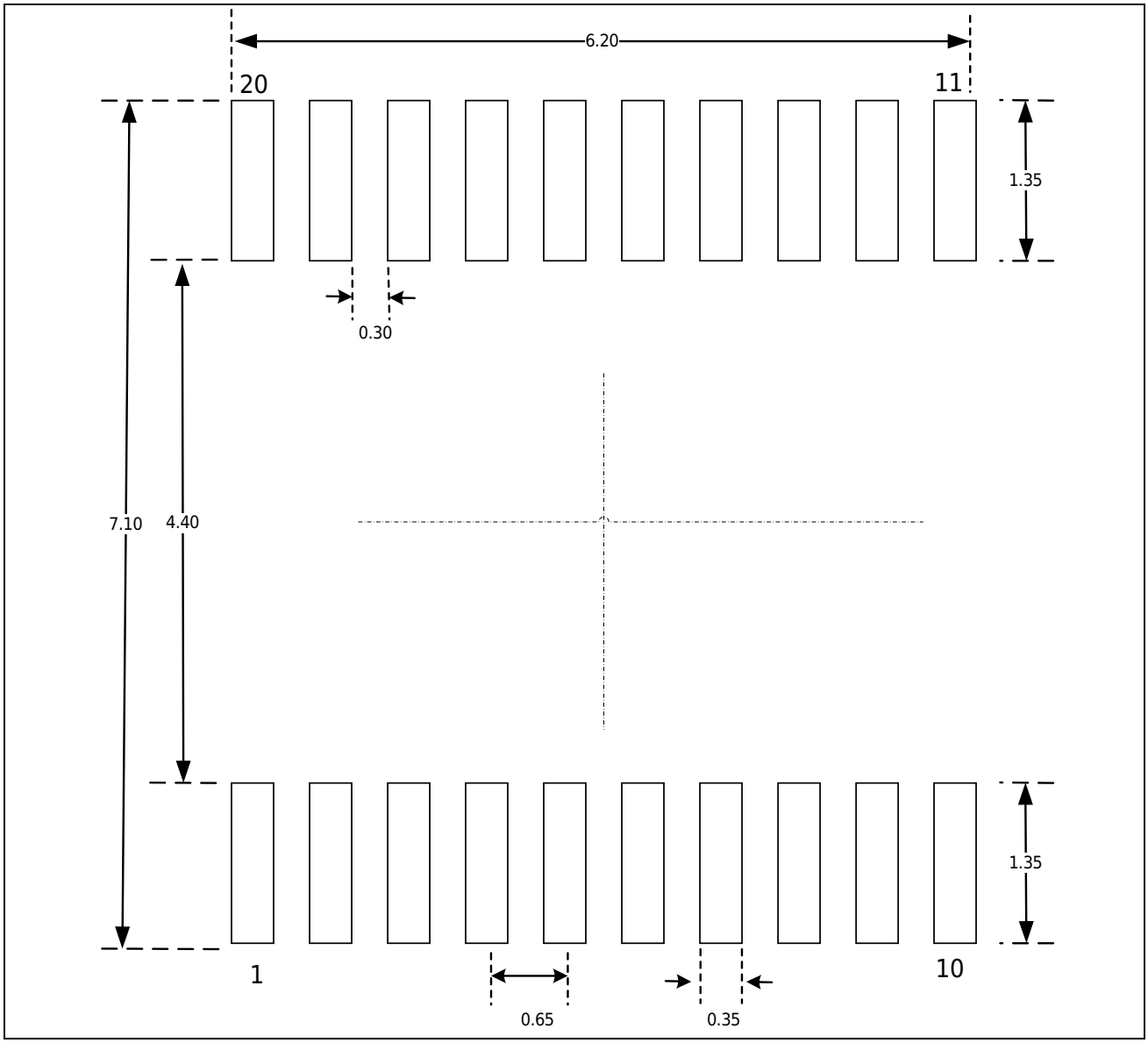
QFN20 packaging (3mm x 3mm)



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

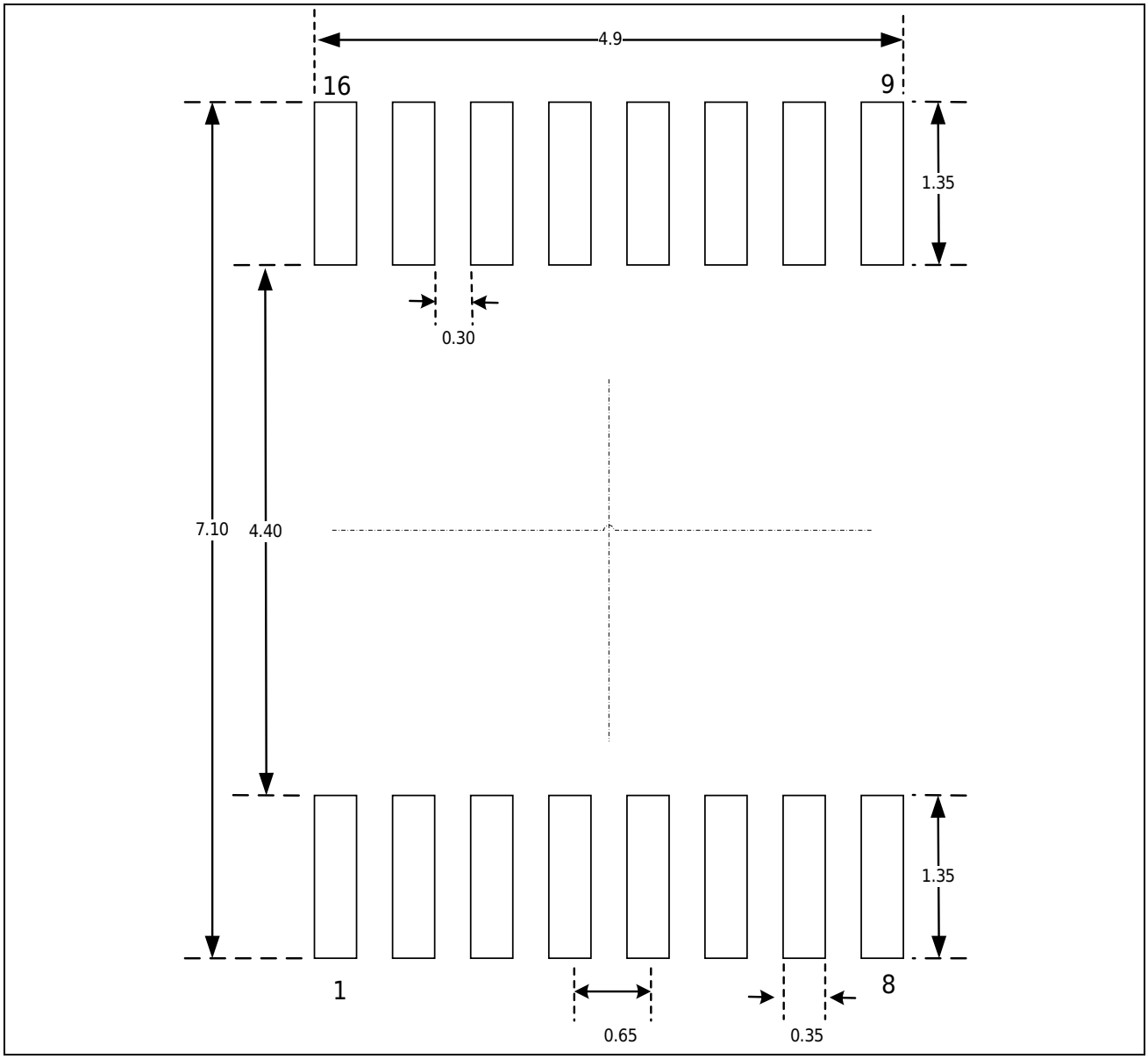
TSSOP20 packaging



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

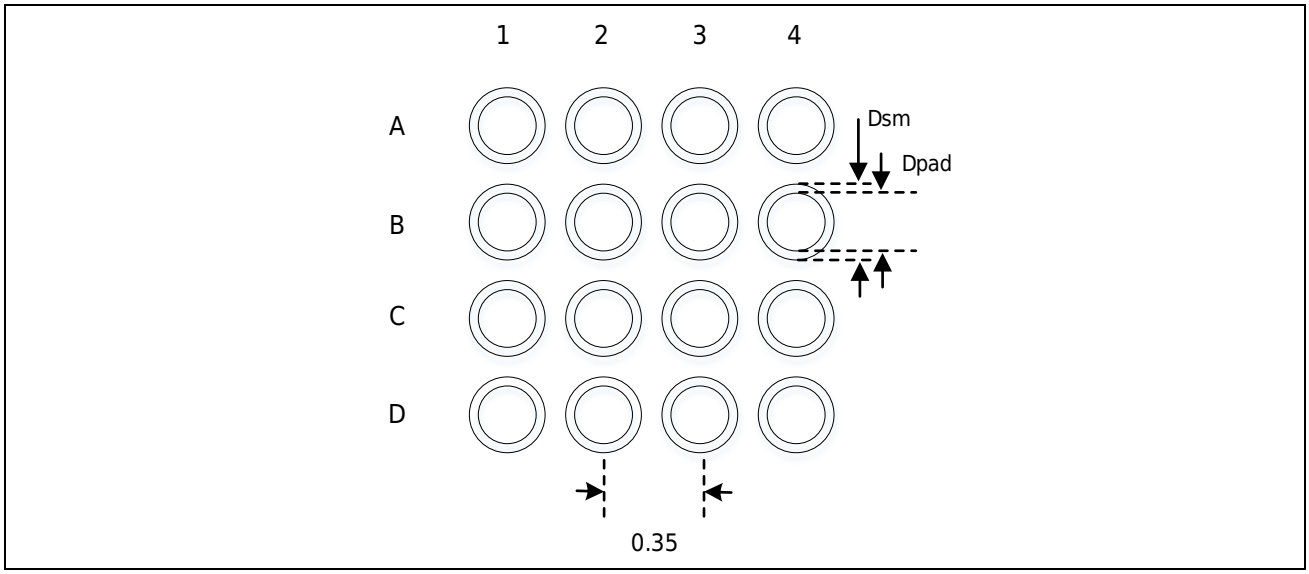
TSSOP16 packaging



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

CSP16 packaging



NOTE:

- **Dimensions are expressed in millimeters.**
- **Dimensions are for reference only.**

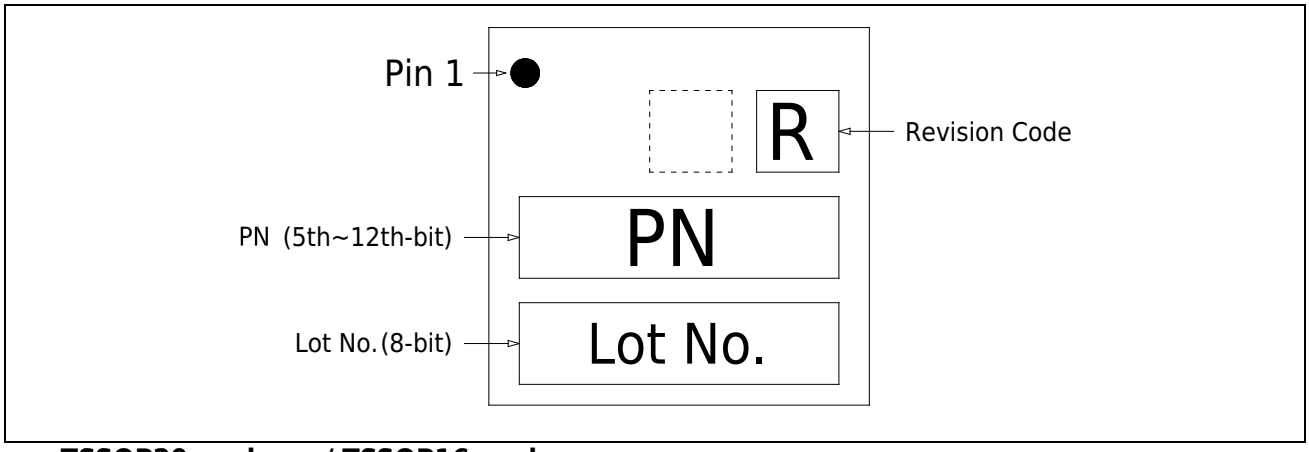
CSP16 recommended PCB design rules (0.35mm pitch)

Dimension	Recommended values
Pitch	0.35mm
Dpad	0.210mm
Dsm	0.275mm typ.（depends on the soldermask registration tolerance）
Stencil opening	0.235mm
Stencil thickness	0.100mm

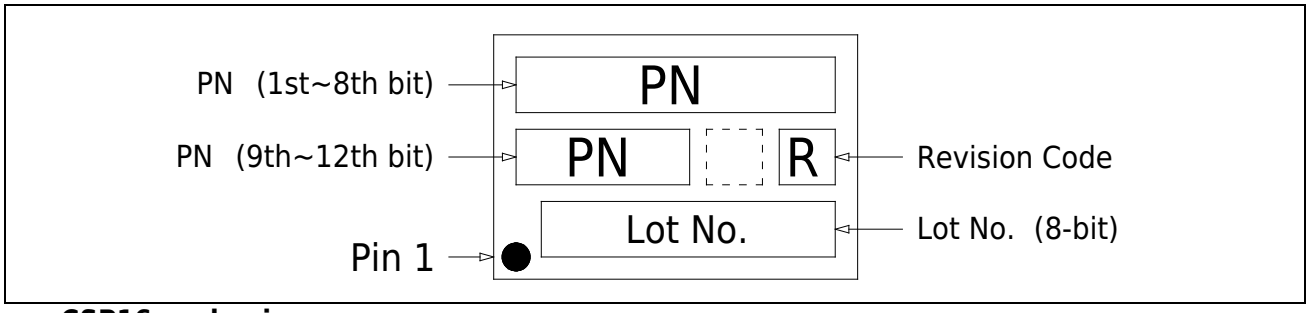
9.3 Silkscreen instructions

The position and information of Pin 1 printed on the front of each package are given below.

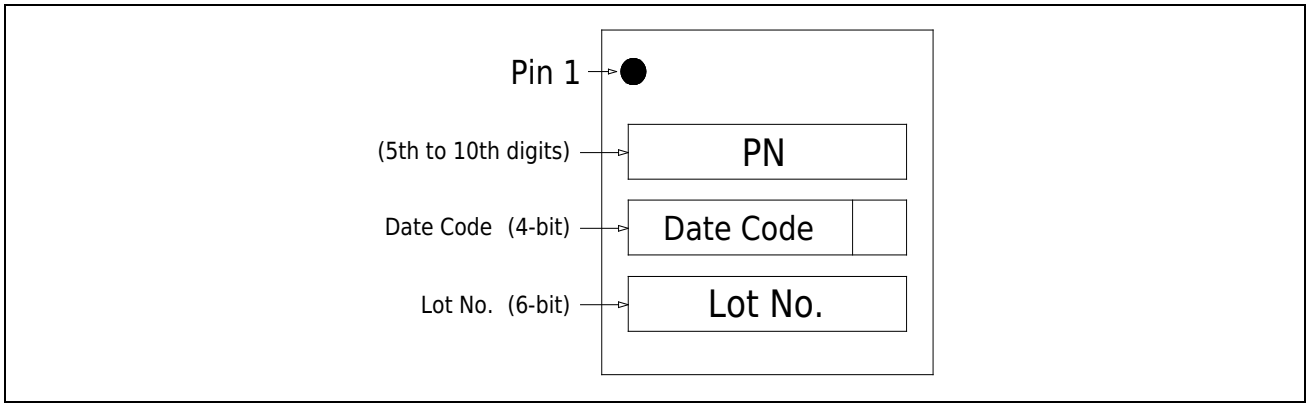
QFN20 packaging (3mm x 3mm)



TSSOP20 package / TSSOP16 package



CSP16 packaging



Note:

– The blank boxes in the above figure indicate optional marks related to production, which are not explained in this section.

9.4 Packaging Thermal Resistance Coefficient

When the packaged chip is working at the specified working environment temperature, the junction temperature T_j (℃) of the chip surface can be calculated according to the following formula:

$$T_j = T_{amb} + (P_D \times \theta_{JA})$$

- T_{amb} refers to the working environment temperature when the packaged chip is working, the unit is ℃;
- θ_{JA} refers to the thermal resistance coefficient of the package to the working environment, the unit is ℃/W;
- P_D is equal to the sum of internal power consumption of the chip and I/O power consumption, and the unit is W. The internal power consumption of the chip is the product's $I_{DD} \times V_{DD}$. I/O power consumption refers to the power consumption generated by the I/O pins when the chip is working. Usually this part of the value is very small and can be ignored.

When the chip is working at the specified working environment temperature, the junction temperature T_j of the chip surface cannot exceed the maximum allowable junction temperature T_J of the chip.

Table 9-1 Thermal resistance coefficient table for each package

Package Type and Size	Thermal Resistance Junction-ambient Value (θ_{JA})	Unit
QFN20 3mm x 3mm / 0.4mm pitch	70 +/- 10%	℃/W
TSSOP16	105 +/- 10%	℃/W
TSSOP20	91 +/- 10%	℃/W

10 Ordering Information

Part Number	HC32L110C6UA-SFN20TR	HC32L110C6PA-TSSOP20	HC32L110C6PA-TSSOP20TR	HC32L110B6PA-TSSOP16	HC32L110B6YA-CSP16TR	HC32L110C4UA-SFN20TR	HC32L110C4PA-TSSOP20	HC32L110C4PA-TSSOP20TR	HC32L110B4PA-TSSOP16	HC32L110B4PA-TSSOP16TR
Flash	32KB	32KB	32KB	32KB	32KB	16KB	16KB	16KB	16KB	16KB
RAM	4KB	4KB	4KB	4KB	4KB	2KB	2KB	2KB	2KB	2KB
GPIO	16+1	16+1	16+1	12+1	12+1	16+1	16+1	16+1	12+1	12+1
Vdd	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V	1.8~5.5V
Timer	6	6	6	6	6	6	6	6	6	6
LPTimer	1	1	1	1	1	1	1	1	1	1
RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
UART	2	2	2	2	2	2	2	2	2	2
LPUART	1	1	1	1	1	1	1	1	1	1
I2C	1	1	1	1	1	1	1	1	1	1
SPI	1	1	1	1	1	1	1	1	1	1
ADC(12bit)	9ch	9ch	9ch	6ch	6ch	9ch	9ch	9ch	6ch	6ch
Vcomp	2	2	2	2	2	2	2	2	2	2
LVD	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LVR	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Package	QFN20(3*3)	TSSOP20	TSSOP20	TSSOP16	CSP16	QFN20(3*3)	TSSOP20	TSSOP20	TSSOP16	TSSOP16
Foot Spacing	0.4mm	0.65mm	0.65mm	0.65mm	0.35mm	0.4mm	0.65mm	0.65mm	0.65mm	0.65mm
Chip thickness	0.75mm	1.2mm	1.2mm	1.2mm	0.535mm	0.75mm	1.2mm	1.2mm	1.2mm	1.2mm
Shipping Form	Tape	Tube	Tape	Tube	Tape	Tape	Tube	Tape	Tube	Tape

Before ordering, please contact the sales window for the latest mass production information.

Version revision history

version number	Revision Date	modify the content
Rev1.00	2018/01/23	The first edition of the HC32L110 series data sheet is released.
Rev1.10	2018/04/04	New version update.
Rev1.20	2018/04/17	Corrected Flash parameters.
Rev1.30	2018/05/03	Updated VC electrical parameters.
Rev1.40	2018/09/25	Adjusted the layout, updated Chapter 7 Electrical Characteristics, and added Chapter 9 ordering information.
Rev1.50	2018/11/15	Added "Silkscreen Instructions" in Chapter 8, and corrected the package dimensions of QFN20 / Tssop20 / Tssop16.
Rev1.60	2018/11/27	Modify the name: UART2→LPUART, add "note" in chapters 3 and 4.
Rev1.70	2019/02/22	Correct the following data: ①ADC Characteristic ②ESD Characteristic ③ECFLASH minimum value in Memory Characteristics ④QFN20/TSSOP16 package silkscreen description ⑤Add NOTE to Packaging Size ⑥Update Ordering Information ⑦Add AVCC/AVSS to Pin configuration.
Rev1.80	2019/06/21	Correct the following data: ①The UID address is corrected to 0x0010_0E74-0x0010_0E7F ②The programming mode is corrected ③The QFN pin configuration diagram style is updated ④The shipping form is added to the Ordering Information.
Rev1.90	2019/12/06	Correct the following data: ①Typical application circuit diagram ②ADC Characteristic unit ③XTH and XTL diagrams and precautions in the External timer characteristic.
Rev2.00	2020/01/17	Amend the following data: ① Add CSP16 package ②Silkscreen instructions.
Rev2.10	2020/03/06	Added notes to "Programming Mode" in the Introduction.
Rev2.20	2020/04/30	Correct the following data: ① Add VCC/3 accuracy in ADC Characteristic; ② Correct typos in 7.3.7; ③ RCL oscillator accuracy in 0.
Rev2.30	2020/07/31	Amend the following data: ① Add sections 0, 7.3.17, 9.2, 9.4; ②7.3.10 level; ③7.3.1 Internal AHB/APB clock frequency; ④0 Input characteristics - ports P0, P1, P2, P3, Values of V_{IH} and V_{IL} in RESET.
Rev2.40	2020/09/30	Correct the following data: ① Clock system description in the Introduction; ② RCH oscillator accuracy in 0; ③ V_{IL} and V_{IH} in 7.3.13; ④ Add SPI features.
Rev2.50	2021/05/31	Modify the following data: ① modify the statement; ② $t_{HD.STA}$ and $t_{SU.STO}$ parameters in the I2C features; ③ serial peripheral interface SPI in the Introduction; ④ data retention period in the Memory Characteristics; ⑤ increase the g_m parameter in the External timer characteristic.
Rev2.60	2022/03/09	Company logo update.
Rev2.61	2022/08/13	Modify the following data: ①Working conditions at power-on and power-off, modify the minimum value, maximum value and unit of VCC rise / fall rate to be consistent with other products; ②Embedded reset and LVD module characteristics, as shown in Figure 7-1 The signal name is inconsistent with the signal name in the reference manual and it is revised to be unified; ③ Built-in reference voltage according to the assessment results, the accuracy range under full temperature and voltage is relaxed to ±2.5%; ④ RESETB pin characteristics, input filter pulse time modification.
Rev2.62	2022/10/25	Update the "3. Pin Configuration" chapter drawing display is not clear.
Rev2.70	2024/05/15	Modify the following data: ①The number of ADC and VC channels in the introduction of Chapter 1 is modified, and the related description of 1.2V is deleted; ② Change the storage temperature range listed in Table 7-3 Temperature characteristics; ③ 7.3.8 Add "Internal Low Speed clock 10k

version number	Revision Date	modify the content
		oscillator" to internal clock source characteristics; ④ Delete 1.2V related descriptions in 7.3.15; ⑤ In Section 10 Ordering Information, two new models "HC32L110C6PA-TSSOP20TR" and "HC32L110C4PA-TSSOP20TR" are added.
Rev2.71	2024/12/12	Update the section on "High speed external clock XTH" and "Low speed external clock XTL" in 7.3.7 External clock source characteristics.
Rev2.72	2025/03/28	Modify the following data: ①Update the relevant parameters of the SPI interface characteristics in Table 7-16; ②Modify the maximum value of the input filter pulse and the minimum value of the input non-filtered pulse in Section 7.3.13 RESETB pin characteristics.