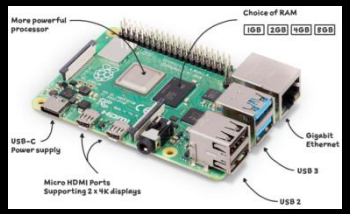
7th China Open Source Annual Conference

(COSCon’22, online)

Hosting FOSS EDA tools for RISC-V cross-platform development on RPi4



Feng Li (李枫)

hkli2013@126.com

Oct 29, 2022

Agenda

I. Background
- Tech Stack
- Testbed

II. RISC-V Toolchain
- GCC
- LLVM

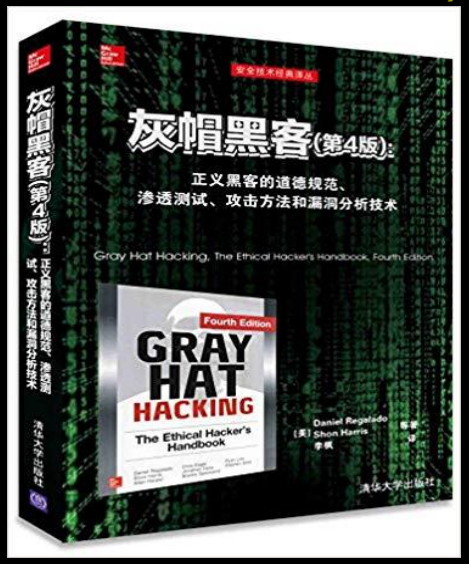
III. FOSS EDA Tools
- Chisel
- SpinalHDL
- Cocotb
- LiteX

IV. HW & SW Infra
- ARM cluster
- Serverless architecture
- Smart runtime
- Python-centric one-stop toolchain

V. Wrap-up

Who Am I

- An indie developer from China
- The main translator of the book «Gray Hat Hacking The Ethical Hacker's Handbook, Fourth Edition» (ISBN：9787302428671) & «Linux Hardening in Hostile Networks, First Edition» (ISBN: 9787115544384)



- Pure SW dev for ~15 years(~11 years on Mobile dev)
- An enthusiast for the Open Source Community
- https://github.com/XianBeiTuoBaFeng2015/MySlides/tree/master/Conf
  https://github.com/XianBeiTuoBaFeng2015/MySlides/tree/master/LTS
- Recently, focus on infrastructure of Cloud/Edge Computing, AI, Virtualization, Program Runtimes, Network, 5G, RISC-V, EDA…

I. Background

1) Tech Stack

1.1 FOSS EDA

- https://en.wikipedia.org/wiki/Comparison_of_EDA_software
- https://semiwiki.com/wikis/industry-wikis/eda-open-source-tools-wiki/
- https://ieeexplore.ieee.org/document/9398963
- https://ieeexplore.ieee.org/document/9398960
- https://ieeexplore.ieee.org/document/9336682
- https://ieeexplore.ieee.org/document/9105619
- …

1.2 RISC-V

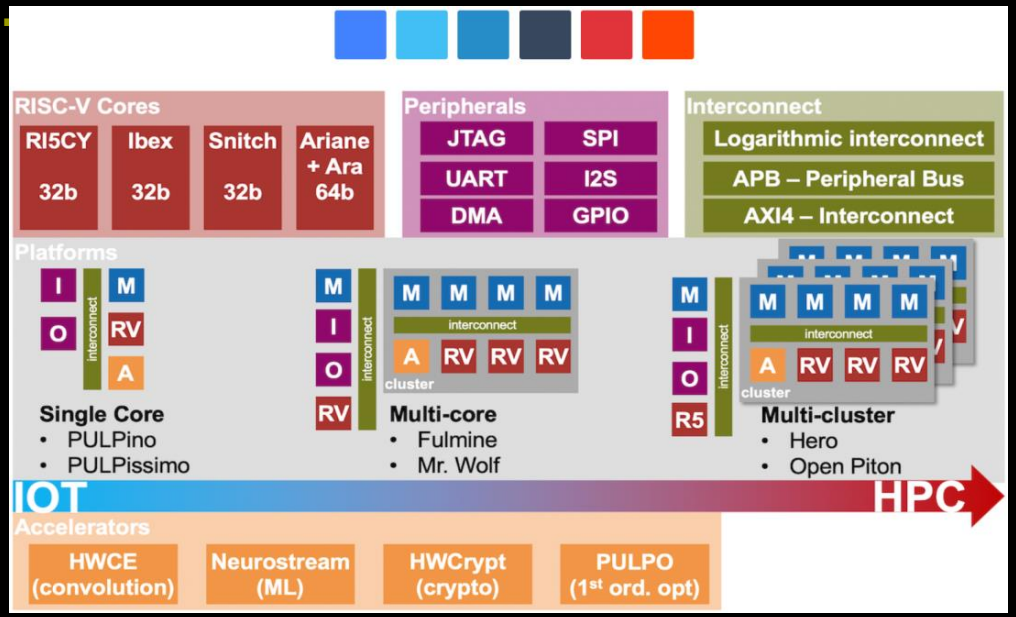
- https://en.wikipedia.org/wiki/RISC-V
- https://riscv.org/

Development

- https://riscv.org/exchange/
- https://github.com/riscv/riscv-isa-manual

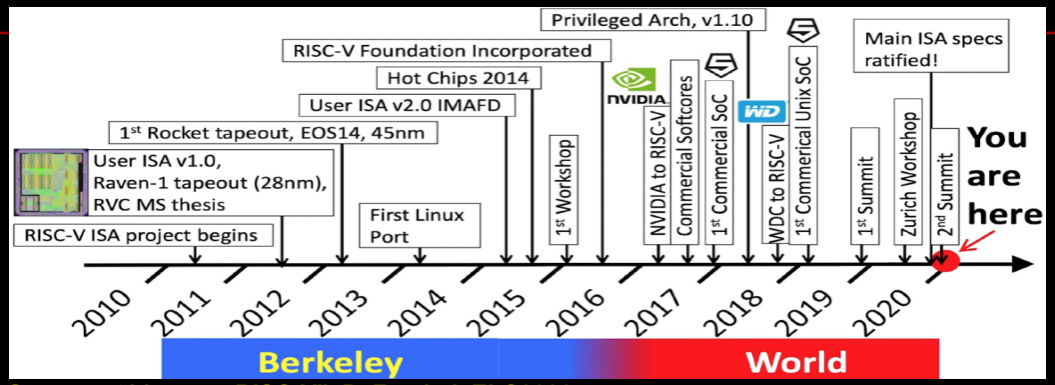
Cores & SoC

- https://github.com/riscv/riscv-cores-list
- https://riscv.org/exchange/cores-socs/
-



Source: https://fuentitech.com/what-is-the-risc-v-ecosystem/19227/

Ecosystem

- https://riscv.org/exchange/
- https://community.riscv.org/events/details/risc-v-foundation-bay-area-risc-v-group-presents-2021-risc-v-ecosystem-updates/
- 

Source: "Linux on RISC-V", D. Fustimi, ELC2020.

- **Incredible industry progress**

- The European Processor Initiative finalized the first version of its **RISC-V accelerator architecture** and will deliver test chip in 2021.
- The RIOS Lab announced PicoRio, an affordable **RISC-V open source small-board computer** available in 2021.
- Imperas announced first **RISC-V verification reference model with UVM encapsulation**.
- Seagate announced **hard disk drive controller** with high-performance RISC-V CPU.
- GreenWaves **ultra-low power GAP9 hearables platform** enabling scene-aware and neural network-based noise reduction.
- Alibaba unveiled RV64GCV core in its Xuantie 910 processor for **cloud and edge servers**.
- Microchip released the first **SoC FPGA development kit** based on the RISC-V ISA.
- Andes released **superscalar multicore and L2 cache controller** processors.
- StarFive released the world's first **RISC-V AI visual processing platform**
- SiFive unveiled world's fastest development board for **RISC-V Personal Computers**.
- Micro Magic announced an incredibly **fast 64-bit RISC-V core** achieving 5GHz and 13,000 CoreMarks at 1.1V.

Source: "RISC-V: The Open Era of Computing", Calista Redmond, The Linux Foundation Spring Member Meeting 2021.

A New Golden Age for Computer Architecture

- https://cacm.acm.org/magazines/2019/2/234352-a-new-golden-age-for-computer-architecture/fulltext

“the Linux of the chip world”

- https://www.zdnet.com/article/risc-v-the-linux-of-the-chip-world-is-starting-to-produce-technological-breakthroughs/

1.3 Evolution of HDLs

- https://en.wikipedia.org/wiki/Hardware_description_language
- https://hdl.github.io/awesome/items/
- Verilog/VHDL → HLS → eDSL

SystemVerilog, SystemC...

High-level Synthesis

https://en.wikipedia.org/wiki/High-level_synthesis

embedded Domain Specific Language

Typical eDSLs

- Haskell as host
  Bluespec, Clash...
- Scala as host
  Chisel, SpinalHDL...
- Python as host
  Amaranth/FHDL, PyGears...
- Finally convert to Verilog/VHDL
  https://en.wikipedia.org/wiki/Source-to-source_compiler

1.3.1 Chisel

- https://www.chisel-lang.org/
- https://github.com/chipsalliance/chisel3

Chisel 3: A Modern Hardware Design Language.

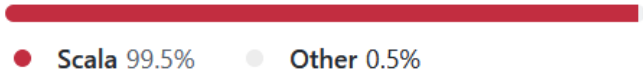
The **Constructing Hardware in a Scala Embedded Language** (**Chisel**) is an open-source hardware description language (HDL) used to describe digital electronics and circuits at the register-transfer level that facilitates **advanced circuit generation and design reuse for both ASIC and FPGA digital logic designs**.

Chisel adds hardware construction primitives to the Scala programming language, providing designers with the power of a modern programming language to write complex, parameterizable circuit generators that produce synthesizable Verilog. This generator methodology enables the creation of re-usable components and libraries, such as the FIFO queue and arbiters in the Chisel Standard Library, raising the level of abstraction in design while retaining fine-grained control.

For more information on the benefits of Chisel see: "What benefits does Chisel offer over classic Hardware Description Languages?"

Chisel is powered by FIRRTL (Flexible Intermediate Representation for RTL), a hardware compiler framework that performs optimizations of Chisel-generated circuits and supports custom user-defined circuit transformations.

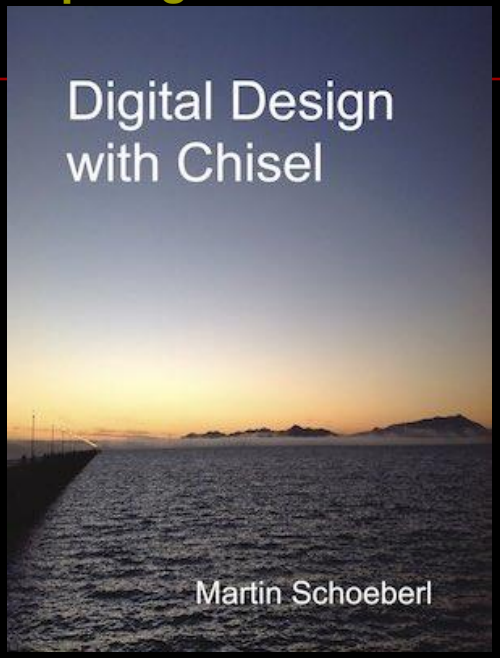
Languages



- https://github.com/topics/chisel
- …

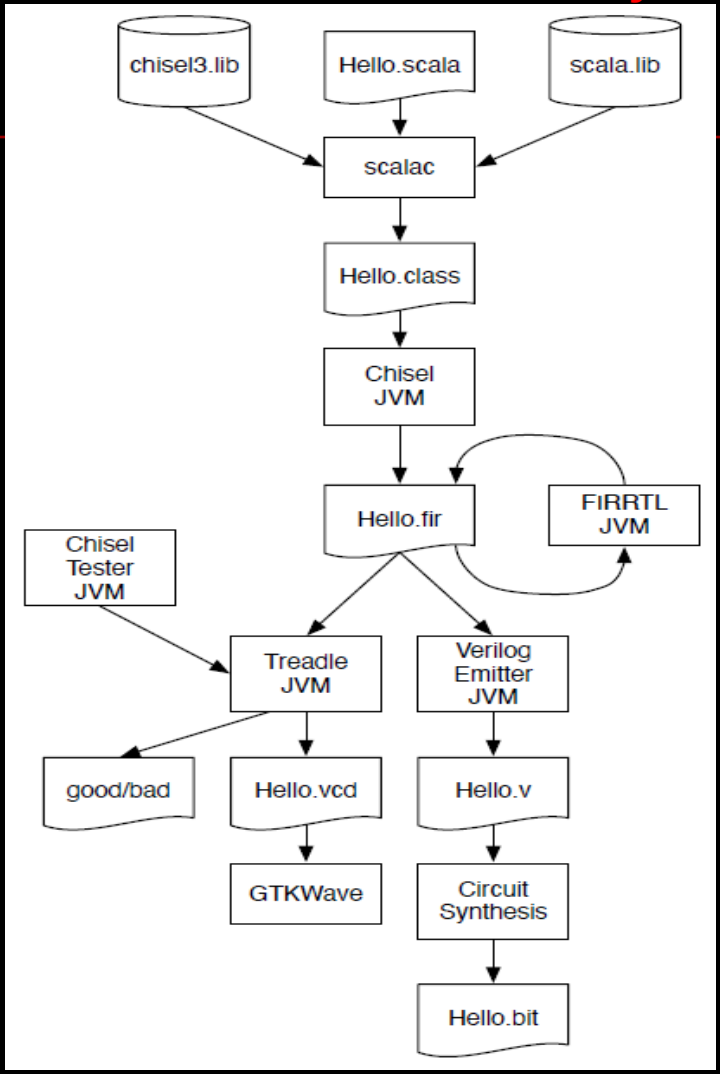
Chisel Books

- http://www.imm.dtu.dk/~masca/chisel-book.html
- https://github.com/schoeberl/chisel-book



Architecture & design

- **Tool flow of the Chisel ecosystem**



Source: http://www.imm.dtu.dk/~masca/chisel-book.pdf

1.3.1.1 Firrtl

Overview

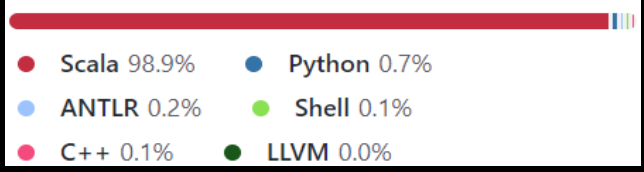
- https://github.com/chipsalliance/firrtl

  Flexible Internal Representation for RTL.

Firrtl is an intermediate representation (IR) for digital circuits designed as a platform for writing circuit-level transformations. This repository consists of a collection of transformations (written in Scala) which simplify, verify, transform, or emit their input circuit.

A Firrtl compiler is constructed by chaining together these transformations, then writing the final circuit to a file.

Languages



- https://github.com/chipsalliance/firrtl/wiki
- https://www.chisel-lang.org/firrtl/
- https://github.com/chipsalliance/firrtl-spec

1.3.1.2 Treadle

Overview

- https://github.com/chipsalliance/treadle

  A Chisel/Firrtl Execution Engine.

Treadle is an experimental circuit simulator that executes low Firrtl IR. It is based on earlier work on the firrtl_interpreter It will be one of the standard back-ends available as part of the chisel-testers project, and thus one of the tools in the freechipsproject/chisel3 hardware synthesis toolbox. This project provides a test harness supporting a peek, poke expect model.

It also provides a interactive simulator shell or repl (see treadle.sh) that allows fine grained incremental execution of a circuit. In combination with a scala debugger such as Eclipse or IntelliJ it can be a very powerful way of analyzing problematic behavior.

Chisel3 is a high-level functional circuit generator. It produces **Flexible Intermediate Representation for RTL** or **FIRRTL**. The Firrtl project parses and transforms firrtl. It also provides mechanisms for emitting verilog, for processing by downstream toolchains. **Treadle** parses and execute the LoFirrtl subset of Firrtl. **Treadle** has a short spin up time and is close to the performance of verilator simulations. It can be useful for an initial debugging of Chisel circuits and is also used for other forms of circuit analysis.

Languages

Scala 99.6% Other 0.4%

- ...

1.3.1.3 Rocket Chip Generator

Overview

- https://github.com/chipsalliance/rocket-chip

Languages

- Scala 95.3%
- C++ 1.2%
- Python 1.2%
- Verilog 0.8%
- Makefile 0.8%
- Shell 0.4%
- Assembly 0.3%

```
[submodule "hardfloat"]
        path = hardfloat
        url = https://github.com/ucb-bar/berkeley-hardfloat.git
[submodule "torture"]
        path = torture
        url = https://github.com/ucb-bar/riscv-torture.git
[submodule "api-config-chipsalliance"]
        path = api-config-chipsalliance
        url = https://github.com/chipsalliance/api-config-chipsalliance.git
```

- https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-17.html

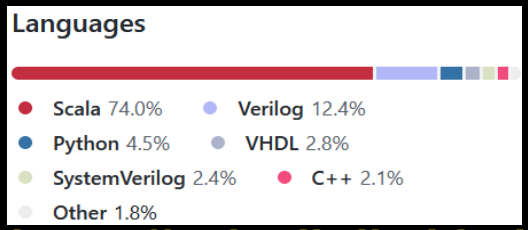
Rocket Chip is an open-source Sysem-on-Chip design generator that emits synthesizable RTL. It leverages the Chisel hardware construction language to compose a library of sophisticated generators for cores, caches, and interconnects into an integrated SoC. Rocket Chip generates general-purpose processor cores that use the open RISC-V ISA, and provides both an in-order core generator (Rocket) and an out-of-order core generator (BOOM). For SoC designers interested in utilizing heterogeneous specialization for added efficiency gains, Rocket Chip supports the integration of custom accelerators in the form of instruction set extensions, coprocessors, or fully independent novel cores. Rocket Chip has been taped out (manufactured) eleven times, and yielded functional silicon prototypes capable of booting Linux.

- …

1.3.2 SpinalHDL

- https://github.com/SpinalHDL/SpinalHDL

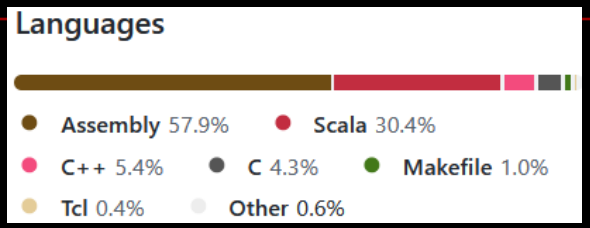
  - A language to describe digital hardware
  - Compatible with EDA tools, as it generates VHDL/Verilog files
  - Much more powerful than VHDL, Verilog, and SystemVerilog in its syntax and features
  - Much less verbose than VHDL, Verilog, and SystemVerilog
  - Not an HLS, nor based on the event-driven paradigm
  - Only generates what you asked it in a one-to-one way (no black-magic, no black box)
  - Not introducing area/performance overheads in your design (versus a hand-written VHDL/Verilog design)
  - Based on the RTL description paradigm, but can go much further
  - Allowing you to use Object-Oriented Programming and Functional Programming to elaborate your hardware and verify it
  - Free and can be used in the industry without any license



- https://spinalhdl.github.io/SpinalDoc-RTD/
- …

1.3.2.1 VexRiscv

- https://github.com/SpinalHDL/VexRiscv
  A FPGA friendly 32 bit RISC-V CPU implementation which is written in SpinalHDL.




```
[submodule "src/test/resources/VexRiscvRegressionData"]
        path = src/test/resources/VexRiscvRegressionData
        url = https://github.com/SpinalHDL/VexRiscvRegressionData.git
```

- The hardware description of this CPU is done by using a very software oriented approach (without any overhead in the generated hardware). Here is a list of software concepts used:
  - There are very few fixed things. Nearly everything is plugin based. The PC manager is a plugin, the register file is a plugin, the hazard controller is a plugin, ...
  - There is an automatic a tool which allows plugins to insert data in the pipeline at a given stage, and allows other plugins to read it in another stage through automatic pipelining.
  - There is a service system which provides a very dynamic framework. For instance, a plugin could provide an exception service which can then be used by other plugins to emit exceptions from the pipeline.

- https://riscv.org/announcements/2018/10/risc-v-contest/

Some specs:

- RV32I[M][A][F[D]][C] instruction set
- Pipelined from 2 to 5+ stages ([Fetch*X], Decode, Execute, [Memory], [WriteBack])
- 1.44 DMIPS/Mhz --no-inline when nearly all features are enabled (1.57 DMIPS/Mhz when the divider lookup table is enabled)
- Optimized for FPGA, does not use any vendor specific IP block / primitive
- AXI4, Avalon, wishbone ready
- Optional MUL/DIV extensions
- Optional F32/F64 FPU (require data cache for now)
- Optional instruction and data caches
- Optional hardware refilled MMU
- Optional debug extension allowing Eclipse debugging via a GDB >> openOCD >> JTAG connection
- Optional interrupts and exception handling with Machine, [Supervisor] and [User] modes as defined in the RISC-V Privileged ISA Specification v1.10.
- Two implementations of shift instructions: single cycle (full barrel shifter) and shiftNumber cycles
- Each stage can have optional bypass or interlock hazard logic
- Linux compatible (SoC : https://github.com/enjoy-digital/linux-on-litex-vexriscv)
- Zephyr compatible
- FreeRTOS port

1.3.2.2 NaxRiscv

- https://github.com/SpinalHDL/NaxRiscv

An RISC-V core currently characterised by :

- Out of order execution with register renaming
- Superscalar (ex : 2 decode, 3 execution units, 2 retire)
- (RV32/RV64)IMAFDCSU (Linux / Buildroot works on hardware)
- High perf config : 2.94 DMIPS/Mhz, 5.00 Coremark/Mhz, 1.68 Embench-iot baseline (Cortex M4) @ 150 Mhz + 14.2 KLUT on Artix 7-3
- Portable HDL, but target FPGA with distributed ram (Xilinx series 7 is the reference used so far)
- Target a (relatively) low area usage and high fmax (not the best IPC)
- Decentralized hardware elaboration (Empty toplevel parametrized with plugins)
- Frontend implemented around a pipelining framework to ease customisation
- Non-blocking Data cache with multiple refill and writeback slots
- BTB + GSHARE + RAS branch predictors
- Hardware refilled MMU (SV32, SV39)
- Load to use latency of 3 cycles via the speculative cache hit predictor
- Pipeline visualisation via verilator simulation and Konata (gem5 file format)
- JTAG / OpenOCD / GDB support by implementing the RISCV External Debug Support v. 0.13.2

Languages

Scala 85.5% C++ 10.7%
Python 2.7% Tcl 0.5%
Makefile 0.3% Verilog 0.2%
C 0.1%

- https://spinalhdl.github.io/NaxRiscv-Rtd/main/index.html

1.3.2.3 SaxonSoc

- https://github.com/SpinalHDL/SaxonSoc

SoC based on VexRiscv and ICE40 UP5K.

This repo experiment multiple things at once :

- The BMB (Banana Memory Bus) which can cover both cached and cacheless SoC without compromises
- A hardware description paradigm made of generators and depedancies which should be able to solve SoC toplevel hell
- Linux and U-Boot on VexRiscv

A few kits are supported :

- ulx3s (ECP5) , documented in bsp/radiona/ulx3s/smp/README.md
- Arty-A7 (Artix 7), documented in bsp/digilent/ArtyA7SmpLinux/README.md
- Efinix Xyloni
- ...

Languages

Scala 47.3% C 34.2%
Verilog 10.8% Makefile 2.8%
Tcl 1.9% Shell 1.6% Other 1.4%

Features

Feature which target the interconnect and adapters :

- Context signals which allow a master to retrieve information from the bus responses, and consequently allow state-less adapters
- State-less adapters allow unlimited number of pending transactions and avoid the usage of RAM/FIFO in adapters
- Address and write data are part of the same link, which allow to have low latency interconnect (in comparison to AXI)
- Allow out of oder completion via the 'source' signals

Feature to make slave implementation easier :

- Address alignment parameter (BYTE, WORD, POW2) to allow simple slave implementations
- Length width parameter, which combined with the alignement parameter, allow a slave to not support bursts (the interconnect will add the required adapters)

Other features :

- WriteOnly, readOnly support

1.3.3 LiteX

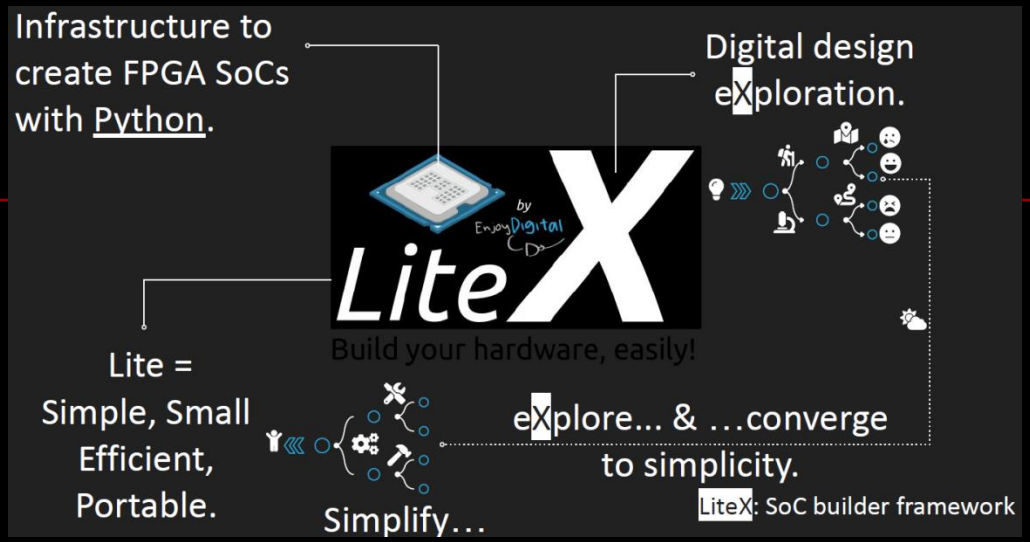
- http://www.enjoy-digital.fr/
  SoC builder framework…
- https://github.com/enjoy-digital/litex

LiteX provides all the common components required to easily create an FPGA Core/SoC:

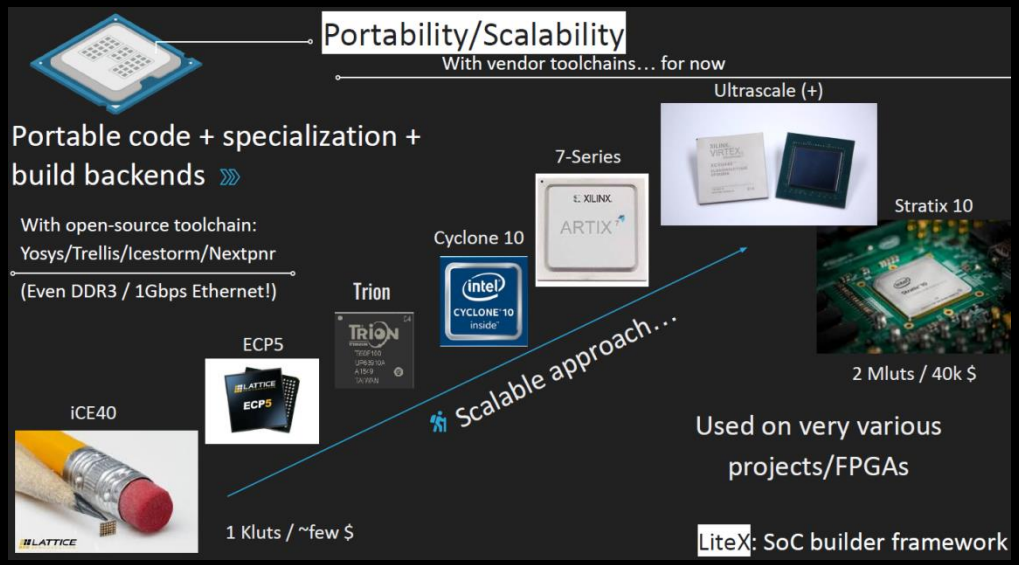
- ✔ Buses and Streams (Wishbone, AXI, Avalon-ST) and their interconnect.
- ✔ Simple cores: RAM, ROM, Timer, UART, JTAG, etc....
- ✔ Complex cores through the ecosystem of cores: LiteDRAM, LitePCIe, LiteEth, LiteSATA, etc...
- ✔ Various CPUs & ISAs: RISC-V, OpenRISC, LM32, Zynq, X86 (through a PCIe), etc...
- ✔ Mixed languages support with VHDL/Verilog/(n)Migen/Spinal-HDL/etc... integration capabilities.
- ✔ Powerful debug infrastructure through the various bridges and Litescope.
- ✔ Direct/Fast simulation through Verilator.
- ✔ Build backends for open-source and vendors toolchains.
- ✔ And a lot more... :)

- https://github.com/litex-hub
- https://github.com/timvideos/litex-buildenv
- https://github.com/m-labs/migen
- https://m-labs.hk/migen/manual/fhdl.html
- https://github.com/litex-hub/litex-boards

Design philosophy

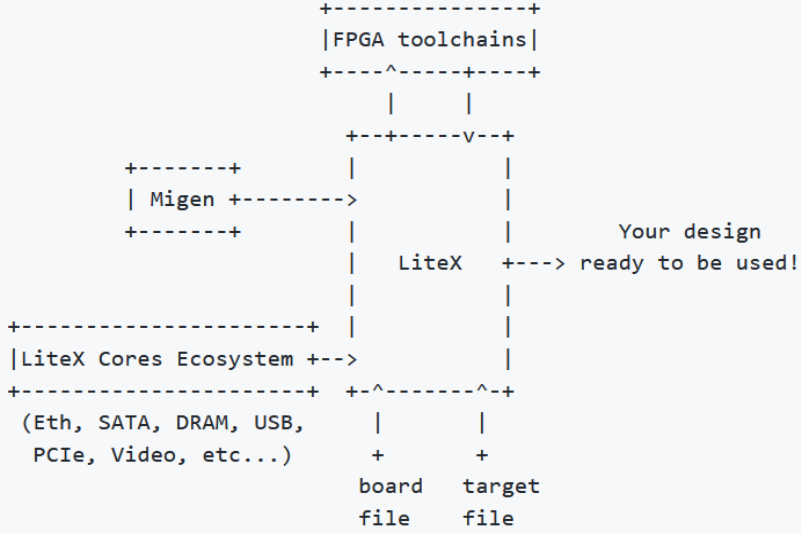
- 

Source: "LiteX: SoC builder framework", Florent Kermarrec

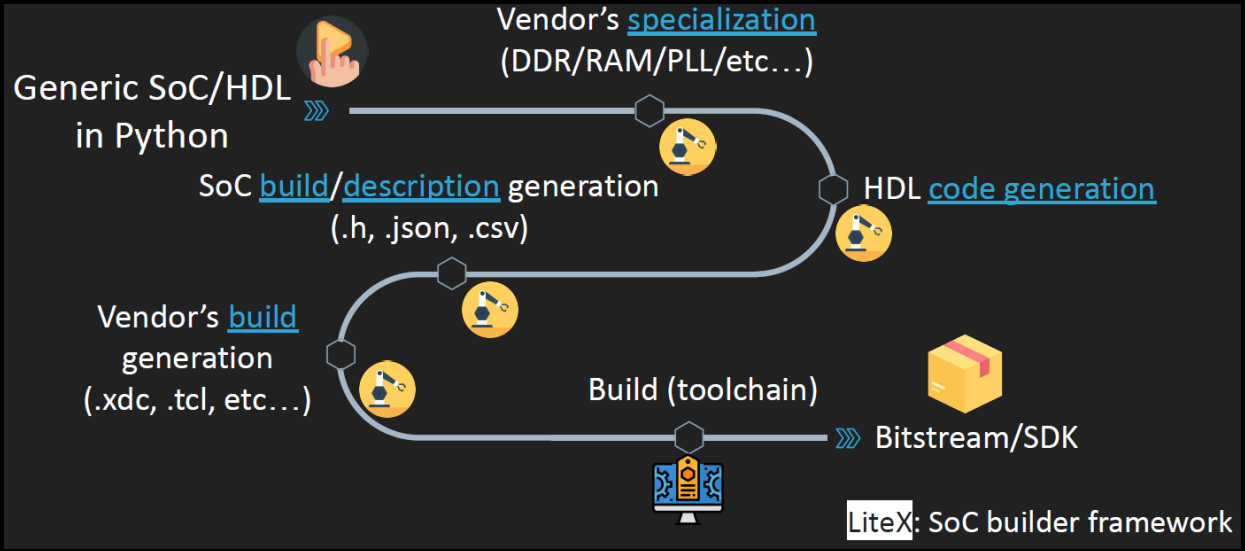
- 

Source: "LiteX: SoC builder framework", Florent Kermarrec

Design flow

- 

  Source: https://github.com/enjoy-digital/litex

- 

  Source: "LiteX: SoC builder framework", Florent Kermarrec

1.4 Hardware verification

- https://en.wikipedia.org/wiki/Hardware_verification_language
- …

1.4.1 UVM

- https://en.wikipedia.org/wiki/Universal_Verification_Methodology

The **Universal Verification Methodology** (UVM) is a standardized methodology for verifying integrated circuit designs. UVM is derived mainly from the OVM (Open Verification Methodology) which was, to a large part, based on the eRM (e Reuse Methodology) for the e Verification Language developed by Verisity Design in 2001. The UVM class library brings much automation to the SystemVerilog language such as sequences and data automation features (packing, copy, compare) etc., and unlike the previous methodologies developed independently by the simulator vendors, is an Accellera standard with support from multiple vendors: Aldec, Cadence, Mentor Graphics, Synopsys, Xilinx Simulator(XSIM).

History [edit]

In December 2009, a technical subcommittee of Accellera — a standards organization in the electronic design automation (EDA) industry — voted to establish the UVM and decided to base this new standard on the Open Verification Methodology (OVM-2.1.1),[1] a verification methodology developed jointly in 2007 by Cadence Design Systems and Mentor Graphics.

On February 21, 2011, Accellera approved the 1.0 version of UVM.[2] UVM 1.0 includes a Reference Guide, a Reference Implementation in the form of a SystemVerilog base class library, and a User Guide.[2]

Definitions [edit]

- Agent - A container that emulates and verifies DUT devices
- Blocking - An interface that blocks tasks from other interfaces until it completes
- DUT - Device under test, what you are actually testing
- DUV - Device Under Verification
- Component - A portion of verification intellectual property that has interfaces and functions.
- Transactor - see component
- Verification Environment Configuration - those settings in the DUT and environment that are alterable while the simulation is running
- VIP - verification intellectual property

…

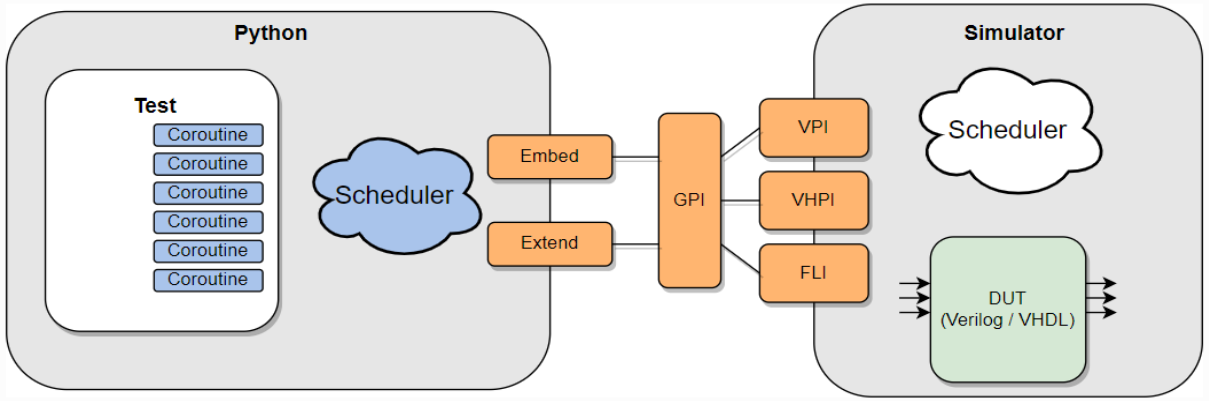
- https://www.accellera.org/community/uvm/
- The latest version of UVM is 1.2, and 2.0 is on the way.

  https://www.accellera.org/downloads/standards/uvm
- …

1.4.2 Cocotb

- https://www.cocotb.org/
  A Coroutine based Cosimulation TestBench environment for verifying VHDL and SystemVerilog RTL using Python.
- https://github.com/cocotb/cocotb
- How it works

A typical cocotb testbench requires no additional RTL code. The Design Under Test (DUT) is instantiated as the toplevel in the simulator without any wrapper code. cocotb drives stimulus onto the inputs to the DUT (or further down the hierarchy) and monitors the outputs directly from Python. Note that cocotb can not instantiate HDL blocks - your DUT must be complete.



A test is simply a Python function. At any given time either the simulator is advancing time or the Python code is executing. The `await` keyword is used to indicate when to pass control of execution back to the simulator. A test can spawn multiple coroutines, allowing for independent flows of execution.

Source: https://docs.cocotb.org/en/stable/

- https://www.reddit.com/r/FPGA/comments/v8fd63/cocotb_in_python_vs_uvm_in_systemverilog/
- ...

UVM-Python

- https://github.com/tpoikela/uvm-python
  UVM 1.2 port to Python
- Current Status:

Current status: Testbenches can already be written with all the typical UVM components. UVM Phasing is in place, and working. Stimulus can be generated using hierarchical sequences. Register layer supports already read/write to registers (via frontdoor), and to memories (frontdoor and backdoor). TLM 1.0 is implemented, put/get/analysis interfaces are done, and master/slave interfaces work. Initial implementation of TLM2.0 has also been added. The table below summarizes the status:

Feature	Status
TLM1.0	Done
TLM2.0	Started, 2/3 examples working
Components	Done
Phases	Done
Objections	Test and env-level objections work
Sequences	Partially done, hier sequences work
Registers	Reg/mem access working, built-in sequences partially done

Further Resources

- https://github.com/cocotb/cocotb/wiki/Further-Resources

...

A list of cocotb extensions module packaged as described in documentation.

Please add yours here! If you publish to PyPI, please add the `Framework :: cocotb` classifier.

- cocotbext-eth: Ethernet (GMII, RGMII, XGMII, PTP clock)
- cocotbext-pcie: PCI Express (PCIe), and hard IP core models for UltraScale and UltraScale+
- cocotbext-axi: AXI, AXI lite, and AXI stream
- cocotbext-i2c: I2C interface modules
- cocotbext-uart: UART interface modules
- cocotbext-wishbone: Drive and monitor Wishbone bus
- cocotbext-uart: UART testing
- cocotbext-spi: Drive SPI bus
- cocomod-fifointerface: FIFO testing
- cocotbext-interfaces: "generalization of digital interfaces and their associated behavioral models"; Avalon ST
- cocotbext-ral: A port of the uvm-python RAL to use BusDrivers

...

- https://github.com/cocotb/cocotb/blob/master/documentation/source/extensions.rst
- https://github.com/antmicro/cocotb-ahb
- ...

1.5 LLVM
1.5.1 MLIR

- https://mlir.llvm.org/

Multi-Level Intermediate Representation

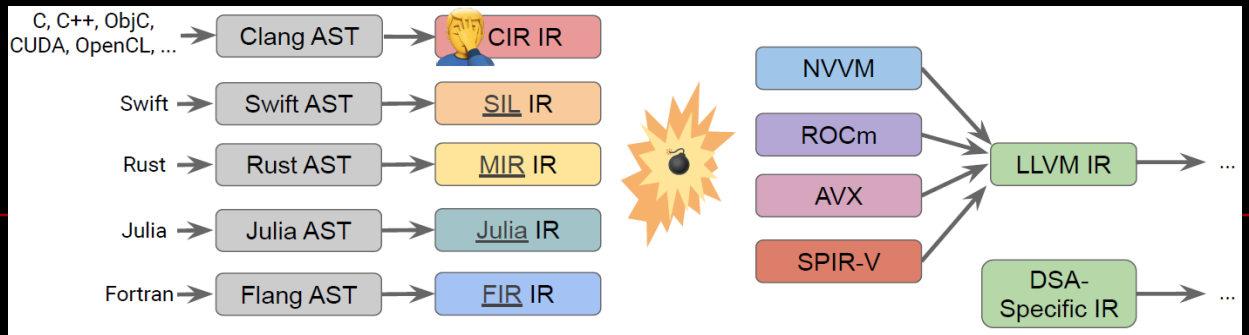
The MLIR project is a novel approach to building reusable and extensible compiler infrastructure. MLIR aims to address software fragmentation, improve compilation for heterogeneous hardware, significantly reduce the cost of building domain specific compilers, and aid in connecting existing compilers together.

- Motivation

MLIR is intended to be a hybrid IR which can support multiple different requirements in a unified infrastructure. For example, this includes:

- The ability to represent dataflow graphs (such as in TensorFlow), including dynamic shapes, the user-extensible op ecosystem, TensorFlow variables, etc.
- Optimizations and transformations typically done on such graphs (e.g. in Grappler).
- Ability to host high-performance-computing-style loop optimizations across kernels (fusion, loop interchange, tiling, etc.), and to transform memory layouts of data.
- Code generation “lowering” transformations such as DMA insertion, explicit cache management, memory tiling, and vectorization for 1D and 2D register architectures.
- Ability to represent target-specific operations, e.g. accelerator-specific high-level operations.
- Quantization and other graph transformations done on a Deep-Learning graph.
- Polyhedral primitives.
- Hardware Synthesis Tools / HLS.

From LLVM to MLIR

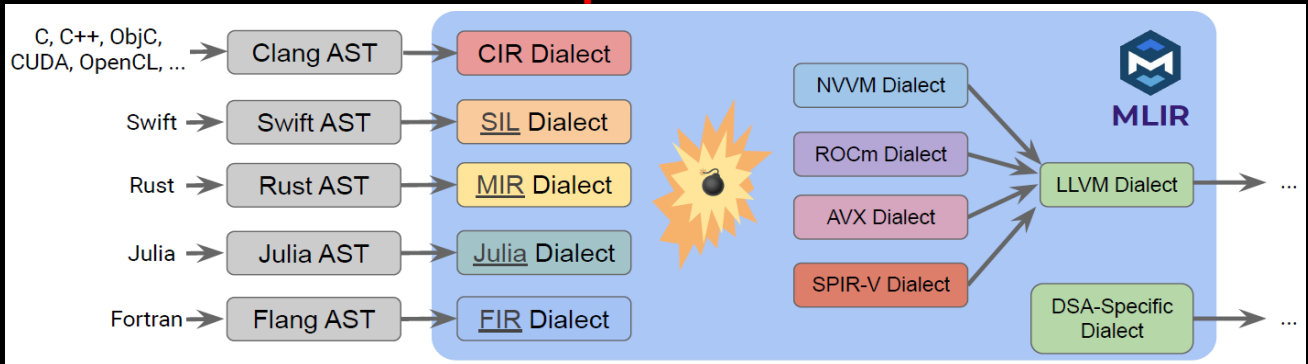


- Different back-ends demand customized IR for optimization
- DSAs even cannot use LLVM for generating back-end codes and demand their own IR for code generation

Severe Fragmentation: IRs have different implementations and "frameworks"

Source: https://hanchenye.com/assets/pdf/Gatech_CIRCT_Slides_Hanchen.pdf

MLIR: "Meta IR" and Compiler Infrastructure



MLIR is a **"Meta IR"** and **compiler infrastructure** for:

- Design and implement **dialect**
- Optimization and transform inside of a **dialect**
- Conversion between different **dialects**
- Code generation of **dialect**

Source: https://hanchenye.com/assets/pdf/Gatech_CIRCT_Slides_Hanchen.pdf

1.5.2 CIRCT

- https://circt.llvm.org/
  Circuit IR Compilers and Tools.
- Motivation

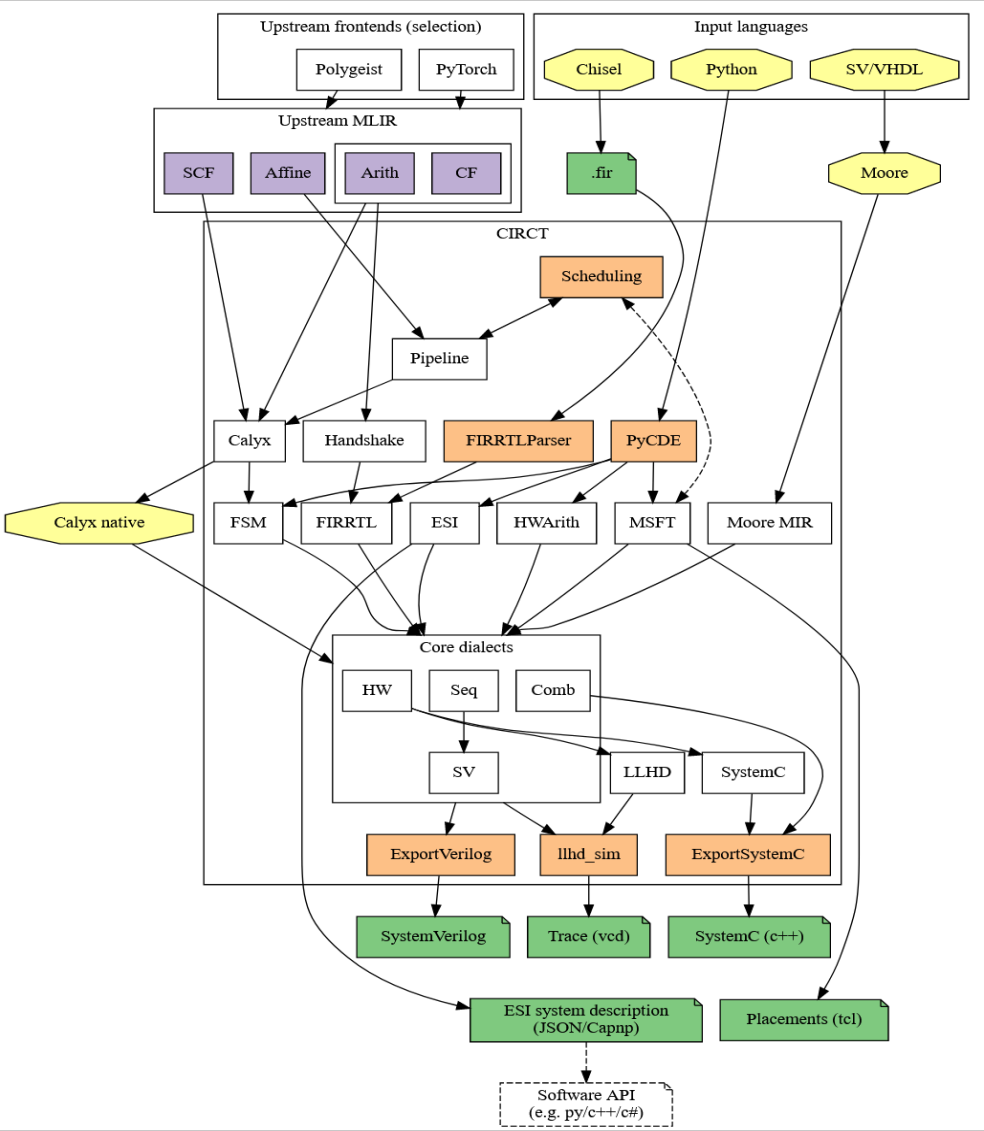
The EDA industry has well-known and widely used proprietary and open source tools. However, these tools are inconsistent, have usability concerns, and were not designed together into a common platform. Furthermore these tools are generally built with Verilog (also VHDL) as the IRs that they interchange. Verilog has well known design issues, and limitations, e.g. suffering from poor location tracking support.

The CIRCT project is an (experimental!) effort looking to apply MLIR and the LLVM development methodology to the domain of hardware design tools. Many of us dream of having reusable infrastructure that is modular, uses library-based design techniques, is more consistent, and builds on the best practices in compiler infrastructure and compiler design techniques.

By working together, we hope that we can build a new center of gravity to draw contributions from the small (but enthusiastic!) community of people who work on open hardware tooling. In turn we hope this will propel open tools forward, enables new higher-level abstractions for hardware design, and perhaps some pieces may even be adopted by proprietary tools in time.

- https://circt.llvm.org/docs/Charter/
- https://mlir.llvm.org/
- https://circt.org/perf/
- …

dialects and how they interact

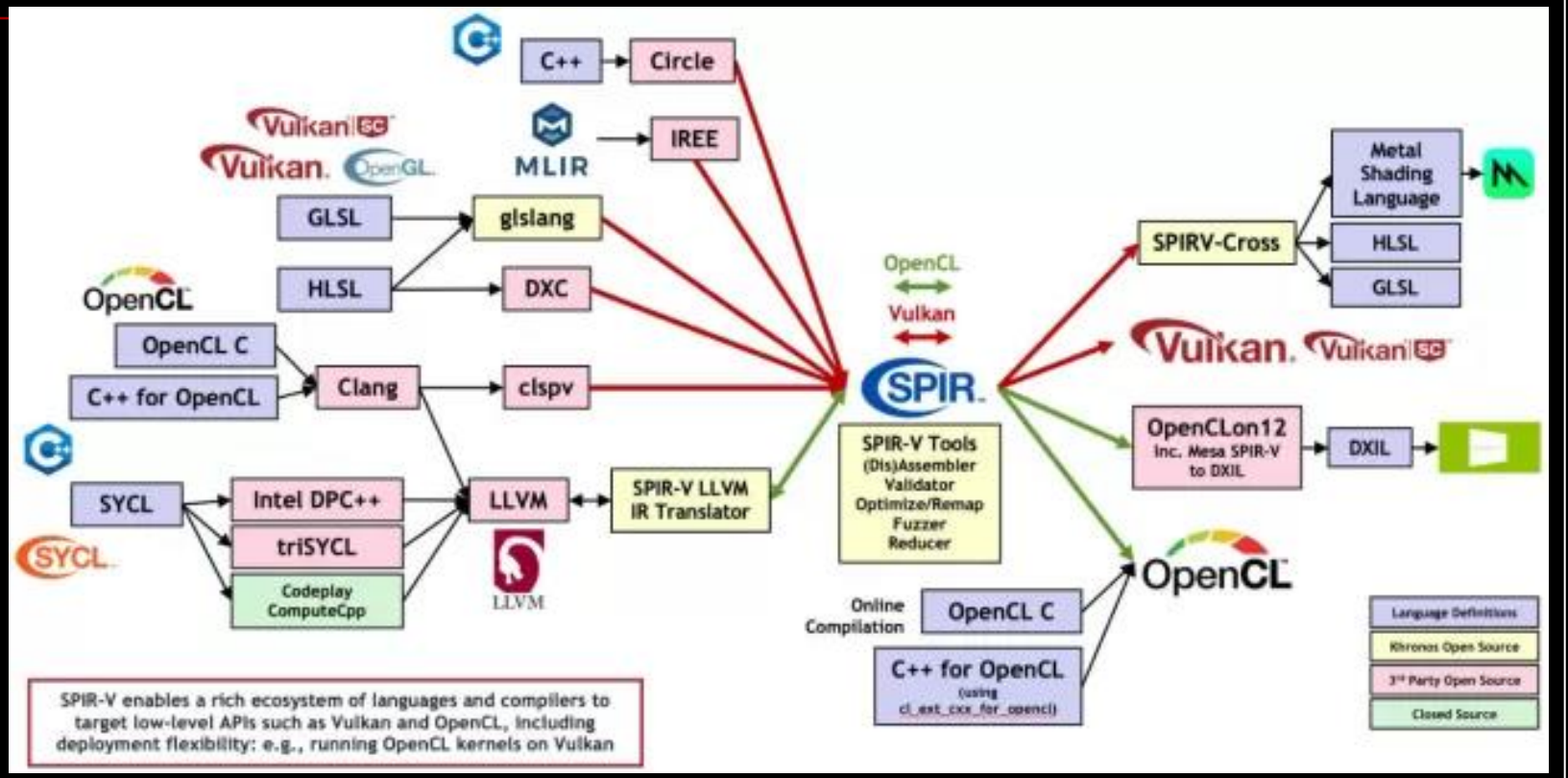


Source: https://circt.llvm.org/includes/img/dialects.svg

1.5.3 Initial SPIR-V Backend Code Lands In LLVM 15

- https://www.phoronix.com/news/LLVM-15-SPIR-V-Backend

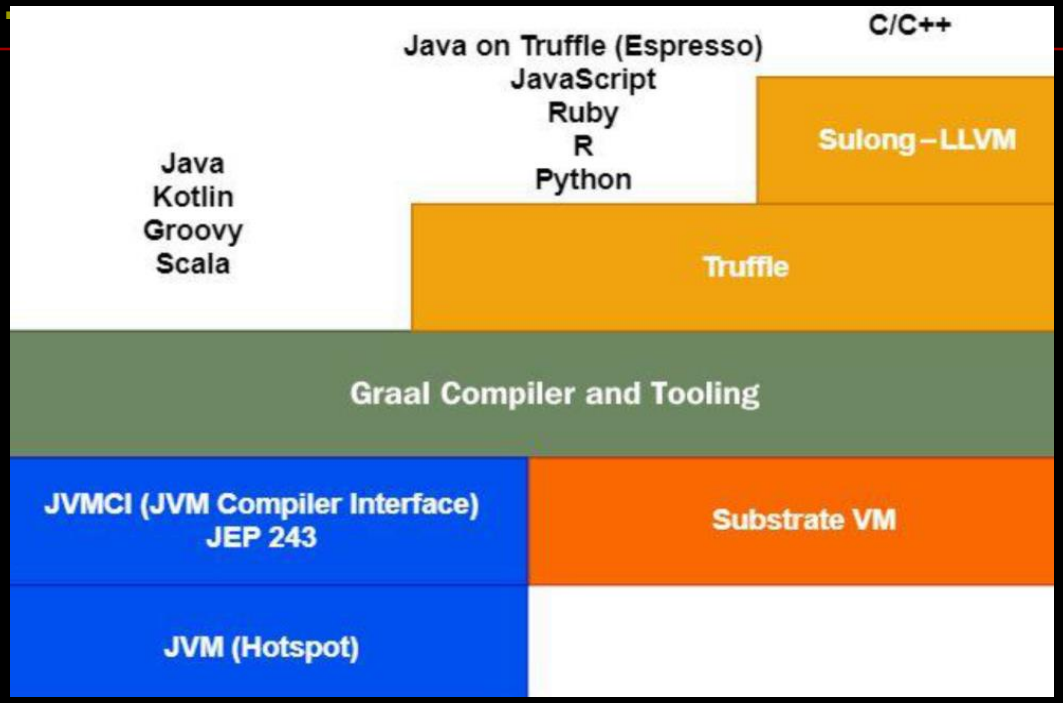
  SPIR-V is at the heart of standards/software and with a mainline LLVM back-end can ultimately open it up to even more.



- https://github.com/llvm/llvm-project/commit/7fd4622d4801cc14823ecde678d55b6f3a106eb9
- https://github.com/KhronosGroup/LLVM-SPIRV-Backend

1.6 GraalVM

- https://en.wikipedia.org/wiki/GraalVM
- https://www.graalvm.org/
-

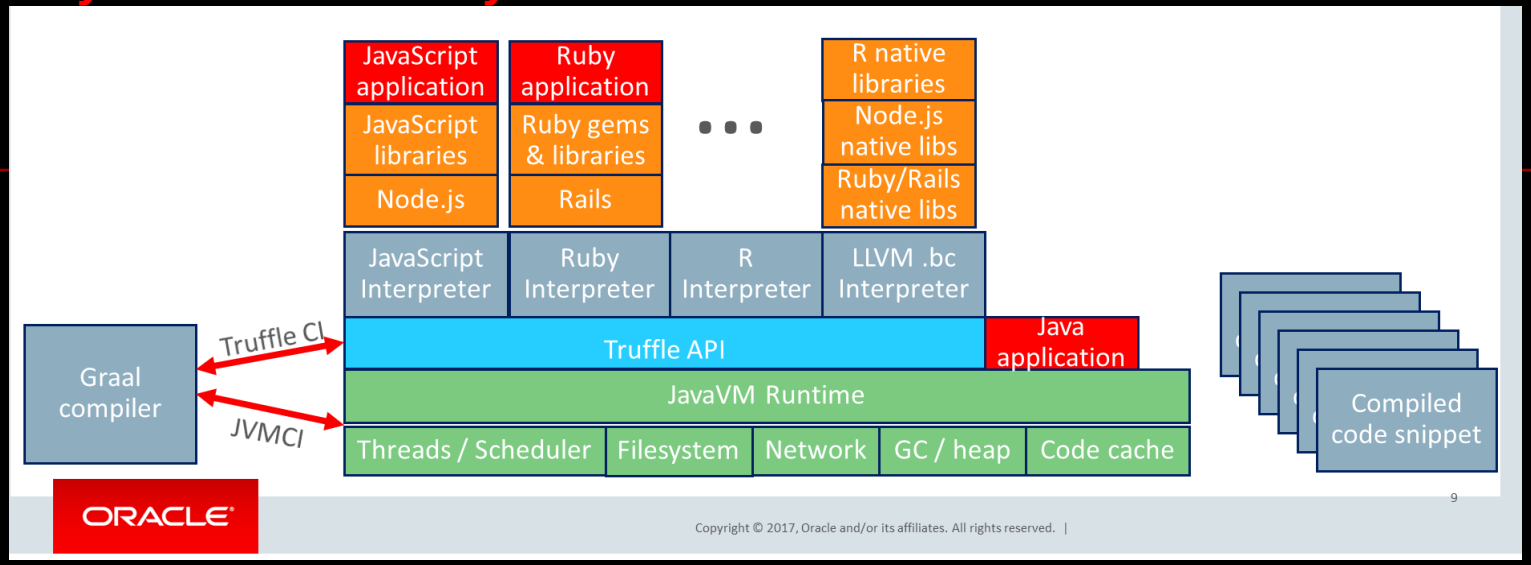


Source: https://static.packt-cdn.com/downloads/9781800564909_ColorImages.pdf

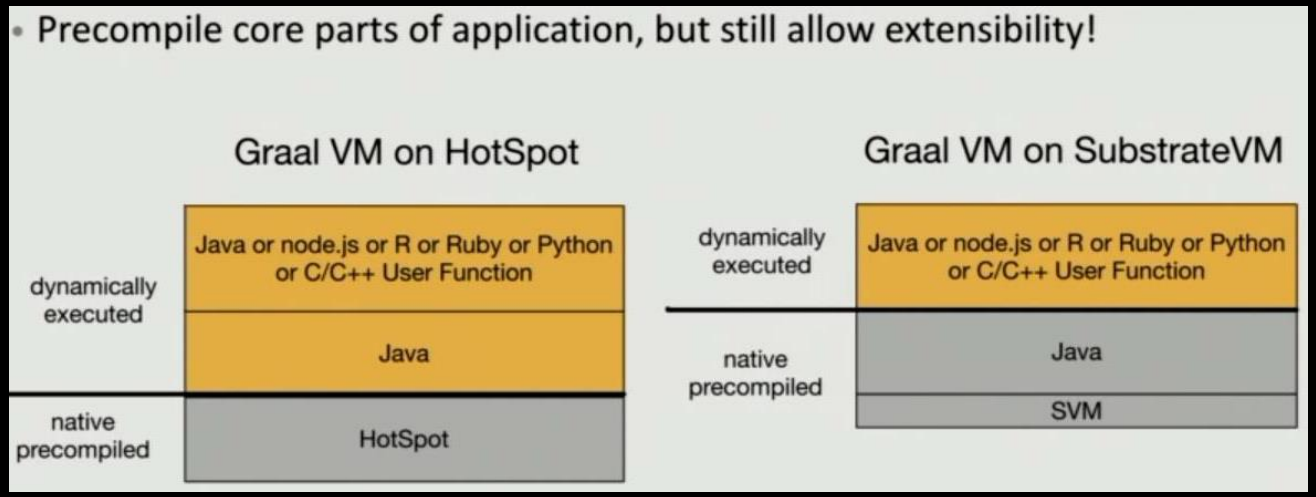
- A Universal High-Performance Polyglot VM
- A meta-runtime for Language-Level Virtualization
- Base on OpenJDK 8, 11, 16, 17 and 19 with JVMCI support.
- https://github.com/graalvm
- https://github.com/oracle/graal

Architecture & design

- A hybrid of static & dynamic runtimes

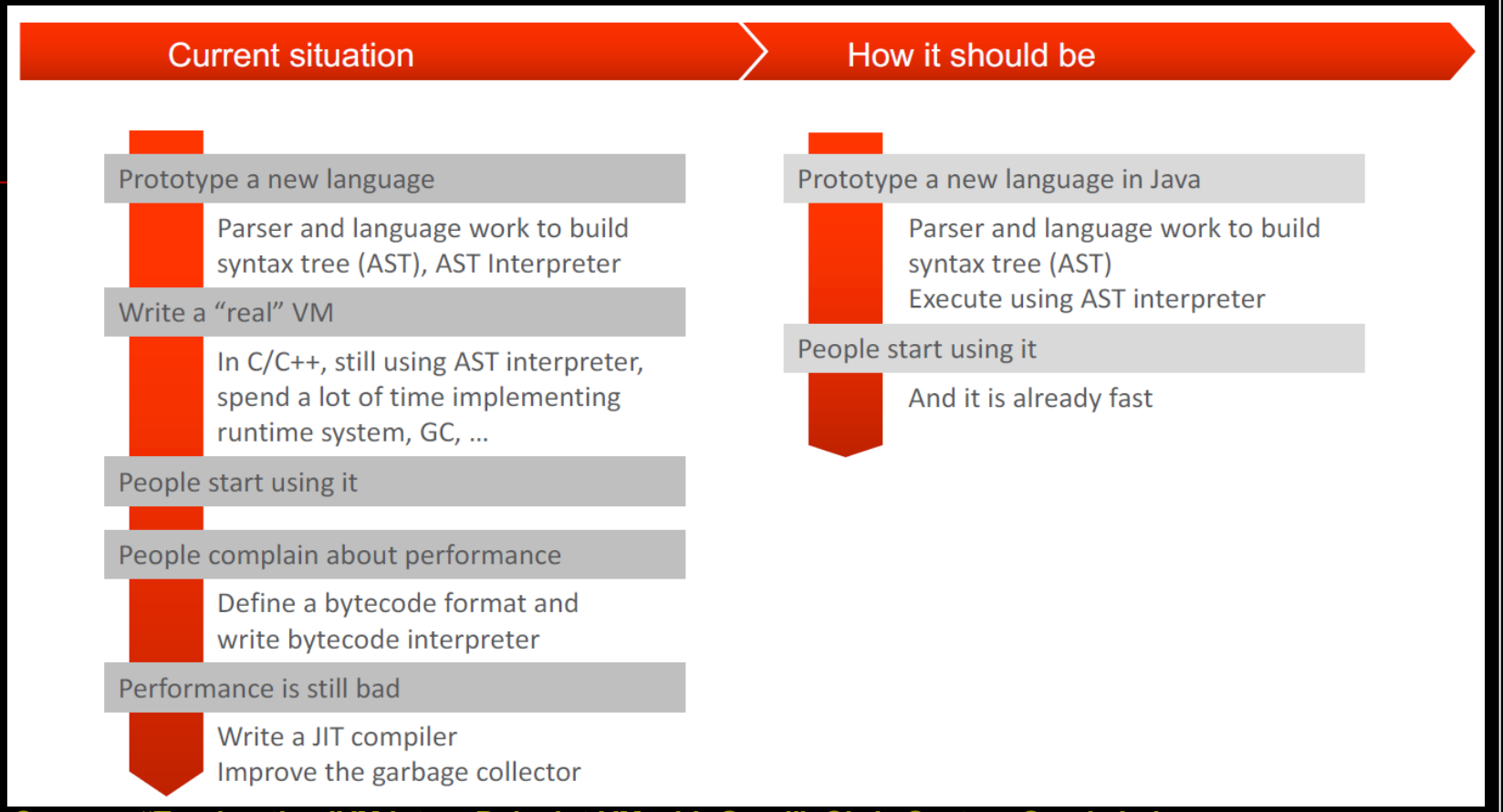


Source: https://ics.psu.edu/wp-content/uploads/2017/02/GraalVM-PSU.pptx



Source: "Adopting Java for the Serverless world", Vadym Kazulkin, JUG London 2020.

Implement a new language runtime



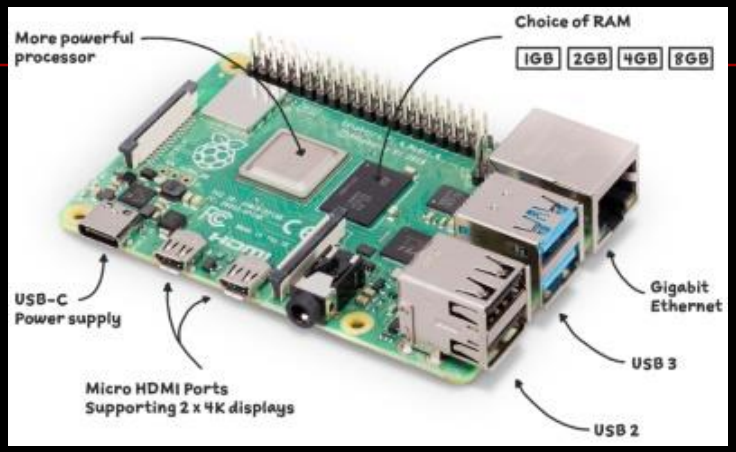
Source: "Turning the JVM into a Polyglot VM with Graal", Chris Seaton, Oracle Labs.

https://www.graalvm.org/22.0/graalvm-as-a-platform/language-implementation-framework/Languages/

2) Testbed

2.1 Raspberry Pi 4(8GB LPDDR4) with Fedora 36

- HW env



SW env

```
[mydev@fedora ~]$ uname -a
Linux fedora 5.19.14-200.fc36.aarch64 #1 SMP PREEMPT_DYNAMIC Wed Oct 5 21:10:47 UTC 2022 aarch64 aarch64 aarch64 GNU/Linux
[mydev@fedora ~]$
[mydev@fedora ~]$ free -m
              total        used        free      shared  buff/cache   available
Mem:           7827         446        5330          13        2051        7115
Swap:          7826           0        7826
[mydev@fedora ~]$
```

```
[mydev@fedora ~]$ gcc -v
Using built-in specs.
COLLECT_GCC=gcc
COLLECT_LTO_WRAPPER=/usr/libexec/gcc/aarch64-redhat-linux/12/lto-wrapper
Target: aarch64-redhat-linux
Configured with: ../configure --enable-bootstrap --enable-languages=c,c++,fortran,objc,obj-c++,ada,go,d,lto --prefix=/usr --mandir=/usr/share/man --infodir=/usr/share/info --with-bugurl=http://bugzilla.redh
at.com/bugzilla --enable-shared --enable-threads=posix --enable-checking=release --enable-multilib --with-system-zlib --enable-__cxa_atexit --disable-libunwind-exceptions --enable-gnu-unique-object --enable
-linker-build-id --with-gcc-major-version-only --enable-libstdcxx-backtrace --with-linker-hash-style=gnu --enable-plugin --enable-initfini-array --with-isl=/builddir/build/BUILD/gcc-12.2.1-20220819/obj-aarc
h64-redhat-linux/isl-install --enable-gnu-indirect-function --build=aarch64-redhat-linux --with-build-config=bootstrap-lto --enable-link-serialization=1
Thread model: posix
Supported LTO compression algorithms: zlib zstd
gcc version 12.2.1 20220819 (Red Hat 12.2.1-2) (GCC)
[mydev@fedora ~]$
[mydev@fedora ~]$ clang -v
clang version 14.0.5 (Fedora 14.0.5-1.fc36)
Target: aarch64-redhat-linux-gnu
Thread model: posix
InstalledDir: /usr/bin
Found candidate GCC installation: /usr/bin/../lib/gcc/aarch64-redhat-linux/12
Selected GCC installation: /usr/bin/../lib/gcc/aarch64-redhat-linux/12
Candidate multilib: .;@m64
Selected multilib: .;@m64
[mydev@fedora ~]$
```

```
[mydev@fedora ~]$ python -V
GraalVM Python 3.8.5 (GraalVM CE Native 22.3.0-dev)
[mydev@fedora ~]$
[mydev@fedora ~]$ java --version
openjdk 19 2022-09-20
OpenJDK Runtime Environment GraalVM CE 22.3.0-dev (build 19+36-jvmci-22.3-b06)
OpenJDK 64-Bit Server VM GraalVM CE 22.3.0-dev (build 19+36-jvmci-22.3-b06, mixed mode, sharing)
[mydev@fedora ~]$
[mydev@fedora ~]$ gu list
ComponentId              Version             Component name                Stability                     Origin
---------------------------------------------------------------------------------------------------------------
graalvm                  22.3.0-dev          GraalVM Core                  Experimental
js                       22.3.0-dev          Graal.js                      Experimental
llvm                     22.3.0-dev          LLVM Runtime Core             Experimental
llvm-toolchain           22.3.0-dev          LLVM.org toolchain            Experimental
native-image             22.3.0-dev          Native Image                  Experimental
native-image-llvm-backend22.3.0-dev          Native Image LLVM Backend     Experimental
python                   22.3.0-dev          GraalVM Python                Experimental
visualvm                 22.3.0-dev          VisualVM                      Experimental
wasm                     22.3.0-dev          GraalWasm                     Experimental
[mydev@fedora ~]$
```

For more details on running GraalPython on RPi4, you may refer to another presentation "Ray--a Swiss Army Knife for Distributed Computing & AI" at COSCon 2022(Online).

```
[mydev@fedora ~]$ go version
go version go1.19.1 linux/arm64
[mydev@fedora ~]$
[mydev@fedora ~]$ rustc -V
rustc 1.64.0 (a55dd71d5 2022-09-19)
[mydev@fedora ~]$
[mydev@fedora ~]$ cargo -V
cargo 1.64.0 (387270bc7 2022-09-16)
[mydev@fedora ~]$
[mydev@fedora ~]$ rustup -V
rustup 1.25.1 (bb60b1e89 2022-07-12)
info: This is the version for the rustup toolchain manager, not the rustc compiler.
info: The currently active `rustc` version is `rustc 1.64.0 (a55dd71d5 2022-09-19)`
[mydev@fedora ~]$
[mydev@fedora ~]$ dotnet --version
7.0.100-rc.1.22431.12
[mydev@fedora ~]$ _
```

```
[mydev@fedora ~]$ cmake --version
cmake version 3.22.2

CMake suite maintained and supported by Kitware (kitware.com/cmake).
[mydev@fedora ~]$
[mydev@fedora ~]$ ninja --version
1.10.2
[mydev@fedora ~]$
[mydev@fedora ~]$ make --version
GNU Make 4.3
Built for aarch64-redhat-linux-gnu
Copyright (C) 1988-2020 Free Software Foundation, Inc.
License GPLv3+: GNU GPL version 3 or later <http://gnu.org/licenses/gpl.html>
This is free software: you are free to change and redistribute it.
There is NO WARRANTY, to the extent permitted by law.
[mydev@fedora ~]$
[mydev@fedora ~]$ mvn --version
Apache Maven 3.8.4 (Red Hat 3.8.4-3)
Maven home: /usr/share/maven
Java version: 19, vendor: GraalVM Community, runtime: /opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19
Default locale: en_US, platform encoding: UTF-8
OS name: "linux", version: "5.19.14-200.fc36.aarch64", arch: "aarch64", family: "unix"
[mydev@fedora ~]$
[mydev@fedora ~]$ bazel version
WARNING: Invoking Bazel in batch mode since it is not invoked from within a workspace (below a directory having a WORKSPACE file).
Build label: 5.3.1
Build target: bazel-out/aarch64-opt/bin/src/main/java/com/google/devtools/build/lib/bazel/BazelServer_deploy.jar
Build time: Mon Sep 19 17:28:14 2022 (1663608494)
Build timestamp: 1663608494
Build timestamp as int: 1663608494
[mydev@fedora ~]$
[mydev@fedora ~]$ gradle --version

------------------------------------------------------------
Gradle 7.5.1
------------------------------------------------------------

Build time:   2022-08-05 21:17:56 UTC
Revision:     d1daa0cbf1a0103000b71484e1dbfe096e095918

Kotlin:       1.6.21
Groovy:       3.0.10
Ant:          Apache Ant(TM) version 1.10.11 compiled on July 10 2021
JVM:          19 (GraalVM Community 19+36-jvmci-22.3-b06)
OS:           Linux 5.19.14-200.fc36.aarch64 aarch64

[mydev@fedora ~]$
```

```
[mydev@fedora .ivy2]$ sbt -V
sbt version in this project: 1.7.2
sbt script version: 1.7.2
[mydev@fedora .ivy2]$
[mydev@fedora .ivy2]$ scalac -version
Scala compiler version 2.13.9 -- Copyright 2002-2021, LAMP/EPFL and Lightbend, Inc.
[mydev@fedora .ivy2]$
```

2.1.1 Fedora

- A Linux distribution developed by the community-supported Fedora Project which is sponsored primarily by Red Hat.
- https://en.wikipedia.org/wiki/Fedora_(operating_system)
- https://getfedora.org/
- https://alt.fedoraproject.org/alt/
- https://spins.fedoraproject.org/
- https://fedoraproject.org/wiki/Architectures/ARM
- https://fedoramagazine.org/
- https://silverblue.fedoraproject.org/
- https://fedoraproject.org/wiki/Changes/RaspberryPi4
- Developer friendly!

2.1.1.1 EDA support

- https://fedoraproject.org/wiki/Electronic_Lab

Installation

- sudo dnf groupinstall "Electronic Lab“

```
[mydev@fedora /]$ dnf -v group info "Electronic Lab"
...
Group: Electronic Lab
 Group-Id: electronic-lab
 Description: Design and simulation tools for hardware engineers
 Default Packages:
   CUnit-2.1.3-25.fc36.aarch64
   LabPlot-2.8.1-6.fc36.aarch64
   acpica-tools-20220331-3.fc36.aarch64
   alliance-5.1.1-25.20160506gitd8c05cd.fc36.aarch64
   arduino
   avarice-2.13-15.fc36.aarch64
   avr-binutils-1:2.37-3.fc36.aarch64
   avr-gcc-1:11.2.0-1.fc36.aarch64
   avr-gcc-c++-1:11.2.0-1.fc36.aarch64
   avra-1.3.0-17.fc36.aarch64
   avrdude-6.4-3.fc36.aarch64
   cgnslib-4.2.0-6.fc36.aarch64
   dfu-programmer-0.7.2-10.fc36.aarch64
   dia-CMOS-0.1-20.fc36.noarch
   dia-Digital-0.1-20.fc36.noarch
   dia-electric2-0.1-20.fc36.noarch
   dia-electronic-0.1-20.fc36.noarch
   electric
   emacs-vregs-mode-1.470-28.fc36.noarch
   espresso-ab-1.0-24.fc36.aarch64
   flterm-1.2-19.fc36.aarch64
   freeDiameter-1.5.0-4.fc36.aarch64
   fritzing-0.9.10-1.20220514.fc36.aarch64
   gerbv-2.9.2-1.fc36.aarch64
   ghc-chalmers-lava2000-devel
   ghdl-0.38~dev-15.20201208git83dfd49.fc36.aarch64
   gnucap-0.35-35.fc36.aarch64
   gnuradio-3.10.1.0-2.fc36.aarch64
   gnusim8085-1.4.1-4.fc36.aarch64
   gpsim-0.31.0-6.fc36.aarch64
   gputils-1.5.0-9.fc36.aarch64
   gr-osmosdr-0.2.3-28.20210217gita100eb02.fc36.aarch64
   gsim85-0.3-28.fc36.aarch64
   gspiceui
   gtkterm-1.1.1-2.fc36.aarch64
   gtkwave-3.3.111-3.fc36.aarch64
   hct-0.7.60-33.fc36.noarch
   hiredis-1.0.2-2.fc36.aarch64
   icaro-2.0-10.fc36.noarch
   icestorm-0-0.22.20220705git2bc5417.fc36.aarch64
   irsim-9.7.104-7.fc36.aarch64
   iverilog-11.0-3.fc35.aarch64
   kicad-1:6.0.8-1.fc36.aarch64
   ktechlab-0.50.0-1.fc36.aarch64
   linsmith-0.99.31-9.fc36.aarch64
   magic-8.3.324-1.fc36.aarch64
   magic-doc-8.3.324-1.fc36.aarch64
   mcu8051ide
   mot-adms-2.3.7-4.fc36.aarch64
   netgen-1.3.7-43.fc36.aarch64
   nextpnr-1-12.20220912gitf1349e1.fc36.aarch64
   ngspice-37-1.fc36.aarch64
   openocd-0.11.0-2.fc36.1.aarch64
   pcb-4.2.0-9.fc36.aarch64
   perl-Hardware-Verilog-Parser-0.13-38.fc36.noarch
   perl-Hardware-Vhdl-Lexer-1.00-39.fc36.noarch
   perl-Hardware-Vhdl-Parser-0.12-39.fc36.noarch
   perl-Hardware-Vhdl-Tidy
   perl-ModelSim-List-0.06-37.fc36.noarch
   perl-Perlilog-1.0-18.fc36.noarch
   perl-SystemC-Vregs-1.470-28.fc36.noarch
   perl-Verilog-CodeGen
   perl-Verilog-Perl-3.478-3.fc36.aarch64
   perl-Verilog-Readmem-0.05-19.fc36.noarch
   picocom-3.1-11.fc36.aarch64
   pulseview-0.4.2-10.fc36.aarch64
   python3-migen-0.9.2-14.20220705git0fb9173.fc36.noarch
   python3-myhdl-0.11-7.fc36.noarch
   qucs-0.0.19-6.fc36.aarch64
   rtl-sdr-0.6.0-11.fc36.aarch64
   sdcc-4.1.0-3.fc36.aarch64
   sigrok-cli-0.7.2-3.fc36.aarch64
   sigrok-firmware-fx2lafw-0.1.7-6.fc36.noarch
   smartsim-1.4-18.fc36.aarch64
   srecord-1.64-22.fc36.aarch64
   tclspice-37-1.fc36.aarch64
   tkcvs-8.2.3-15.fc36.noarch
   tkgate-2.0-36.beta10.fc36.aarch64
   toped-0.9.81-31.svn2211.fc36.aarch64
   trellis-1.2.1-10.20220821git98e0ea3.fc36.aarch64
   uisp-20050207-31.fc36.aarch64
   verilator-4.108-3.fc35.aarch64
   vhd2vl-2.5-14.fc36.aarch64
   vrq
   xcircuit-3.10.30-4.fc36.aarch64
   xorg-x11-fonts-100dpi-7.5-33.fc36.noarch
   xorg-x11-fonts-ISO8859-1-100dpi-7.5-33.fc36.noarch
   xorg-x11-fonts-ISO8859-9-100dpi-7.5-33.fc36.noarch
   xorg-x11-fonts-Type1-7.5-33.fc36.noarch
   yosys-0.21-1.20220912gitd98738d.fc36.aarch64
 Optional Packages:
   kdesvn-2.1.0-5.fc36.aarch64
   minicom-2.8-1.fc36.aarch64
```

- sudo dnf install libevent libevent-devel boost boost-devel verilator yosys z3 z3-devel z3-libs java-z3 python-z3
- sudo dnf install python3-pytest dfu-util json-c json-c-devel
- sudo dnf install libftdi libftdi-devel python3-libftdi python3-pyftdi

2.1.1.2 Fedora 37

- https://fedoraproject.org/wiki/Releases/37/ChangeSet

Raspberry Pi 4

- Fedora 37 To Offer Official Support On Raspberry Pi 4 Devices

  https://www.phoronix.com/news/Raspberry-Pi-4-Fedora-37

A month ago there was the Fedora 37 change proposal for Fedora to officially support the Raspberry Pi 4, including its accelerated Broadcom graphics and to better advertise Fedora for the Raspberry Pi. The Fedora Engineering and Steering Committee (FESCo) has now signed off on this "official" support for the Raspberry Pi 4.

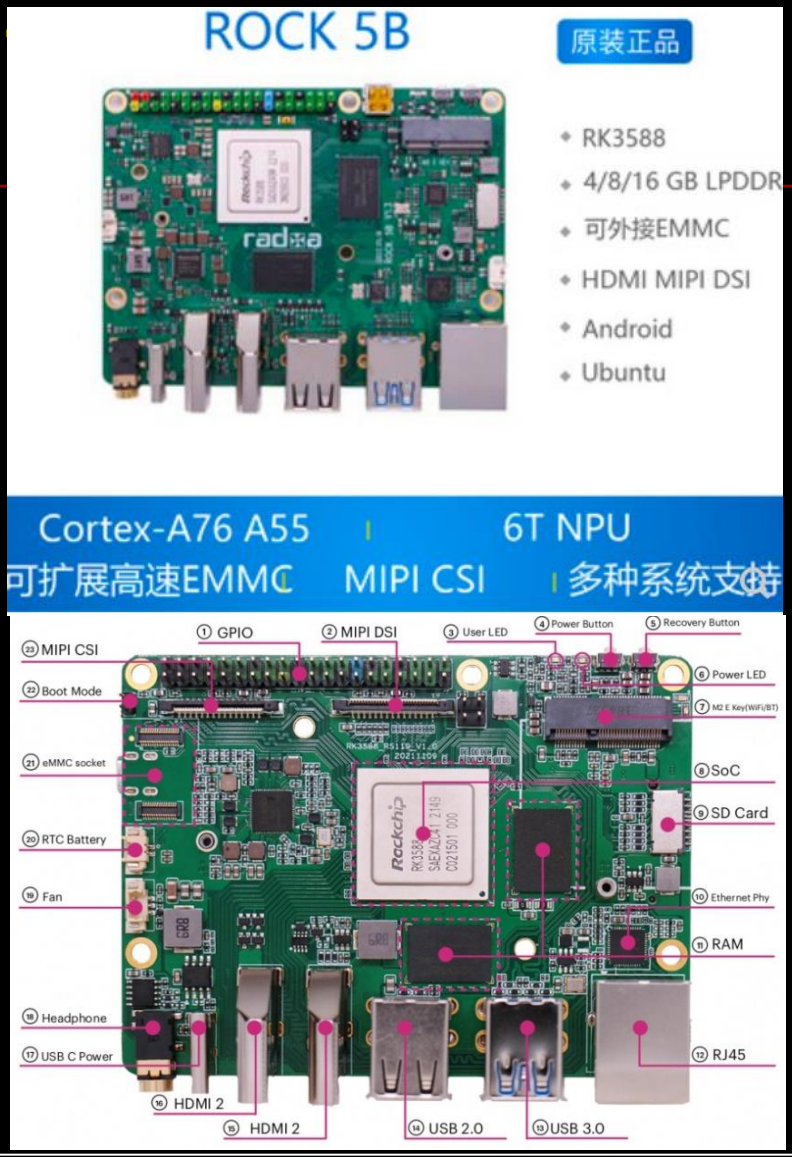
The Raspberry Pi 4 to date hasn't been a significant focus for Fedora Workstation due to various patches not being upstreamed-- most notably, waiting on the open-source 3D graphics bits to be upstreamed in the kernel. Now though that those upstream bits are coming together, Fedora 37 will be focusing on advertising its support for the Raspberry Pi 4 Model B as well as the Raspberry Pi 400 and Raspberry Pi CM4 compute module.

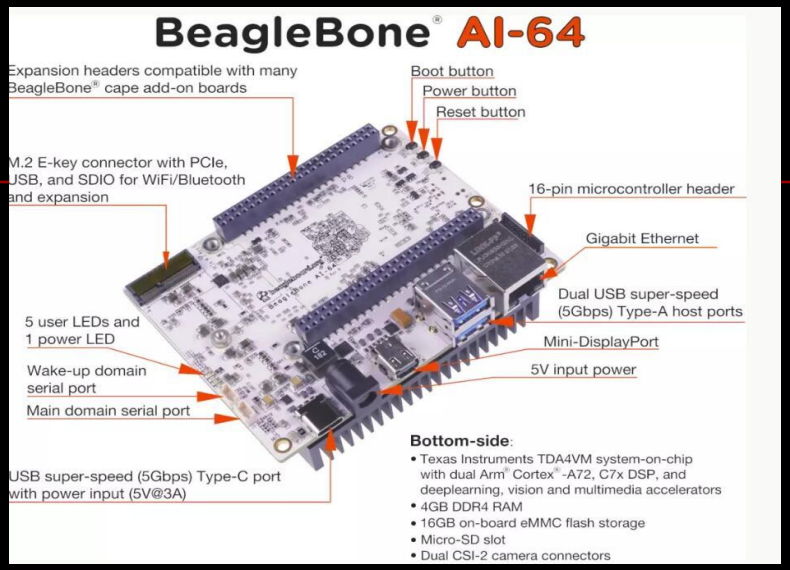
With the open-source OpenGL and Vulkan support, these latest Raspberry Pi boards are suitable for Fedora Workstation usage. The latest milestones there are V3DV just having crossed Vulkan 1.2 and Raspberry Pi 4 V3D DRM/KMS driver support in Linux 6.0. However, there still are upstream issues surrounding WiFi support for the Raspberry Pi 400, the Raspberry Pi CM4 not necessarily being very suitable for desktop use but more edge/IoT/embedded, and some device support such as around audio may be problematic.

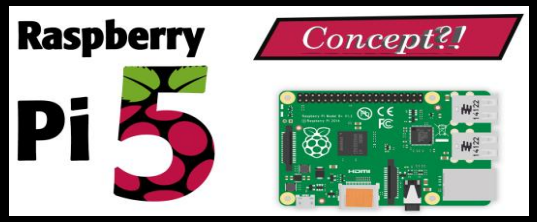
> ***The Raspberry Pi 4 is a widely available, reasonably priced device. It has worked well in Fedora for some time in IoT and Server use cases, and now with a fully accelerated graphics stack available it's a great device from a price-per-performance perspective, and it has a wide ecosystem, so fully supporting this in Fedora makes a compelling case.***

- https://www.phoronix.com/news/Fedora-37-Beta

2.2 Switching to more powerful development boards







II. RISC-V Toolchain

1) GCC

Overview

- https://gcc.gnu.org/onlinedocs/gcc/RISC-V-Options.html

1.1 Install from distribution package

- ...

1.2.1 Fedora

```
[mydev@fedora /]$ dnf search riscv
================================================ Name & Summary Matched: riscv ================
binutils-riscv64-linux-gnu.aarch64 : Cross-build binary utilities for riscv64-linux-gnu
gcc-c++-riscv64-linux-gnu.aarch64 : Cross-build binary utilities for riscv64-linux-gnu
gcc-riscv64-linux-gnu.aarch64 : Cross-build binary utilities for riscv64-linux-gnu
qemu-user-static-riscv.aarch64 : QEMU user mode emulation of riscv qemu targets static build
===================================================== Name Matched: riscv ====================
qemu-system-riscv.aarch64 : QEMU system emulator for RISC-V
qemu-system-riscv-core.aarch64 : QEMU system emulator for RISC-V
[mydev@fedora /]$
```

e.g., sudo dnf --installroot=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V /GCC/Fedora --releasever=/ install gcc-riscv64-linux-gnu

```
[mydev@fedora /]$ tree -L 1 /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora
├── bin → usr/bin
├── boot
├── dev
├── etc
├── home
├── lib → usr/lib
├── lib64 → usr/lib64
├── media
├── mnt
├── opt
├── proc
├── root
├── run
├── sbin → usr/sbin
├── srv
├── sys
├── tmp
├── usr
└── var
```

```
[mydev@fedora /]$ ll /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/bin
lrwxrwxrwx. 1 root root 7 Jul 21  2021 /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/bin → usr/bin/
[mydev@fedora /]$ ll /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/usr/bin
total 47664
dr-xr-xr-x. 1 root root     1616 Apr  2 10:31 ./
drwxr-xr-x. 1 root root      134 Apr  2 10:25 ../
-rwxr-xr-x. 1 root root       33 Jul 21  2021 alias*
-rwxr-xr-x. 1 root root  1433664 Jul 21  2021 bash*
lrwxrwxrwx. 1 root root       10 Jul 21  2021 bashbug → bashbug-64*
-rwxr-xr-x. 1 root root     7057 Jul 21  2021 bashbug-64*
-rwxr-xr-x. 1 root root       30 Jul 21  2021 bg*
-rwxr-xr-x. 1 root root     3289 Mar 15  2022 catchsegv*
-rwxr-xr-x. 1 root root       30 Jul 21  2021 cd*
-rwxr-xr-x. 1 root root       35 Jul 21  2021 command*
-rwxr-xr-x. 1 root root       30 Jul 21  2021 fc*
-rwxr-xr-x. 1 root root       30 Jul 21  2021 fg*
-rwxr-xr-x. 1 root root    70216 Mar 15  2022 gencat*
-rwxr-xr-x. 1 root root    69456 Mar 15  2022 getconf*
-rwxr-xr-x. 1 root root    70072 Mar 15  2022 getent*
-rwxr-xr-x. 1 root root       35 Jul 21  2021 getopts*
-rwxr-xr-x. 1 root root       32 Jul 21  2021 hash*
-rwxr-xr-x. 1 root root    70824 Mar 15  2022 iconv*
-rwxr-xr-x. 1 root root       32 Jul 21  2021 jobs*
-rwxr-xr-x. 1 root root     5347 Mar 15  2022 ldd*
lrwxrwxrwx. 1 root root       31 Mar 15  2022 ld.so → ../../lib/ld-linux-aarch64.so.1*
-rwxr-xr-x. 1 root root    78024 Mar 15  2022 locale*
-rwxr-xr-x. 1 root root   343448 Mar 15  2022 localedef*
-rwxr-xr-x. 1 root root    69576 Mar 15  2022 pldd*
-rwxr-xr-x. 1 root root       32 Jul 21  2021 read*
-rwxr-xr-x. 1 root root  1139128 Oct 28  2021 riscv64-linux-gnu-addr2line*
-rwxr-xr-x. 2 root root  1072856 Oct 28  2021 riscv64-linux-gnu-ar*
-rwxr-xr-x. 2 root root  1667920 Oct 28  2021 riscv64-linux-gnu-as*
-rwxr-xr-x. 2 root root  1144216 Aug  1  2021 riscv64-linux-gnu-c++*
-rwxr-xr-x. 1 root root   136736 Oct 28  2021 riscv64-linux-gnu-c++filt*
-rwxr-xr-x. 1 root root  1144144 Aug  1  2021 riscv64-linux-gnu-cpp*
-rwxr-xr-x. 1 root root    70136 Oct 28  2021 riscv64-linux-gnu-elfedit*
-rwxr-xr-x. 2 root root  1144216 Aug  1  2021 riscv64-linux-gnu-g++*
-rwxr-xr-x. 1 root root  1144248 Aug  1  2021 riscv64-linux-gnu-gcc*
-rwxr-xr-x. 1 root root    70912 Aug  1  2021 riscv64-linux-gnu-gcc-ar*
-rwxr-xr-x. 1 root root    70912 Aug  1  2021 riscv64-linux-gnu-gcc-nm*
-rwxr-xr-x. 1 root root    70920 Aug  1  2021 riscv64-linux-gnu-gcc-ranlib*
-rwxr-xr-x. 1 root root   612432 Aug  1  2021 riscv64-linux-gnu-gcov*
-rwxr-xr-x. 1 root root   544104 Aug  1  2021 riscv64-linux-gnu-gcov-dump*
-rwxr-xr-x. 1 root root   545160 Aug  1  2021 riscv64-linux-gnu-gcov-tool*
-rwxr-xr-x. 1 root root  1206240 Oct 28  2021 riscv64-linux-gnu-gprof*
-rwxr-xr-x. 4 root root  3643768 Oct 28  2021 riscv64-linux-gnu-ld*
-rwxr-xr-x. 4 root root  3643768 Oct 28  2021 riscv64-linux-gnu-ld.bfd*
-rwxr-xr-x. 1 root root 16619672 Aug  1  2021 riscv64-linux-gnu-lto-dump*
-rwxr-xr-x. 2 root root  1205768 Oct 28  2021 riscv64-linux-gnu-nm*
-rwxr-xr-x. 2 root root  1341512 Oct 28  2021 riscv64-linux-gnu-objcopy*
-rwxr-xr-x. 2 root root  2529936 Oct 28  2021 riscv64-linux-gnu-objdump*
-rwxr-xr-x. 2 root root  1072856 Oct 28  2021 riscv64-linux-gnu-ranlib*
-rwxr-xr-x. 2 root root   935544 Oct 28  2021 riscv64-linux-gnu-readelf*
-rwxr-xr-x. 1 root root  1072504 Oct 28  2021 riscv64-linux-gnu-size*
-rwxr-xr-x. 1 root root  1072536 Oct 28  2021 riscv64-linux-gnu-strings*
-rwxr-xr-x. 2 root root  1341472 Oct 28  2021 riscv64-linux-gnu-strip*
lrwxrwxrwx. 1 root root        4 Jul 21  2021 sh → bash*
-rwxr-xr-x. 1 root root     4282 Mar 15  2022 sotruss*
-rwxr-xr-x. 1 root root    69640 Mar 15  2022 sprof*
-rwxr-xr-x. 1 root root       32 Jul 21  2021 type*
-rwxr-xr-x. 1 root root    15352 Mar 15  2022 tzselect*
-rwxr-xr-x. 1 root root       34 Jul 21  2021 ulimit*
-rwxr-xr-x. 1 root root       33 Jul 21  2021 umask*
-rwxr-xr-x. 1 root root       35 Jul 21  2021 unalias*
-rwxr-xr-x. 1 root root       32 Jul 21  2021 wait*
-rwxr-xr-x. 1 root root    69576 Mar 15  2022 zdump*
[mydev@fedora /]$
```

```
[mydev@fedora /]$ /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/usr/bin/riscv64-linux-gnu-gcc -v
Using built-in specs.
COLLECT_GCC=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/usr/bin/riscv64-linux-gnu-gcc
COLLECT_LTO_WRAPPER=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Fedora/usr/bin/../libexec/gcc/riscv64-linux-gnu/11
/lto-wrapper
Target: riscv64-linux-gnu
Configured with: ../gcc-11.2.1-20210728/configure --bindir=/usr/bin --build=aarch64-redhat-linux-gnu --datadir=/us
r/share --disable-decimal-float --disable-dependency-tracking --disable-gold --disable-libgcj --disable-libgomp --
disable-libmpx --disable-libquadmath --disable-libssp --disable-libunwind-exceptions --disable-shared --disable-si
lent-rules --disable-sjlj-exceptions --disable-threads --with-ld=/usr/bin/riscv64-linux-gnu-ld --enable-__cxa_atex
it --enable-checking=release --enable-gnu-unique-object --enable-initfini-array --enable-languages=c,c++ --enable-
linker-build-id --enable-lto --enable-nls --enable-obsolete --enable-plugin --enable-targets=all --exec-prefix=/us
r --host=aarch64-redhat-linux-gnu --includedir=/usr/include --infodir=/usr/share/info --libexecdir=/usr/libexec --
localstatedir=/var --mandir=/usr/share/man --prefix=/usr --program-prefix=riscv64-linux-gnu- --sbindir=/usr/sbin -
-sharedstatedir=/var/lib --sysconfdir=/etc --target=riscv64-linux-gnu --with-bugurl=http://bugzilla.redhat.com/bug
zilla/ --with-gcc-major-version-only --with-isl --with-newlib --with-plugin-ld=/usr/bin/riscv64-linux-gnu-ld --wit
h-sysroot=/usr/riscv64-linux-gnu/sys-root --with-system-libunwind --with-system-zlib --without-headers --with-link
er-hash-style=gnu
Thread model: single
Supported LTO compression algorithms: zlib zstd
gcc version 11.2.1 20210728 (Red Hat Cross 11.2.1-1) (GCC)
[mydev@fedora /]$
```

1.2 Build from source

1.2.1 Official

- https://github.com/riscv/riscv-gnu-toolchain

binutils @ b51c2fe	Switch gcc to upstream and update binutils commits	last month
contrib	Vagrant plugin check so it will not fail in the middle of provisioning	2 years ago
gcc @ 2ee5e43	Bump gcc branch to 12.2 release. (#1128)	7 days ago
glibc @ 9826b03	Update glibc and newlib paths	7 months ago
linux-headers/include	Update linux header to 5.10.5	2 years ago
musl @ 85e0e35	Add musl libc submodule	7 months ago
newlib @ 415fdd4	Update glibc and newlib paths	7 months ago
pk @ 2efabd3	Add option '--with-sim' to set simulator	4 months ago
qemu @ 823a3f1	Bump qemu to 7.0	4 months ago
regression	Delete accidental regression/output file.	4 years ago
riscv-dejagnu @ 4ea498a	Bump dejagnu to include newlib-nano testsuite support.	3 years ago
riscv-gdb @ 5da071e	Bump gdb for ctf related build fix.	2 years ago
scripts	Pass right extension info to qemu	4 months ago
spike @ a0298a3	Add option '--with-sim' to set simulator	4 months ago
test	Bump gcc branch to 12.2 release. (#1128)	7 days ago

Getting the sources

This repository uses submodules, but submodules will fetch automatically on demand, so `--recursive` or `git submodule update --init --recursive` is not needed.

Warning: git clone takes around 6.65 GB of disk and download size

for ELF with multilib enabled:

```
./configure --prefix=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF --enable-multilib
```

make -j1:

```
[mydev@fedora /]$ tree -L 1 /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF
├── bin
├── include
├── lib
├── lib64
├── libexec
├── riscv64-unknown-elf
└── share
```

```
[mydev@fedora /]$ tree /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/bin
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/bin
├── riscv64-unknown-elf-addr2line
├── riscv64-unknown-elf-ar
├── riscv64-unknown-elf-as
├── riscv64-unknown-elf-c++
├── riscv64-unknown-elf-c++filt
├── riscv64-unknown-elf-cpp
├── riscv64-unknown-elf-elfedit
├── riscv64-unknown-elf-g++
├── riscv64-unknown-elf-gcc
├── riscv64-unknown-elf-gcc-12.2.0
├── riscv64-unknown-elf-gcc-ar
├── riscv64-unknown-elf-gcc-nm
├── riscv64-unknown-elf-gcc-ranlib
├── riscv64-unknown-elf-gcov
├── riscv64-unknown-elf-gcov-dump
├── riscv64-unknown-elf-gcov-tool
├── riscv64-unknown-elf-gdb
├── riscv64-unknown-elf-gdb-add-index
├── riscv64-unknown-elf-gprof
├── riscv64-unknown-elf-ld
├── riscv64-unknown-elf-ld.bfd
├── riscv64-unknown-elf-lto-dump
├── riscv64-unknown-elf-nm
├── riscv64-unknown-elf-objcopy
├── riscv64-unknown-elf-objdump
├── riscv64-unknown-elf-ranlib
├── riscv64-unknown-elf-readelf
├── riscv64-unknown-elf-run
├── riscv64-unknown-elf-size
├── riscv64-unknown-elf-strings
└── riscv64-unknown-elf-strip
```

directly built on RPi4 against "riscv64-unknown-elf-" for ~6.5h (depends on network speed).

for Linux with multilib enabled:

```
./configure --prefix=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/Linux --enable-multilib
```

make linux -j1

```
[mydev@fedora /]$ tree -L 1 /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/Linux
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/Linux
├── bin
├── include
├── lib
├── lib64
├── libexec
├── riscv64-unknown-linux-gnu
├── share
└── sysroot
```

```
[mydev@fedora /]$ tree /opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/Linux/bin
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/Linux/bin
├── riscv64-unknown-linux-gnu-addr2line
├── riscv64-unknown-linux-gnu-ar
├── riscv64-unknown-linux-gnu-as
├── riscv64-unknown-linux-gnu-c++
├── riscv64-unknown-linux-gnu-c++filt
├── riscv64-unknown-linux-gnu-cpp
├── riscv64-unknown-linux-gnu-elfedit
├── riscv64-unknown-linux-gnu-g++
├── riscv64-unknown-linux-gnu-gcc
├── riscv64-unknown-linux-gnu-gcc-12.2.0
├── riscv64-unknown-linux-gnu-gcc-ar
├── riscv64-unknown-linux-gnu-gcc-nm
├── riscv64-unknown-linux-gnu-gcc-ranlib
├── riscv64-unknown-linux-gnu-gcov
├── riscv64-unknown-linux-gnu-gcov-dump
├── riscv64-unknown-linux-gnu-gcov-tool
├── riscv64-unknown-linux-gnu-gdb
├── riscv64-unknown-linux-gnu-gdb-add-index
├── riscv64-unknown-linux-gnu-gfortran
├── riscv64-unknown-linux-gnu-gprof
├── riscv64-unknown-linux-gnu-ld
├── riscv64-unknown-linux-gnu-ld.bfd
├── riscv64-unknown-linux-gnu-lto-dump
├── riscv64-unknown-linux-gnu-nm
├── riscv64-unknown-linux-gnu-objcopy
├── riscv64-unknown-linux-gnu-objdump
├── riscv64-unknown-linux-gnu-ranlib
├── riscv64-unknown-linux-gnu-readelf
├── riscv64-unknown-linux-gnu-run
├── riscv64-unknown-linux-gnu-size
├── riscv64-unknown-linux-gnu-strings
└── riscv64-unknown-linux-gnu-strip
```

directly built on RPi4 against "riscv64-unknown-linux-gnu-" for ~9.5 hours (depends on network speed).

2) LLVM

- No available binary packages currently

1.2.1 Build from source on RPi4

- https://llvm.org/docs/CMake.html
- https://llvm.org/docs/GettingStarted.html
- Build

1. git clone https://github.com/llvm/llvm-project
   (On main branch, last commit: 910ad36e1a2592915b32941844cf089442972d7a)
   cd $SRC_LLVM;mkdir -p build/Install;cd build
2. our configurations:

```
cmake -G Ninja -DCMAKE_BUILD_TYPE=Release -DLLVM_TARGETS_TO_BUILD="RISCV;BPF;WebAssembly" -DLLVM_ENABLE_PROJECTS="
clang;clang-tools-extra;libclc;libcxx;libcxxabi;lld;lldb;mlir;cross-project-tests" -DLLVM_DEFAULT_TARGET_TRIPLE="r
iscv64-unknown-linux-gnu" -DCMAKE_INSTALL_PREFIX=$PWD/Install ../llvm
```

3. build command:

```
ninja -j$(nproc)
```

   it costed ~11 hours on my RPi4 for finish the full build

```
[mydev@fedora llvm-project-main]$ tree -L 1 build//Install/
build//Install/
├── bin
├── include
├── lib
├── libexec
├── local
└── share
```

```
[mydev@fedora llvm-project-main]$ tree build//Install/bin
build//Install/bin
├── analyze-build
├── bugpoint
├── c-index-test
├── clang → clang-16
├── clang++ → clang
├── clang-16
├── clang-apply-replacements
├── clang-change-namespace
├── clang-check
├── clang-cl → clang
├── clang-cpp → clang
├── clangd
├── clang-doc
├── clang-extdef-mapping
├── clang-format
├── clang-include-fixer
├── clang-linker-wrapper
├── clang-move
├── clang-offload-bundler
├── clang-offload-packager
├── clang-pseudo
├── clang-query
├── clang-refactor
├── clang-rename
├── clang-reorder-fields
├── clang-repl
├── clang-scan-deps
├── clang-tblgen
├── clang-tidy
├── diagtool
├── dsymutil
├── find-all-symbols
├── git-clang-format
├── hmaptool
├── intercept-build
├── ld64.lld → lld
├── ld.lld → lld
├── llc
├── lld
├── lldb
├── lldb-argdumper
├── lldb-instr
├── lldb-server
├── lldb-vscode
├── lld-link → lld
├── lli
├── llvm-addr2line → llvm-symbolizer
├── llvm-ar
├── llvm-as
├── llvm-bcanalyzer
├── llvm-bitcode-strip → llvm-objcopy
├── llvm-cat
├── llvm-cfi-verify
├── llvm-config
├── llvm-cov
├── llvm-c-test
├── llvm-cvtres
├── llvm-cxxdump
├── llvm-cxxfilt
├── llvm-cxxmap
├── llvm-debuginfod
├── llvm-debuginfod-find
├── llvm-dis
├── llvm-dlltool → llvm-ar
├── llvm-dwarfdump
├── llvm-dwarfutil
├── llvm-dwp
├── llvm-exegesis
├── llvm-extract
├── llvm-gsymutil
├── llvm-ifs
├── llvm-install-name-tool → llvm-objcopy
├── llvm-jitlink
├── llvm-lib → llvm-ar
├── llvm-libtool-darwin
├── llvm-link
├── llvm-lipo
├── llvm-lto
├── llvm-lto2
├── llvm-mc
├── llvm-mca
├── llvm-ml
├── llvm-modextract
├── llvm-mt
├── llvm-nm
├── llvm-objcopy
├── llvm-objdump
├── llvm-opt-report
├── llvm-otool → llvm-objdump
├── llvm-pdbutil
├── llvm-profdata
├── llvm-profgen
├── llvm-ranlib → llvm-ar
├── llvm-rc
```

```
├── llvm-readelf → llvm-readobj
├── llvm-readobj
├── llvm-reduce
├── llvm-remark-size-diff
├── llvm-remarkutil
├── llvm-rtdyld
├── llvm-sim
├── llvm-size
├── llvm-split
├── llvm-stress
├── llvm-strings
├── llvm-strip → llvm-objcopy
├── llvm-symbolizer
├── llvm-tapi-diff
├── llvm-tblgen
├── llvm-tli-checker
├── llvm-undname
├── llvm-windres → llvm-rc
├── llvm-xray
├── mlir-linalg-ods-yaml-gen
├── mlir-lsp-server
├── mlir-opt
├── mlir-pdll
├── mlir-pdll-lsp-server
├── mlir-reduce
├── mlir-tblgen
├── mlir-translate
├── modularize
├── opt
├── pp-trace
├── run-clang-tidy
├── sancov
```

```
├── sanstats
├── scan-build
├── scan-build-py
├── scan-view
├── tblgen-lsp-server
├── verify-uselistorder
└── wasm-ld → lld
```

...

III. FOSS EDA Tools

1) Chisel

1.1 Firrtl

Tetralogy

Code:

On master branch, last commit: 79c17c8448c8c15a245c3435d9c97c128738121e

- **Compile**

```
[mydev@fedora firrtl-master]$ sbt compile
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project firrtl-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/project
[info] loading settings for project firrtl from build.sbt ...
[info] set current project to firrtl (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/)
[info] Executing in batch mode. For better performance use sbt's shell
[info] Compiling 1 protobuf files to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/src_managed/main/compiled_protobuf
[info] Compiling schema /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/src/main/proto/firrtl.proto
protoc-jar: protoc version: 3.5.1, detected platform: linux-aarch_64 (linux/aarch64)
protoc-jar: downloading: https://maven.aliyun.com/repository/central/com/google/protobuf/protoc/maven-metadata.xml
```

...

```
[mydev@fedora firrtl-master]$ sbt test
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project firrtl-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/project
[info] loading settings for project firrtl from build.sbt ...
[info] set current project to firrtl (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/)
[info] compiling 160 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/test-classes ...
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/src/test/scala/firrtlTests/options/PhaseManagerSpec.scala:625:44: match may not be exhaustive.
[warn] It would fail on the following input: Dependency(Right(_))
[warn]     val expectedClasses = expectedDeps.map { case Dependency(Left(c)) ⇒ c }
[warn]                                              ^
```

- **Test**

```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/src/main/scala/tutorial/lesson2-ir-fields/AnalyzeCircuit.scala:82:20: object LowForm in package firrtl is deprecated (since FIRRTL 1.3): Mi
x-in the DependencyAPIMigration trait into your Transform and specify its Dependency API dependencies. See: https://bit.ly/2Voppre
[warn]   def outputForm = LowForm
[warn]                    ^
[warn] 85 warnings found
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/src_managed/main/compiled_protobuf/firrtl/FirrtlProtos.java: FirrtlProtos.java uses or overrides a deprecated API.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/src_managed/main/compiled_protobuf/firrtl/FirrtlProtos.java: Recompile with -Xlint:deprecation for details.
[success] Total time: 461 s (07:41), completed Oct 7, 2022, 7:41:58 AM
[mydev@fedora firrtl-master]$
```

...

errors and failures

```
...
/usr/share/verilator/include/verilated.cpp: In function ‘IData VL_FGETS_NI(std::string&, IData)’:
/usr/share/verilator/include/verilated.cpp:1318:36: error: ‘numeric_limits’ is not a member of ‘std’
 1318 |     return getLine(dest, fpi, std::numeric_limits<size_t>::max());
      |                                    ^~~~~~~~~~~~~~
/usr/share/verilator/include/verilated.cpp:1318:57: error: expected primary-expression before ‘>’ token
 1318 |     return getLine(dest, fpi, std::numeric_limits<size_t>::max());
      |                                                         ^
/usr/share/verilator/include/verilated.cpp:1318:60: error: ‘::max’ has not been declared; did you mean ‘std::max’?
 1318 |     return getLine(dest, fpi, std::numeric_limits<size_t>::max());
      |                                                           ^~
      |                                                           std::max
In file included from /usr/include/c++/12/algorithm:61,
                 from /usr/share/verilator/include/verilated_heavy.h:29,
                 from ./VMultiExtModuleTester.h:11,
                 from <command-line>:
/usr/include/c++/12/bits/stl_algo.h:5756:5: note: ‘std::max’ declared here
 5756 |     max(initializer_list<_Tp> __l, _Compare __comp)
      |     ^~
...
At global scope:
cc1plus: note: unrecognized command-line option ‘-Wno-undefined-bool-conversion’ may have been intended to silence earlier diagnostics
make: *** [/usr/share/verilator/include/verilated.mk:241: verilated.o] Error 1
make: *** Waiting for unfinished jobs....
[info] - should work
[info] Squeeze with disjoint intervals
[info] - MultiExtModuleTester should execute correctly *** FAILED ***
[info]   java.io.IOException: Cannot run program "./VMultiExtModuleTester" (in directory "test_run_dir/MultiExtModuleTester/20221007081355141127028308382819 78"): error=2, No such file or directory
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1143)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:75)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:106)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$anonfun$runBuffered$1(ProcessBuilderImpl.scala:154)
[info]   at scala.runtime.java8.JFunction0$mcI$sp.apply(JFunction0$mcI$sp.java:23)
[info]   at scala.sys.process.ProcessLogger$$anon$1.buffer(ProcessLogger.scala:103)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.runBuffered(ProcessBuilderImpl.scala:154)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$bang(ProcessBuilderImpl.scala:120)
[info]   at firrtl.util.BackendCompilationUtilities$.executeExpectingFailure(BackendCompilationUtilities.scala:179)
[info]   ...
[info]   Cause: java.io.IOException: error=2, No such file or directory
[info]   at java.base/java.lang.ProcessImpl.forkAndExec(Native Method)
[info]   at java.base/java.lang.ProcessImpl.<init>(ProcessImpl.java:319)
[info]   at java.base/java.lang.ProcessImpl.start(ProcessImpl.java:249)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1110)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:75)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:106)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$anonfun$runBuffered$1(ProcessBuilderImpl.scala:154)
[info]   at scala.runtime.java8.JFunction0$mcI$sp.apply(JFunction0$mcI$sp.java:23)
[info]   at scala.sys.process.ProcessLogger$$anon$1.buffer(ProcessLogger.scala:103)
[info]   ...
-----------------------------------------------------------------------------
Warning: 6 verification statements (assert, assume or cover) were removed when compiling to Verilog because the basic Verilog standard does not support them. If this was not intended, compile to System Veri
log instead using the `-X sverilog` compiler flag.
-----------------------------------------------------------------------------
...
[info] - should generate identical RTLIL for RotationCordic
[info] Run completed in 11 minutes, 56 seconds.
[info] Total number of tests run: 1910
[info] Suites: completed 221, aborted 0
[info] Tests: succeeded 1810, failed 100, canceled 0, ignored 12, pending 0
[info] *** 100 TESTS FAILED ***
[error] Failed tests:
[error]         firrtlTests.MultiExtModuleExecutionTest
...
[error]         firrtlTests.WriteFirstMemToggleSpecRL2
[error] (Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 1035 s (17:15), completed Oct 7, 2022, 8:25:48 AM
[mydev@fedora firrtl-master]$
```

fix the issue and rerun the tests

https://gitlab.com/wg1/jpeg-xl/-/issues/84

```
[mydev@fedora firrtl-master]$ sudo vim /usr/share/verilator/include/verilated.cpp
...
#include <utility>
#include <limits>

// clang-format off
...
```

```
CompilerAnnotation is deprecated since FIRRTL 1.4.0. Please use 'RunFirrtlTransformAnnotation(new firrtl.MinimumVerilogEmitter)' instead.
input = 0, expected = 0, expr = 0, equal = 1
[info] - should support xorreduce_zero
[info] Run completed in 13 minutes, 19 seconds.
[info] Total number of tests run: 1910
[info] Suites: completed 221, aborted 0
[info] Tests: succeeded 1859, failed 51, canceled 0, ignored 12, pending 0
[info] *** 51 TESTS FAILED ***
[error] Failed tests:
[error]         firrtlTests.stage.FirrtlMainSpec
[error]         firrtlTests.options.OptionParserSpec
[error]         firrtlTests.options.phases.WriteOutputAnnotationsSpec
[error] (Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 810 s (13:30), completed Oct 7, 2022, 9:06:37 AM
[mydev@fedora firrtl-master]$
```

- **Assembly**

```
[mydev@fedora firrtl-master]$ sbt assembly
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project firrtl-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/project
[info] loading settings for project firrtl from build.sbt ...
[info] set current project to firrtl (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/)
[info] Strategy 'discard' was applied to 17 files (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 4 files (Run the task at debug level to see details)
[success] Total time: 28 s, completed Oct 7, 2022, 9:24:37 AM
[mydev@fedora firrtl-master]$
```

```
[mydev@fedora firrtl-master]$ tree utils/
utils/
└── bin
    ├── firrtl
    ├── firrtl.jar
    └── firrtl-profiling
```

Publish

```
[mydev@fedora firrtl-master]$ sbt publishLocal
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project firrtl-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/project
[info] loading settings for project firrtl from build.sbt ...
[info] set current project to firrtl (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/)
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/firrtl_2.12-1.6-SNAPSHOT.pom
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/unidoc...
model contains 1204 documentable templates
[info] Main Scala API documentation successful.
[info] :: delivering :: edu.berkeley.cs#firrtl_2.12;1.6-SNAPSHOT :: 1.6-SNAPSHOT :: integration :: Fri Oct 07 09:34:31 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/firrtl-master/target/scala-2.12/ivy-1.6-SNAPSHOT.xml
[info]  published firrtl_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12/1.6-SNAPSHOT/poms/firrtl_2.12.pom
[info]  published firrtl_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12/1.6-SNAPSHOT/jars/firrtl_2.12.jar
[info]  published firrtl_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12/1.6-SNAPSHOT/srcs/firrtl_2.12-sources.jar
[info]  published firrtl_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12/1.6-SNAPSHOT/docs/firrtl_2.12-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12/1.6-SNAPSHOT/ivys/ivy.xml
[success] Total time: 271 s (04:31), completed Oct 7, 2022, 9:34:31 AM
[mydev@fedora firrtl-master]$
```

```
[mydev@fedora firrtl-master]$ tree ~/.ivy2/local/edu.berkeley.cs/firrtl_2.12
/home/mydev/.ivy2/local/edu.berkeley.cs/firrtl_2.12
└── 1.6-SNAPSHOT
    ├── docs
    │   ├── firrtl_2.12-javadoc.jar
    │   ├── firrtl_2.12-javadoc.jar.md5
    │   └── firrtl_2.12-javadoc.jar.sha1
    ├── ivys
    │   ├── ivy.xml
    │   ├── ivy.xml.md5
    │   └── ivy.xml.sha1
    ├── jars
    │   ├── firrtl_2.12.jar
    │   ├── firrtl_2.12.jar.md5
    │   └── firrtl_2.12.jar.sha1
    ├── poms
    │   ├── firrtl_2.12.pom
    │   ├── firrtl_2.12.pom.md5
    │   └── firrtl_2.12.pom.sha1
    └── srcs
        ├── firrtl_2.12-sources.jar
        ├── firrtl_2.12-sources.jar.md5
        └── firrtl_2.12-sources.jar.sha1
```

1.2 Treadle

Tetralogy

Code:

On master branch, last commit: 9de24c4bf46775338b9e9560fd1a29d0d6781fbe

- **Compile**

```
[mydev@fedora treadle-master]$ sbt compile
[info] [launcher] getting org.scala-sbt sbt 1.5.6  (this may take some time)...
java.lang.ClassCastException: class java.lang.UnsupportedOperationException cannot be cast to class xsbti.FullReload (java.lang.UnsupportedOperationException is in module java.base of loader 'bootstrap'; xs
bti.FullReload is in unnamed module of loader 'app')
        at sbt.internal.XMainConfiguration.run(XMainConfiguration.java:59)
        at sbt.xMain.run(Main.scala:46)
        at xsbt.boot.Launch$.$anonfun$run$1(Launch.scala:149)
        at xsbt.boot.Launch$.withContextLoader(Launch.scala:176)
        at xsbt.boot.Launch$.run(Launch.scala:149)
        at xsbt.boot.Launch$.$anonfun$apply$1(Launch.scala:44)
        at xsbt.boot.Launch$.launch(Launch.scala:159)
        at xsbt.boot.Launch$.apply(Launch.scala:44)
        at xsbt.boot.Launch$.apply(Launch.scala:21)
        at xsbt.boot.Boot$.runImpl(Boot.scala:78)
        at xsbt.boot.Boot$.run(Boot.scala:73)
        at xsbt.boot.Boot$.main(Boot.scala:21)
        at xsbt.boot.Boot.main(Boot.scala)
[error] [launcher] error during sbt launcher: java.lang.ClassCastException: class java.lang.UnsupportedOperationException cannot be cast to class xsbti.FullReload (java.lang.UnsupportedOperationException is
 in module java.base of loader 'bootstrap'; xsbti.FullReload is in unnamed module of loader 'app')
[mydev@fedora treadle-master]$
```

This is a known issue(https://github.com/sbt/sbt/issues/6925) in sbt 1.5.x, so just upgrade the sbt version and rebuild it:

```
[mydev@fedora treadle-master]$ git diff
diff --git a/project/build.properties b/project/build.properties
index bb3a9b7..c8fcab5 100644
--- a/project/build.properties
+++ b/project/build.properties
@@ -1 +1 @@
-sbt.version=1.5.6
+sbt.version=1.6.2
[mydev@fedora treadle-master]$
[mydev@fedora treadle-master]$ sbt compile
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project treadle-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/project
https://repo1.maven.org/maven2/com/eed3si9n/sbt-assembly_2.12_1.0/1.0.0/sbt-assembly-1.0.0.pom
  100.0% [##########] 2.4 KiB (1.3 KiB / s)
https://repo1.maven.org/maven2/org/scalameta/sbt-scalafmt_2.12_1.0/2.4.3/sbt-scalafmt-2.4.3.pom
  100.0% [##########] 2.5 KiB (1.3 KiB / s)
...
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/build.sbt:79: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www.s
cala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  scalacOptions in Compile in doc ++= Seq(
                 ^
[info] loading settings for project treadle from build.sbt ...
[info] set current project to treadle (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/)
[info] Executing in batch mode. For better performance use sbt's shell
[info] compiling 74 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/target/scala-2.12/classes ...
[info] Non-compiled module 'compiler-bridge_2.12' for Scala 2.12.14. Compiling...
[info]   Compilation completed in 55.235s.
[success] Total time: 174 s (02:54), completed Oct 7, 2022, 10:02:57 AM
[mydev@fedora treadle-master]$
```

Test

```
[mydev@fedora treadle-master]$ sbt test
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project treadle-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/project
[info] loading settings for project treadle from build.sbt ...
[info] set current project to treadle (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/)
[info] compiling 86 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/target/scala-2.12/test-classes ...
[info] PrintfOnDerivedClockSpec:
[info] - Printf in submodule in scope of withClock should appear in output
```

...

```
[info] BigIntGenerator
[info] - should return a bunch of BigInts
[info] - should return a allow negative  to positive range
[info] - should return a allow negative to negative range
[info] - should work with very big numbers
[info] - should work with very big numbers by specifying widths
[info] - should never repeat a value
[info] Run completed in 2 minutes, 11 seconds.
[info] Total number of tests run: 255
[info] Suites: completed 80, aborted 0
[info] Tests: succeeded 255, failed 0, canceled 0, ignored 3, pending 0
[info] All tests passed.
[success] Total time: 277 s (04:37), completed Oct 7, 2022, 10:14:08 AM
[mydev@fedora treadle-master]$
```

Assembly

```
[mydev@fedora treadle-master]$ sbt assembly
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project treadle-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/project
[info] loading settings for project treadle from build.sbt ...
[info] set current project to treadle (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/)
[warn] multiple main classes detected: run 'show discoveredMainClasses' to see the list
[info] Strategy 'discard' was applied to 23 files (Run the task at debug level to see details)
[info] Strategy 'filterDistinctLines' was applied to a file (Run the task at debug level to see details)
[info] Strategy 'rename' was applied to 4 files (Run the task at debug level to see details)
[success] Total time: 24 s, completed Oct 7, 2022, 10:19:18 AM
[mydev@fedora treadle-master]$
```

```
[mydev@fedora treadle-master]$ tree utils/
utils/
└── bin
    ├── treadle
    └── treadle.jar
```

Publish

```
[mydev@fedora treadle-master]$ sbt publishLocal
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project treadle-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/project
[info] loading settings for project treadle from build.sbt ...
[info] set current project to treadle (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/)
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/target/scala-2.12/treadle_2.12-1.6-SNAPSHOT.pom
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/target/scala-2.12/api...
[warn] multiple main classes detected: run 'show discoveredMainClasses' to see the list
model contains 390 documentable templates
[info] Main Scala API documentation successful.
[info] :: delivering :: edu.berkeley.cs#treadle_2.12;1.6-SNAPSHOT :: 1.6-SNAPSHOT :: integration :: Fri Oct 07 10:22:44 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/treadle-master/target/scala-2.12/ivy-1.6-SNAPSHOT.xml
[info]  published treadle_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12/1.6-SNAPSHOT/poms/treadle_2.12.pom
[info]  published treadle_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12/1.6-SNAPSHOT/jars/treadle_2.12.jar
[info]  published treadle_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12/1.6-SNAPSHOT/srcs/treadle_2.12-sources.jar
[info]  published treadle_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12/1.6-SNAPSHOT/docs/treadle_2.12-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12/1.6-SNAPSHOT/ivys/ivy.xml
[success] Total time: 123 s (02:03), completed Oct 7, 2022, 10:22:44 AM
[mydev@fedora treadle-master]$
```

```
[mydev@fedora treadle-master]$ tree /home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12
/home/mydev/.ivy2/local/edu.berkeley.cs/treadle_2.12
└── 1.6-SNAPSHOT
    ├── docs
    │   ├── treadle_2.12-javadoc.jar
    │   ├── treadle_2.12-javadoc.jar.md5
    │   └── treadle_2.12-javadoc.jar.sha1
    ├── ivys
    │   ├── ivy.xml
    │   ├── ivy.xml.md5
    │   └── ivy.xml.sha1
    ├── jars
    │   ├── treadle_2.12.jar
    │   ├── treadle_2.12.jar.md5
    │   └── treadle_2.12.jar.sha1
    ├── poms
    │   ├── treadle_2.12.pom
    │   ├── treadle_2.12.pom.md5
    │   └── treadle_2.12.pom.sha1
    └── srcs
        ├── treadle_2.12-sources.jar
        ├── treadle_2.12-sources.jar.md5
        └── treadle_2.12-sources.jar.sha1
```

1.3 Chisel3

Tetralogy

Code:

On master branch, last commit: 0ff99ca8d573e3487ef496a21c95d962689c3cba

- **Compile**

```
[mydev@fedora chisel3-master]$ sbt compile
[info] [launcher] getting org.scala-sbt sbt 1.5.8  (this may take some time)...
java.lang.ClassCastException: class java.lang.UnsupportedOperationException cannot be cast to class xsbti.FullReload (java.lang.UnsupportedOperationException is in module java.base of loader 'bootstrap'; xs
bti.FullReload is in unnamed module of loader 'app')
        at sbt.internal.XMainConfiguration.run(XMainConfiguration.java:59)
        at sbt.xMain.run(Main.scala:46)
        at xsbt.boot.Launch$.$anonfun$run$1(Launch.scala:149)
        at xsbt.boot.Launch$.withContextLoader(Launch.scala:176)
        at xsbt.boot.Launch$.run(Launch.scala:149)
        at xsbt.boot.Launch$.$anonfun$apply$1(Launch.scala:44)
        at xsbt.boot.Launch$.launch(Launch.scala:159)
        at xsbt.boot.Launch$.apply(Launch.scala:44)
        at xsbt.boot.Launch$.apply(Launch.scala:21)
        at xsbt.boot.Boot$.runImpl(Boot.scala:78)
        at xsbt.boot.Boot$.run(Boot.scala:73)
        at xsbt.boot.Boot$.main(Boot.scala:21)
        at xsbt.boot.Boot.main(Boot.scala)
[error] [launcher] error during sbt launcher: java.lang.ClassCastException: class java.lang.UnsupportedOperationException cannot be cast to class xsbti.FullReload (java.lang.UnsupportedOperationException is
 in module java.base of loader 'bootstrap'; xsbti.FullReload is in unnamed module of loader 'app')
[mydev@fedora chisel3-master]$
```

The same sbt version issue as Treadle, so upgrade the sbt version and rebuild it:

```
[mydev@fedora chisel3-master]$ git diff
diff --git a/project/build.properties b/project/build.properties
index e64c208f..c8fcab54 100644
--- a/project/build.properties
+++ b/project/build.properties
@@ -1 +1 @@
-sbt.version=1.5.8
+sbt.version=1.6.2
[mydev@fedora chisel3-master]$
[mydev@fedora chisel3-master]$ sbt compile
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project chisel3-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/project
[info] Updating
https://repo1.maven.org/maven2/ch/epfl/scala/sbt-scalafix_2.12_1.0/0.9.33/sbt-scalafix-0.9.33.pom
  100.0% [##########] 3.3 KiB (1.8 KiB / s)
https://repo1.maven.org/maven2/org/scalameta/sbt-mdoc_2.12_1.0/2.3.2/sbt-mdoc-2.3.2.pom
  100.0% [##########] 2.9 KiB (1.6 KiB / s)
...
```

```
[info] Resolved  dependencies
[info] Fetching artifacts of
https://repo1.maven.org/maven2/com/headius/backport9/1.2/backport9-1.2.jar
  100.0% [##########] 12.5 KiB (45.5 KiB / s)
https://repo1.maven.org/maven2/ch/epfl/scala/sbt-scalafix_2.12_1.0/0.9.33/sbt-scalafix-0.9.33.jar
  100.0% [##########] 263.0 KiB (212.6 KiB / s)
https://repo1.maven.org/maven2/org/jruby/jruby/9.2.7.0/jruby-9.2.7.0.jar
  100.0% [##########] 41.3 KiB (42.5 KiB / s)
```

...

```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/src/main/scala/chisel3/util/experimental/LoadMemoryTransform.scala:204:33: object LowForm in package firrtl is deprecated (since FIRRTL 1.
3): Mix-in the DependencyAPIMigration trait into your Transform and specify its Dependency API dependencies. See: https://bit.ly/2Voppre
[warn]   def outputForm: CircuitForm = LowForm
[warn]                                 ^
[warn] 21 warnings found
[success] Total time: 383 s (06:23), completed Oct 7, 2022, 10:45:42 AM
[mydev@fedora chisel3-master]$ _
```

- **Test**

```
[mydev@fedora chisel3-master]$ sbt test
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project chisel3-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/project
[info] loading settings for project chisel from build.sbt ...
[info] set current project to chisel3 (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/)
[info] compiling 166 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/target/scala-2.12/test-classes ...
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/src/test/scala/chiselTests/CompatibilitySpec.scala:91:51: Type parameter should not be specified because it will be erased at runtime, ple
ase use _ instead.  Note that in future version of ScalaTest this will give a compiler error.
[warn]       new ArbiterIO(data, 2) shouldBe a[ArbiterIO[UInt]]
[warn]                                                ^
```

...

```
[info] - It should be possible to bulk connect a Vec and a Seq
[error] Vec.scala:491: Vec and Seq being bulk connected have different lengths! in class chiselTests.VecSpec$$anon$10
[error] There were 1 error(s) during hardware elaboration.
[info] - Bulk connecting a Vec and Seq of different sizes should report a ChiselException
[info] - It should be possible to initialize a Vec with DontCare
[info] - Indexing a Chisel type Vec by a hardware type should give a sane error message
[info] - reduceTree should preserve input/output type
[info] - Vecs of empty Bundles and empty Records should work
[info] Run completed in 1 hour, 44 minutes, 20 seconds.
[info] Total number of tests run: 1217
[info] Suites: completed 172, aborted 0
[info] Tests: succeeded 1185, failed 32, canceled 0, ignored 27, pending 0
[info] *** 32 TESTS FAILED ***
[error] Failed tests:
[error]         chiselTests.StrongEnumSpec
[error]         circtTests.stage.ChiselStageSpec
[error]         chiselTests.TraceSpec
[error]         circtTests.stage.CIRCTStageSpec
[error]         chiselTests.stage.ChiselMainSpec
[error] (Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 6666 s (01:51:06), completed Oct 7, 2022, 12:49:06 PM
[mydev@fedora chisel3-master]$
```

- **Assembly**

Not a valid command(you may check $SRC_CHISEL3/build.sbt)

Publish

```
[mydev@fedora chisel3-master]$ sbt publishLocal
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project chisel3-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/project
[info] loading settings for project chisel from build.sbt ...
[info] set current project to chisel3 (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/)
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/macros/target/scala-2.12/chisel3-macros_2.12-3.6-SNAPSHOT.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/plugin/target/scala-2.12.17/chisel3-plugin_2.12.17-3.6-SNAPSHOT.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/core/target/scala-2.12/chisel3-core_2.12-3.6-SNAPSHOT.pom
[info] Wrote /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/target/scala-2.12/chisel3_2.12-3.6-SNAPSHOT.pom
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/plugin/target/scala-2.12.17/api...
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/macros/target/scala-2.12/api...
[info] Main Scala API documentation to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/core/target/scala-2.12/api...
[info] Updating
https://repo1.maven.org/maven2/org/scalameta/mdoc_2.12/2.3.2/mdoc_2.12-2.3.2.pom
  100.0% [##########] 4.1 KiB (1.4 KiB / s)
```

...

```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/core/src/main/scala/chisel3/VerificationStatement.scala:53:3: Could not find any member to link for "printf.apply(fmt:Printable)".
[warn]   /** Checks for a condition to be valid in the circuit at all times. If the
[warn]   ^
[warn] 85 warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: edu.berkeley.cs#chisel3_2.12;3.6-SNAPSHOT :: 3.6-SNAPSHOT :: integration :: Fri Oct 07 13:14:09 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/Chisel/chisel3-master/target/scala-2.12/ivy-3.6-SNAPSHOT.xml
[info]  published chisel3_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/chisel3_2.12/3.6-SNAPSHOT/poms/chisel3_2.12.pom
[info]  published chisel3_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/chisel3_2.12/3.6-SNAPSHOT/jars/chisel3_2.12.jar
[info]  published chisel3_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/chisel3_2.12/3.6-SNAPSHOT/srcs/chisel3_2.12-sources.jar
[info]  published chisel3_2.12 to /home/mydev/.ivy2/local/edu.berkeley.cs/chisel3_2.12/3.6-SNAPSHOT/docs/chisel3_2.12-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/edu.berkeley.cs/chisel3_2.12/3.6-SNAPSHOT/ivys/ivy.xml
[success] Total time: 286 s (04:46), completed Oct 7, 2022, 1:14:09 PM
[mydev@fedora chisel3-master]$
```

```
[mydev@fedora chisel3-master]$ tree -L 2 /home/mydev/.ivy2/local/edu.berkeley.cs
/home/mydev/.ivy2/local/edu.berkeley.cs
├── chisel3_2.12
│   └── 3.6-SNAPSHOT
├── chisel3-core_2.12
│   └── 3.6-SNAPSHOT
├── chisel3-macros_2.12
│   └── 3.6-SNAPSHOT
├── chisel3-plugin_2.12.17
│   └── 3.6-SNAPSHOT
├── firrtl_2.12
│   └── 1.6-SNAPSHOT
└── treadle_2.12
    └── 1.6-SNAPSHOT
```

2) SpinalHDL

2.1 SpinalHDL

Tetralogy

Code:

On dev branch, last commit: 530a200105546759f2650bd7c9c60fa468952dbe

- **Compile**

```
[mydev@fedora SpinalHDL-dev]$ sbt compile
[info] [launcher] getting org.scala-sbt sbt 1.6.0  (this may take some time)...
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] compiling 1 Scala source to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project/target/scala-2.12/sbt-1.0/classes ...
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
...
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompilation.java: Some input files use or override a deprecated API.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompilation.java: Recompile with -Xlint:deprecation for details.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompiler.java: DynamicCompiler.java uses unchecked or unsafe operations.
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/main/java/DynamicCompiler.java: Recompile with -Xlint:unchecked for details.
[success] Total time: 764 s (12:44), completed Oct 7, 2022, 1:50:31 PM
[mydev@fedora SpinalHDL-dev]$
```

- **Test**

```
[mydev@fedora SpinalHDL-dev]$ git diff
diff --git a/build.sbt b/build.sbt
index b275d8cac..3086f45c4 100644
--- a/build.sbt
+++ b/build.sbt
@@ -14,13 +14,13 @@ val defaultSettings = Defaults.coreDefaultSettings ++ xerial.sbt.Sonatype.sonaty
   fork := true,

   //Enable parallel tests
-  Test / testForkedParallel := true,
-  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
+  Test / testForkedParallel := false,
+//  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
 //    for(i <- 0 until 4) yield {
 //      Group("g" + i,  group.tests.zipWithIndex.filter(_._2 % 4 == i).map(_._1), SubProcess(ForkOptions()))
 //    }
-    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
-  },
+//    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
+//  },
 //  concurrentRestrictions := Seq(Tags.limit(Tags.ForkedTestGroup, 4)),

   libraryDependencies += "org.scala-lang" % "scala-library" % scalaVersion.value,
[mydev@fedora SpinalHDL-dev]$
```

```
[mydev@fedora SpinalHDL-dev]$ sbt test
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
```

```
...
[Info] Test 'test' was reallocated as 'test_9' to avoid collision
[Progress] Start SpinalSimVerilatorIoTestTop test_9 simulation with seed 218567579
#
# If you would like to submit a bug report, please visit:
#   https://github.com/oracle/graal/issues
# The crash happened outside the Java Virtual Machine in native code.
# See problematic frame for where to report the bug.
#
- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tmp/job_201/unamed.v:23: Verilog $finish
Exception in thread "Thread-8" java.io.EOFException
  | => tat java.base/java.io.ObjectInputStream$BlockDataInputStream.peekByte(ObjectInputStream.java:3239)
        at java.base/java.io.ObjectInputStream.readObject0(ObjectInputStream.java:1711)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:538)
        at java.base/java.io.ObjectInputStream.readObject(ObjectInputStream.java:496)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1$React.react(Framework.scala:839)
        at org.scalatest.tools.Framework$ScalaTestRunner$Skeleton$1.run(Framework.scala:828)
        at java.base/java.lang.Thread.run(Thread.java:1589)
[info] Run completed in 1 hour, 31 minutes, 54 seconds.
[info] Total number of tests run: 478
[info] Suites: completed 48, aborted 0
[info] Tests: succeeded 470, failed 8, canceled 0, ignored 0, pending 0
[info] *** 8 TESTS FAILED ***
```

```
...
[error] Error during tests:
[error]         Running java with options -classpath /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/target/scala-2.11/test-classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/Spi
nalHDL-dev/tester/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/sim/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/t
arget/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/idslplugin/target/scala-2.11/spinalhdl-idsl-plugin_2.11-dev.jar:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/Spina
lHDL-dev/idslpayload/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/deb
ugger/target/scala-2.11/classes:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/demo/target/scala-2.11/classes:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala
-library/2.11.12/scala-library-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest_2.11/3.2.5/scalatest_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.
maven.org/maven2/commons-io/commons-io/2.4/commons-io-2.4.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/openhft/affinity/3.21ea1.1/affinity-3.21ea1.1.jar:/home/mydev/.cache/coursier/v1
/https/repo1.maven.org/maven2/org/slf4j/slf4j-simple/1.7.25/slf4j-simple-1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/oshi/oshi-core/5.2.0/oshi-core-5.2.0.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-reflect/2.11.12/scala-reflect-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/github/scopt/scopt_2.11/3.7.1
/scopt_2.11-3.7.1.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/lihaoyi/sourcecode_2.11/0.2.7/sourcecode_2.11-0.2.7.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/
github/purejavacomm/purejavacomm/1.0.2.RELEASE/purejavacomm-1.0.2.RELEASE.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/liftweb/lift-json_2.11/3.4.3/lift-json_2.11-3.4.3.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-core_2.11/3.2.5/scalatest-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-fe
aturespec_2.11/3.2.5/scalatest-featurespec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-flatspec_2.11/3.2.5/scalatest-flatspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-freespec_2.11/3.2.5/scalatest-freespec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-funsuite_2.11/3.2.5/scalatest-funsuite_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-funspec_2.11/3.2.5/scalatest-funspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-propspec_2.11/3.2.5/scalatest-propspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-refspec_2.11/3.2.5/scalatest-refspec_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-wordspec_2.11/3.2.5/scalatest-wordspec_2.11-3.2.5.jar:/home/myde
v/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-diagrams_2.11/3.2.5/scalatest-diagrams_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scal
atest-matchers-core_2.11/3.2.5/scalatest-matchers-core_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-shouldmatchers_2.11/3.2.5/scalatest-shouldmatchers_2
.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-mustmatchers_2.11/3.2.5/scalatest-mustmatchers_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.mav
en.org/maven2/org/slf4j/slf4j-api/1.7.25/slf4j-api-1.7.25.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/net/java/dev/jna/jna/5.5.0/jna-5.5.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.
maven.org/maven2/net/java/dev/jna/jna-platform/5.5.0/jna-platform-5.5.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/jetbrains/annotations/19.0.0/annotations-19.0.0.jar:/home/mydev/.c
ache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scala-compiler/2.11.12/scala-compiler-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/scalap/2.11.12/scala
p-2.11.12.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/com/thoughtworks/paranamer/paranamer/2.8/paranamer-2.8.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lan
g/modules/scala-xml_2.11/1.2.0/scala-xml_2.11-1.2.0.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scalatest/scalatest-compatible/3.2.5/scalatest-compatible-3.2.5.jar:/home/mydev/.cache
/coursier/v1/https/repo1.maven.org/maven2/org/scalactic/scalactic_2.11/3.2.5/scalactic_2.11-3.2.5.jar:/home/mydev/.cache/coursier/v1/https/repo1.maven.org/maven2/org/scala-lang/modules/scala-parser-combinat
ors_2.11/1.0.4/scala-parser-combinators_2.11-1.0.4.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-agent-1.6.0.jar:/home/mydev/.sbt/boot/scala-2.12.15/org.scala-sbt/sbt/1.6.0/test-inter
face-1.0.jar sbt.ForkMain 42453 failed with exit code 134
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 5772 s (01:36:12), completed Oct 8, 2022, 6:16:44 AM
[mydev@fedora SpinalHDL-dev]$
```

- **Assembly**

```
[mydev@fedora SpinalHDL-dev]$ git diff
diff --git a/build.sbt b/build.sbt
index b275d8cac..942e75017 100644
--- a/build.sbt
+++ b/build.sbt
@@ -13,14 +13,17 @@ val defaultSettings = Defaults.coreDefaultSettings ++ xerial.sbt.Sonatype.sonaty
   baseDirectory in test := file("/out/"),
   fork := true,

+  concurrentRestrictions in Global += Tags.limit(Tags.CPU, 2),
+  concurrentRestrictions in Global += Tags.limit(Tags.Test, 1),
+
   //Enable parallel tests
-  Test / testForkedParallel := true,
-  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
+//  Test / testForkedParallel := false,
+//  testGrouping in Test := (testGrouping in Test).value.flatMap { group =>
 //   for(i <- 0 until 4) yield {
 //     Group("g" + i,  group.tests.zipWithIndex.filter(_._2 % 4 == i).map(_._1), SubProcess(ForkOptions()))
 //   }
-    Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
-  },
+//   Seq(Group("g",  group.tests, SubProcess(ForkOptions())))
+//  },
 //  concurrentRestrictions := Seq(Tags.limit(Tags.ForkedTestGroup, 4)),

   libraryDependencies += "org.scala-lang" % "scala-library" % scalaVersion.value,
[mydev@fedora SpinalHDL-dev]$
```

```
[mydev@fedora SpinalHDL-dev]$ sbt assembly
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13: warning: method in in trait ScopingSetting is deprecated (since 1.5.0): `in` is deprecated; migrate to slash syntax - https://www
.scala-sbt.org/1.x/docs/Migrating-from-sbt-013x.html#slash
  baseDirectory in test := file("/out/"),
                ^
```

...

```
[info] - ghdl_testRecompile2
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 12:25:01
[Progress] at 2714.642 : Elaborate components
[Progress] at 2714.660 : Checks and transforms
[Progress] at 2714.662 : Generate VHDL
[Done] at 2714.692
[Info] Workspace 'unamed' was reallocated as 'unamed_46' to avoid collision
[Progress] Simulation workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_46
[Progress] GHDL compilation started
[Progress] GHDL compilation done in 0.689 ms
loading VPI module '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/././simWorkspace/.pluginsCachePath/vpi_ghdl.vpi'
VPI module loaded!
[Progress] Start unamed test simulation with seed 430714424
Shared memory key : SpinalHDL_0_179_1334276245_-1747164204_1665257102580_-390283830068594317
Start of simulation
End of simulation
[Done] Simulation done in 36.295 ms
```

...

```
[info] - verilator_simulate
[info] FormalFifoCCTester:
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 14:44:51
[Progress] at 11104.734 : Elaborate components
[Progress] at 11104.786 : Checks and transforms
[Progress] at 11104.812 : Generate Verilog
[Warning] 36 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 11104.862
[Info] Workspace 'unamed' was reallocated as 'unamed_18' to avoid collision
[Progress] Formal verification workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_18
[Progress] Yosys compilation started
[Progress] Yosys compilation done in 1.600 ms
[Progress] Start unamed formal verification with formal.
[info] - formal_fifo-verify fast pop *** FAILED **
[info]   java.io.IOException: Cannot run program "sby" (in directory "/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/./simWorkspace/unamed_18"): error=2, No such file or directory
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1143)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[Runtime] SpinalHDL dev    git head : 530a200105546759f2650bd7c9c60fa468952dbe
[Runtime] JVM max memory : 1958.0MiB
[Runtime] Current date : 2022.10.08 14:44:51
[Progress] at 11104.914 : Elaborate components
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.runBuffered(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.$bang(ProcessBuilderImpl.scala:114)
[info]   at spinal.core.formal.SymbiYosysBackend.doVerify(SymbiYosysBackend.scala:164)
[info]   ...
[info]   Cause: java.io.IOException: error=2, No such file or directory
[info]   at java.base/java.lang.ProcessImpl.forkAndExec(Native Method)
[info]   at java.base/java.lang.ProcessImpl.<init>(ProcessImpl.java:319)
[info]   at java.base/java.lang.ProcessImpl.start(ProcessImpl.java:249)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1110)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder$$anonfun$runBuffered$1.apply(ProcessBuilderImpl.scala:148)
[info]   at spinal.core.formal.SymbiYosysBackend$Logger.buffer(SymbiYosysBackend.scala:157)
[info]   ...
[Progress] at 11104.943 : Checks and transforms
[Progress] at 11104.963 : Generate Verilog
[Warning] 36 signals were pruned. You can call printPruned on the backend report to get more informations.
[Done] at 11105.004
```

```
Sim speed : 0.853000 khz
Sim speed : 0.990000 khz
 20710.00ns INFO     cocotb.Axi4SharedOnChipRamTester   Cocotb test done
 20710.00ns INFO     cocotb.regression                  test1 passed
 20710.00ns INFO     cocotb.regression                  **************************************************************************************
                                                        ** TEST                                STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        **************************************************************************************
                                                        ** Axi4SharedOnChipRamTester.test1   PASS       20710.00          25.55        810.44  **
                                                        **************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0                20710.00          25.59        809.36  **
                                                        **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester'

/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:12: DeprecationWarning: Use of attribute 'log' is deprecat
ed, use '_log' instead
  dut.log.info("Cocotb test boot")
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:17: DeprecationWarning: cocotb.fork has been deprecated in
 favor of cocotb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(ClockDomainAsyncReset(dut.clk, dut.reset))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:89: DeprecationWarning: Setting values on handles using the ``handle <= value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  reset <= 1
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:90: DeprecationWarning: Setting values on handles using the ``handle <= value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  clk <= 0
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4SharedOnChipRamTester/Axi4SharedOnChipRamTester.py:18: DeprecationWarning: cocotb.fork has been deprecated in
 favor of cocotb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(simulationSpeedPrinter(dut.clk))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/Stream.py:130: DeprecationWarning: cocotb.fork has been deprecated in favor of cocotb.start_soon and cocotb.st
art.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(self.stim())
```

```
[info] - cocotbVerilog
- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tmp/job_201/unamed.v:23: Verilog $finish
[info] Run completed in 3 hours, 6 minutes, 30 seconds.
[info] Total number of tests run: 862
[info] Suites: completed 120, aborted 0
[info] Tests: succeeded 841, failed 21, canceled 0, ignored 0, pending 0
[info] *** 21 TESTS FAILED ***
[error] Failed tests:
[error]         spinal.tester.scalatest.FormalSimpleTester
[error]         spinal.tester.scalatest.FormalFifoTester
[error]         spinal.tester.scalatest.FormalForkTester
[error]         spinal.tester.scalatest.Axi4StreamWidthAdapterTester
[error]         spinal.tester.scalatest.FormalDispatcherSequencialTester
[error]         spinal.tester.scalatest.FormalStreamExtender
[error]         spinal.tester.scalatest.FormalAxi4DownsizerTester
[error]         spinal.tester.scalatest.FormalHistoryModifyableTester
[error]         spinal.tester.scalatest.FormalDeMuxTester
[error]         spinal.tester.scalatest.FormalMuxTester
[error]         spinal.tester.scalatest.FormalFifoCCTester
[error] (tester / Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 11351 s (03:09:11), completed Oct 8, 2022, 2:46:14 PM
[mydev@fedora SpinalHDL-dev]$
```

Publish

```
[mydev@fedora SpinalHDL-dev]$ sbt publishLocal
[info] welcome to sbt 1.6.0 (GraalVM Community Java 19)
[info] loading settings for project spinalhdl-dev-build from plugin.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/project
[info] loading settings for project all from build.sbt ...
[info] set current project to SpinalHDL-all (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/)
[warn] there are 9 keys that are not used by any other settings/tasks:
[warn]
[warn] * all / test / baseDirectory
[warn]   +- /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/build.sbt:13
[warn] * core / test / baseDirectory
```

...

```
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/src/main/scala/spinal/lib/bus/regif/BusIfAdapter/WishboneBusInterface.scala:5:37: imported `ClassName' is permanently hidden by defi
nition of object ClassName in package regif
[warn] import spinal.lib.bus.regif.{BusIf, ClassName}
[warn]                                    ^
[warn] 11 warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-core_2.11;dev :: dev :: release :: Sat Oct 08 15:00:10 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/core/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/poms/spinalhdl-core_2.11.pom
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/jars/spinalhdl-core_2.11.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/srcs/spinalhdl-core_2.11-sources.jar
[info]  published spinalhdl-core_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/docs/spinalhdl-core_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11/dev/ivys/ivy.xml
[warn] there were 33 deprecation warnings; re-run with -deprecation for details
[warn] there were 5 feature warnings; re-run with -feature for details
model contains 1670 documentable templates
[warn] 5 warnings found
[info] Main Scala API documentation successful.
[info] :: delivering :: com.github.spinalhdl#spinalhdl-lib_2.11;dev :: dev :: release :: Sat Oct 08 15:03:59 PDT 2022
[info]  delivering ivy file to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/lib/target/scala-2.11/ivy-dev.xml
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/poms/spinalhdl-lib_2.11.pom
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/jars/spinalhdl-lib_2.11.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/srcs/spinalhdl-lib_2.11-sources.jar
[info]  published spinalhdl-lib_2.11 to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/docs/spinalhdl-lib_2.11-javadoc.jar
[info]  published ivy to /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-lib_2.11/dev/ivys/ivy.xml
[success] Total time: 529 s (08:49), completed Oct 8, 2022, 3:03:59 PM
[mydev@fedora SpinalHDL-dev]$
```

```
[mydev@fedora SpinalHDL-dev]$ tree -L 2 /home/mydev/.ivy2/local/com.github.spinalhdl
/home/mydev/.ivy2/local/com.github.spinalhdl
├── spinalhdl-core_2.11
│   └── dev
├── spinalhdl-idsl-payload_2.11
│   └── dev
├── spinalhdl-idsl-plugin_2.11
│   └── dev
├── spinalhdl-lib_2.11
│   └── dev
└── spinalhdl-sim_2.11
    └── dev
```

```
[mydev@fedora SpinalHDL-dev]$ tree /home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
/home/mydev/.ivy2/local/com.github.spinalhdl/spinalhdl-core_2.11
└── dev
    ├── docs
    │   ├── spinalhdl-core_2.11-javadoc.jar
    │   ├── spinalhdl-core_2.11-javadoc.jar.md5
    │   └── spinalhdl-core_2.11-javadoc.jar.sha1
    ├── ivys
    │   ├── ivy.xml
    │   ├── ivy.xml.md5
    │   └── ivy.xml.sha1
    ├── jars
    │   ├── spinalhdl-core_2.11.jar
    │   ├── spinalhdl-core_2.11.jar.md5
    │   └── spinalhdl-core_2.11.jar.sha1
    ├── poms
    │   ├── spinalhdl-core_2.11.pom
    │   ├── spinalhdl-core_2.11.pom.md5
    │   └── spinalhdl-core_2.11.pom.sha1
    └── srcs
        ├── spinalhdl-core_2.11-sources.jar
        ├── spinalhdl-core_2.11-sources.jar.md5
        └── spinalhdl-core_2.11-sources.jar.sha1
```

2.2 VexRiscv

Tetralogy

Code:

On master branch, last commit: 7b9891829a3498c0178eaca660ab95cfc8f93390

- **Compile**

```
[mydev@fedora VexRiscv-master]$ sbt compile
downloading sbt launcher 1.7.2
copying runtime jar...
[info] [launcher] getting org.scala-sbt sbt 1.4.7  (this may take some time)...
[info] [launcher] getting Scala 2.12.12 (for sbt)...
java.lang.UnsupportedOperationException: The Security Manager is deprecated and will be removed in a future release
        at java.base/java.lang.System.setSecurityManager(System.java:423)
        at sbt.TrapExit$.installManager(TrapExit.scala:54)
        at sbt.StandardMain$.runManaged(Main.scala:187)
        at sbt.xMain$.$anonfun$run$8(Main.scala:102)
        at scala.util.DynamicVariable.withValue(DynamicVariable.scala:62)
        at scala.Console$.withIn(Console.scala:230)
        at sbt.internal.util.Terminal$.withIn(Terminal.scala:560)
        at sbt.internal.util.Terminal$.$anonfun$withStreams$1(Terminal.scala:350)
        at scala.util.DynamicVariable.withValue(DynamicVariable.scala:62)
        at scala.Console$.withOut(Console.scala:167)
        at sbt.internal.util.Terminal$.$anonfun$withOut$2(Terminal.scala:550)
        at scala.util.DynamicVariable.withValue(DynamicVariable.scala:62)
        at scala.Console$.withErr(Console.scala:196)
        at sbt.internal.util.Terminal$.withOut(Terminal.scala:550)
        at sbt.internal.util.Terminal$.withStreams(Terminal.scala:350)
        at sbt.xMain$.run(Main.scala:86)
        at java.base/jdk.internal.reflect.DirectMethodHandleAccessor.invoke(DirectMethodHandleAccessor.java:104)
        at java.base/java.lang.reflect.Method.invoke(Method.java:578)
        at sbt.internal.XMainConfiguration.run(XMainConfiguration.scala:83)
        at sbt.xMain.run(Main.scala:46)
        at xsbt.boot.Launch$.$anonfun$run$1(Launch.scala:149)
        at xsbt.boot.Launch$.withContextLoader(Launch.scala:176)
        at xsbt.boot.Launch$.run(Launch.scala:149)
        at xsbt.boot.Launch$.$anonfun$apply$1(Launch.scala:44)
        at xsbt.boot.Launch$.launch(Launch.scala:159)
        at xsbt.boot.Launch$.apply(Launch.scala:44)
        at xsbt.boot.Launch$.apply(Launch.scala:21)
        at xsbt.boot.Boot$.runImpl(Boot.scala:78)
        at xsbt.boot.Boot$.run(Boot.scala:73)
        at xsbt.boot.Boot$.main(Boot.scala:21)
        at xsbt.boot.Boot.main(Boot.scala)
[error] [launcher] error during sbt launcher: java.lang.UnsupportedOperationException: The Security Manager is deprecated and will be removed in a future release
[mydev@fedora VexRiscv-master]$
```

The similar sbt version issue as before, so upgrade the sbt version and rebuild it:

```
[mydev@fedora VexRiscv-master]$ git diff
diff --git a/project/build.properties b/project/build.properties
index 0b2e09c..c8fcab5 100644
--- a/project/build.properties
+++ b/project/build.properties
@@ -1 +1 @@
-sbt.version=1.4.7
+sbt.version=1.6.2
[mydev@fedora VexRiscv-master]$
```

```
[mydev@fedora VexRiscv-master]$ sbt compile
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project vexriscv-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/project
[info] loading settings for project root from build.sbt ...
[info] set current project to VexRiscv (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/)
[info] Executing in batch mode. For better performance use sbt's shell
[info] compiling 91 Scala sources to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/target/scala-2.11/classes ...
[warn] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/src/main/scala/vexriscv/VexRiscv.scala:36:17: match may not be exhaustive.
[warn] It would fail on the following input: None
[warn]     plugins.find(_.getClass == clazz) match {
[warn]                 ^
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/src/main/scala/vexriscv/demo/smp/VexRiscvSmpLitexMpCluster.scala:1:1:
[info] Found names but no class, trait or object is defined in the compilation unit.
[info] The incremental compiler cannot record the dependency information in such case.
[info] Some errors like unused import referring to a non-existent class might not be reported.
[info]
[info] package vexriscv.demo.smp
[info] ^
[info] /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/src/main/scala/vexriscv/demo/smp/VexRiscvSmpLitexMpCluster.scala:1:1:
[info] Found top level imports but no class, trait or object is defined in the compilation unit.
[info] The incremental compiler cannot record the dependency information in such case.
[info] Some errors like unused import referring to a non-existent class might not be reported.
[info]
[info] package vexriscv.demo.smp
[info] ^
[warn] there were 40 deprecation warnings; re-run with -deprecation for details
[warn] there were two feature warnings; re-run with -feature for details
[warn] three warnings found
[success] Total time: 295 s (04:55), completed Oct 8, 2022, 3:45:44 PM
[mydev@fedora VexRiscv-master]$
```

- **Test**

```
[mydev@fedora VexRiscv-master]$ sbt test
[info] welcome to sbt 1.6.2 (GraalVM Community Java 19)
[info] loading settings for project vexriscv-master-build from plugins.sbt ...
[info] loading project definition from /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/project
[info] loading settings for project root from build.sbt ...
[info] set current project to VexRiscv (in build file:/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/)
[info] compiling 9 Scala sources and 1 Java source to /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/target/scala-2.11/test-classes ...
[warn] there were two deprecation warnings; re-run with -deprecation for details
[warn] one warning found
Seed=-8534522807158069343
[info] TestIndividualFeatures:
MAIN_SEED=-8534522807158069343
```

...

```
make  -j1 -C obj_dir/ -f VVexRiscv.mk VVexRiscv
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/simWorkspace/test_id_0_/obj_dir'
g++  -I.  -MMD -I/usr/share/verilator/include -I/usr/share/verilator/include/vltstd -DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -DVM_TRACE_FST=1 -faligned-new -fcf-protection=none -Wno-bool-operation -Wno-sign-c
ompare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-unused-parameter -Wno-unused-variable -Wno-shadow     -std=c++11 -DREGRESSION_PATH=\"../../src/test/cpp/regression/\" -DIBUS_SIMPLE -DIBUS_DATA_WI
DTH=32 -DDBUS_LOAD_DATA_WIDTH=32 -DDBUS_STORE_DATA_WIDTH=32 -DDBUS_SIMPLE -DREDO=10 -pthread -Wno-unused-result -DTHREAD_COUNT=1 -O3 -DCONCURRENT_OS_EXECUTIONS -DLINUX_REGRESSION -DARCH_LINUX=\"rv32ima\" -D
VMLINUX=\"../../resources/VexRiscvRegressionData/sim/linux/rv32ima/Image\" -DDTB=\"../../resources/VexRiscvRegressionData/sim/linux/rv32ima/rv32.dtb\" -DRAMDISK=\"../../resources/VexRiscvRegressionData/sim/
g++  -I.  -MMD -I/usr/share/verilator/include -I/usr/share/verilator/include/vltstd -DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -DVM_TRACE_FST=1 -faligned-new -fcf-protection=none -Wno-bool-operation -Wno-sign-c
ompare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-unused-parameter -Wno-unused-variable -Wno-shadow     -std=c++11 -DREGRESSION_PATH=\"../../src/test/cpp/regression/\" -DIBUS_SIMPLE -DIBUS_DATA_WI
DTH=32 -DDBUS_LOAD_DATA_WIDTH=32 -DDBUS_STORE_DATA_WIDTH=32 -DDBUS_SIMPLE -DREDO=10 -pthread -Wno-unused-result -DTHREAD_COUNT=1 -O3 -DCONCURRENT_OS_EXECUTIONS -DLINUX_REGRESSION -DARCH_LINUX=\"rv32ima\" -D
VMLINUX=\"../../resources/VexRiscvRegressionData/sim/linux/rv32ima/Image\" -DDTB=\"../../resources/VexRiscvRegressionData/sim/linux/rv32ima/rv32.dtb\" -DRAMDISK=\"../../resources/VexRiscvRegressionData/sim/
linux/rv32ima/rootfs.cpio\" -DEMULATOR=\"../../resources/VexRiscvRegressionData/sim/linux/emulator/emulator.bin\" -DCOREMARK -DWITH_RISCV_REF -DTIMER_INTERRUPT -DEXTERNAL_INTERRUPT -DSUPERVISOR -DDHRYSTONE
-DSTALL=1 -DSEED=846653699 -DTRACE -DCSR -DLRSC -DISA_TEST -DMMU -DMUL -DDIV -DDEBUG_PLUGIN -DDEBUG_PLUGIN_STD -DTRACE_START=100000000000ll -DFREERTOS -DFREERTOS_COUNT=0 -DZEPHYR -DZEPHYR_COUNT=4  -std=gnu+
+14 -Os -c -o main.o ../main.cpp
../main.cpp: In member function ‘virtual void IBusSimple::postCycle()’:
../main.cpp:23:42: error: too few arguments to function ‘IData VL_RANDOM_I(int)’
   23 | #define VL_RANDOM_I_WIDTH(w) (VL_RANDOM_I() & (1l << w)-1l)
      |                                          ~~~~~~~~~~~^~
../main.cpp:2057:52: note: in expansion of macro ‘VL_RANDOM_I_WIDTH’
 2057 |                 if(rPtr != wPtr && (!ws->iStall || VL_RANDOM_I_WIDTH(7) < 100)){
      |                                                    ^~~~~~~~~~~~~~~~~
In file included from /usr/share/verilator/include/verilated_heavy.h:27,
                 from ./VVexRiscv.h:11,
                 from ../main.cpp:1:
/usr/share/verilator/include/verilated.h:656:14: note: declared here
```

...

```
[Progress] Simulation workspace in /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/VexRiscv-master/./simWorkspace/FpuCore
[Progress] Verilator compilation started
[Progress] Verilator compilation done in 16269.791 ms
[Progress] Start FpuCore test simulation with seed 42
[Error] Simulation failed at time=0
[info] - f32 *** FAILED ***
[info]   java.io.IOException: Cannot run program "testfloat_gen": error=2, No such file or directory
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1143)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:99)
[info]   at vexriscv.ip.fpu.ProcessStream.<init>(FpuTest.scala:1648)
[info]   at vexriscv.ip.fpu.FpuTest$$anonfun$testP$2$TestCase$1$$anon$2.<init>(FpuTest.scala:73)
[info]   at vexriscv.ip.fpu.FpuTest$$anonfun$testP$2$TestCase$1.build(FpuTest.scala:73)
[info]   at vexriscv.ip.fpu.FpuTest$$anonfun$testP$2$TestCase$1.RAW$lzycompute(FpuTest.scala:146)
[info]   at vexriscv.ip.fpu.FpuTest$$anonfun$testP$2$TestCase$1.RAW(FpuTest.scala:146)
[info]   ...
[info]   Cause: java.io.IOException: error=2, No such file or directory
[info]   at java.base/java.lang.ProcessImpl.forkAndExec(Native Method)
[info]   at java.base/java.lang.ProcessImpl.<init>(ProcessImpl.java:319)
[info]   at java.base/java.lang.ProcessImpl.start(ProcessImpl.java:249)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1110)
[info]   at java.base/java.lang.ProcessBuilder.start(ProcessBuilder.java:1073)
[info]   at scala.sys.process.ProcessBuilderImpl$Simple.run(ProcessBuilderImpl.scala:69)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:100)
[info]   at scala.sys.process.ProcessBuilderImpl$AbstractBuilder.run(ProcessBuilderImpl.scala:99)
[info]   at vexriscv.ip.fpu.ProcessStream.<init>(FpuTest.scala:1648)
[info]   at vexriscv.ip.fpu.FpuTest$$anonfun$testP$2$TestCase$1$$anon$2.<init>(FpuTest.scala:73)
[info]   ...
[info] Run completed in 14 minutes, 29 seconds.
[info] Total number of tests run: 222
[info] Suites: completed 4, aborted 0
[info] Tests: succeeded 102, failed 120, canceled 0, ignored 0, pending 0
[info] *** 120 TESTS FAILED ***
[error] Failed tests:
[error]         vexriscv.ip.fpu.FpuTest
[error]         vexriscv.DhrystoneBench
[error]         vexriscv.TestIndividualFeatures
[error] (Test / test) sbt.TestsFailedException: Tests unsuccessful
[error] Total time: 961 s (16:01), completed Oct 8, 2022, 4:02:39 PM
[mydev@fedora VexRiscv-master]$
```

```
[mydev@fedora VexRiscv-master]$ verilator --version
Verilator 4.108 2021-01-10 rev v4.106-158-g484b76e5b
[mydev@fedora VexRiscv-master]$
[mydev@fedora VexRiscv-master]$ cat /usr/share/verilator/include/verilated.h |grep VL_RANDOM_I
inline IData VL_RANDOM_I(int obits) VL_MT_SAFE { return vl_rand64() & VL_MASK_I(obits); }
[mydev@fedora VexRiscv-master]$ _
```

```
[mydev@fedora VexRiscv-master]$ cat /usr/share/verilator/include/verilated.cpp |grep VL_RANDOM_I
    return VL_RANDOM_I(obits);
        data = VL_RANDOM_I(obits);
[mydev@fedora VexRiscv-master]$
```

check the latest source code of Verilator:

```
[mydev@fedora verilator-master]$ cat include/verilated.cpp |grep -i VL_RANDOM_I
    seedr = VL_RANDOM_I();
    return VL_RANDOM_I();
    return VL_RANDOM_I();
        data = VL_RANDOM_I();
[mydev@fedora verilator-master]$
```

So the root cause of those failures is due to the old version of Verilator, will soon upgrade to the upcoming Fedora 37 and Verilator 5.x for retesting…

3) Cocotb

3.1 Installation

- https://docs.cocotb.org/en/stable/install.html

Install with pip

```
[mydev@fedora /]$ pip install --user cocotb
Collecting cocotb
  Downloading cocotb-1.7.1.tar.gz (293 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 294.0/294.0 kB 17.3 kB/s eta 0:00:00
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Building wheels for collected packages: cocotb
  Building wheel for cocotb (pyproject.toml) ... done
  Created wheel for cocotb: filename=cocotb-1.7.1-cp310-cp310-linux_aarch64.whl size=3798698 sha256=6067ae213b52afaafb384dc
3758b83240402c1f0aeb4f9e0931ef5ee8100ad9f
  Stored in directory: /home/mydev/.cache/pip/wheels/83/d6/b8/57330670b554fa4e166f8802cb51ec0ba5b95f44856941444b
Successfully built cocotb
Installing collected packages: cocotb
Successfully installed cocotb-1.7.1
[mydev@fedora /]$
[mydev@fedora /]$
```

or

```
[mydev@fedora /]$ pip install --user cocotb[bus]
Collecting cocotb[bus]
  Downloading cocotb-1.7.1.tar.gz (293 kB)
     ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 294.0/294.0 kB 103.2 kB/s eta 0:00:00
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Collecting cocotb-bus
  Downloading cocotb-bus-0.2.1.tar.gz (28 kB)
  Installing build dependencies ... done
  Getting requirements to build wheel ... done
  Preparing metadata (pyproject.toml) ... done
Building wheels for collected packages: cocotb, cocotb-bus
  Building wheel for cocotb (pyproject.toml) ... done
  Created wheel for cocotb: filename=cocotb-1.7.1-cp310-cp310-linux_aarch64.whl size=3798640 sha256=2f0ac6187ace754d677f371a21de814e0928034a87c1378888f8c17dfed41e2d
  Stored in directory: /home/mydev/.cache/pip/wheels/83/d6/b8/57330670b554fa4e166f8802cb51ec0ba5b95f44856941444b
  Building wheel for cocotb-bus (pyproject.toml) ... done
  Created wheel for cocotb-bus: filename=cocotb_bus-0.2.1-py3-none-any.whl size=34898 sha256=0102cbcdaaae687bfcd7b271935b261c2494f41c2fb44647fea6dc9d233d6f9f
  Stored in directory: /home/mydev/.cache/pip/wheels/82/d3/d4/e389d7694f7b3dcaf7aa90a1aaaf14e92885434226adef6f94
Successfully built cocotb cocotb-bus
Installing collected packages: cocotb, cocotb-bus
Successfully installed cocotb-1.7.1 cocotb-bus-0.2.1
WARNING: There was an error checking the latest version of pip.
[mydev@fedora /]$
```

3.2 Usage

A simple D flip-flop on RPi4

- https://github.com/cocotb/cocotb

```
[mydev@fedora DFF]$ ll
total 12
drwxr-xr-x. 1 mydev mydev  50 Oct  8 13:36 ./
drwxr-xr-x. 1 mydev mydev   6 Oct  8 13:35 ../
-rw-r--r--. 1 mydev mydev 135 Oct  8 13:35 dff.sv
-rw-r--r--. 1 mydev mydev 152 Oct  8 13:36 Makefile
-rw-r--r--. 1 mydev mydev 589 Oct  8 13:36 test_dff.py
[mydev@fedora DFF]$
```

```
[mydev@fedora DFF]$ make SIM=icarus
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/Tests/DFF'
mkdir -p sim_build
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s dff -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/Tests/DFF/dff.sv
rm -f results.xml
MODULE=test_dff TESTCASE= TOPLEVEL=dff TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.10/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python interpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.1 from /home/mydev/.local/lib/python3.10/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1665303047
     0.00ns INFO     cocotb.regression                  Found test test_dff.test_dff_simple
     0.00ns INFO     cocotb.regression                  running test_dff_simple (1/1)
                                                          Test that d propagates to q
 95000.00ns INFO     cocotb.regression                  test_dff_simple passed
 95000.00ns INFO     cocotb.regression                  **************************************************************************************
                                                        ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        **************************************************************************************
                                                        ** test_dff.test_dff_simple       PASS       95000.00           0.01   13504334.18  **
                                                        **************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0              95000.00           1.11      85767.42  **
                                                        **************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Verification/Cocotb/Official/Tests/DFF'
[mydev@fedora DFF]$
```

```
[mydev@fedora DFF]$ tree
.
├── dff.sv
├── Makefile
├── __pycache__
│   └── test_dff.cpython-310-pytest-6.2.5.pyc
├── results.xml
├── sim_build
│   ├── cmds.f
│   └── sim.vvp
└── test_dff.py
```

Cocotb in SpinalHDL

- ...

```
rm -f results.xml
make -f Makefile results.xml
make[1]: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester'
/usr/bin/iverilog -o sim_build/sim.vvp -D COCOTB_SIM=1 -s Axi4CrossbarTester -f sim_build/cmds.f -g2012   /opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/common/
../../../../../../Axi4CrossbarTester.v
rm -f results.xml
MODULE=Axi4CrossbarTester TESTCASE= TOPLEVEL=Axi4CrossbarTester TOPLEVEL_LANG=verilog \
         /usr/bin/vvp -M /home/mydev/.local/lib/python3.10/site-packages/cocotb/libs -m libcocotbvpi_icarus   sim_build/sim.vvp
     -.--ns INFO     gpi                                ..mbed/gpi_embed.cpp:76   in set_program_name_in_venv        Did not detect Python virtual environment. Using system-wide Python interpreter
     -.--ns INFO     gpi                                ../gpi/GpiCommon.cpp:101  in gpi_print_registered_impl       VPI registered
     0.00ns INFO     cocotb                             Running on Icarus Verilog version 11.0 (stable)
     0.00ns INFO     cocotb                             Running tests with cocotb v1.7.1 from /home/mydev/.local/lib/python3.10/site-packages/cocotb
     0.00ns INFO     cocotb                             Seeding Python random module with 1665311293
     0.00ns INFO     cocotb.regression                  Found test Axi4CrossbarTester.test1
     0.00ns INFO     cocotb.regression                  running test1 (1/1)
     0.00ns INFO     cocotb.Axi4CrossbarTester          Cocotb test boot
Sim speed : 0.022000 khz
Sim speed : 0.072000 khz
Sim speed : 0.068000 khz
Sim speed : 0.068000 khz
Sim speed : 0.078000 khz
Sim speed : 0.080000 khz
Sim speed : 0.080000 khz
```

- ...

```
Sim speed : 0.088000 khz
Sim speed : 0.084000 khz
Sim speed : 0.093000 khz
Sim speed : 0.127000 khz
Sim speed : 0.138000 khz
Sim speed : 0.098000 khz
  4504.50ns INFO     cocotb.Axi4CrossbarTester          Cocotb test done
  4504.50ns INFO     cocotb.regression                  test1 passed
  4504.50ns INFO     cocotb.regression                  ************************************************************************************
                                                        ** TEST                          STATUS  SIM TIME (ns)  REAL TIME (s)  RATIO (ns/s) **
                                                        ************************************************************************************
                                                        ** Axi4CrossbarTester.test1       PASS        4504.50          62.65         71.90  **
                                                        ************************************************************************************
                                                        ** TESTS=1 PASS=1 FAIL=0 SKIP=0               4504.50          64.23         70.13  **
                                                        ************************************************************************************

make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester'

/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:232: DeprecationWarning: Use of attribute 'log' is deprecated, use '_log
' instead
  dut.log.info("Cocotb test boot")
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:235: DeprecationWarning: cocotb.fork has been deprecated in favor of coc
otb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(ClockDomainAsyncReset(dut.clk, dut.reset))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:89: DeprecationWarning: Setting values on handles using the ``handle <= value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  reset <= 1
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/misc.py:90: DeprecationWarning: Setting values on handles using the ``handle <= value`` syntax is deprecated.
Instead use the ``handle.value = value`` syntax
  clk <= 0
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/spinal/Axi4CrossbarTester/Axi4CrossbarTester.py:236: DeprecationWarning: cocotb.fork has been deprecated in favor of coc
otb.start_soon and cocotb.start.
In most cases you can simply substitute cocotb.fork with cocotb.start_soon.
For more information about when you would want to use cocotb.start see the docs,
https://docs.cocotb.org/en/latest/coroutines.html#concurrent-execution
  cocotb.fork(simulationSpeedPrinter(dut.clk))
/opt/MyWorkSpace/MyProjs/HW-EDA/RISC-V/SpinalHDL/SpinalHDL-dev/tester/src/test/python/cocotblib/Stream.py:92: DeprecationWarning: cocotb.fork has been deprecated in favor of cocotb.start_soon and cocotb.sta
rt.
```

- ...

cocotblib

```
[submodule "tester/src/test/python/cocotblib"]
        path = tester/src/test/python/cocotblib
        url = https://github.com/SpinalHDL/CocotbLib.git
```

```
[mydev@fedora SpinalHDL-dev]$ tree tester/src/test/python/cocotblib
tester/src/test/python/cocotblib
├── AhbLite3.py
├── Apb3.py
├── Axi4.py
├── ClockDomain.py
├── Flow.py
├── __init__.py
├── LICENSE
├── misc.py
├── Phase.py
├── Scorboard.py
├── Spi.py
├── Stream.py
└── TriState.py
```

4) LiteX

4.1 Installation

- https://github.com/enjoy-digital/litex/wiki/Installation
- https://github.com/litex-hub/litex-boards

Quick start

- 1. Install Python 3.6+ and FPGA vendor's development tools and/or Verilator.
  2. Install Migen/LiteX and the LiteX's cores:

```
$ wget https://raw.githubusercontent.com/enjoy-digital/litex/master/litex_setup.py
$ chmod +x litex_setup.py
$ ./litex_setup.py --init --install --user (--user to install to user directory) --config=(minimal, standard, f
```

Later, if you need to update all repositories:

```
$ ./litex_setup.py --update
```

> **Note:** On MacOS, make sure you have HomeBrew installed. Then do, `brew install wget`.

> **Note:** On Windows, it's possible you'll have to set `SHELL` environment variable to `SHELL=cmd.exe`.

3. Install a RISC-V toolchain (Only if you want to test/create a SoC with a CPU):

```
$ pip3 install meson ninja
$ ./litex_setup.py --gcc=riscv
```

4. Build the target of your board...:

Go to litex-boards/litex_boards/targets and execute the target you want to build.

5. ... and/or install Verilator and test LiteX directly on your computer without any FPGA board:

On Linux (Ubuntu):

```
$ sudo apt install libevent-dev libjson-c-dev verilator
$ litex_sim --cpu-type=vexriscv
```

Source: https://github.com/enjoy-digital/litex

6. Run a terminal program on the board's serial port at 115200 8-N-1.

You should get the BIOS prompt like the one below.

```
      __   _ __      ___   _ __  __
     / /  (_) /____  / _ | / /_/ /
    / /__/ / __/ -_)/ __ |/ __  <
   /____/_/\__/\__/\__/_/|_|
   Build your hardware, easily!

 (c) Copyright 2012-2020 Enjoy-Digital
 (c) Copyright 2007-2015 M-Labs

 BIOS built on Feb 15 2020 10:39:50
 BIOS CRC passed (aae1476d)

 Migen git sha1: e2e6c72
 LiteX git sha1: 18a9d4ff

--================ SoC ==================--
CPU:       VexRiscv @ 1MHz
ROM:       32KB
SRAM:      4KB
MAIN-RAM:  262144KB

--=============== Boot ==================--
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
Timeout
No boot medium found

--============= Console ================--
litex>
```

Source: https://github.com/enjoy-digital/litex

- https://github.com/enjoy-digital/litex/blob/master/litex_setup.py

...

```python
def gcc_toolchain_download(url, filename):
    print_status("Downloading GCC toolchain...", underline=True)
    if not os.path.exists(filename):
        full_url = url + filename
        print_status(f"Downloading {full_url} to {filename}...")
        urllib.request.urlretrieve(full_url, filename)
    else:
        print_status(f"Using existing file {filename}.")

    print_status(f"Extracting {filename}...")
    shutil.unpack_archive(filename)

# RISC-V toolchain.
# -----------------

def riscv_gcc_toolchain_download():
    base_url  = "https://static.dev.sifive.com/dev-tools/freedom-tools/v2020.08/"
    base_file = "riscv64-unknown-elf-gcc-10.1.0-2020.08.2-x86_64-"

    # Windows
    if (sys.platform.startswith("win") or sys.platform.startswith("cygwin")):
        end_file = "w64-mingw32.zip"
    # Linux
    elif sys.platform.startswith("linux"):
        os_release = (open("/etc/os-release").read()).lower()
        if "fedora" in os_release:
            end_file = "linux-centos6.tar.gz"
        else:
            end_file = "linux-ubuntu14.tar.gz"

    # Mac OS
    elif sys.platform.startswith("darwin"):
        end_file = "apple-darwin.tar.gz"
    else:
        raise NotImplementedError(sys.platform)

    # Download/Extract.
    gcc_toolchain_download(url=base_url, filename=base_file + end_file)

```

...

https://static.dev.sifive.com/dev-tools/freedom-tools/v2020.08/riscv64-unknown-elf-gcc-10.1.0-2020.08.2-x86_64-linux-centos6.tar.gz

D:\Tmp\riscv64-unknown-elf-gcc-10.1.0-2020.08.2-x86_64-linux-centos6.tar.gz\riscv64-unknown-elf-gcc-10.1.0-2020.08.2-x86_64-linux-centos6.tar\riscv64-unknown-elf-gcc-10.1.0-2020.08.2-x86_64-linux-centos6\bin\

名称	大小	压缩...	修改...	模式	用户	组	链接	硬链接	特征	文件夹	文件	创建...	访问...	User ID	Grou...	注释	Devic...	Devic...
riscv64-unknown-elf-addr2line	905 3...	905 7...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-ar	938 9...	939 0...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-as	1 364 ...	1 364 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-c++	6 940 ...	6 940 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-c++filt	899 9...	900 0...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-cpp	6 940 ...	6 940 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-elfedit	38 424	38 912	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-g++	6 940 ...	6 940 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcc	6 936 ...	6 936 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcc-10.1.0	6 936 ...	6 936 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcc-ar	39 136	39 424	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcc-nm	35 040	35 328	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcc-ranlib	35 048	35 328	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcov	1 815 ...	1 816 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcov-dump	853 4...	853 5...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gcov-tool	879 4...	879 6...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gdb	8 676 ...	8 676 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gdb-add-index	4 045	4 096	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gdb-add-index-py	4 045	4 096	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gdb-py	24 67...	24 67...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-gprof	972 9...	973 3...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-ld	1 474 ...	1 474 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-ld.bfd	1 474 ...	1 474 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-lto-dump	57 70...	57 70...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-nm	920 7...	921 0...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-objcopy	1 057 ...	1 057 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-objdump	1 512 ...	1 512 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-ranlib	938 9...	939 0...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-readelf	809 4...	809 4...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-run	1 449 ...	1 449 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-run-py	1 449 ...	1 449 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-size	905 4...	905 7...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-strings	905 1...	905 2...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			
riscv64-unknown-elf-strip	1 057 ...	1 057 ...	2020-...	-rwxr-...	jenkins	jenkins			0 GN...					501	501			

- **Test on RPi4**

some findings:

1. **The REPL of GraalPython installed in GraalVM does not work on ARM**

```
[mydev@fedora /]$ which python
/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/bin/python
[mydev@fedora /]$
[mydev@fedora /]$ python -V
GraalVM Python 3.8.5 (GraalVM CE Native 22.3.0-dev)
[mydev@fedora /]$
[mydev@fedora /]$ python
```

While that of the standalone installation works

```
[mydev@fedora LiteX]$ export PATH=/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin:$PATH
[mydev@fedora LiteX]$ which python
/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin/python
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ python
Python 3.8.5 (Mon Oct 03 21:12:17 UTC 2022)
[Graal, GraalVM CE, Java 11.0.17] on linux
Type "help", "copyright", "credits" or "license" for more information.
>>> import pip
Traceback (most recent call last):
  File "<stdin>", line 1, in <module>
ModuleNotFoundError: No module named 'pip'
```

For these two versions of GraalPython, you may refer to another presentation "Ray--a Swiss Army Knife for Distributed Computing & AI" at COSCon 2022(Online).

2. **PYTHONPATH does not work with GraalPython on ARM**

```
[mydev@fedora /]$ /usr/bin/python
Python 3.10.7 (main, Sep  7 2022, 00:00:00) [GCC 12.2.1 20220819 (Red Hat 12.2.1-1)] on linux
Type "help", "copyright", "credits" or "license" for more information.
>>> import sys
>>> print(sys.path)
['', '/usr/lib64/python310.zip', '/usr/lib64/python3.10', '/usr/lib64/python3.10/lib-dynload', '/home/mydev/.local/lib/python3.10/site-packages', '/opt/MyWorkSpace/MyProjs/HCI/Ray/Official/ray-master/python',
 '/usr/local/lib/python3.10/site-packages', '/usr/lib64/python3.10/site-packages', '/usr/lib/python3.10/site-packages']
```

```
[mydev@fedora LiteX]$ export PYTHONPATH=/usr/lib64/python3.10:/usr/lib64/python3.10/lib-dynload:/home/mydev/.local/lib/python3.10/site-packages:/usr/local/lib/python3.10/site-packages:/usr/lib64/python3.10/si
te-packages:/usr/lib/python3.10/site-packages
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ python -V
ERROR: LookupError(fmt="unknown encoding %s", args = (a com.oracle.truffle.api.strings.TruffleString, ) )
[mydev@fedora LiteX]$
```

initial testing

```
[mydev@fedora LiteX]$ ll
total 20
drwxr-xr-x. 1 mydev mydev    28 Oct 11 15:37 ./
drwxr-xr-x. 1 mydev mydev    68 Oct 11 14:32 ../
-rwxr-xr-x. 1 mydev mydev 18159 Oct 11 15:37 litex_setup.py*
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ which python
/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/bin/python
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ ./litex_setup.py --init --install --user --config=full

         __   _ __      _  __
        / /  (_) /___   | |/ /
       / /__/ / __/ -_)>  <
      /____/_/\__/\__/_/|_|
    Build your hardware, easily!
         LiteX Setup utility.

[   1.678] LiteX Setup auto-update...
[   1.688] Initializing Git repositories...
[   1.688] -------------------------------
[   1.692] Cloning migen Git repository...
Cloning into 'migen'...
remote: Enumerating objects: 12615, done.
remote: Counting objects: 100% (184/184), done.
remote: Compressing objects: 100% (76/76), done.
remote: Total 12615 (delta 124), reused 156 (delta 108), pack-reused 12431
Receiving objects: 100% (12615/12615), 3.08 MiB | 1.94 MiB/s, done.
Resolving deltas: 100% (8204/8204), done.
Already on 'master'
Your branch is up to date with 'origin/master'.
[   6.494] Cloning pythondata-software-picolibc Git repository...
```

...

```
[ 584.489] Installing migen Git repository...
/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/bin/python3: No module named pipTraceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/litex_setup.py", line 448, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/litex_setup.py", line 430, in main
    litex_setup_install_repos(config=args.config, user_mode=args.user)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/litex_setup.py", line 283, in litex_setup_install_repos
    ), shell=True)
  File "/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/languages/python/lib-python/3/subprocess.py", line 364, in check_call
    raise CalledProcessError(retcode, cmd)
subprocess.CalledProcessError: Command '"/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/bin/python3" -m pip install --editable . --user' returned non-zero exit status 1.
[mydev@fedora Official]$
```

or

```
[ 585.705] Installing migen Git repository...
Obtaining file:///opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/migen
  Preparing metadata (setup.py) ... done
Traceback (most recent call last):
  File "<module>", line 271, in run
  File "<module>", line 332, in resolve
  File "<module>", line 137, in _add_to_criteria
  File "<module>", line 150, in __bool__
  File "<module>", line 557, in wrapper
  File "<module>", line 557, in wrapper
  File "<module>", line 812, in generate
  File "<module>", line 28, in dumps
  File "<module>", line 755, in _pack
  File "<module>", line 964, in _pack_map_pairs
writeByte not implemented
Traceback (most recent call last):
  File "<module>", line 271, in run
  File "<module>", line 332, in resolve
  File "<module>", line 137, in _add_to_criteria
  File "<module>", line 150, in __bool__
  File "<module>", line 557, in wrapper
  File "<module>", line 557, in wrapper
  File "<module>", line 812, in generate
  File "<module>", line 28, in dumps
  File "<module>", line 755, in _pack
  File "<module>", line 964, in _pack_map_pairs
com.oracle.truffle.api.CompilerDirectives$ShouldNotReachHere: writeByte not implemented
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 448, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 430, in main
    litex_setup_install_repos(config=args.config, user_mode=args.user)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 283, in litex_setup_install_repos
    ), shell=True)
  File "/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/languages/python/lib-python/3/subprocess.py", line 364, in check_call
    raise CalledProcessError(retcode, cmd)
subprocess.CalledProcessError: Command '"/opt/MyWorkSpace/DevSW/Java/JDK/GraalVM/CE/v22.3.0-dev-20221004/Java19/bin/python3" -m pip install --editable . --user' returned non-zero exit status 1.
[mydev@fedora LiteX]$
```

retried with standalone GraalPython with special PYTHONPATH

```
[mydev@fedora LiteX]$ ll
total 20
drwxr-xr-x. 1 mydev mydev    28 Oct 12 11:29 ./
drwxr-xr-x. 1 mydev mydev    68 Oct 11 14:32 ../
-rwxr-xr-x. 1 mydev mydev 18159 Oct 12 11:29 litex_setup.py*
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ export PATH=/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin:$PATH
[mydev@fedora LiteX]$ which python
/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin/python
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ export PYTHONPATH=/usr/lib64/python3.10/site-packages
[mydev@fedora LiteX]$ python
Python 3.8.5 (Mon Oct 03 21:12:17 UTC 2022)
[Graal, GraalVM CE, Java 11.0.17] on linux
Type "help", "copyright", "credits" or "license" for more information.
>>> exit()
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ ./litex_setup.py --init --install --user --config=full

        / /  (_) /____ |_|/_/
       / /__/ / __/ -_)>  <
      /____/_/\__/\__/_/|_|
    Build your hardware, easily!
        LiteX Setup utility.

[   1.249] LiteX Setup auto-update...
[   1.261] Initializing Git repositories...
[   1.261] --------------------------------
[   1.267] Cloning migen Git repository...
Cloning into 'migen'...
remote: Enumerating objects: 12615, done.
remote: Counting objects: 100% (184/184), done.
remote: Compressing objects: 100% (76/76), done.
remote: Total 12615 (delta 124), reused 156 (delta 108), pack-reused 12431
Receiving objects: 100% (12615/12615), 3.08 MiB | 1.70 MiB/s, done.
Resolving deltas: 100% (8204/8204), done.
Already on 'master'
Your branch is up to date with 'origin/master'.
[   5.986] Cloning pythondata-software-picolibc Git repository...
```

...

```
[ 573.378] Installing migen Git repository...
Obtaining file:///opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/migen
  Preparing metadata (setup.py) ... done
Traceback (most recent call last):
  File "<module>", line 271, in run
  File "<module>", line 332, in resolve
  File "<module>", line 137, in _add_to_criteria
  File "<module>", line 150, in __bool__
  File "<module>", line 557, in wrapper
  File "<module>", line 557, in wrapper
  File "<module>", line 812, in generate
  File "<module>", line 28, in dumps
  File "<module>", line 755, in _pack
  File "<module>", line 964, in _pack_map_pairs
writeByte not implemented
Traceback (most recent call last):
  File "<module>", line 271, in run
  File "<module>", line 332, in resolve
  File "<module>", line 137, in _add_to_criteria
  File "<module>", line 150, in __bool__
  File "<module>", line 557, in wrapper
  File "<module>", line 557, in wrapper
  File "<module>", line 812, in generate
  File "<module>", line 28, in dumps
  File "<module>", line 755, in _pack
  File "<module>", line 964, in _pack_map_pairs
com.oracle.truffle.api.CompilerDirectives$ShouldNotReachHere: writeByte not implemented
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 448, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 430, in main
    litex_setup_install_repos(config=args.config, user_mode=args.user)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex_setup.py", line 283, in litex_setup_install_repos
    ), shell=True)
  File "/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/lib-python/3/subprocess.py", line 364, in check_call
    raise CalledProcessError(retcode, cmd)
subprocess.CalledProcessError: Command '"/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin/python3" -m pip install --editable . --user' returned non-zero exit status 1.
[mydev@fedora LiteX]$
```

```
[mydev@fedora LiteX]$ which python
/opt/MyWorkSpace/DevSW/Python/GraalPython/v22.3.0-dev/bin/python
[mydev@fedora LiteX]$ unset PYTHONPATH
[mydev@fedora LiteX]$ export PYTHONPATH=/usr/lib64/python310.zip:/usr/lib64/python3.10:/usr/lib64/python3.10/lib-dynload:/home/mydev/.local/lib/python3.10/site-packages:/usr/local/lib/python3.10/site-packages
:/usr/lib64/python3.10/site-packages:/usr/lib/python3.10/site-packages
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ python
ERROR: LookupError(fmt="unknown encoding %s", args = (a com.oracle.truffle.api.strings.TruffleString, ) )
[mydev@fedora LiteX]$
```

retried with CPython and resulted in success

```
[mydev@fedora LiteX]$ ll
total 20
drwxr-xr-x. 1 mydev mydev    28 Oct 12 12:01 ./
drwxr-xr-x. 1 mydev mydev    68 Oct 11 14:32 ../
-rwxr-xr-x. 1 mydev mydev 18159 Oct 12 12:01 litex_setup.py*
[mydev@fedora LiteX]$ export PATH=/usr/bin:$PATH
[mydev@fedora LiteX]$ which python
/usr/bin/python
[mydev@fedora LiteX]$
[mydev@fedora LiteX]$ ./litex_setup.py --init --install --user --config=full

        __   _ __      _ __
       / /  (_) /____ |_|/ /
      / /__/ / __/ -_)>  <
     /____/_/\__/\__/_/|_|
   Build your hardware, easily!
        LiteX Setup utility.

[   0.005] LiteX Setup auto-update...
[   0.689] Initializing Git repositories...
[   0.689] ------------------------------
[   0.689] Cloning migen Git repository...
Cloning into 'migen'...
remote: Enumerating objects: 12615, done.
remote: Counting objects: 100% (184/184), done.
remote: Compressing objects: 100% (76/76), done.
remote: Total 12615 (delta 124), reused 156 (delta 108), pack-reused 12431
Receiving objects: 100% (12615/12615), 3.08 MiB | 1.42 MiB/s, done.
Resolving deltas: 100% (8204/8204), done.
Already on 'master'
Your branch is up to date with 'origin/master'.
[   5.640] Cloning pythondata-software-picolibc Git repository...
```

```
[ 638.036] Installing migen Git repository...
Obtaining file:///opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/migen
  Preparing metadata (setup.py) ... done
Requirement already satisfied: colorama in /usr/lib/python3.10/site-packages (from migen==0.9.2) (0.4.4)
Installing collected packages: migen
  Running setup.py develop for migen
Successfully installed migen
```

```
[mydev@fedora LiteX]$ ll
total 20
drwxr-xr-x. 1 mydev mydev  1258 Oct 12 15:40 ./
drwxr-xr-x. 1 mydev mydev    68 Oct 11 14:32 ../
drwxr-xr-x. 1 mydev mydev   212 Oct 12 15:50 linux-on-litex-vexriscv/
drwxr-xr-x. 1 mydev mydev   194 Oct 12 12:05 litedram/
drwxr-xr-x. 1 mydev mydev   168 Oct 12 12:05 liteeth/
drwxr-xr-x. 1 mydev mydev   152 Oct 12 12:05 liteiclink/
drwxr-xr-x. 1 mydev mydev   160 Oct 12 12:05 litejesd204b/
drwxr-xr-x. 1 mydev mydev   192 Oct 12 12:05 litepcie/
drwxr-xr-x. 1 mydev mydev   170 Oct 12 12:05 litesata/
drwxr-xr-x. 1 mydev mydev   162 Oct 12 12:05 litescope/
drwxr-xr-x. 1 mydev mydev   166 Oct 12 12:05 litesdcard/
drwxr-xr-x. 1 mydev mydev   152 Oct 12 12:05 litespi/
drwxr-xr-x. 1 mydev mydev   202 Oct 12 12:04 litex/
drwxr-xr-x. 1 mydev mydev   146 Oct 12 12:05 litex-boards/
-rwxr-xr-x. 1 mydev mydev 18159 Oct 12 12:01 litex_setup.py*
drwxr-xr-x. 1 mydev mydev   172 Oct 12 12:02 migen/
drwxr-xr-x. 1 mydev mydev   280 Oct 12 12:07 pythondata-cpu-blackparrot/
drwxr-xr-x. 1 mydev mydev   292 Oct 12 12:07 pythondata-cpu-cv32e40p/
drwxr-xr-x. 1 mydev mydev   248 Oct 12 12:07 pythondata-cpu-cv32e41p/
drwxr-xr-x. 1 mydev mydev   240 Oct 12 12:08 pythondata-cpu-cva5/
drwxr-xr-x. 1 mydev mydev   262 Oct 12 12:08 pythondata-cpu-cva6/
drwxr-xr-x. 1 mydev mydev   240 Oct 12 12:09 pythondata-cpu-ibex/
drwxr-xr-x. 1 mydev mydev   262 Oct 12 12:05 pythondata-cpu-lm32/
drwxr-xr-x. 1 mydev mydev   252 Oct 12 12:05 pythondata-cpu-marocchino/
drwxr-xr-x. 1 mydev mydev   272 Oct 12 12:06 pythondata-cpu-microwatt/
drwxr-xr-x. 1 mydev mydev   268 Oct 12 12:09 pythondata-cpu-minerva/
drwxr-xr-x. 1 mydev mydev   266 Oct 12 12:05 pythondata-cpu-mor1kx/
drwxr-xr-x. 1 mydev mydev   236 Oct 12 12:09 pythondata-cpu-naxriscv/
drwxr-xr-x. 1 mydev mydev   270 Oct 12 12:09 pythondata-cpu-picorv32/
drwxr-xr-x. 1 mydev mydev   266 Oct 12 12:10 pythondata-cpu-rocket/
drwxr-xr-x. 1 mydev mydev   262 Oct 12 12:11 pythondata-cpu-serv/
drwxr-xr-x. 1 mydev mydev   292 Oct 12 12:11 pythondata-cpu-vexriscv/
drwxr-xr-x. 1 mydev mydev   316 Oct 12 12:11 pythondata-cpu-vexriscv-smp/
drwxr-xr-x. 1 mydev mydev   268 Oct 12 12:05 pythondata-misc-tapcfg/
drwxr-xr-x. 1 mydev mydev   238 Oct 12 12:05 pythondata-misc-usb_ohci/
drwxr-xr-x. 1 mydev mydev   272 Oct 12 12:04 pythondata-software-compiler_rt/
drwxr-xr-x. 1 mydev mydev   280 Oct 12 12:02 pythondata-software-picolibc/
drwxr-xr-x. 1 mydev mydev   248 Oct 12 12:05 valentyusb/
[mydev@fedora LiteX]$
```

build the target board

```
[mydev@fedora LiteX]$ pushd litex-boards/litex_boards/targets
/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX
[mydev@fedora targets]$
[mydev@fedora targets]$ ./muselab_icesugar_pro.py --build --load
INFO:ECP5PLL:Creating ECP5PLL.
INFO:ECP5PLL:Registering Single Ended ClkIn of 25.00MHz.
INFO:ECP5PLL:Creating ClkOut0 sys of 50.00MHz (+-10000.00ppm).
INFO:ECP5PLL:Creating ClkOut1 sys_ps of 50.00MHz (+-10000.00ppm).
INFO:ECP5PLL:Creating ClkOut2 eth of 50.00MHz (+-10000.00ppm).
INFO:SoC:
INFO:SoC:        __   __  __  __  ____  __  __
INFO:SoC:       /  /  (_)/ /_/ /_/ __ |/ /_/
INFO:SoC:      / /__/ / / __/ -_)> <
INFO:SoC:     /____/_/\__/\__/\__/_/|_|
INFO:SoC:  Build your hardware, easily!
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Creating SoC ... (2022-10-13 00:41:03)
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:FPGA device : LFE5U-25F-6BG256C.
INFO:SoC:System clock: 50.000MHz.
INFO:SoCBusHandler:Creating Bus Handler ...
INFO:SoCBusHandler:32-bit wishbone Bus, 4.0GiB Address Space.
INFO:SoCBusHandler:Adding reserved Bus Regions ...
INFO:SoCBusHandler:Bus Handler created.
INFO:SoCCSRHandler:Creating CSR Handler ...
INFO:SoCCSRHandler:32-bit CSR Bus, 32-bit Aligned, 16.0KiB Address Space, 2048B Paging, big Ordering (Up to 32 Locations).
INFO:SoCCSRHandler:Adding reserved CSRs ...
INFO:SoCCSRHandler:CSR Handler created.
INFO:SoCIRQHandler:Creating IRQ Handler ...
INFO:SoCIRQHandler:IRQ Handler (up to 32 Locations).
INFO:SoCIRQHandler:Adding reserved IRQs ...
INFO:SoCIRQHandler:IRQ Handler created.
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Initial SoC:
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:32-bit wishbone Bus, 4.0GiB Address Space.
INFO:SoC:32-bit CSR Bus, 32-bit Aligned, 16.0KiB Address Space, 2048B Paging, big Ordering (Up to 32 Locations).
INFO:SoC:IRQ Handler (up to 32 Locations).
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Controller ctrl added.
INFO:SoC:CPU vexriscv added.
```

...

```
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 201, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 194, in main
    builder.build(**builder_kargs)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/builder.py", line 332, in build
    self._generate_includes(with_bios=with_bios)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/builder.py", line 179, in _generate_includes
    variables_contents = self._get_variables_contents()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/builder.py", line 149, in _get_variables_contents
    for k, v in export.get_cpu_mak(self.soc.cpu, self.compile_software):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/export.py", line 92, in get_cpu_mak
    selected_triple = select_triple(triple)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/export.py", line 90, in select_triple
    raise OSError(msg)
OSError: Unable to find any of the cross compilation toolchains:
- riscv64-pc-linux-musl
- riscv64-unknown-elf
- riscv64-unknown-linux-gnu
- riscv64-elf
- riscv64-linux
- riscv64-linux-gnu
- riscv-sifive-elf
- riscv64-none-elf
- riscv32-unknown-elf
- riscv32-unknown-linux-gnu
- riscv32-elf
- riscv-none-embed
- riscv-none-elf

[mydev@fedora targets]$
```

...

```
[mydev@fedora targets]$ export PATH=/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/bin:$PATH
[mydev@fedora targets]$ which riscv64-unknown-elf-gcc
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/bin/riscv64-unknown-elf-gcc
[mydev@fedora targets]$
[mydev@fedora targets]$ ./muselab_icesugar_pro.py --build --load
INFO:ECP5PLL:Creating ECP5PLL.
INFO:ECP5PLL:Registering Single Ended ClkIn of 25.00MHz.
```

```
picolibc 1.7.9

  User defined options
    Cross files          : cross.txt
    includedir           : picolibc/riscv64-unknown-elf/include
    libdir               : picolibc/riscv64-unknown-elf/lib
    atomic-ungetc        : false
    format-default       : integer
    io-long-long         : true
    multilib             : false
    picocrt              : false
    thread-local-storage: false

Found ninja-1.10.2 at /usr/bin/ninja
meson compile
[875/875] Generating newlib/libc_duplicates with a custom command
cp newlib/libc.a __libc.a
 CC       _libc.a
 AR       _libc.a
```

```
 CC       bios.elf
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/lib/gcc/riscv64-unknown-elf/12.2.0/../../../../riscv64-unknown-elf/bin/ld: warning: bios.elf has a LOAD segment with RWX permissions
chmod -x bios.elf
 OBJCOPY  bios.bin
chmod -x bios.bin
python3 -m litex.soc.software.crcfbigen bios.bin --little
python3 -m litex.soc.software.memusage bios.elf /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/build/muselab_icesugar_pro/software/bios/.
./include/generated/regions.ld riscv64-unknown-elf

ROM usage: 24.61KiB     (19.22%)
RAM usage: 1.61KiB      (20.12%)

rm crt0.o
make: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/build/muselab_icesugar_pro/software/bios'
INFO:SoC:Initializing ROM rom with contents (Size: 0x627c).
INFO:SoC:Auto-Resizing ROM rom from 0x20000 to 0x627c.

 /----------------------------------------------------------------------------\
 |                                                                            |
 |  yosys -- Yosys Open SYnthesis Suite                                       |
 |                                                                            |
 |  Copyright (C) 2012 - 2020  Claire Xenia Wolf <claire@yosyshq.com>         |
 |                                                                            |
 |  Permission to use, copy, modify, and/or distribute this software for any  |
 |  purpose with or without fee is hereby granted, provided that the above    |
 |  copyright notice and this permission notice appear in all copies.         |
 |                                                                            |
 |  THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES  |
 |  WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF          |
 |  MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR   |
 |  ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES    |
 |  WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN     |
 |  ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF   |
 |  OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.            |
 |                                                                            |
 \----------------------------------------------------------------------------/

 Yosys 0.21+7 (git sha1 d98738db5c, gcc 12.2.1 -O2 -fexceptions -fstack-protector-strong -mbranch-protection=standard -fasynchronous-unwind-tables -fstack-clash-protection -fPIC -Os)


-- Executing script file `muselab_icesugar_pro.ys' --

1. Executing Verilog-2005 frontend: /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv/pythondata_cpu_vexriscv/verilog/VexRiscv.v
Parsing Verilog input from `/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv/pythondata_cpu_vexriscv/verilog/VexRiscv.v' to AST representation.
Storing AST representation for module `$abstract\VexRiscv'.
Storing AST representation for module `$abstract\DataCache'.
Storing AST representation for module `$abstract\InstructionCache'.
Successfully finished Verilog frontend.
```

```
Info: Program finished normally.
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 201, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 198, in main
    prog.load_bitstream(builder.get_bitstream_filename(mode="sram"))
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/lattice/programmer.py", line 183, in load_bitstream
    self.call(["ecpdap",
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/generic_programmer.py", line 95, in call
    if (subprocess.call(command) != 0) and check:
  File "/usr/lib64/python3.10/subprocess.py", line 345, in call
    with Popen(*popenargs, **kwargs) as p:
  File "/usr/lib64/python3.10/subprocess.py", line 969, in __init__
    self._execute_child(args, executable, preexec_fn, close_fds,
  File "/usr/lib64/python3.10/subprocess.py", line 1845, in _execute_child
    raise child_exception_type(errno_num, err_msg, err_filename)
FileNotFoundError: [Errno 2] No such file or directory: 'ecpdap'
[mydev@fedora targets]$
```

开源社 kaiyuanshe

2022 第七届中国开源年会 OPEN THE WORLD

build ecpdap(https://github.com/adamgreig/ecpdap)

```
[mydev@fedora ecpdap]$ cargo build --release
    Updating `ustc` index
  Downloaded aho-corasick v0.7.19 (registry `ustc`)
  Downloaded anyhow v1.0.65 (registry `ustc`)
...
   Compiling jtagdap v0.1.1
   Compiling spi-flash v0.3.0
   Compiling ecpdap v0.2.0 (/opt/MyWorkSpace/MyProjs/HW-EDA/Dev/Debugging/ECPDAP/Official/Bak/ecpdap)
    Finished release [optimized] target(s) in 6m 35s
[mydev@fedora ecpdap]$
```

```
[mydev@fedora ecpdap]$ file target/release/ecpdap
target/release/ecpdap: ELF 64-bit LSB pie executable, ARM aarch64, version 1 (SYSV), dynamically linked, interpreter /lib/ld-linux-aarch64.so.1, BuildID[sha1]=1a1b520ad488a7217aaab3852fba55e5fd9f3125, for GNU
/Linux 3.7.0, with debug_info, not stripped
[mydev@fedora ecpdap]$
[mydev@fedora ecpdap]$ sudo cp target/release/ecpdap /usr/local/bin
[sudo] password for mydev:
[mydev@fedora ecpdap]$
```

rebuild

```
[mydev@fedora targets]$ which ecpdap
/usr/local/bin/ecpdap
[mydev@fedora targets]$ ./muselab_icesugar_pro.py --build --load
INFO:ECP5PLL:Creating ECP5PLL.
INFO:ECP5PLL:Registering Single Ended ClkIn of 25.00MHz.
INFO:ECP5PLL:Creating ClkOut0 sys of 50.00MHz (+-10000.00ppm).
...
Info: Program finished normally.
Error: no CMSIS-DAP probes found.
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 201, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex-boards/litex_boards/targets/./muselab_icesugar_pro.py", line 198, in main
    prog.load_bitstream(builder.get_bitstream_filename(mode="sram"))
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/lattice/programmer.py", line 183, in load_bitstream
    self.call(["ecpdap",
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/generic_programmer.py", line 101, in call
    raise OSError(msg)
OSError: Error occured during EcpDapProgrammer's call, please check:
- EcpDapProgrammer installation.
- Access permissions.
- Hardware and cable.
- Bitstream presence.
[mydev@fedora targets]$
```

FYI: https://os.mbed.com/handbook/CMSIS-DAP

working on a workaround solution…

4.2 Linux on LiteX-VexRiscv

Introduction

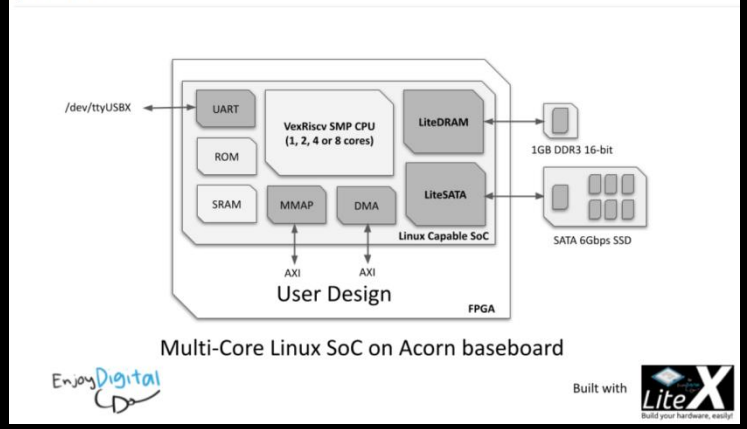
- https://github.com/litex-hub/linux-on-litex-vexriscv

This project is an experiment to run Linux with VexRiscv-SMP CPU, a 32-bits Linux Capable RISC-V CPU written in Spinal HDL. LiteX is used to create the SoC around the VexRiscv-SMP CPU and provides the infrastructure and peripherals (LiteDRAM, LiteEth, LiteSDCard, etc...). All the components used to create the SoC are open-source and the flexibility of Spinal HDL/LiteX allow targeting easily very various FPGA devices/boards: Xilinx, Intel, Lattice, Microsemi, Efinix FPGAs are tested with very various configuration: SDRAM/DDR/DDR2/DDR3/DDR4 or HyperRAM RAMs, RMII/MII/RGMII/1000BASE-X Ethernet PHYs, SDCard (in SPI or SD mode), SATA, PCIe, etc...

On Lattice ECP5 FPGAs, the open source toolchain even allows creating full open-source SoC with open-source cores **and** toolchain!

This project demonstrates **how high level HDLs framework like Spinal HDL, LiteX can enable new possibilities and complement each other**. Results shown here are the results of a productive collaboration between various open-source communities.

[> Demo



[> Supported boards

All boards supported in LiteX-Boards with...:

- Enough FPGA logic to fit VexRiscv-SMP + LiteX SoC.
- 32MB of RAM (Reduced to 8MB when rootfs can be put on a SDCard).
- A UART.

Test on RPi4

```
[mydev@fedora linux-on-litex-vexriscv]$ ll
total 80
drwxr-xr-x. 1 mydev mydev   212 Oct 12 15:50 ./
drwxr-xr-x. 1 mydev mydev  1258 Oct 12 15:40 ../
drwxr-xr-x. 1 mydev mydev     6 Oct 12 15:50 build/
drwxr-xr-x. 1 mydev mydev   118 Oct 12 15:40 buildroot/
drwxr-xr-x. 1 mydev mydev   138 Oct 12 15:40 .git/
drwxr-xr-x. 1 mydev mydev    18 Oct 12 15:40 .github/
-rw-r--r--. 1 mydev mydev   292 Oct 12 15:40 .gitignore
-rw-r--r--. 1 mydev mydev  3700 Oct 12 15:40 HOWTO.md
drwxr-xr-x. 1 mydev mydev   182 Oct 12 15:54 images/
-rw-r--r--. 1 mydev mydev  1349 Oct 12 15:40 LICENSE
-rwxr-xr-x. 1 mydev mydev 32258 Oct 12 15:40 make.py*
-rw-r--r--. 1 mydev mydev 16021 Oct 12 15:40 README.md
-rwxr-xr-x. 1 mydev mydev  6847 Oct 12 15:40 sim.py*
-rwxr-xr-x. 1 mydev mydev  2310 Oct 12 15:40 .sim-test.py*
-rw-r--r--. 1 mydev mydev  7827 Oct 12 15:40 soc_linux.py
drwxr-xr-x. 1 mydev mydev    48 Oct 12 15:40 test/
[mydev@fedora linux-on-litex-vexriscv]$
```

```
[mydev@fedora linux-on-litex-vexriscv]$ tree images
images
├── boot.json
├── Image
├── linux_2022_03_23.zip
├── opensbi.bin
├── rootfs.cpio
└── rv32.dtb

0 directories, 6 files
[mydev@fedora linux-on-litex-vexriscv]$ which openocd
/usr/local/bin/openocd
[mydev@fedora linux-on-litex-vexriscv]$ which riscv64-unknown-elf-gcc
/opt/MyWorkSpace/DevSW/Toolchain/RISC-V/GCC/Official/ELF/bin/riscv64-unknown-elf-gcc
[mydev@fedora linux-on-litex-vexriscv]$
```

https://github.com/litex-hub/linux-on-litex-vexriscv/files/8331338/linux_2022_03_23.zip

built with FTDI enabled(./configure --enable-ftdi)

```
[mydev@fedora linux-on-litex-vexriscv]$ ./sim.py
INFO:SoC:
INFO:SoC:       __   _ __      _ __
INFO:SoC:      / /  (_) /____ | |/ /
INFO:SoC:     / /__/ / __/ -_)>  <
INFO:SoC:    /____/_/\__/\__/_/|_|
INFO:SoC:  Build your hardware, easily!
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Creating SoC ... (2022-10-13 12:51:42)
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:FPGA device : SIM.
INFO:SoC:System clock: 100.000MHz.
INFO:SoCBusHandler:Creating Bus Handler ...
INFO:SoCBusHandler:32-bit wishbone Bus, 4.0GiB Address Space.
INFO:SoCBusHandler:Adding reserved Bus Regions ...
INFO:SoCBusHandler:Bus Handler created.
INFO:SoCCSRHandler:Creating CSR Handler ...
INFO:SoCCSRHandler:32-bit CSR Bus, 32-bit Aligned, 16.0KiB Address Space, 2048B Paging, big Ordering (Up to 32 Locations).
INFO:SoCCSRHandler:Adding reserved CSRs ...
INFO:SoCCSRHandler:CSR Handler created.
INFO:SoCIRQHandler:Creating IRQ Handler ...
INFO:SoCIRQHandler:IRQ Handler (up to 32 Locations).
INFO:SoCIRQHandler:Adding reserved IRQs ...
INFO:SoCIRQHandler:IRQ Handler created.
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Initial SoC:
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:32-bit wishbone Bus, 4.0GiB Address Space.
INFO:SoC:32-bit CSR Bus, 32-bit Aligned, 16.0KiB Address Space, 2048B Paging, big Ordering (Up to 32 Locations).
INFO:SoC:IRQ Handler (up to 32 Locations).
INFO:SoC:--------------------------------------------------------------------------------
INFO:SoC:Controller ctrl added.
INFO:SoC:CPU vexriscv_smp added.
```

```
python3 -m litex.soc.software.crcfbigen bios.bin --little
python3 -m litex.soc.software.memusage bios.elf /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/software/bios/../include/generated/regions
.ld riscv64-unknown-elf

ROM usage: 24.04KiB     (37.56%)
RAM usage: 1.36KiB      (16.99%)

rm crt0.o
make: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/software/bios'
INFO:SoC:Initializing ROM rom with contents (Size: 0x6038).
INFO:SoC:Auto-Resizing ROM rom from 0x10000 to 0x6038.
Traceback (most recent call last):
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/./sim.py", line 177, in <module>
    main()
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/./sim.py", line 168, in main
    builder.build(sim_config=sim_config,
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/builder.py", line 364, in build
    vns = self.soc.build(build_dir=self.gateware_dir, **kwargs)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/soc/integration/soc.py", line 1287, in build
    return self.platform.build(self, *args, **kwargs)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/platform.py", line 54, in build
    return self.toolchain.build(self, *args, **kwargs)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/verilator.py", line 254, in build
    _compile_sim(build_name, verbose)
  File "/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/verilator.py", line 162, in _compile_sim
    raise OSError("Subprocess failed with {}\n{}".format(p.returncode, "\n".join(error_messages)))
OSError: Subprocess failed with 2
make: Entering directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware'
mkdir -p modules
make -C modules -f /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/core/modules/Makefile
```

```
cc -c -ggdb -Wall -O3   -o /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware/obj_dir/parse.o /opt/MyWorkSpace/MyProjs/HW-EDA/Langua
ges/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/core/parse.c
cc -c -ggdb -Wall -O3   -o /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware/obj_dir/sim.o /opt/MyWorkSpace/MyProjs/HW-EDA/Language
s/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/core/sim.c
verilator -Wno-fatal -O3 --cc /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv-smp/pythondata_cpu_vexriscv_smp/verilog/Ram_1w_1rs_Generic.v --cc /opt
/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv-smp/pythondata_cpu_vexriscv_smp/verilog/VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4
_Ldw32_Ood.v --cc /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware/sim.v  --top-module sim --exe \
        -DPRINTF_COND=0 \
        sim_init.cpp /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/core/veril.cpp libdylib.o modules.o pads.o parse.o sim.o \
        --top-module sim \
         \
        -CFLAGS "-ggdb -Wall -O3   -I/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/litex/litex/build/sim/core" \
        -LDFLAGS "-lpthread -Wl,--no-as-needed -ljson-c -lz -lm -lstdc++ -Wl,--no-as-needed -ldl -levent" \
        --trace \
         \
         \
        --unroll-count 256 \
        --output-split 5000 \
        --output-split-cfuncs 500 \
        --output-split-ctrace 500 \
         \
        -Wno-BLKANDNBLK \
        -Wno-WIDTH \
        --relative-includes
%Error-TIMESCALEMOD: /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv-smp/pythondata_cpu_vexriscv_smp/verilog/Ram_1w_1rs_Generic.v:2:8: Timescale mis
sing on this module as other modules have it (IEEE 1800-2017 3.14.2.2)
                        /opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/pythondata-cpu-vexriscv-smp/pythondata_cpu_vexriscv_smp/verilog/VexRiscvLitexSmpCluster_Cc1_Iw32Is4096I
y1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood.v:7:8:  ... Location of module with timescale
     7 | module VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood (
       |        ^~~~
```

rerun the simulation

```
[mydev@fedora linux-on-litex-vexriscv]$ ./sim.py
INFO:SoC:
INFO:SoC:
INFO:SoC:
INFO:SoC:
INFO:SoC:  Build your hardware, easily!
INFO:SoC:----------------------------------------------------------------------------
INFO:SoC:Creating SoC ... (2022-10-13 13:08:57)
INFO:SoC:----------------------------------------------------------------------------
INFO:SoC:FPGA device : SIM.
INFO:SoC:System clock: 100.000MHz.
INFO:SoCBusHandler:Creating Bus Handler ...
...
```

```
g++  -I.  -MMD -I/usr/share/verilator/include -I/usr/share/verilator/include/vltstd -DVM_COVERAGE=0 -DVM_SC=0 -DVM_TRACE=1 -DVM_TRACE_FST=0 -faligned-new -fcf-protection=none -Wno-bool-operation -Wno-sign-com
pare -Wno-uninitialized -Wno-unused-but-set-variable -Wno-unused-parameter -Wno-unused-variable -Wno-shadow     -ggdb -Wall -O3   -I/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Officia
l/LiteX/litex/litex/build/sim/core  -std=gnu++14  -c -o Vsim__Trace__3__Slow.o Vsim__Trace__3__Slow.cpp
Archive ar -cr Vsim__ALL.a Vsim.o Vsim_sim.o Vsim_sim__1.o Vsim_sim__2.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds
4096Dy1_ITs4DTs4_Ldw32_Ood__1.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__2.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__3.o Vsim_V
exRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__4.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__5.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096I
y1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__6.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__7.o Vsim_VexRiscv.o Vsim_VexRiscv__1.o Vsim_VexRiscv__2.o Vsim_VexRiscv__3.o Vsim__Dpi
.o Vsim__Trace.o Vsim__Trace__1.o Vsim__Trace__2.o Vsim__Slow.o Vsim_sim__Slow.o Vsim_sim__1__Slow.o Vsim_sim__2__Slow.o Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__Slow.o
 Vsim_VexRiscvLitexSmpCluster_Cc1_Iw32Is4096Iy1_Dw32Ds4096Dy1_ITs4DTs4_Ldw32_Ood__1__Slow.o Vsim_VexRiscv__Slow.o Vsim_VexRiscv__1__Slow.o Vsim_VexRiscv__2__Slow.o Vsim__Syms.o Vsim__Trace__Slow.o Vsim__Trace
__1__Slow.o Vsim__Trace__2__Slow.o Vsim__Trace__3__Slow.o
g++    veril.o sim_init.o verilated.o verilated_dpi.o verilated_vcd_c.o Vsim__ALL.a   libdylib.o modules.o pads.o parse.o sim.o -lpthread -Wl,--no-as-needed -ljson-c -lz -lm -lstdc++ -Wl,--no-as-needed -ldl -
levent    -o Vsim
make[1]: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware/obj_dir'
make: Leaving directory '/opt/MyWorkSpace/MyProjs/HW-EDA/Languages/Python/LiteX/Enjoy-Digital/Official/LiteX/linux-on-litex-vexriscv/build/sim/gateware'

[gmii_ethernet] loaded (0xffff99a21000)
[spdeeprom] loaded (addr = 0x0)
[clocker] loaded
[serial2tcp] loaded (0xffff99a21000)
[serial2console] loaded (0xffff99a21000)
[ethernet] loaded (0xffff99a21000)
[xgmii_ethernet] loaded (0xffff99a21000)
[clocker] sys_clk: freq_hz=1000000, phase_deg=0


      __   _ __      _ __
     / /  (_) /____ | |/_/
    / /__/ / __/ -_)>  <
   /____/_/_\__\__/_/|_|
  Build your hardware, easily!

 (c) Copyright 2012-2022 Enjoy-Digital
 (c) Copyright 2007-2015 M-Labs

 BIOS built on Oct 13 2022 13:09:21
 BIOS CRC passed (20bcd7cc)
 LiteX git sha1: efdc9ece

--=============== SoC ==================--
CPU:            VexRiscv SMP-LINUX @ 100MHz
BUS:            WISHBONE 32-bit @ 4GiB
CSR:            32-bit data
ROM:            64KiB
SRAM:           8KiB
SDRAM:          65536KiB 32-bit @ 100MT/s (CL-2 CWL-2)

--=========== Initialization ============--
Initializing SDRAM @0x40000000...
Switching SDRAM to software control.
Switching SDRAM to hardware control.

--=============== Boot ==================--
Booting from serial...
Press Q or ESC to abort boot completely.
sL5DdSMmkekro
Timeout
Executing booted program at 0x40f00000
```

```
--============= Liftoff! ===============--

OpenSBI v0.8-1-gecf7701
   ____                    _____ ____ _____
  / __ \                  / ____|  _ \_   _|
 | |  | |_ __   ___ _ __ | (___ | |_) || |
 | |  | | '_ \ / _ \ '_ \ \___ \|  _ < | |
 | |__| | |_) |  __/ | | |____) | |_) || |_
  \____/| .__/ \___|_| |_|_____/|____/_____|
        | |
        |_|

Platform Name       : LiteX / VexRiscv-SMP
Platform Features   : timer,mfdeleg
Platform HART Count : 8
Boot HART ID        : 0
Boot HART ISA       : rv32imas
BOOT HART Features  : time
BOOT HART PMP Count : 0
Firmware Base       : 0x40f00000
Firmware Size       : 124 KB
Runtime SBI Version : 0.2

MIDELEG : 0x00000222
MEDELEG : 0x0000b101
[    0.000000] Linux version 5.14.0 (florent@panda) (riscv32-buildroot-linux-gnu-gcc.br_real (Buildroot 2021.08-381-g279167ee8d) 10.3.0, GNU ld (GNU Binutils) 2.36.1) #1 SMP Tue Sep 21 12:57:31 CEST 2021
[    0.000000] earlycon: liteuart0 at I/O port 0x0 (options '')
[    0.000000] Malformed early option 'console'
[    0.000000] earlycon: liteuart0 at MMIO 0xf0001000 (options '')
[    0.000000] printk: bootconsole [liteuart0] enabled
[    0.000000] Zone ranges:
[    0.000000]   Normal   [mem 0x0000000040000000-0x0000000043ffffff]
[    0.000000] Movable zone start for each node
[    0.000000] Early memory node ranges
[    0.000000]   node   0: [mem 0x0000000040000000-0x0000000043ffffff]
[    0.000000] Initmem setup node 0 [mem 0x0000000040000000-0x0000000043ffffff]
[    0.000000] SBI specification v0.2 detected
[    0.000000] SBI implementation ID=0x1 Version=0x8
[    0.000000] SBI TIME extension detected
[    0.000000] SBI IPI extension detected
[    0.000000] SBI RFENCE extension detected
[    0.000000] SBI v0.2 HSM extension detected
[    0.000000] riscv: ISA extensions aimp
[    0.000000] riscv: ELF capabilities aim
[    0.000000] percpu: Embedded 8 pages/cpu s11340 r0 d21428 u32768
[    0.000000] Built 1 zonelists, mobility grouping on.  Total pages: 16256
[    0.000000] Kernel command line: console=liteuart earlycon=liteuart,0xf0001000 rootwait root=/dev/ram0
[    0.000000] Dentry cache hash table entries: 8192 (order: 3, 32768 bytes, linear)
[    0.000000] Inode-cache hash table entries: 4096 (order: 2, 16384 bytes, linear)
[    0.000000] Sorting __ex_table...
[    0.000000] mem auto-init: stack:off, heap alloc:off, heap free:off
[    0.000000] Memory: 48644K/65536K available (5685K kernel code, 572K rwdata, 883K rodata, 209K init, 221K bss, 16892K reserved, 0K cma-reserved)
[    0.000000] SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=1, Nodes=1
[    0.000000] rcu: Hierarchical RCU implementation.
[    0.000000] rcu:     RCU restricting CPUs from NR_CPUS=8 to nr_cpu_ids=1.
[    0.000000] rcu: RCU calculated value of scheduler-enlistment delay is 25 jiffies.
[    0.000000] rcu: Adjusting geometry for rcu_fanout_leaf=16, nr_cpu_ids=1
[    0.000000] NR_IRQS: 64, nr_irqs: 64, preallocated irqs: 0
[    0.000000] riscv-intc: 32 local interrupts mapped
[    0.000000] plic: interrupt-controller@f0c00000: mapped 32 interrupts with 1 handlers for 2 contexts.
[    0.000000] random: get_random_bytes called from start_kernel+0x4ac/0x63c with crng_init=0
[    0.000000] riscv_timer_init_dt: Registering clocksource cpuid [0] hartid [0]
[    0.000000] clocksource: riscv_clocksource: mask: 0xffffffffffffffff max_cycles: 0x171024e7e0, max_idle_ns: 440795205315 ns
[    0.000017] sched_clock: 64 bits at 100MHz, resolution 10ns, wraps every 4398046511100ns
[    0.002164] Console: colour dummy device 80x25
[    0.003097] Calibrating delay loop (skipped), value calculated using timer frequency.. 200.00 BogoMIPS (lpj=400000)
[    0.004634] pid_max: default: 32768 minimum: 301
[    0.008055] Mount-cache hash table entries: 1024 (order: 0, 4096 bytes, linear)
[    0.009092] Mountpoint-cache hash table entries: 1024 (order: 0, 4096 bytes, linear)
[    0.029602] ASID allocator using 9 bits (512 entries)
[    0.032202] rcu: Hierarchical SRCU implementation.
[    0.037673] smp: Bringing up secondary CPUs ...
[    0.038235] smp: Brought up 1 node, 1 CPU
[    0.043649] devtmpfs: initialized
[    0.067172] clocksource: jiffies: mask: 0xffffffff max_cycles: 0xffffffff, max_idle_ns: 7645041785100000 ns
[    0.068496] futex hash table entries: 256 (order: 2, 16384 bytes, linear)
[    0.076186] NET: Registered PF_NETLINK/PF_ROUTE protocol family
[    0.219368] pps_core: LinuxPPS API ver. 1 registered
[    0.219903] pps_core: Software ver. 5.3.6 - Copyright 2005-2007 Rodolfo Giometti <giometti@linux.it>
[    0.221322] PTP clock support registered
[    0.224488] FPGA manager framework
[    0.237864] clocksource: Switched to clocksource riscv_clocksource
```

```
[    0.388310] NET: Registered PF_INET protocol family
[    0.390444] IP idents hash table entries: 2048 (order: 2, 16384 bytes, linear)
[    0.397993] tcp_listen_portaddr_hash hash table entries: 512 (order: 0, 6144 bytes, linear)
[    0.399314] TCP established hash table entries: 1024 (order: 0, 4096 bytes, linear)
[    0.400543] TCP bind hash table entries: 1024 (order: 1, 8192 bytes, linear)
[    0.401753] TCP: Hash tables configured (established 1024 bind 1024)
[    0.403182] UDP hash table entries: 256 (order: 1, 8192 bytes, linear)
[    0.404274] UDP-Lite hash table entries: 256 (order: 1, 8192 bytes, linear)
[    0.422111] Unpacking initramfs ...
[    0.457924] workingset: timestamp_bits=30 max_order=14 bucket_order=0
[    0.665012] io scheduler mq-deadline registered
[    0.665874] io scheduler kyber registered
[    0.914509] LiteX SoC Controller driver initialized
[    4.159431] Freeing initrd memory: 8192K
[    4.663497] f0001000.serial: ttyLXU0 at MMIO 0x0 (irq = 0, base_baud = 0) is a liteuart
[    4.664780] printk: console [liteuart0] enabled
[    4.664780] printk: console [liteuart0] enabled
[    4.665718] printk: bootconsole [liteuart0] disabled
[    4.665718] printk: bootconsole [liteuart0] disabled
[    4.686406] i2c_dev: i2c /dev entries driver
[    4.723480] NET: Registered PF_INET6 protocol family
[    4.736993] Segment Routing with IPv6
[    4.738084] In-situ OAM (IOAM) with IPv6
[    4.739621] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[    4.752560] NET: Registered PF_PACKET protocol family
[    4.764132] Freeing unused kernel image (initmem) memory: 204K
[    4.764910] Kernel memory protection not selected by kernel config.
[    4.766183] Run /init as init process
Starting syslogd: OK
Starting klogd: OK
Running sysctl: OK
Saving random seed: [    6.821751] random: dd: uninitialized urandom read (512 bytes read)
OK
Starting network: OK
```

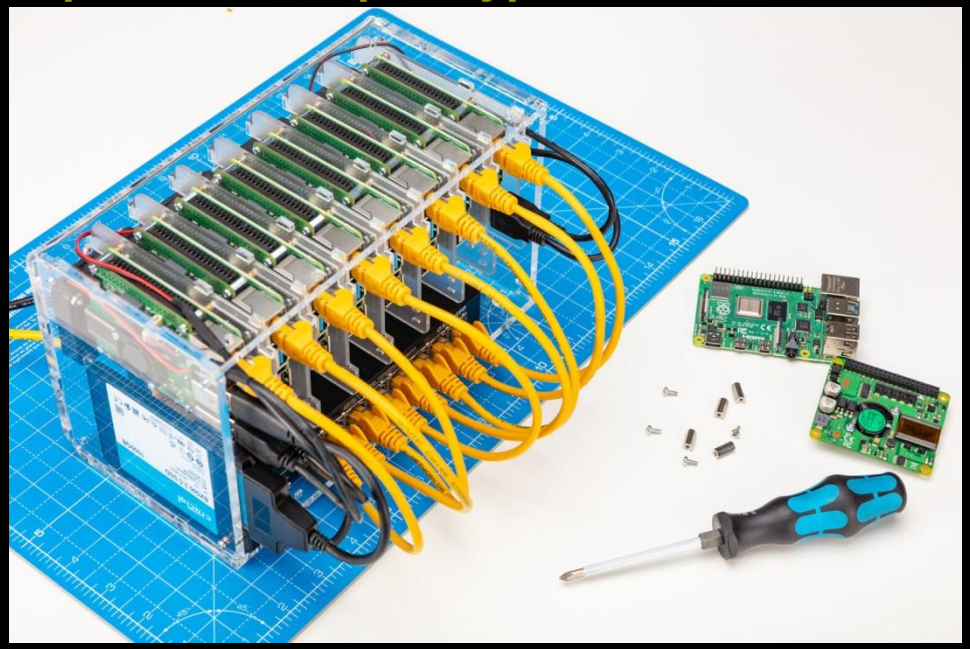
```
Welcome to Buildroot
buildroot login: root
                   __    _
                  / /   (_)__  __ ____ __
                 / /__ / /  _ \/ // /\ \ /
                /____/_/_//_\_,_//_\_\
                         /  _ \
   __   _ __      _  _\___/_//_/        ___  _
  / /  (_) /____ | |/_/__| | / /____ __ / _ \(_)__ _____ __
 / /__/ / __/ -_)>  <\___/ |/ / -_) \ // , _/ (_-</ __/ |/ /
/____/_/\__/\__/_/|_|____|___/\__/_\_\/_/|_/_/___/\__/|___/
                  / __/  |/  / _ \
                 _\ \/ /|_/ / ___/
                /___/_/  /_/_/
  32-bit RISC-V Linux running on LiteX / VexRiscv-SMP.

login[70]: root login on 'console'
root@buildroot:~#
root@buildroot:~#
root@buildroot:~# help
Built-in commands:
------------------
        . : [ [[ alias bg break cd chdir command continue echo eval exec
        exit export false fg getopts hash help history jobs kill let
        local printf pwd read readonly return set shift source test times
        trap true type ulimit umask unalias unset wait
root@buildroot:~#
```

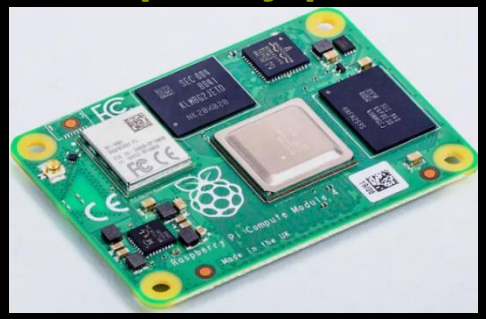
IV. HW & SW Infra

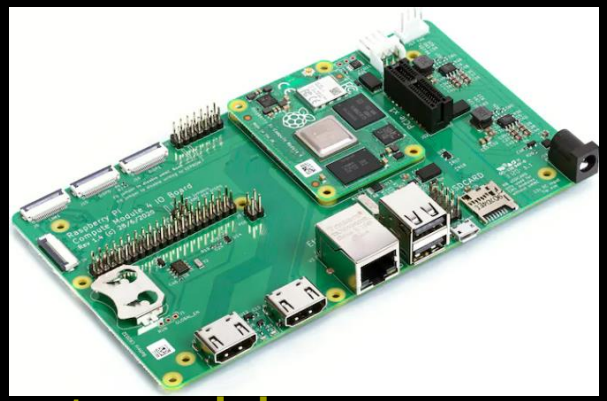
1) ARM cluster

1.1 RPi4 cluster

- https://www.raspberrypi.com/tutorials/cluster-raspberry-pi-tutorial/



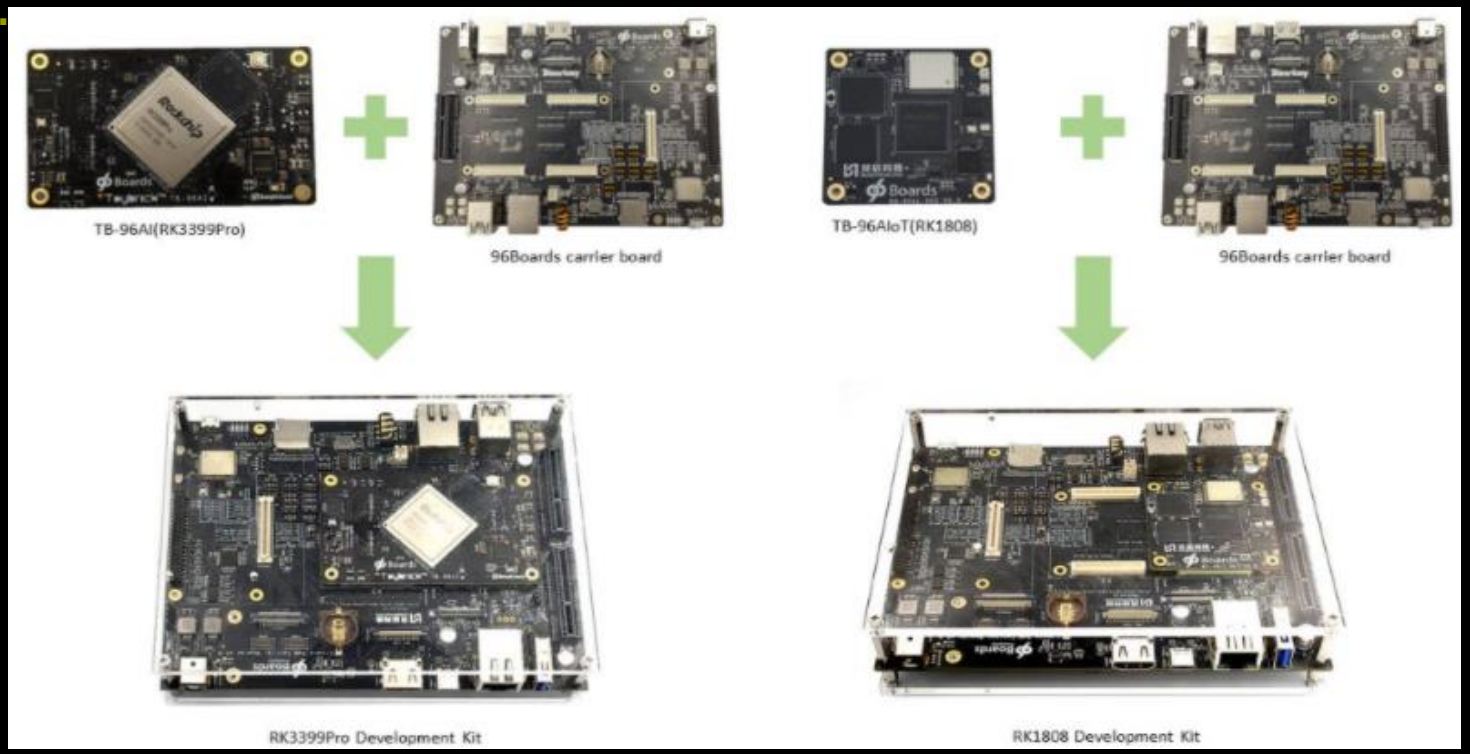




- https://www.raspberrypi.com/products/compute-module-4/?variant=raspberry-pi-cm4001000
- https://www.raspberrypi.com/products/compute-module-4-io-board/
- ...

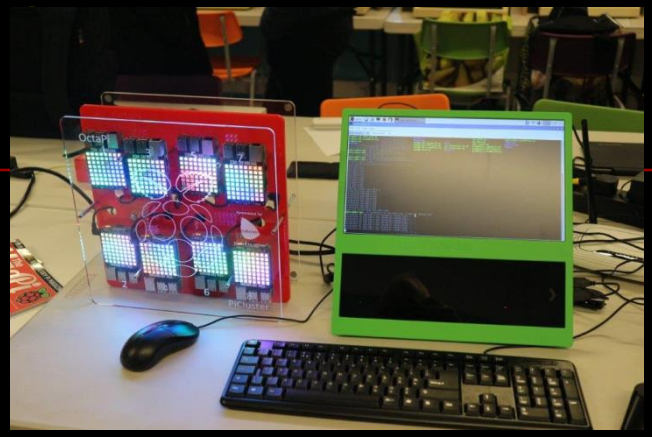
SOM/COM

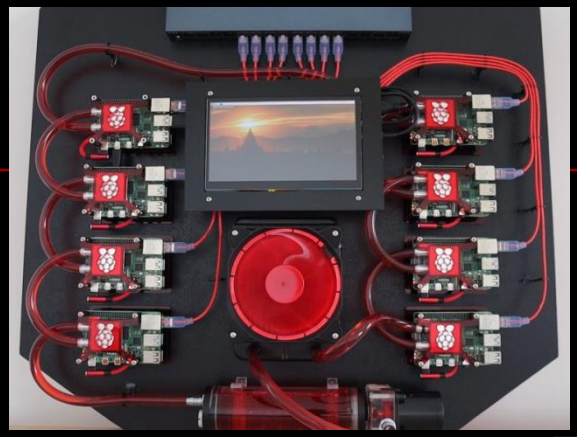
- https://www.linaro.org/news/linaro-announces-launch-of-96boards-system-on-module-som-specification/
- http:///linuxgizmos.com/linaro-launches-two-96boards-som-specifications/
- http://static.linaro.org/assets/specifications/96BoardsComputeSoMSpecificationV1.0.pdf
- https://static.linaro.org/assets/specifications/96BoardsWirelessSoMSpecificationV1.0.pdf
- .

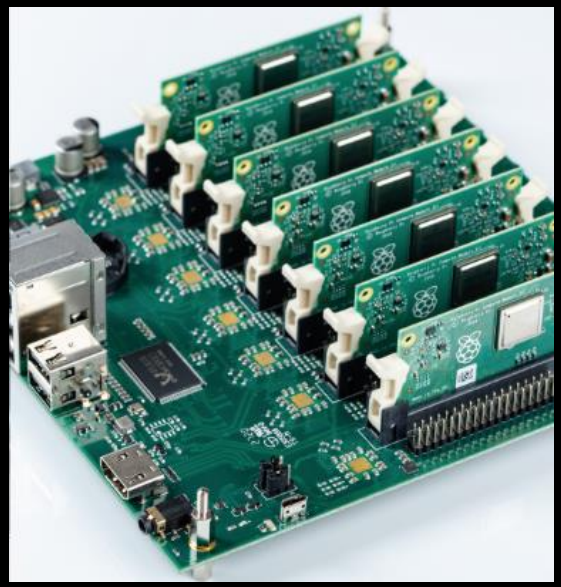


Source: http://www.beiqicloud.com/product_detail.html?pid=CarrierBoard

1.1.1 Clustering







Turing Pi 2

- https://turingpi.com/

RELIABLE, SCALABLE, CLOUD-NATIVE COMPUTER FOR THE EDGE

Turing Pi is a compact ARM cluster that unites four compute modules on a Mini ITX motherboard. 24/7, fanless and quiet with power consumption under 60 W. Turing Pi architecture is fully compatible with Kubernetes. You can connect clusters to each other and quickly scale your infra.

- 4x CPU w/ 1 GbE each
- Onboard L2 Managed Switch 1 GbE
- VLAN Support
- 2x SATA III Ports 6 Gbps
- 2x Mini PCI Express Slots
- Baseboard Management Controller

32 GB of RAM	< 60W TDP	4 x CPU CM4 or Jetson

- 1 GbE L2 Managed Switch
- 3 x USB 3.0
- VLAN Support
- Sim Slot
- 2x SATA III Ports 6 Gbps
- Power supply 24 pin ATX
- 2x Mini PCI Express Slots
- Power Consumption <60w
- 1 x HDMI
- RTC Battery
- 1 x DSI
- 1 x 40 pin GPIO
- 2 x Ethernet
- Baseboard Management Controller

All flavors of compute modules

GENERAL COMPUTE

Vendor	Model	CPU	Cores	RAM up to
Turing Pi	RK1	Rockchip RK3588	8	32
Raspberry Pi	CM4	Broadcom BCM2711	4	8

MACHINE LEARNING

Vendor	Model	CPU	Cores	RAM up to
Nvidia	Jetson Nano	Quad-core ARM Cortex-A57 MPCore	4	4
Nvidia	Jetson TX2 NX	Dual-core NVIDIA Denver 2 Quad-core ARM A57 Complex	6	4
Nvidia	Jetson Xavier NX	NVIDIA Carmel ARM® v8.2	6	16

- ## Use cases

→ **Blockchain**

Run RPC and staking nodes with NVMe support

→ **Self-hosted**

Host open-source apps locally or at the edge

→ **Learning**

Learn Kubernetes, Docker, Serverless

→ **Development**

Build cloud-native local dev environment

AS EASY AS

Interact with a cluster using just a command-line interface. Turing Pi open-source firmware offers a set of remote management features for authentication, serial console over LAN, OS images flashing, self-testing, and OTA updates.

```
$ tpictl login
$ tpictl info

$ tpictl get nodes
$ tpictl flash -node 1 -f ./ubuntu.img
$ tpictl reboot -node 1
$ tpictl serial -node 1

$ tpictl drain -node 2
$ tpictl power -off -node 2
```

- https://turingpi.com/turing-pi-v2-is-here/
- https://turingpi.com/12-amazing-raspberry-pi-cluster-use-cases/
- ...

Arkade

- https://github.com/alexellis/arkade
  Open Source Marketplace for Kubernetes.
- https://kccncna20.sched.com/event/ekAF/the-past-present-and-future-of-kubernetes-on-raspberry-pi-alex-ellis-openfaas-ltd

-

arkade is how developers install the latest versions of their favourite tools and Kubernetes apps.

With `arkade get`, you'll have `kubectl`, `kind`, `terraform`, and `jq` on your machine faster than you can type `apt-get install/brew update`.

2) Serverless architecture

Overview

- https://en.wikipedia.org/wiki/Serverless_computing

Serverless computing is a cloud computing execution model in which the cloud provider allocates machine resources on demand, taking care of the servers on behalf of their customers. "Serverless" is a misnomer in the sense that servers are still used by cloud service providers to execute code for developers. However, developers of serverless applications are not concerned with capacity planning, configuration, management, maintenance, fault tolerance, or scaling of containers, VMs, or physical servers. Serverless computing does not hold resources in volatile memory; computing is rather done in short bursts with the results persisted to storage. When an app is not in use, there are no computing resources allocated to the app. Pricing is based on the actual amount of resources consumed by an application.[1] It can be a form of utility computing.

Serverless computing can simplify the process of deploying code into production. Serverless code can be used in conjunction with code deployed in traditional styles, such as microservices or monoliths. Alternatively, applications can be written to be purely serverless and use no provisioned servers at all.[2] This should not be confused with computing or networking models that do not require an actual server to function, such as peer-to-peer (P2P).

Serverless runtimes

Serverless vendors offer compute runtimes, also known as Function as a Service (FaaS) platforms, which execute application logic but do not store data. Common languages supported by serverless runtimes are Java, Python and PHP. Generally, the functions run under isolation boundaries, such as, Linux containers.

https://en.wikipedia.org/wiki/Function_as_a_service

Function as a service (**FaaS**) is a category of cloud computing services that provides a platform allowing customers to develop, run, and manage application functionalities without the complexity of building and maintaining the infrastructure typically associated with developing and launching an app.[1] Building an application following this model is one way of achieving a "serverless" architecture, and is typically used when building microservices applications.

FaaS was initially offered by various start-ups circa 2010, such as PiCloud.[2]

AWS Lambda[3] was the first FaaS offering by a large public cloud vendor, followed by Google Cloud Functions, Microsoft Azure Functions, IBM/Apache's OpenWhisk (open source) in 2016 and Oracle Cloud Fn (open source) in 2017.

Pros

Cost [edit]

Serverless can be more cost-effective than renting or purchasing a fixed quantity of servers,[16] which generally involves significant periods of underutilization or idle time.[1] It can even be more cost-efficient than provisioning an autoscaling group, due to more efficient bin-packing of the underlying machine resources.

This can be described as pay-as-you-go computing[16] or bare-code[16] as you are charged based solely upon the time and memory allocated to run your code; without associated fees for idle time.[16]

Immediate cost benefits are related to the lack of operating costs, including: licenses, installation, dependencies, and personnel cost for maintenance, support, or patching.[16] The lack of personnel cost is an advantage that applies broadly to cloud computing.

Elasticity versus scalability [edit]

See also: Scalability and Elasticity (cloud computing)

In addition, a serverless architecture means that developers and operators do not need to spend time setting up and tuning autoscaling policies or systems; the cloud provider is responsible for scaling the capacity to the demand.[1][17][16] As Google puts it: "from prototype to production to planet-scale."[16]

As cloud native systems inherently scale down as well as up, these systems are known as elastic rather than scalable.

Small teams of developers are able to run code themselves without the dependence upon teams of infrastructure and support engineers; more developers are becoming DevOps skilled and distinctions between being a software developer or hardware engineer are blurring.[16]

Productivity [edit]

With function as a service, the units of code exposed to the outside world are simple event driven functions. This means that typically, the programmer does not have to worry about multithreading or directly handling HTTP requests in their code, simplifying the task of back-end software development.

Cons

Performance [edit]

Infrequently-used serverless code may suffer from greater response latency than code that is continuously running on a dedicated server, virtual machine, or container. This is because, unlike with autoscaling, the cloud provider typically "spins down" the serverless code completely when not in use. This means that if the runtime (for example, the Java runtime) requires a significant amount of time to start up, it will create additional latency.[18]

Resource limits [edit]

Serverless computing is not suited to some computing workloads, such as high-performance computing, because of the resource limits imposed by cloud providers, and also because it would likely be cheaper to bulk-provision the number of servers believed to be required at any given point in time.[19]

Monitoring and debugging [edit]

Diagnosing performance or excessive resource usage problems with serverless code may be more difficult than with traditional server code, because although entire functions can be timed,[2] there is typically no ability to dig into more detail by attaching profilers, debuggers or APM tools.[20] Furthermore, the environment in which the code runs is typically not open source, so its performance characteristics cannot be precisely replicated in a local environment.

Security [edit]

Serverless is sometimes mistakenly considered as more secure than traditional architectures. While this is true to some extent because OS vulnerabilities are taken care of by the cloud provider, the total attack surface is significantly larger as there are many more components to the application compared to traditional architectures and each component is an entry point to the serverless application. Moreover, the security solutions customers used to have to protect their cloud workloads become irrelevant as customers cannot control and install anything on the endpoint and network level such as an intrusion detection/prevention system (IDS/IPS).[21]

This is intensified by the mono-culture properties of the entire server network. (A single flaw can be applied globally.) According to Protego, the "solution to secure serverless apps is close partnership between developers, DevOps, and AppSec, also known as DevSecOps. Find the balance where developers don't own security, but they aren't absolved from responsibility either. Take steps to make it everyone's problem. Create cross-functional teams and work towards tight integration between security specialists and development teams. Collaborate so your organization can resolve security risks at the speed of serverless."[22]

Privacy [edit]

Many serverless function environments are based on proprietary public cloud environments. Here, some privacy implications have to be considered, such as shared resources and access by external employees. However, serverless computing can also be done on private cloud environment or even on-premises, using for example the Kubernetes platform. This gives companies full control over privacy mechanisms, just as with hosting in traditional server setups.

Standards [edit]

Serverless computing is covered by International Data Center Authority (IDCA) in their Framework AE360.[23] However, the part related to portability can be an issue when moving business logic from one public cloud to another for which the Docker solution was created. Cloud Native Computing Foundation (CNCF) is also working on developing a specification with Oracle.[24]

Vendor lock-in [edit]

Serverless computing is provided as a third-party service. Applications and software that run in the serverless environment are by default locked to a specific cloud vendor.[25] Therefore, serverless can cause multiple issues during migration.[26]

2.1 EDA in the Cloud

- https://www.arm.com/company/news/2020/12/arm-moves-production-level-electronic-design-automation-to-the-cloud-with-the-help-of-aws;
- Serverless architecture is a good fit for Cloud-based EDA;

- Today, FOSS EDA tools are written in various programming languages. So a lightweight and common runtime is mostly preferred running these EDA software, which could greatly reduce the burden of operations and developers, and can also achieve general optimization;
- As GraalVM has strong abilities to host many programming languages and provides good interoperability at the same time. So from our point of view, GraalVM is just one of the best candidates for such a common runtime in EDA ecosystem.
  For more details, you may refer to our new talk "GraalVM as a common runtime for FOSS EDA".

2.2 GaaS

- GraalVM as a Service
- For more details, you may refer to my previous talk "Revisiting GraalVM-based unified runtime for eBPF & Wasm" at OpenInfra Days China 2021(Beijing) and the upcoming follow-ups.

2.2.1 Quarkus

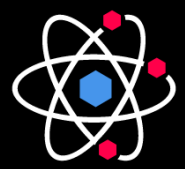
- https://quarkus.io/

  A Kubernetes Native Java stack tailored for OpenJDK HotSpot and GraalVM, crafted from the best of breed Java libraries and standards.

- Features:

Container First

Quarkus tailors your application for GraalVM and HotSpot. Amazingly fast boot time, incredibly low RSS memory (not just heap size!) offering near instant scale up and high density memory utilization in container orchestration platforms like Kubernetes. We use a technique we call compile time boot.



Unifies imperative and reactive

Combine both the familiar imperative code and the reactive style when developing applications.

Community and Standards

Quarkus provides a cohesive, fun to use, full-stack framework by leveraging a growing list of over fifty best-of-breed libraries that you love and use. All wired on a standard backbone.

Kube-Native

The combination of Quarkus and Kubernetes provides an ideal environment for creating scalable, fast, and lightweight applications. Quarkus significantly increases developer productivity with tooling, pre-built integrations, application services, and more.

Developer Joy

A cohesive platform for optimized developer joy with unified configuration and no hassle native executable generation. Zero config, live reload in the blink of an eye and streamlined code for the 80% common usages, flexible for the remainder 20%.

- https://github.com/quarkusio/quarkus

- **Amazingly fast boot time, incredibly low RSS memory!**

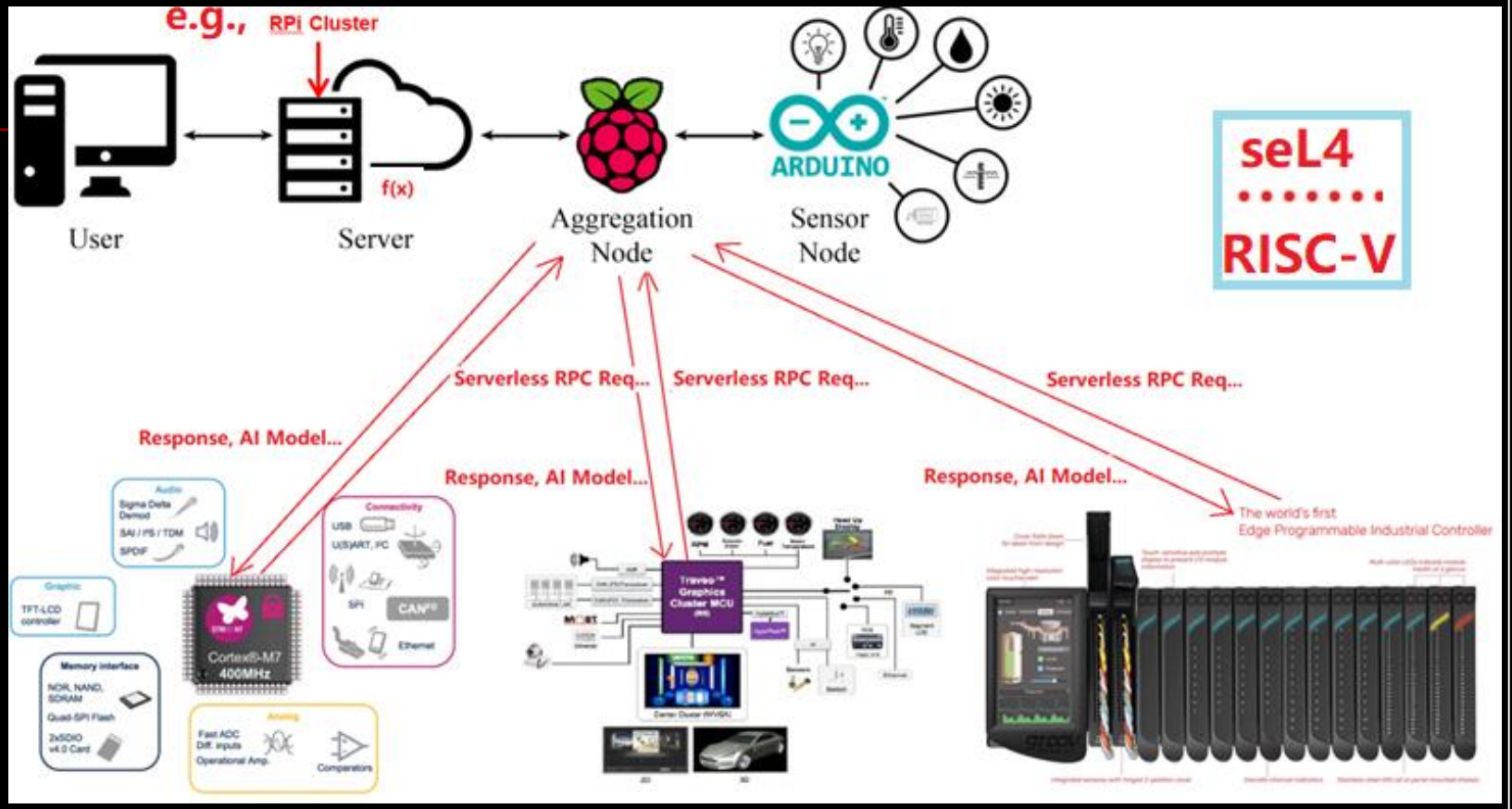
Mandrel

- **https://github.com/graalvm/mandrel**

Mandrel is a downstream distribution of the GraalVM community edition. Mandrel's main goal is to provide a `native-image` release specifically to support Quarkus. The aim is to align the `native-image` capabilities from GraalVM with OpenJDK and Red Hat Enterprise Linux libraries to improve maintainability for native Quarkus applications. Mandrel can best be described as a distribution of a regular OpenJDK with a specially packaged GraalVM Native Image builder (`native-image`).

2.3 Usage scenarios

- Case of Serverless



For more details, you may refer to my previous talk "AOT compilation based Wasm compiler and runtime for Serverless Edge computing" at OpenInfra Days China 2021(Beijing) and upcoming follow-ups.

3) Smart Runtime

3.1 What is it (from our point of view)

Traditional Runtime + AI + xBPF?

- XPU-aware compilation
- Auto-scheduling
- Auto-tuning
- Auto-debugging
- Self-enhancing
- …

3.2 Design and implementation

3.2.1 Current scheme

GraalVM + TornadoVM + eBPF + AI

- For GraalVM + TornadoVM, you may refer to our previous talk "GraalVM for Heterogeneous Parallel Computing" at OSDT China 2021(Online);
- For eBPF and AI, you may refer to our previous talk "Revisiting the eBPF-centric new approach for Hyper-Converged Infrastructure & Edge Computing" at K+ Summit 2021(Shanghai);
- And for more details on Smart Runtime, you may look forward to our new talk "The first exploration of Smart Runtime".

4) Python-centric one-stop toolchain

Ideas

- For historical reasons, most of the popular FOSS EDA software that requires high performance are implemented by C++/C, e.g., Verilator, Yosys, KiCad…another "barrier" is that LLVM is also written in C++. But most of them provides Python binding or wrapper to various extents.
- Most of the main stream AI frameworks like Tensorflow, PyTorch and MXNet embrace Python/C++ for their software layers design.
  A similar phenomenon also takes place in the world of FOSS EDA…
- Today, there are a lot of new FOSS EDA tools like F4PGA, LiteX and Cocotb are choosing Python as their primary development language, some projects are even written in pure Python.
  And many Python-based HDLs such as Amaranth/FHDL and PyGears.
- We are also deeply impressed by the successful story of PYNQ – the productivity of Python and interactive development experience with Jupyter, which inspires us to try to build a fully open-sourced Python-centric one-stop toolchain for HW-SW co-designed systems that base on RISC-V and FPGA, especially for Edge AI.

4.1 Current plans

Design Goals:

- A fully open-sourced alternative to PYNQ(Xilinx) for Edge, while supports more FPGA/eFPGA hardware.
- Well-designed modular architecture as well as with flexible plug-in mechanism.
- An Openstack-inspired but more lightweight infrastructure for FOSS EDA tools.

Integration

- A customized Jupyter for FOSS EDA.
- F4PGA + LiteX + Cocotb + Amaranth + HWT + SpyDrNet + PlatformIO…
- Plugins: FABulous, CFU-Playground, Exo…

Toolchain

- LLVM-centric.

Edge AI

- A new Torch-MLIR centric framework.
- Wasm-based runtime for resource-limited Edge device like Microcontroller.
- Add support for reinforcement learning and distributed AI by leveraging Ray AI Runtime.
- Make fully use of what from Antmicro etc.

Distributed Cooperation

- A customized version of Ray Core as the universal distributed engine.

Runtime

- Adopt GraalVM as a common runtime for FOSS EDA.
- Embrace new Python runtime for performance and HW-SW co-development purpose.

Virtual Prototyping

- Customize/re-implement Renode for our targets.

V. Wrap-up

- Next generation Core/SoC frameworks that base on eDSL bring higher productivity to hardware development.

- Open source EDA tools are booming, its ecosystem is maturing at a fast pace.
- Migrating traditional cross-platform development work from X86 hosts to that of ARM meets the trend that ARM's HW/SW ecosystem is entering a new outbreak period.
- Cost-effective development board like Raspberry Pi with strong clustering abilities provides a good base platform for developing RISC-V locally.
- Many FOSS EDA tools focus on X86 only, and may not be well-tested on other ISA like ARM and RISC-V, so in some cases, we will meet various issues and have to resolve them by ourselves …

开源社
kaiyuanshe

THANK YOU

QUESTIONS?

微信公众号：开源社KAIYUANSHE
视频号：开源社KAIYUANSHE
新浪微博：开源社
B站：2020开源社

简书：开源社
头条：开源社
Facebook：KaiyuansheChina
Twitter：KAIYUANSHE

扫码关注开源社公众号

Reference

Slides/materials from many and varied sources:

- http://en.wikipedia.org/wiki/
- http://www.slideshare.net/

- https://www.anyscale.com/ray-summit-2022/agenda
- https://www.graalvm.org/release-notes/version-roadmap/
- https://www.micahlerner.com/2021/06/27/ray-a-distributed-framework-for-emerging-ai-applications.html
- https://www.databricks.com/blog/2021/11/19/ray-on-databricks.html
- https://web.archive.org/web/20101223025529/http://www.stackless.com/
- https://iq.opengenus.org/mlir-compiler-infrastructure/
- https://en.wikipedia.org/wiki/List_of_HDL_simulators
- https://github.com/verilator/verilator/issues/2838
- …