X3M Register Reference Manual
USB Host and Device

Revision History

Revision	Date	Description
1.0	August-26-2020	Initial Release

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	0H	CAPLENGTH	R	[31:16]	HCIVERSION	16'h110	HC Interface Version Number (HCIVERSION) This is a two-byte register containing a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte contains the minor revision extensions. e.g. 0100h corresponds to xHCI version 1.0.0, or 0110h corresponds to xHCI version 1.1.0, etc.
				[15:8]	Reserved		
				[7:0]	CAPLENGTH	8'h20	Capability Registers Length (CAPLENGTH) This register is used as an offset to add to register base to find the beginning of the Operational Register Space.
	04H	HCSPARAMS1	R	[31:24]	MAXPORTS	8'h2	Number of Ports (MaxPorts) This field specifies the maximum Port Number value, i.e. the highest numbered Port Register Set that are addressable in the Operational Register Space (refer to Table 5-18 of the xHCI Specification). Valid values are in the range of 1h to FFh. The value in this field shall reflect the maximum Port Number value assigned by an xHCI Supported Protocol Capability, described in section 7.2 of the xHCI Specification. Software shall refer to these capabilities to identify whether a specific Port Number is valid, and the protocol supported by the associated Port Register Set.
				[23:19]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[18:8]	MAXINTRS	11'h1	Number of Interrupters (MaxIntrs) This field specifies the number of Interrupters implemented on this host controller. Each Interrupter may be allocated to a MSI or MSI-X vector and controls its generation and moderation. The value of this field determines how many Interrupter Register Sets are addressable in the Runtime Register Space (refer to section 5.5 of the xHCI Specification). Valid values are in the range of 1h to 400h. The value of 0 in this field is undefined.
				[7:0]	MAXSLOTS	8'h40	Number of Device Slots (MaxSlots) This field specifies the maximum number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255. The value of 0 is reserved.
	08H	HCSPARAMS2	R	[31:27]	MAXSCRATCHPADBUFS	5'h1	Max Scratchpad Buffers (Max Scratchpad Bufs Lo) Valid values for Max Scratchpad Buffers (Hi and Lo) are 0 - 1023. This field indicates the low order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to section 4.20 of the xHCI Specification for more information.
				[26]	SPR	1'h1	Scratchpad Restore (SPR) If Max Scratchpad Buffers is > 0 then this flag indicates whether the xHC uses the Scratchpad Buffers for saving state when executing Save and Restore State operations. If Max Scratchpad Buffers equal 0 then this flag shall be 0. Refer to section 4.23.2 of the xHCI Specification for more information. 0: The Scratchpad Buffer space may be freed and reallocated between power events. 1: The xHC requires the integrity of the Scratchpad Buffer space to be maintained across power events.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[25:21]	MAXSCRATCHPADBUFS_HI	5'h0	Max Scratchpad Buffers (Max Scratchpad Bufs Hi) This field indicates the high order 5 bits of the number of Scratchpad Buffers system software shall reserve for the xHC. Refer to section 4.20 of the xHCI Specification for more information.
				[20:8]	Reserved		
				[7:4]	ERSTMAX	4'hf	Event Ring Segment Table Max (ERST Max) Valid values are 0 – 15. This field determines the maximum value supported the Event Ring Segment Table Base Size registers, where: The maximum number of Event Ring Segment Table entries = 2 ERST Max. e.g. if the ERST Max = 7, then the xHC Event Ring Segment Table(s) supports up to 128 entries, 15 then 32K entries, etc.
				[3:0]	IST	4'h1	Isochronous Scheduling Threshold (IST) The value in this field indicates to system software the minimum distance (in time) that it is required to stay ahead of the host controller while adding TRBs, in order to have the host controller process them at the correct time. The value shall be specified in terms of number of frames/microframes. If bit [3] of IST is cleared to 0, software can add a TRB no later than IST[2:0] Microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1, software can add a TRB no later than IST[2:0] Frames before that TRB is scheduled to be executed. Refer to Section 4.14.2 of the xHCI Specification for details on how software uses this information for scheduling isochronous transfers.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	0CH	HCSPARAMS3	R	[31:16]	U2_DEVICE_EXIT_LAT	16'h7ff	U2 Device Exit Latency Worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: 0000h: Zero. 0001h: Less than 1 µs. 0002h: Less than 2 µs. ... 07FFh: Less than 2047 µs. 0800-FFFFh: Reserved.
				[15:8]	Reserved		
				[7:0]	U1_DEVICE_EXIT_LAT	8'ha	U1 Device Exit Latency Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: 00h: Zero. 01h: Less than 1 µs. 02h: Less than 2 µs. ... 0Ah: Less than 10 µs. 0B-FFh: Reserved.
	10H	HCCPARAMS1	R	[31:16]	XECP	16'h220	xHCI Extended Capabilities Pointer (xECP) This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability. For example, using the offset of Base is 1000h and the xECP value of 0068h, we can calculated the following effective address of the first extended capability: 1000h + (0068h << 2) -> 1000h + 01A0h -> 11A0h

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:12]	MAXPSASIZE	4'hf	Maximum Primary Stream Array Size (MaxPSASize) This fields identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = 2MaxPSASize+1. Valid MaxPSASize values are 0 to 15, where 0 indicates that Streams are not supported.
				[11]	CFC	1'h1	Contiguous Frame ID Capability (CFC) This flag indicates that the host controller implementation is capable of matching the Frame ID of consecutive Isoch TDs. Refer to section 4.11.2.5 of the xHCI Specification for more information.
				[10]	SEC	1'h1	Stopped EDTLA Capability (SEC) This flag indicates that the host controller implementation Stream Context support a Stopped EDTLA field. Refer to sections 4.6.9, 4.12, and 6.4.4.1 of the xHCI Specification for more information. Stopped EDTLA Capability support (i.e. SEC = 1) shall be mandatory for all xHCI 1.1 and xHCI 1.2 compliant xHCs.
				[9]	SPC	1'h1	Stopped - Short Packet Capability (SPC) This flag indicates that the host controller implementation is capable of generating a Stopped - Short Packet Completion Code. Refer to section 4.6.9 of the xHCI Specification for more information.
				[8]	PAE	1'h0	Parse All Event Data (PAE) This flag indicates whether the host controller implementation Parses all Event Data TRBs while advancing to the next TD after a Short Packet, or it skips all but the first Event Data TRB. 0: Only the first Event Data TRB is parsed (refer to section 4.10.1.1 of the xHCI Specification). 1: All Event Data TRBs are parsed.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	NSS	1'h0	No Secondary SID Support (NSS) This flag indicates whether the host controller implementation supports Secondary Stream IDs. 0: Secondary Stream ID decoding is supported. (refer to Sections 4.12.2 and 6.2.3 of the xHCI Specification). 1: Secondary Stream ID decoding is not supported.
				[6]	LTC	1'h1	Latency Tolerance Messaging Capability (LTC) This flag indicates whether the host controller implementation supports Latency Tolerance Messaging (LTM). 0: LTM is not supported. Refer to section 4.13.1 of the xHCI Specification for more information on LTM. 1: LTM is supported.
				[5]	LHRC	1'h1	Light HC Reset Capability (LHRC) This flag indicates whether the host controller implementation supports a Light Host Controller Reset. 0: Light Host Controller Reset is not supported. 1: Light Host Controller Reset is supported. The value of this flag affects the functionality of the Light Host Controller Reset (LHCRST) flag in the USBCMD register (refer to Section 5.4.1 of the xHCI Specification).
				[4]	PIND	1'h0	Port Indicators (PIND) This bit indicates whether the xHC root hub ports support port indicator control. When this bit is 1, the port status and control registers include a read/writeable field for controlling the state of the port indicator. Refer to Section 5.4.8 of the xHCI Specification for definition of the Port Indicator Control field.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	PPC	1'h1	Port Power Control (PPC) This flag indicates whether the host controller implementation includes port power control. A 1 in this bit indicates the ports have port power switches. A 0 in this bit indicates the port do not have port power switches. The value of this flag affects the functionality of the PP flag in each port status and control register (refer to Section 5.4.8 of the xHCI Specification).
				[2]	CSZ	1'h1	Context Size (CSZ) If this bit is set to 1, then the xHC uses 64 byte Context data structures. If this bit is cleared to 0, then the xHC uses 32 byte Context data structures.
				[1]	BNC	1'h0	BW Negotiation Capability (BNC) This flag identifies whether the xHC has implemented the Bandwidth Negotiation. Values for this flag have the following interpretation: 0: BW Negotiation not implemented. 1: BW Negotiation implemented. Refer to section 4.16 of the xHCI Specification for more information on Bandwidth Negotiation.
				[0]	AC64	1'h1	64-bit Addressing Capability77 (AC64) This flag documents the addressing range capability of this implementation. The value of this flag determines whether the xHC has implemented the high order 32 bits of 64 bit register and data structure pointer fields. Values for this flag have the following interpretation: 0: 32-bit address memory pointers implemented. 1: 64-bit address memory pointers implemented. If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64 bit data structure pointer fields, and system software shall ignore the high order 32 bits of 64 bit xHC registers.

USB Host

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
14H	DBOFF	R	[31:2]	DOORBELL_ARRAY_OFFSET	30'h120	Doorbell Array Offset This field defines the offset in Dwords of the Doorbell Array base address from the Base (i.e. the base address of the xHCI Capability register address space).
			[1:0]	Reserved		
18H	RTSOFF	R	[31:5]	RUNTIME_REG_SPACE_OFFSET	27'h22	Runtime Register Space Offset Default = 27'h22. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. i.e. Runtime Register Base Address = Base + Runtime Register Set Offset.
			[4:0]	Reserved		
1CH	HCCPARAMS2	R	[31:6]	Reserved		
			[5]	CIC	1'h1	Configuration Information Capability (CIC) This bit indicates if the xHC supports extended Configuration Information. 0: The extended Input Control Context fields are not supported. 1: The Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context are supported. Refer to section 6.2.5.1 of the xHCI Specification for more information.
			[4]	LEC	1'h0	Large ESIT Payload Capability (LEC) This bit indicates whether the xHC supports ESIT Payloads greater than 48K bytes. 0: ESIT Payloads greater than 48K bytes are not supported. 1: ESIT Payloads greater than 48K bytes are supported. Refer to section 6.2.3.8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	CTC	1'h1	Compliance Transition Capability (CTC) This bit indicates whether the xHC USB3 Root Hub ports support the Compliance Transition Enabled (CTE) flag. 0: USB3 Root Hub port state machine transitions to the Compliance substate are automatically enabled. 1: USB3 Root Hub port state machine transitions to the Compliance substate shall be explicitly enabled software. Refer to section 4.19.1.2.4.1 of the xHCI Specification for more information.
				[2]	FSC	1'h1	Force Save Context Capability (FSC) This bit indicates whether the xHC supports the Force Save Context Capability. When this bit is 1, the Save State operation shall save any cached Slot, Endpoint, Stream or other Context information to memory. Refer to Implementation Note “FSC and Context handling by Save and Restore”, and sections 4.23.2 and 5.4.1 of the xHCI Specification for more information.
				[1]	CMC	1'h1	Configure Endpoint Command Max Exit Latency Too Large Capability (CMC) This bit indicates whether a Configure Endpoint Command is capable of generating a Max Exit Latency Too Large Capability Error. 0: A Max Exit Latency Too Large Capability Error shall not be returned by a Configure Endpoint Command. 1: A Max Exit Latency Too Large Capability Error may be returned by a Configure Endpoint Command. This capability is enabled by the CME flag in the USBCMD register. Refer to sections 4.23.5.2 and 5.4.1 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	U3C	1'h1	U3 Entry Capability (U3C) This bit indicates whether the xHC Root Hub ports support port Suspend Complete notification. When this bit is 1, PLC shall be asserted on any transition of PLS to the U3 State. Refer to section 4.15.1 of the xHCI Specification for more information.
	20H	USBCMD	RW	[31:12]	Reserved		
				[11]	EU3S	1'b0	Enable U3 MFINDEX Stop (EU3S) 0: The xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, Training, or Powered-off state. 1: The xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. Refer to section 4.14.2 of the xHCI Specification for more information.
				[10]	EWE	1'b0	Enable Wrap Event (EWE) 0: No MFINDEX Wrap Events are generated. 1: The xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. Refer to section 4.14.2 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the generation of MFINDEX Wrap Events to VFs shall be emulated by the VMM.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9]	CRS	1'b0	Controller Restore State (CRS) When set to 1, and HCHalted (HCH) = 1, then the xHC shall perform a Restore State operation and restore its internal state. When set to 1 and Run/Stop (R/S) = 1 or HCHalted (HCH) = 0, or when cleared to 0, no Restore State operation shall be performed. This flag always returns 0 when read. Refer to the Restore State Status (RSS) flag in the USBSTS register for information on Restore State completion. Refer to section 4.23.2 of the xHCI Specification for more information. **Note:** Undefined behavior may occur if a Restore State operation is initiated while Save State Status (SSS) = 1. When this register is exposed by a Virtual Function (VF), this bit only controls restoring the state of the xHC instance presented by the selected VF. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[8]	CSS	1'b0	Controller Save State (CSS) When written by software with 1 and HCHalted (HCH) = 1, then the xHC shall save any internal state (that may be restored by a subsequent Restore State operation) and if FSC = 1 any cached Slot, Endpoint, Stream, or other Context information (so that software may save it). When written by software with 1 and HCHalted (HCH) = 0, or written with 0, no Save State operation shall be performed. This flag always returns 0 when read. Refer to the Save State Status (SSS) flag in the USBSTS register for information on Save State completion. Refer to section 4.23.2 of the xHCI Specification for more information on xHC Save/Restore operation. **Note:** Undefined behavior may occur if a Save State operation is initiated while Restore State Status (RSS) = 1. When this register is exposed by a Virtual Function (VF), this bit only controls saving the state of the xHC instance presented by the selected VF. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	LHCRST	1'b0	Light Host Controller Reset (LHCRST) If the Light HC Reset Capability (LHRC) bit in the HCCPARAMS1 register is 1, then this flag allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0 indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as 1 indicates the Light Host Controller Reset has not yet completed. If not implemented, a read of this flag shall always return 0. All registers in the Aux Power well shall maintain the values that had been asserted prior to the Light Host Controller Reset. Refer to section 4.23.1 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), this bit only generates a Light Reset to the xHC instance presented by the selected VF, e.g. Disable the VFs' device slots and set the associated VF Run bit to Stopped. Refer to section 8 of the xHCI Specification for more information.
				[6:4]	Reserved		
				[3]	HSEE	1'b0	Host System Error Enable (HSEE) When this bit is 1, and the HSE bit in the USBSTS register is 1, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit. Refer to section 4.10.2.6 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the effect of the assertion of this bit on the Physical Function (PF0) is determined by the VMM. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	INTE	1'b0	Interrupter Enable (INTE) This bit provides system software with a means of enabling or disabling the host system interrupts generated by Interrupters. When this bit is 1, then Interrupter host system interrupt generation is allowed, e.g. the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (e.g. MSI, MSI-X, etc.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism. When this register is exposed by a Virtual Function (VF), this bit only enables the set of Interrupters assigned to the selected VF. Refer to section 7.7.2 of the xHCI Specification for more information.
				[1]	HCRST	1'b0	Host Controller Reset (HCRST) This control bit is used by software to reset the host controller. The effects of this bit on the xHC and the Root Hub registers are similar to a Chip Hardware Reset. When software writes 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on the USB is immediately terminated. A USB reset shall not be driven on USB2 downstream ports, however a Hot or Warm Reset shall be initiated on USB3 Root Hub downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Software shall reinitialize the host controller as described in Section 4.2 of the xHCI Specification in order to return the host controller to an operational state.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							This bit is cleared to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing 0 to this bit and shall not write any xHC Operational or Runtime registers until while HCRST is 1. **Note:** The completion of the xHC reset process is not gated by the Root Hub port reset process. Software shall not set this bit to 1 when the HCHalted (HCH) bit in the USBSTS register is 0. Attempting to reset an actively running host controller may result in undefined behavior. When this register is exposed by a Virtual Function (VF), this bit only resets the xHC instance presented by the selected VF. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				0	R_S	1'b0	Run/Stop (R/S) 0: Stop. The xHC completes any current or queued commands or TDs, and any USB transactions associated with them, then halts. 1: Run. The xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1. Refer to section 5.4.1.1 of the xHCI Specification for more information on how R/S shall be managed. The xHC shall halt within 16 ms. after software clears the Run/Stop bit if the above conditions have been met. The HCHalted (HCH) bit in the USBSTS register indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write 1 to this flag unless the xHC is in the Halted state (i.e. HCH in the USBSTS register is 1). Doing so may yield undefined results. Writing 0 to this flag when the xHC is in the Running state (i.e. HCH = 0) and any Event Rings are in the Event Ring Full state (refer to section 4.9.4 of the xHCI Specification) may result in lost events.
	24H	USBSTS	R	[31:13]	Reserved		
			R	[12]	HCE	1'b0	Host Controller Error (HCE) 0: No internal xHC error conditions exist. 1: Internal xHC error condition. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and reinitialize the xHC. Refer to section 4.24.1 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[11]	CNR	1'b1	Controller Not Ready (CNR) 0: Ready. 1: Not Ready. Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0. This flag is set by the xHC after a Chip Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0) until the next Chip Hardware Reset.
			W1C	[10]	SRE	1'b0	Save/Restore Error (SRE) If an error occurs during a Save or Restore operation this bit shall be set to 1. This bit shall be cleared to 0 when a Save or Restore operation is initiated or when written with 1. Refer to section 4.23.2 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Save/Restore completion status for the selected VF. Refer to section 8 of the xHCI Specification for more information.
			R	[9]	RSS	1'b0	Restore State Status (RSS) When the Controller Restore State (CRS) flag in the USBCMD register is written with 1 this bit shall be set to 1 and remain 1 while the xHC restores its internal state. When the Restore State operation is complete, this bit shall be cleared to 0. Refer to section 4.23.2 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the restoring the state for the selected VF. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[8]	SSS	1'b0	Save State Status (SSS) When the Controller Save State (CSS) flag in the USBCMD register is written with 1 this bit shall be set to 1 and remain 1 while the xHC saves its internal state. When the Save State operation is complete, this bit shall be cleared to 0. Refer to section 4.23.2 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the saving the state for the selected VF. Refer to section 8 of the xHCI Specification for more information.
			R	[7:5]	Reserved		
			W1C	[4]	PCD	1'b0	Port Change Detect (PCD) The xHC sets this bit to 1 when any port has a change bit transition from 0 to 1. This bit is allowed to be maintained in the Aux Power well. Alternatively, it is also acceptable that on a D3 to D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits. Refer to section 4.19.3 of the xHCI Specification. This bit provides system software an efficient means of determining if there has been Root Hub port activity. Refer to section 4.15.2.3 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the VMM determines the state of this bit as a function of the Root Hub Ports associated with the Device Slots assigned to the selected VF. Refer to section 8 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[3]	EINT	1'b0	Event Interrupt (EINT) The xHC sets this bit to 1 when the Interrupt Pending (IP) bit of any Interrupter transitions from 0 to 1. Refer to section 7.1.2 of the xHCI Specification for use. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition may occur if software clears the IP flags then clears the EINT flag, and between the operations another IP 0 to 1 transition occurs. In this case the new IP transition shall be lost. When this register is exposed by a Virtual Function (VF), this bit is the logical 'OR' of the IP bits for the Interrupters assigned to the selected VF. And it shall be cleared to 0 when all associated interrupter IP bits are cleared, i.e. all the VF's Interrupter Event Ring(s) are empty. Refer to section 8 for more information.
			W1C	[2]	HSE	1'b0	Host System Error (HSE) The xHC sets this bit to 1 when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. (In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort.) When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USBCMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USBCMD register is 1, the xHC shall also assert out-of-band error signaling to the host. Refer to section 4.10.2.6 of the xHCI Specification for more information. When this register is exposed by a Virtual Function (VF), the assertion of this bit affects all VFs and reflects the Host System Error state of the Physical Function (PF0). Refer to section 8 of the xHCI Specification for more information.
			R	[1]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[0]	HCH	1'b1	HCHalted (HCH) This bit is 0 whenever the Run/Stop (R/S) bit is 1. The xHC sets this bit to 1 after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0, either by software or by the xHC hardware (e.g. internal error). If this bit is 1, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC, and any received Transaction Packet shall be dropped. When this register is exposed by a Virtual Function (VF), this bit only reflects the Halted state of the xHC instance presented by the selected VF. Refer to section 8 for more information.
	28H	PAGESIZE	R	[31:16]	Reserved		
				[15:0]	Page_Size	16'b1	Page Size This field defines the page size supported by the xHC implementation. This xHC supports a page size of 2^(n+12) if bit n is Set. For example, if bit 0 is Set, the xHC supports 4k byte page sizes. For a Virtual Function, this register reflects the page size selected in the System Page Size field of the SR-IOV Extended Capability structure. For the Physical Function 0, this register reflects the implementation dependent default xHC page size. Various xHC resources reference PAGESIZE to describe their minimum alignment requirements. The maximum possible page size is 128M.
	34H	DNCTRL	RW	[31:16]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:0]	Notification Enable (N0-N15)	16'b0	Notification Enable (N0-N15) When a Notification Enable bit is set, a Device Notification Event shall be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to 1 enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to 1 (FUNCTION_WAKE), etc.
	38H	CRCR_DWord0	RW	[31:6]	CRP_Lo	26'b0	Command Ring Pointer This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer. Writes to this field are ignored when Command Ring Running (CRR) = 1. If the CRCR is written while the Command Ring is stopped (CRR = 0), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0) then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer. Reading this field always returns 0.
			R	[5:4]	Reserved		
			R	[3]	CRR	1'b0	Command Ring Running (CRR) This flag is set to 1 if the Run/Stop (R/S) bit is 1 and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0 when the Command Ring is “stopped” after writing 1 to the Command Stop (CS) or Command Abort (CA) flags, or if the R/S bit is cleared to 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1S	[2]	CA	1'b0	Command Abort (CA) Writing 1 to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped. Refer to section 4.6.1.2 of the xHCI Specification for more information on aborting a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit always returns 0.
			W1S	[1]	CS	1'b0	Command Stop (CS) Writing 1 to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer. Refer to section 4.6.1.1 of the xHCI Specification for more information on stopping a command. The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation. Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0. Reading this bit shall always return 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[0]	RCS	1'b0	Ring Cycle State (RCS) This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer. Refer to section 4.9.3 of the xHCI Specification for more information. Writes to this flag are ignored if Command Ring Running (CRR) is 1. If the CRCR is written while the Command Ring is stopped (CRR = 0), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. If the CRCR is not written while the Command Ring is stopped (CRR = 0), then the Command Ring shall begin fetching Command TRBs using the current value of the internal Command Ring CCS flag. Reading this flag always returns 0.
	3CH	CRCR_DWord1	RW	[31:0]	CRP_Hi	32'b0	Command Ring Pointer CRP[63:32], high order bits of CRP.
	50H	DCBAAP_DWord0	RW	[31:6]	DCBAAP_Lo	26'b0	Device Context Base Address Array Pointer This field defines high order bits of the 64-bit base address of the Device Context Pointer Array. A table of address pointers that reference Device Context structures for the devices attached to the host.
				[5:0]	Reserved		
	54H	DCBAAP_DWord1	RW	[31:0]	DCBAAP_Hi	32'b0	Device Context Base Address Array Pointer DCBAAP[63:32], high order bits of DCBAAP.
	58H	CONFIG	RW	[31:10]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9]	CIE	1'b0	Configuration Information Enable (CIE) When set to 1, the software shall initialize the Configuration Value, Interface Number, and Alternate Setting fields in the Input Control Context when it is associated with a Configure Endpoint Command. When this bit is 0, the extended Input Control Context fields are not supported. Refer to section 6.2.5.1 of the xHCI Specification for more information.
				[8]	U3E	1'b0	U3 Entry Enable (U3E) The xHC shall assert the PLC flag (1) when a Root Hub port transitions to the U3 State. Refer to section 4.15.1 of the xHCI Specification for more information.
				[7:0]	MaxSlotsEn	8'b0	Max Device Slots Enabled (MaxSlotsEn) This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0 to MaxSlots. Enabled Devices Slots are allocated contiguously. e.g. A value of 16 specifies that Device Slots 1 to 16 are active. A value of 0 disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references. This field shall not be modified by software if the xHC is running (Run/Stop (R/S) = 1).
	420H	PORTSC_20	R	[31]	Reserved		
			R	[30]	DR	1'b0	Device Removable97 (DR) This flag indicates if this port has a removable device attached. 0: Device is removable. 1: Device is non-removable.
			R	[29:28]	Reserved		
			RW	[27]	WOE	1'b0	Wake on Over-current Enable (WOE) Writing 1 to this bit enables the port to be sensitive to over-current conditions as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[26]	WDE	1'b0	Wake on Disconnect Enable (WDE) Writing 1 to this bit enables the port to be sensitive to device disconnects as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.
			RW	[25]	WCE	1'b0	Wake on Connect Enable (WCE) Writing 1 to this bit enables the port to be sensitive to device connects as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.
			R	[24]	CAS	1'b0	Cold Attach Status (CAS) 1: Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Refer to sections 4.19.8 of the xHCI Specification for more details on the Cold Attach Status (CAS) assertion conditions. Software shall clear this bit by writing 1 to WPR or the xHC shall clear this bit if CCS transitions to 1. This flag is 0 if PP is 0 or for USB2 protocol ports.
			R	[23]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[22]	PLC	1'b0	Port Link State Change (PLC) This flag is set to 1 due to the following PLS transitions: U3 -> Resume: Wakeup signaling from a device. Resume -> Recovery -> U0: Device Resume complete (USB3 protocol ports only). Resume -> U0: Device Resume complete (USB2 protocol ports only). U3 -> Recovery -> U0: Software Resume complete (USB3 protocol ports only). U3 -> U0: Software Resume complete (USB2 protocol ports only). U2 -> U0: L1 Resume complete (USB2 protocol ports only). U0 -> U0: L1 Entry Reject (USB2 protocol ports only). Any State -> U3: U3 Entry complete. **Note:** PLC is asserted only if U3E = 1. Any state -> Inactive: Error (USB3 protocol ports only). **Note:** This flag shall not be set if the PLS transition was due to software setting PP to 0. Refer to section 4.23.5 for more information. 0: No change. 1: Link Status Changed. Software shall clear this bit by writing a 1 to it. Refer to "PLC Condition:" references in section 4.19.1 of the xHCI Specification for the specific port state transitions that set this flag. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[21]	PRC	1'b0	Port Reset Change (PRC) This flag is set to 1 due to a 1 to 0 transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. **Note:** This flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to 0. 0: No change. 1: Reset complete. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.5 of the xHCI Specification Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.
			W1C	[20]	OCC	1'b0	Over-current Change (OCC) This bit shall be set to 1 when there is 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.
			R	[19]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[18]	PEC	1'b0	Port Enabled/Disabled Change (PEC) 0: No change. 1: change in PED. **Note:** This flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[17]	CSC	1'b0	Connect Status Change (CSC) 0: No change. 1: Change in CCS. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. **Note:** This flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status92, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.
			RW	[16]	LWS	1'b0	Port Link State Write Strobe (LWS) When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
			RW	[15:14]	PIC	2'd0	Port Indicator Control (PIC) Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS1 register is 0. If PIND bit is 1, then the bit encodings are: 0: Port indicators are off. 1: Amber. 2: Green . 3: Undefined. This field is 0 if PP is 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[13:10]	Port_Speed	4'd0	Port Speed (Port Speed) This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed. Refer to section 4.19.3 of the xHCI Specification. 0: Undefined Speed. 1 - 15: Protocol Speed ID (PSI), refer to section 7.2.1 of the xHCI Specification for the definition of PSIV field in the PSI Dword. **Note:** This field is invalid on a USB2 protocol port until after the port is reset.
			RW	[9]	PP	1'b1	Port Power (PP) This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a 0 the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again91, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							If the Port Power Control (PPC) flag in the HCCPARAMS1 register is 1, then xHC has port power control switches and this bit represents the current setting of the switch (0 = off, 1 = on). If the Port Power Control (PPC) flag in the HCCPARAMS1 register is 0, then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from 1 to 0 (removing power from the port). Refer to section 4.19.4 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[8:5]	PLS	4'd5	Port Link State (PLS) This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. CTE = 1. Refer to section 4.19.1.2.4.1 for more information. 1, 4, 6 - 9, 11 - 14 Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the Resume substate, else ignored. Refer to section 4.15.2 for more information. **Note:** The Port Link State Write Strobe (LWS) shall also be set to 1 to write this . For USB2 protocol ports: Writing a value of 2 to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of 0 shall deassert L1 signaling on the USB. Writing a value of 1 shall have no effect. The U1 state shall never be reported by a USB2 protocol port.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							Read value and its meaning: 0: Link is in the U0 State. 1: Link is in the U1 State. 2: Link is in the U2 State. 3: Link is in the U3 State (Device Suspended). 4: Link is in the Disabled State. 5: Link is in the RxDetect State. 6: Link is in the Inactive State. 7: Link is in the Polling State. 8: Link is in the Recovery State. 9: Link is in the Hot Reset State. 10: Link is in the Compliance Mode State. 11: Link is in the Test Mode State. 12-14: Reserved. 15: Link is in the Resume State. This field is undefined if PP = 0. **Note:** Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 for PLS transition conditions.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1S	4	PR	1'b0	Port Reset (PR) 0: Port is not in Reset. 1: Port Reset signaling is asserted. When software writes 1 to this bit generating 0 to 1 transition, the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Specification. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Spec. PR remains set until reset signaling is completed by the root hub. **Note:** Software shall write 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1 of the xHCI Specification This flag is 0 if PP is 0.
			R	3	OCA	1'b0	Over-current Active (OCA) 0: This port does not have an over-current condition. 1: This port currently has an over-current condition. This bit shall automatically transition from 1 to 0 when the over-current condition is removed.
			R	2	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	1	PED	1'b0	Port Enabled/Disabled (PED) 0: Disabled. 1: Enabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing 1 to this flag. A port may be disabled by software writing 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB2 protocol ports: When the port is in the Disabled state, software shall reset the port (PR = 1) to transition PED to 1 and the port to the Enabled state. **Note:** When software writes this bit to 1, it shall also write 0 to the PR bit. This flag is 0 if PP is 0.
			R	0	CCS	1'b0	Current Connect Status (CCS) 0: A device is not connected. 1: A device is connected81 to the port. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 of the xHCI Specification for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	424H	PORTPMSC_20	RW	[31:28]	Port_Test_Control	4'd0	Port Test Control (Test Mode) When this field is 0, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Powered-Off state (PLS = Disabled). If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. Refer to section 4.19.6 of the xHCI Specification for the operational model for using these test modes. The encoding of the Test Mode bits for a USB2 protocol port are: 0: Test mode not enabled. 1: Test J_STATE. 2: Test K_STATE. 3: Test SE0_NAK. 4: Test Packet. 5: Test FORCE_ENABLE. 6-14: Reserved. 15: Port Test Control Error. Refer to the sections 7.1.20 and 11.24.2.13 of the USB2 spec for more information on Test Modes.
			R	[27:17]	Reserved		
			RW	[16]	HLE	1'd0	Hardware LPM Enable (HLE) If this bit is set to 1, then hardware controlled LPM shall be enabled for this port. Refer to section 4.23.5.1.1.1 of the xHCI Specification. If the USB2 Hardware LPM Capability is not supported (HLC = 0) this field shall be reserved. **Note:** BESL LPM Capability support (i.e. HLE = 1 and BLC = 1) shall be mandatory for all xHCI 1.1 and xHCI 1.2 compliant xHCs.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[15:8]	L1_Device_Slot	8'd0	L1 Device Slot System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of 0 indicates no device is present. The xHC uses this field to lookup information necessary to generate the LPM Token packet.
			RW	[7:4]	BESL	4'd0	Best Effort Service Latency (BESL) System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. **Note:** The BESL field is used by both software and hardware controlled LPM. Refer to section 4.23.5.1.1 of the xHCI Specification for more information on BESL use. Refer to section 5.2.5 of the xHCI Specification for information on how DBESL may be used to establish an initial value for BESL.
			RW	[3]	RWE	1'd0	Remote Wake Enable (RWE) System software sets this flag to enable or disable the device for remote wake from L1. The value of this flag shall temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, revision 2.0, Chapter 9.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[2:0]	L1S	3'd0	L1 Status (L1S) This field is used by software to determine whether an L1-based suspend request (LPM transaction) was successful, specifically: 0: Invalid - This field shall be ignored by software. 1: Success - Port successfully transitioned to L1 (ACK). 2: Not Yet - Device is unable to enter L1 at this time (NYET). 3: Not Supported - Device does not support L1 transitions (STALL). 4: Timeout/Error - Device failed to respond to the LPM Transaction or an error occurred. 5-7: Reserved. The value of this field is only valid when the port resides in the L0 or L1 state (PLS = 0 or 2). Refer to section 4.23.5.1.1 of the xHCI Specification for more information.
	428H	PORTLI_20	RO	[31:0]	Reserved		
	42CH	PORTHLPMC_20	RW	[31:14]	Reserved		
				[13:10]	BESLD	4'd0	Best Effort Service Latency Deep (BESLD) System software sets this field to indicate to the recipient device how long the xHC will drive resume on an exit from U2. Refer to section 4.23.5.1.1.1 of the xHCI Specification for more information on BESLD use. The BESLD value encoding is defined in Table 13. Refer to section 5.2.6 for information on how DBESLD may be used to establish an initial value for BESLD.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9:2]	L1_Timeout	8'd0	L1 Timeout Timeout value for the L1 inactivity timer (LPM Timer). This field shall be set to 00h by the assertion of PR to 1. Refer to section 4.23.5.1.1.1 of the xHCI Specification for more information on L1 Timeout operation. The following are permissible values: 00h: 128 µs. (default) 01h: 256 µs. 02h: 512 µs. 03h: 768 µs. ... FFh: 65,280 µs.
				[1:0]	HIRDM	2'd0	Host Initiated Resume Duration Mode (HIRDM) Indicates which HIRD value should be used. The following are permissible values: 0: Initiate L1 using BESL only on timeout. (default) 1: Initiate L1 using BESLD on timeout. If rejected by device, initiate L1 using BESL. 3-2: Reserved.
	430H	PORTSC_30	W1S	[31]	WPR	1'b0	Warm Port Reset (WPR) When software writes 1 to this bit, the Warm Reset sequence as defined in the USB3 Specification is initiated and the PR flag is set to 1. Once initiated, the PR, PRC, and WRC flags shall reflect the progress of the Warm Reset sequence. This flag shall always return 0 when read. Refer to section 4.19.5.1 of the xHCI Specification
			R	[30]	DR	1'b0	Device Removable97 (DR) This flag indicates if this port has a removable device attached. 0: Device is removable. 1: Device is non-removable.
			R	[29:28]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[27]	WOE	1'b0	Wake on Over-current Enable (WOE) Writing 1 to this bit enables the port to be sensitive to over-current conditions as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.
			RW	[26]	WDE	1'b0	Wake on Disconnect Enable (WDE) Writing 1 to this bit enables the port to be sensitive to device disconnects as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.
			RW	[25]	WCE	1'b0	Wake on Connect Enable (WCE) Writing 1 to this bit enables the port to be sensitive to device connects as system wake-up events96. Refer to section 4.15 of the xHCI Specification for operational model.
			R	[24]	CAS	1'b0	Cold Attach Status (CAS) 1: Far-end Receiver Terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Refer to sections 4.19.8 of the xHCI Specification for more details on the Cold Attach Status (CAS) assertion conditions. Software shall clear this bit by writing 1 to WPR or the xHC shall clear this bit if CCS transitions to 1. This flag is 0 if PP is 0 or for USB2 protocol ports.
			W1C	[23]	CEC	1'b0	Port Config Error Change (CEC) This flag indicates that the port failed to configure. 0: No change. 1: Port Config Error detected. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[22]	PLC	1'b0	Port Link State Change (PLC) This flag is set to 1 due to the following PLS transitions: U3 -> Resume: Wakeup signaling from a device. Resume -> Recovery -> U0: Device Resume complete (USB3 protocol ports only). Resume -> U0: Device Resume complete (USB2 protocol ports only). U3 -> Recovery -> U0: Software Resume complete (USB3 protocol ports only). U3 -> U0: Software Resume complete (USB2 protocol ports only). U2 -> U0: L1 Resume complete (USB2 protocol ports only). U0 -> U0: L1 Entry Reject (USB2 protocol ports only). Any State -> U3: U3 Entry complete. **Note:** PLC is asserted only if U3E = 1. Any state -> Inactive: Error (USB3 protocol ports only). **Note:** This flag shall not be set if the PLS transition was due to software setting PP to 0. Refer to section 4.23.5 for more information. 0: No change. 1: Link Status Changed. Software shall clear this bit by writing a 1 to it. Refer to "PLC Condition:" references in section 4.19.1 of the xHCI Specification for the specific port state transitions that set this flag. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[21]	PRC	1'b0	Port Reset Change (PRC) This flag is set to 1 due to a 1 to 0 transition of Port Reset (PR). e.g. when any reset processing (Warm or Hot) on this port is complete. **Note:** This flag shall not be set to 1 if the reset processing was forced to terminate due to software clearing PP or PED to 0. 0: No change. 1: Reset complete. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.5 of the xHCI Specification Refer to section 4.19.2 of the xHCI Specification or more information on change bit usage.
			W1C	[20]	OCC	1'b0	Over-current Change (OCC) This bit shall be set to 1 when there is 0 to 1 or 1 to 0 transition of Over-current Active (OCA). Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.
			W1C	[19]	WRC	1'b0	Warm Port Reset Change (WRC) This bit is set when Warm Reset processing on this port completes. 0: No change. 1: Warm Reset complete. **Note:** This flag shall not be set to 1 if the Warm Reset processing was forced to terminate due to software clearing PP or PED to 0. Software shall clear this bit by writing a 1 to it. Refer to section 4.19.5.1. of the xHCI Specification Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[18]	PEC	1'b0	Port Enabled/Disabled Change (PEC) 0: No change. 1: change in PED. **Note:** This flag shall not be set if the PED transition was due to software setting PP to 0. Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 of the xHCI Specification for more information on change bit usage. For a USB2 protocol port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point (refer to section 11.8.1 of the USB2 Specification for the definition of a Port Error). For a USB3 protocol port, this bit shall never be set to 1.
			W1C	[17]	CSC	1'b0	Connect Status Change (CSC) This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits. 0: No change. 1: Change in CCS. **Note:** This flag shall not be set if the CCS transition was due to software setting PP to 0, or the CAS transition was due to software setting WPR to 1. The xHC sets this bit to 1 for all changes to the port device connect status92, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (i.e., the bit will remain 1). Software shall clear this bit by writing 1 to it. Refer to section 4.19.2 for more information on change bit usage.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[16]	LWS	1'b0	Port Link State Write Strobe (LWS) When this bit is set to 1 on a write reference to this register, this flag enables writes to the PLS field. When 0, write data in PLS field is ignored. Reads to this bit return 0.
			RW	[15:14]	PIC	2'd0	Port Indicator Control (PIC) Writing to these bits has no effect if the Port Indicators (PIND) bit in the HCCPARAMS1 register is 0. If PIND bit is 1, then the bit encodings are: 0: Port indicators are off 1: Amber 2: Green 3: Undefined This field is 0 if PP is 0.
			R	[13:10]	Port_Speed	4'd0	Port Speed (Port Speed). This field identifies the speed of the connected USB Device. This field is only relevant if a device is connected (CCS = 1) in all other cases this field shall indicate Undefined Speed. Refer to section 4.19.3 of the xHCI Specification. 0: Undefined Speed 1 - 15: Protocol Speed ID (PSI), refer to section 7.2.1 of the xHCI Specification for the definition of PSIV field in the PSI Dword. **Note:** This field is invalid on a USB2 protocol port until after the port is reset.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[9]	PP	1'b1	Port Power (PP) This flag reflects a port's logical, power control state. Because host controllers can implement different methods of port power switching, this flag may or may not represent whether (VBus) power is actually applied to the port. When PP equals a 0 the port is nonfunctional and shall not report attaches, detaches, or Port Link State (PLS) changes. However, the port shall report over-current conditions when PP = 0 if PPC = 0. After modifying PP, software shall read PP and confirm that it is reached its target state before modifying it again91, undefined behavior may occur if this procedure is not followed. 0: This port is in the Powered-off state. 1: This port is not in the Powered-off state. If the Port Power Control (PPC) flag in the HCCPARAMS1 register is 1, then xHC has port power control switches and this bit represents the current setting of the switch (0 = off, 1 = on). If the Port Power Control (PPC) flag in the HCCPARAMS1 register is 0, then xHC does not have port power control switches and each port is hard wired to power, and not affected by this bit. When an over-current condition is detected on a powered port, the xHC shall transition the PP bit in each affected port from 1 to 0 (removing power from the port). Refer to section 4.19.4 of the xHCI Specification for more information.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[8:5]	PLS	4'd5	Port Link State (PLS) This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port. 0: The link shall transition to a U0 state from any of the U states. 2: USB2 protocol ports only. The link should transition to the U2 State. 3: The link shall transition to a U3 state from the U0 state. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub shall respond to resume signaling from the port. 5: USB3 protocol ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							10: USB3 protocol ports only. Shall enable a link transition to the Compliance state, i.e. CTE = 1. Refer to section 4.19.1.2.4.1 for more information. 1, 4, 6 - 9, 11 - 14 Ignored. 15: USB2 protocol ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the Resume substate, else ignored. Refer to section 4.15.2 for more information. **Note:** The Port Link State Write Strobe (LWS) shall also be set to 1 to write this . For USB2 protocol ports: Writing a value of 2 to this field shall request LPM, asserting L1 signaling on the USB2 bus. Software may read this field to determine if the transition to the U2 state was successful. Writing a value of 0 shall deassert L1 signaling on the USB. Writing a value of 1 shall have no effect. The U1 state shall never be reported by a USB2 protocol port.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							Read value and its meaning: 0: Link is in the U0 State. 1: Link is in the U1 State. 2: Link is in the U2 State. 3: Link is in the U3 State (Device Suspended). 4: Link is in the Disabled State. 5: Link is in the RxDetect State. 6: Link is in the Inactive State. 7: Link is in the Polling State. 8: Link is in the Recovery State. 9: Link is in the Hot Reset State. 10: Link is in the Compliance Mode State. 11: Link is in the Test Mode State. 12 - 14: Reserved. 15: Link is in the Resume State. This field is undefined if PP = 0. **Note:** Transitions between different states are not reflected until the transition is complete. Refer to section 4.19 for PLS transition conditions.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1S	[4]	PR	1'b0	Port Reset (PR) 0: Port is not in Reset. 1: Port Reset signaling is asserted. When software writes 1 to this bit generating 0 to 1 transition, the bus reset sequence is initiated; USB2 protocol ports shall execute the bus reset sequence as defined in the USB2 Specification. USB3 protocol ports shall execute the Hot Reset sequence as defined in the USB3 Specification. PR remains set until reset signaling is completed by the root hub. **Note:** Software shall write 1 to this flag to transition a USB2 port from the Polling state to the Enabled state. Refer to sections 4.15.2.3 and 4.19.1.1 of the xHCI Specification. This flag is 0 if PP is 0.
			R	[3]	OCA	1'b0	Over-current Active (OCA) 0: This port does not have an over-current condition. 1: This port currently has an over-current condition. This bit shall automatically transition from 1 to 0 when the over-current condition is removed.
			R	[2]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W1C	[1]	PED	1'b0	Port Enabled/Disabled (PED) – RW1CS. 0: Disabled. 1: Enabled. Ports may only be enabled by the xHC. Software cannot enable a port by writing 1 to this flag. A port may be disabled by software writing 1 to this flag. This flag shall automatically be cleared to 0 by a disconnect event or other fault condition. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller or bus events. When the port is disabled (PED = 0) downstream propagation of data is blocked on this port, except for reset. For USB3 protocol ports: When the port is in the Polling state (after detecting an attach), the port shall automatically transition to the Enabled state and set PED to 1 upon the completion of successful link training. When the port is in the Disabled state, software shall write 5 (RxDetect) to the PLS field to transition the port to the Disconnected state. Refer to section 4.19.1.2 of the xHCI Specification PED shall automatically be cleared to 0 when PR is set to 1, and set to 1 when PR transitions from 1 to 0 after a successful reset. Refer to Port Reset (PR) bit for more information on how the PED bit is managed. **Note:** When software writes this bit to 1, it shall also write 0 to the PR bit. This flag is 0 if PP is 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[0]	CCS	1'b0	Current Connect Status (CCS) 0: A device is not connected. 1: A device is connected81 to the port. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change (CSC) bit to be set to 1. Refer to sections 4.19.3 and 4.19.4 of the xHCI Specification for more details on the Connect Status Change (CSC) assertion conditions. This flag is 0 if PP is 0.
	434H	PORTPMSC_30	RW	[31:17]	Reserved		
				[16]	FLA	1'b0	Force Link PM Accept (FLA) 0: The port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit de-asserted (0). 1: The port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted (1). This flag shall be set to 0 by the assertion of PR to 1 or when CCS = transitions from 0 to 1. Writes to this flag have no effect if PP = 0. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from 0 to 1 or 1 to 0. Refer to Sections 8.4.2 and 10.14.2.2 of the USB3 specification for more details. Improper use of the SS Force_LinkPM_Accept functionality can impact the performance of the link significantly. This bit shall only be used for compliance and testing purposes. Software shall ensure that there are no pending packets at the link level before setting this bit. This flag is 0 if PP is 0.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:8]	U2_Timeout	1'b0	U2 Timeout Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to 0 by the assertion of PR to 1. Refer to section 4.19.4.1 of the xHCI Specification for more information on U2 Timeout operation. The following are permissible values: 00h: Zero (default). 01h: 256 µs. 02h: 512 µs. ... FEh: 65,024 ms. FFh: Infinite. A U2 Inactivity Timeout LMP shall be sent by the xHC to the device connected on this port when this field is written. Refer to Sections 8.4.3 of the xHCI Specification and 10.4.2.10 of the USB3 specification for more details.
				[7:0]	U1_Timeout	1'b0	U1 Timeout Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to 0 by the assertion of PR to 1. Refer to section 4.19.4.1 of the xHCI Specification for more information on U1 Timeout operation. The following are permissible values: 00h: Zero (default). 01h: 1 µs. 02h: 2 µs. ... 7Fh: 127 µs. 80h–FEh: Reserved. FFh: Infinite.
	438H	PORTLI_30	R	[31:16]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:0]	Link_Error_Count	1'b0	Link Error Count This field returns the number of link errors detected by the port. This value shall be reset to 0 by the assertion of a Chip Hardware Reset, HCRST, when PR transitions from 1 to 0, or when reset by software by writing 0 to it. This register will increment by one each time a port transitions from U0 to Recovery to recover an error event and will saturate at max.
	43CH	PORTHLPMC_30	R	[31:0]	Reserved		
	440H	MFINDEX	R	[31:14]	Reserved		
				[13:0]	Microframe_Index	14'b0	Microframe Index The value in this register increments at the end of each microframe (e.g. 125us.). Bits [13:3] may be used to determine the current 1ms. Frame Index.
	460H	IMAN	R	[31:2]	Reserved		
			RW	[1]	IE	1'b0	Interrupt Enable (IE) This flag specifies whether the Interrupter is capable of generating an interrupt. When this bit and the IP bit are set (1), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0. If this bit is 0, then the Interrupter is prohibited from generating interrupts.
			W1C	[0]	IP	1'b0	Interrupt Pending (IP) This flag represents the current state of the Interrupter. If IP = 1, an interrupt is pending for this Interrupter. A value of 0 indicates that no interrupt is pending for the Interrupter. Refer to section 4.17.3 of the xHCI Specification for the conditions that modify the state of this flag.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	464H	IMOD	RW	[31:16]	IMODC	16'b0	Interrupt Moderation Counter (IMODC) Down counter. Loaded with the IMODI value whenever IP is cleared to 0, counts down to 0, and stops. The associated interrupt shall be signaled whenever this counter is 0, the Event Ring is not empty, the IE and IP flags = 1, and EHB = 0. This counter may be directly written by software at any time to alter the interrupt rate.
				[15:0]	IMODI	16'd4000	Interrupt Moderation Interval (IMODI) Default = '4000' (~1ms). Minimum inter-interrupt interval. The interval is specified in 250ns increments. A value of 0 disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.
	468H	ERSTSZ	RW	[31:16]	Reserved		
				[15:0]	ERSTSZ	16'b0	Event Ring Segment Table Size This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register. The maximum value supported by an xHC implementation for this register is defined by the ERST Max field in the HCSPARAMS2 register. For Secondary Interrupters: Writing 0 to this field disables the Event Ring. Any events targeted at this Event Ring when it is disabled shall result in undefined behavior of the Event Ring. For the Primary Interrupter: Writing 0 to this field shall result in undefined behavior of the Event Ring. The Primary Event Ring cannot be disabled.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	470H	ERSTBA_DWord0	RW	[31:6]	ERSTBA_Lo	26'b0	Event Ring Segment Table Base Address Register This field defines the high order bits of the start address of the Event Ring Segment Table. Writing this register sets the Event Ring State Machine: EREP Advancement to the Start state. Refer to Figure 4-12 of the xHCI Specification for more information. For Secondary Interrupters: This field may be modified at any time. For the Primary Interrupter: This field shall not be modified if HCHalted (HCH) = 0.
			R	[5:0]	Reserved		
	474H	ERSTBA_DWord1	RW	[31:0]	ERSTBA_Hi	32'b0	Event Ring Segment Table Base Address Register ERSTBA[63:32], high order bits of ERSTBA.
	478H	ERDP_DWord0	RW	[31:4]	ERDP_Lo	28'b0	Event Ring Dequeue Pointer This field defines the high order bits of the 64-bit address of the current Event Ring Dequeue Pointer.
			W1C	[3]	EHB	1'b0	Event Handler Busy (EHB) This flag shall be set to 1 when the IP bit is set to 1 and cleared to 0 by software when the Dequeue Pointer register is written. Refer to section 4.17.2 of the xHCI Specification for more information.
			RW	[2:0]	DESI	3'b0	Dequeue ERST Segment Index (DESI) This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low order 3 bits of the offset of the ERST entry which defines the Event Ring segment that the Event Ring Dequeue Pointer resides in. Refer to section 6.5 of the xHCI Specification for the definition of an ERST entry.
	47CH	ERDP_DWord1	RW	[31:0]	ERDP_Hi	32'b0	Event Ring Dequeue Pointer ERDP[63:32], high order bits of ERDP.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	480H	Doorbell_Register	RW	[31:16]	DB_Stream_ID	16'b0	DB Stream ID Doorbell Stream ID. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint defines Streams (MaxPStreams > 0), then 0, 65535 (No Stream) and 65534 (Prime) are reserved Stream ID values and shall not be written to this field. If the endpoint does not define Streams (MaxPStreams = 0) and a non-0 value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to 0 for Host Controller Command Doorbells. This field returns 0 when read.
				[15:8]	Reserved		
				[7:0]	DB_Target	8'b0	Doorbell Target This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Device Context Doorbells (1 - 255) 0: Reserved 1: Control EP 0 Enqueue Pointer Update 2: EP 1 OUT Enqueue Pointer Update 3: EP 1 IN Enqueue Pointer Update 4: EP 2 OUT Enqueue Pointer Update 5: EP 2 IN Enqueue Pointer Update

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							... 30: EP 15 OUT Enqueue Pointer Update 31: EP 15 IN Enqueue Pointer Update 32 - 247: Reserved 248 - 255: Vendor Defined Host Controller Doorbell (0) 0: Command Doorbell 1 - 247: Reserved 248 - 255: Vendor Defined This field returns 0 when read and should be treated as “ undefined” by software. When the Command Doorbell is written, the DB Stream ID field shall be cleared to 0.
	880H	USBLEGSUP	R	[31:25]	Reserved		
			RW	[24]	HC_OS_Owned_Semaphore	1'h0	HC OS Owned Semaphore System software sets this bit to request ownership of the xHC. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as 0.
			R	[23:17]	Reserved		
			RW	[16]	HC_BIOS_Owned_Semaphore	1'h0	HC BIOS Owned Semaphore The BIOS sets this bit to establish ownership of the xHC. System BIOS will set this bit to 0 in response to a request for ownership of the xHC by system software.
			R	[15:8]	Next_Capability_Pointer	8'h4	Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 7-1 of the xHCI Specification for more information on this field.

USB Host

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
		R	[7:0]	Capability_ID	8'd1	Capability ID This field identifies the extended capability. Refer to Table 7-2 of the xHCI Specification for the value that identifies the capability as Legacy Support. This extended capability requires one additional 32-bit register for control/status information (USBLEGCTLSTS).
884H	USBLEGCTLSTS	W1C	[31]	SMI_On_BAR	1'h0	SMI on BAR This bit is set to 1 whenever the Base Address Register (BAR) is written.
		W1C	[30]	SMI_On_PCI_Command	1'h0	SMI on PCI Command This bit is set to 1 whenever the PCI Command Register is written.
		W1C	[29]	SMI_On_OS_Ownership_Change	1'h0	SMI on OS Ownership Change This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to 0 or 0 to 1.
		R	[28:21]	Reserved		
		R	[20]	SMI_On_Host_System_Error	1'h0	SMI on OS Ownership Change This bit is set to 1 whenever the HC OS Owned Semaphore bit in the USBLEGSUP register transitions from 1 to 0 or 0 to 1.
		R	[19:17]	Reserved		
		R	[16]	SMI_On_Event_Interrupt	1'h0	SMI on Event Interrupt Shadow bit of Event Interrupt (EINT) bit in the USBSTS register. Refer to Section 5.4.2 of the xHCI Specification for definition. This bit follows the state the Event Interrupt (EINT) bit in the USBSTS register, e.g. it automatically clears when EINT clears or set when EINT is set.
		RW	[15]	SMI_On_BAR_Enable	1'h0	SMI on BAR Enable When this bit is 1 and SMI on BAR is 1, then the host controller will issue an SMI.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[14]	SMI_On_PCI_Command_Enable	1'h0	SMI on PCI Command Enable When this bit is 1 and SMI on PCI Command is 1, then the host controller will issue an SMI.
			RW	[13]	SMI_On_OS_Ownership_Enable	1'h0	SMI on OS Ownership Enable When this bit is 1 AND the OS Ownership Change bit is 1, the host controller will issue an SMI.
			R	[12:5]	Reserved		
			RW	[4]	SMI_On_Host_System_Error_Enable	1'h0	SMI on Host System Error Enable When this bit is 1, and the SMI on Host System Error bit (below) in this register is 1, the host controller will issue an SMI immediately.
			R	[3:1]	Reserved		
			RW	[0]	USB_SMI_Enable	1'h0	USB SMI Enable When this bit is 1, and the SMI on Event Interrupt bit (below) in this register is 1, the host controller will issue an SMI immediately.
	890H	USB2_Supported_Protocol_Capability_DWord0	R	[31:24]	Revision_Major	8'h2	Major Revision Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.
				[23:16]	Revision_Minor	8'h0	Minor Revision Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:8]	Next_Capability_Pointer	8'h4	Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 7-1 of the xHCI Specification for more information on this field.
				[7:0]	Capability_ID	8'd2	Capability ID Refer to Table 7-2 of the xHCI Specification for the value that identifies the capability as Supported Protocol.
	894H	USB2_Supported_Protocol_Capability_DWord1	R	[31:0]	Name_String	32'h20425355	Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are: alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to section 7.2.2 of the xHCI Specification for defined values.
	898H	USB2_Supported_Protocol_Capability_DWord2	R	[31:28]	PSIC	4'h0	Protocol Speed ID Count (PSIC) This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. Refer to section 7.2.2 of the xHCI Specification and its subsections for protocol specific requirements related to this field.
				[27:25]	MHD	3'h0	Hub Depth (MHD) Default = Implementation dependent. If this field is 0, then the standard USB2 hub depth constrains apply, if this field is > 0, then it indicates the maximum hub depth supported by the USB2 ports.
				[24:21]	Reserved		

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[20]	BLC	1'h1	BESL LPM Capability121 (BLC) 0: The ports described by this xHCI Supported Protocol Capability shall apply HIRD timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. 1: The ports described by this xHCI Supported Protocol Capability shall apply BESL timing to BESL and BESLD fields of the PORTPMSC and PORTHLPMC registers. Refer to section 4.23.5.1.1.1 of the xHCI Specification for more information.
				[19]	HLC	1'h1	Hardware LPM Capability (HLC) If this bit is set to 1, the ports described by this xHCI Supported Protocol Capability support hardware controlled USB2 Link Power Management. Refer to section 4.23.5.1.1.1 of the xHCI Specification. **Note:** the Hardware LPM Capability support (i.e. HLC = 1) shall be mandatory for all xHCI 1.1 and xHCI 1.2 compliant xHCs.
				[18]	IHI	1'h0	Integrated Hub Implemented (IHI) 0: The Root Hub to External xHC port mapping adheres to the default mapping described in section 4.24.2.1 of the xHCI Specification. 1: The Root Hub to External xHC port mapping does not adhere to the default mapping described in section 4.24.2.1 of the xHCI Specification, and an ACPI or other mechanism is required to define the mapping.

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USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17]	HSO	1'h0	High-speed Only (HSO) 0: The USB2 ports described by this capability are Low-, Full-, and High-speed capable. 1: The USB2 ports described by this capability are High-speed only, e.g. the ports don't support Low- or Full-speed operation. High-speed only implementations may introduce a "Tier mismatch", refer to section 4.24.2 of the xHCI Specification of the xHCI Specification for more information.
				[16]	Reserved		
				[15:8]	Compatible_Port_Count	8'h1	Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
				[7:0]	Compatible_Port_Offset	8'h1	Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts.
	89CH	USB2_Supported_Protocol_Capability_DWord3	R	[31:5]	Reserved		
				[4:0]	Protocol_Slot_Type	5'd0	Protocol Slot Type This field specifies the Slot Type value which may be specified when allocating Device Slots that support this protocol. Valid values are 0 to 31.
	8A0H	USB3_Supported_Protocol_Capability_DWord0	R	[31:24]	Revision_Major	8'h3	Major Revision Major Specification Release Number in Binary-Coded Decimal (i.e., version 3.x is 03h). This field identifies the major release number component of the specification with which the xHC is compliant.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23:16]	Revision_Minor	8'h0	Minor Revision Minor Specification Release Number in Binary-Coded Decimal (i.e., version x.10 is 10h). This field identifies the minor release number component of the specification with which the xHC is compliant.
				[15:8]	Next_Capability_Pointer	8'h0	Next Capability Pointer This field indicates the location of the next capability with respect to the effective address of this capability. Refer to Table 7-1 of the xHCI Specification for more information on this field.
				[7:0]	Capability_ID	8'd2	Capability ID Refer to Table 7-2 of the xHCI Specification for the value that identifies the capability as Supported Protocol.
	8A4H	USB3_Supported_Protocol_Capability_DWord1	R	[31:0]	Name_String	32'h20425355	Name String This field is a mnemonic name string that references the specification with which the xHC is compliant. Four ASCII characters may be defined. Allowed characters are alphanumeric, space, and underscore. Alpha characters are case sensitive. Refer to section 7.2.2 of the xHCI Specification for defined values.
	8A8H	USB3_Supported_Protocol_Capability_DWord2	R	[31:28]	PSIC	4'h0	Protocol Speed ID Count (PSIC) This field indicates the number of Protocol Speed ID (PSI) Dwords that the xHCI Supported Protocol Capability data structure contains. If this field is non-zero, then all speeds supported by the protocol shall be defined using PSI Dwords, i.e. no implied Speed ID mappings apply. Refer to section 7.2.2 of the xHCI Specification and its subsections for protocol specific requirements related to this field.

USB Host	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27:25]	MHD	3'h0	Hub Depth (MHD) If this field is 0, then the standard USB3 hub depth constrains apply, if this field is > 0, then it indicates the maximum hub depth supported by the USB3 ports.
				[24:16]	Reserved		
				[15:8]	Compatible_Port_Count	8'h1	Compatible Port Count This field identifies the number of consecutive Root Hub Ports (starting at the Compatible Port Offset) that support this protocol. Valid values are 1 to MaxPorts.
				[7:0]	Compatible_Port_Offset	8'h2	Compatible Port Offset This field specifies the starting Port Number of Root Hub Ports that support this protocol. Valid values are 1 to MaxPorts.
	8ACH	USB3_Supported_Protocol_Capability_DWord3	R	[31:5]	Reserved		
				[4:0]	Protocol_Slot_Type	5'd0	Protocol Slot Type This field specifies the Slot Type value which may be specified when allocating Device Slots that support this protocol. Valid values are 0 to 1.

USB Device	BASE_ADDR: 0xB200_0000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
	C100H	GSBUSCFG0	RW	[31:28]	DATRDREQINFO	4'h0	DATRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Read (DatRdReqInfo) Input to BUS-GM.
				[27:24]	DESRDREQINFO	4'h0	DESRDREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Read (DesRdReqInfo). Input to BUS-GM.
				[23:20]	DATWRREQINFO	4'h0	DATWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Data Write (DatWrReqInfo). Input to BUS-GM.
				[19:16]	DESWRREQINFO	4'h0	DESWRREQINFO AHB-prot/AXI-cache/OCP-ReqInfo for Descriptor Write (DesWrReqInfo) Input to BUS-GM.
				[15:12]	Reserved		
				[11]	DATBIGEND	1'h0	Data Access is Big Endian This bit controls the endian mode for data accesses. 0: Little-endian (default). 1: Big-endian. **Note:** Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI master, this bit must be set to zero.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[10]	DESBIGEND	1'h0	Descriptor Access is Big Endian This bit controls the endian mode for descriptor accesses. 0: Little-endian (default). 1: Big-endian. Data is considered as 'embedded data' in the descriptors in the following cases: - Device mode: The buffer pointer of a Setup TRB points to the Setup TRB itself. - Host mode: The Immediate Data (IDT) bit in a Transfer TRB is set to 1. In device mode, if the system uses different endian modes for descriptor and data, software must not use 'embedded' data. In host mode, if the system uses different endian modes for data and descriptors, the controller treats 'embedded data' as descriptor (not as data) in terms of endian mode handling. If this is not the expectation of the system, the software must manipulate the 'embedded data' accordingly. **Note:** Since AXI requires byte invariant endianness, setting DescBigend and DatBigEnd to one causes an address invariant transform to be applied, which is not appropriate. See section 9.3 and 9.4 of the AMBA AXI Specification. Hence for an AXI master, this bit must be set to zero.
			[9:8]	Reserved		
			[7]	INCR256BRSTENA	1'h0	INCR256 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 256-beat burst.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6]	INCR128BRSTENA	1'h0	INCR128 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 128-beat burst.
				[5]	INCR64BRSTENA	1'h0	INCR64 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 64-beat burst.
				[4]	INCR32BRSTENA	1'h0	INCR32 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 32-beat burst.
				[3]	INCR16BRSTENA	1'h0	INCR16 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 16-beat burst.
				[2]	INCR8BRSTENA	1'h0	INCR8 Burst Type Enable Input to BUS-GM. For the AHB/AXI configuration, if software sets this bit to 1, the AHB/AXI master uses INCR to do the 8-beat burst.
				[1]	INCR4BRSTENA	1'h0	INCR4 Burst Type Enable Input to BUS-GM. For the AXI configuration, when this bit is enabled the controller is allowed to do bursts of beat length 1, 2, and 4. It is highly recommended that this bit is enabled to prevent descriptor reads and writes from being broken up into separate transfers.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	INCRBRSTENA	1'h1	Undefined Length INCR Burst Type Enable (INCRBrstEna) Input to BUS-GM. This bit determines the set of burst lengths the master interface uses. It works in conjunction with the GSBUSCFG0[7:1] enables (INCR256/128/64/32/16/8/4). 0: INCRX burst mode. HBURST (for AHB configurations) and ARLEN/AWLEN (for AXI configurations), do not use INCR except in case of non-aligned burst transfers. In the case of address-aligned transfers, they use only the following burst lengths: 1. 2, 4 (if GSBUSCFG0.INCR4BrstEna = 1). 8 (if GSBUSCFG0.INCR8BrstEna = 1). 16 (if GSBUSCFG0.INCR16BrstEna = 1). 32 (if GSBUSCFG0.INCR32BrstEna = 1). 64 (if GSBUSCFG0.INCR64BrstEna = 1). 128 (if GSBUSCFG0.INCR128BrstEna = 1). 256 (if GSBUSCFG0.INCR256BrstEna = 1). **Note:** In case of non-address-aligned transfers, INCR may get generated at the beginning and end of the transfers to align the address boundaries, even though INCR is disabled. In AHB mode, if INCRX burst mode is enabled, but none

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
						of the supported INCRx bursts bits are enabled, then the controller will perform (undefined length) INCR bursts. 1: INCR (undefined length) burst mode. AHB configurations: HBURST uses SINGLE or INCR of any length with handling 1KB boundary breakup. AXI configurations: ARLEN/AWLEN uses any length less than or equal to the largest-enabled burst length of INCR32/64/128/256. For cache line-aligned applications, this bit is typically set to 0 to ensure that the master interface uses only power-of-2 burst lengths (as enabled via GSBUSCFG0[7:0]).
C104H	GSBUSCFG1	RW	[31:13]	Reserved		
			[12]	EN1KPAGE	1'h0	1k Page Boundary Enable By default (this bit is disabled) the AXI breaks transfers at the 4k page boundary. When this bit is enabled, the AXI master (DMA data) breaks transfers at the 1k page boundary.
			[11:8]	PipeTransLimit	4'h3	AXI Pipelined Transfers Burst Request Limit The field controls the number of outstanding pipelined transfer requests the AXI master pushes to the AXI slave. When the AXI master reaches this limit, it does not make any more requests on the AXI ARADDR and AWADDR buses until the associated data phases complete. This field is encoded as follows: 'h0: 1 request. 'h1: 2 requests. 'h2: 3 requests. 'h3: 4 requests. ... 'hF: 16 requests.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:0]	Reserved		
	C108H	GTXTHRCFG	RW	[31:30]	Reserved		
				[29]	UsbTxPktCntSel	1'h0	USB Transmit Packet Count Enable This field enables/disables the USB transmission multi-packet thresholding: 0: USB transmission multi-packet thresholding is disabled. The controller can start transmission on the USB after the entire (one full) packet has been fetched into the corresponding TXFIFO. 1: USB transmission multi-packet thresholding is enabled. The controller can only start transmission on the USB after USB Transmit Packet Count amount of packets for the USB transaction (burst) are already in the corresponding TXFIFO. This mode is valid in both host and device modes. It is only used for SuperSpeed operation.
				[28]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27:24]	UsbTxPktCnt	4'h0	USB Transmit Packet Count This field specifies the number of packets that must be in the TXFIFO before the controller can start transmission for the corresponding USB transaction (burst). This field is only valid when the USB Transmit Packet Count Enable field is set to 1. Valid values are from 1 to 15. **Note:** In device mode, if device controller does not have the TRBs for the number of packets or if it cannot fetch the TRBs because of high latency or switching between other endpoints, then it does not wait for the threshold number of packets. The threshold number of packets will be honored only when the TRBs are available in the controller for the number of packets before it starts the data fetch. This field must be less than or equal to the USB Maximum TX Burst Size field.
				[23:16]	UsbMaxTxBurstSize	8'h0	USB Maximum TX Burst Size When UsbTxPktCntSel is one, this field specifies the Maximum Bulk OUT burst the controller can do. When the system bus is slower than the USB, TX FIFO can underrun during a long burst. User can program a smaller value to this field to limit the TX burst size that the controller can do. Host mode: It only applies to SS Bulk, Isochronous, and Interrupt OUT endpoints. Device mode: This value is not used in device mode, but users need to program a value when using the TX threshold feature to make sure that the value programmed in UsbTxPktCnt is less than this value. Valid values are from 1 to 16.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[15:0]	Reserved		
C10CH	GRXTHRCFG	RW	[31:30]	Reserved		
			[29]	UsbRxPktCntSel	1'h0	USB Receive Packet Count Enable This field enables/disables the USB reception multi-packet thresholding: 0: The controller can only start reception on the USB when the RX FIFO has space for at least one packet. 1: The controller can only start reception on the USB when the RX FIFO has space for at least UsbRxPktCnt amount of packets. This mode is valid in both host and device mode. It is only used for SuperSpeed. In device mode： - Setting this bit to 1 also enables the functionality of reporting NUMP in the ACK TP based on the RX FIFO space instead of reporting a fixed NUMP derived from DCFG.NUMP for non-control endpoints. - If you are using external buffer control (EBC) feature, disable this mode by setting UsbRxPktCntSel to 0.
			[28]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27:24]	UsbRxPktCnt	4'h0	USB Receive Packet Count In host mode, this field specifies the space (in terms of the number of packets) that must be available in the RX FIFO before the controller can start the corresponding USB RX transaction (burst). In device mode, this field specifies the space (in terms of the number of packets) that must be available in the RX FIFO before the controller can send ERDY for a flow-controlled endpoint. This field is valid only when the USB Receive Packet Count Enable field is set to 1. The valid values for this field are from 1 to 15. **Note:** This field must be less than or equal to the USB Maximum Receive Burst Size field.
				[23:19]	UsbMaxRxBurstSize	5'h0	USB Maximum Receive Burst Size When the system bus is slower than the USB, RX FIFO can overrun during a long burst. You can program a smaller value to this field to limit the RX burst size that the controller can perform. It only applies to SS Bulk, Isochronous, and Interrupt IN endpoints in the host mode. In device mode, this field specifies the NUMP value that is sent in ERDY for an OUT endpoint. The programmed value should not exceed the RXFIFO size. This field is valid only when UsbRxPktCntSel is 1. The valid values for this field are from 1 to 16.
				[18:13]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12:0]	ResvISOCOUTSpc	13'h0	Space reserved in Rx FIFO for ISOC OUT In host mode, this field is not applicable and must be set to 0. In device mode, this value represents the amount of space to be reserved for ISOC OUT packets. The value to be programmed should be chosen so as to ensure that non ISOC packets are not completely dropped. If no space needs to be reserved for ISOC OUT packets, program this field to 0. This field is valid only in device mode. The maximum configurable depth of RX FIFO is 8192. Therefore, this field is 13 bits wide. The maximum configurable depth of RX FIFO is 8192. Therefore, this field is 13 bits wide. For SS, the space reservation is always rounded off to the nearest packet boundary. Therefore, it is always recommended to program a value corresponding to MPS or its multiples. For HS/FS, the space reservation is the actual value. **Note:** For SS, reserve space for ISOC when the Rx FIFO space can accommodate two MPS or more. Otherwise, this may result in degraded performance for non-ISOC packets. If the space is entirely allocated for ISOC, the non-ISOC packets will be completely dropped.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C110H	GCTL	RW	[31:19]	PWRDNSCALE	13'h618	Power Down Scale (PwrDnScale) The USB3 suspend_clk input replaces pipe3_rx_pclk as a clock source to a small part of the USB3 controller that operates when the SS PHY is in its lowest power (P3) state, and therefore does not provide a clock. The Power Down Scale field specifies how many suspend_clk periods fit into a 16 kHz clock period. When performing the division, round up the remainder. For example, when using an 8-bit/16-bit/32-bit PHY and 25 MHz Suspend clock, Power Down Scale = 25000 kHz/16 kHz = 13'd1563 (rounder up). **Note:** - Minimum Suspend clock frequency is 32 kHz. - Maximum Suspend clock frequency is 125 MHz. The LTSSM uses Suspend clock for 12-ms and 100-ms timers during suspend mode. According to the USB 3.0 specification, the accuracy on these timers is 0% to +50%. - 12 ms + 0~+50% accuracy = 18 ms (Range is 12 m ~ 18 ms). - 100ms + 0~+50% accuracy = 150ms (Range is 100 ms ~ 150 ms). The suspend clock accuracy requirement is: - (12,000/62.5) * (GCTL[31:19]) * actual suspend_clk_period must be between 12,000 and 18,000. - (100,0000/62.5) * (GCTL[31:19]) * actual suspend_clk_period must be between 100,000 and 150,000. For example, if your suspend_clk frequency varies from 7.5 MHz to 10.5MHz, then the value needs to programmed is: Power Down Scale = 10500/16 = 657 (rounded up; and fastest frequency used).

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[18]	MASTERFILTBYPASS	1'h0	Master Filter Bypass When this bit is set to 1'b1, all the filters in the usb3_filter module are bypassed. The double synchronizers to mac_clk preceding the filters are also bypassed. For enabling the filters, this bit must be 1'b0.
				[17]	BYPSSETADDR	1'h0	Bypass SetAddress in Device Mode. When BYPSSETADDR bit is set, the device controller uses the value in the DCFG[DevAddr] bits directly for comparing the device address in the tokens. For simulation, you can use this feature to avoid sending an actual SET ADDRESS control transfer on the USB, and make the device controller respond to a new address. **Note:** You can set this bit for simulation purposes only. In the actual hardware, this bit must be set to 1'b0.
				[16]	U2RSTECN	1'h1	U2RSTECN If the SuperSpeed connection fails during POLL or LMP exchange, the device connects at non-SS mode. If this bit is set, then device attempts three more times to connect at SS, even if it previously failed to operate in SS mode. For each attempt, the device checks receiver termination eight times. From 2.60a release, this bit controls whether to check for Rx.Detect eight times or one time for every attempt. Device controller on USB 2.0 reset checks for receiver termination eight times per attempt if this bit is set to zero, or only once per attempt if the bit is set to one. **Note:** This bit is applicable only in device mode.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:14]	FRMSCLDWN	2'h0	FRMSCLDWN This field scales down device view of a SOF/USOF/ITP duration. For SS/HS mode: 2'h3: Implements interval to be 15.625 us. 2'h2: Implements interval to be 31.25 us. 2'h1: Implements interval to be 62.5 us. 2'h0: Implements interval to be 125us. For FS mode, the scale-down value is multiplied by 8.
				[13:12]	PRTCAPDIR	2'h2	PRTCAPDIR: Port Capability Direction (PrtCapDir) 2'b01: For Host configurations. 2'b10: For Device configurations.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	CORESOFTRESET	1'h0	Core Soft Reset (CoreSoftReset) 0: No soft reset. 1: Soft reset to controller. Clears the interrupts and all the CSRs except the following registers: - GCTL - GUCTL - GSTS - GSNPSID - GGPIO - GUID - GUSB2PHYCFG - GUSB3PIPECTL - DCFG - DCTL - DEVTEN - DSTS When you reset PHYs (using GUSB2PHYCFG or GUSB3PIPECTL registers), you must keep the controller in reset state until PHY clocks are stable. This controls the bus, ram, and mac domain resets. **Note:** This bit is for debug purposes only.
				[10]	SOFITPSYNC	1'h0	SOFITPSYNC 0: Operating in host mode. 1: Operating in host mode.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9]	U1U2TimerScale	1'h0	Disable U1/U2 timer Scaledown (U1U2TimerScale). If set to 1 along with GCTL[5:4] (ScaleDown) = 2'bX1, disables the scale down of U1/U2 inactive timer values. This is for simulation mode only.
				[8]	DEBUGATTACH	1'h0	Debug Attach When this bit is set, - SS Link proceeds directly to the Polling link state (after RUN/STOP in the DCTL register is asserted) without checking remote termination. - Link LFPS polling timeout is infinite. - Polling timeout during TS1 is infinite (in case link is waiting for TXEQ to finish).

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:6]	RAMCLKSEL	2'h0	RAM Clock Select (RAMClkSel) 2'b00: Bus clock. 2'b01: Pipe clock (Only used in device mode). 2'b10: In device mode, pipe/2 clock. In Host mode, controller switches ram_clk between pipe/2 clock, mac2_clk and bus_clk based on the status of the U2/U3 ports 2'b11: In device mode, selects mac2_clk as ram_clk (when 8-bit UTMI or ULPI used. Not supported in 16-bit UTMI mode) In Host mode, controller switches ram_clk between pipe_clk, mac2_clk and bus_clk based on the status of the U2/U3 ports. In device mode, upon a USB reset and USB disconnect, the hardware clears these bits to 2'b00. **Note:** In device mode, if you set RAMClkSel to 2'b11 (mac2_clk), the controller internally switches the ram_clk to bus_clk when the link state changes to Suspend (L2 or L3), and switches the ram_clk back to mac2_clk when the link state changes to resume or U2.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:6]	RAMCLKSEL	2'h0	In host mode, if a value of 2/3 is chosen, then controller switches ram_clk between bus_clk, mac2_clk and pipe_clk, pipe_clk/2, based on the state of the U2/U3 ports. For example, if only the U2 port is active and the U3 ports are suspended, then the ram_clk is switched to mac2_clk. When only the U3 ports are active and the U2 ports are suspended, the controller internally switches the ram_clk to pipe3 clock and when all U2 and U3 ports are suspended, it switches the ram_clk to bus_clk. This allows decoupling the ram_clk from the bus_clk, and depending on the bandwidth requirement allows the bus_clk to be run at a lower frequency than the ram_clk requirements. The bus_clk frequency still cannot be less than 60MHz in host mode, and this is not verified. A value of 2 can be chosen only if the pipe data width is 8 or 16 bits. In this case the when the ram_clk is switched to pipe_clk, it uses pipe_clk/2 instead of pipe_clk. If a value of 3 is chosen for RAMClkSel, then when ram_clk is switched to pipe_clk, then pipe_clk is used without any divider.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							In device mode, when RAMClkSel != 2'b00, the bus_-clk_early frequency can be a minimum of 1 MHz. This is tested in simulation and also in hardware with Linux, Micro-soft Windows 8, and MCCI Windows7 host drivers. Only control and non periodic transfers are supported when bus_clk is 1 MHz. For periodic applications, the bus_-clk_early minimum frequency is higher depending on your application and SoC bus. Even though 1 MHz has been tested with standard host drivers, Synopsys recommends 5 MHz minimum for ASIC designs to provide a margin or at least have a backup option to increase the bus_clk frequency to 5 MHz if needed.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5:4]	SCALEDOWN	2'h0	Scale-Down Mode When Scale-Down mode is enabled for simulation, the controller uses scaled-down timing values, resulting in faster simulations. When Scale-Down mode is disabled, actual timing values are used. This is required for hardware operation. HS/FS/LS Modes: - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scale-down of all timing values except Device mode suspend and resume. These include Speed enumeration, HNP/SRP, and Host mode suspend and resume - 2'b10: Enables scale-down of Device mode suspend and resume timing values only. - 2'b11: Enables bit 0 and bit 1 scale-down timing values. SS Mode: - 2'b00: Disables all scale-downs. Actual timing values are used. - 2'b01: Enables scaled down SS timing and repeat values including: (1) Number of TxEq training sequences reduce to 8; (2) LFPS polling burst time reduce to 256 nS; (3) LFPS warm reset receive reduce to 30 uS. - 2'b10: No TxEq training sequences are sent. Overrides Bit 4. - 2'b11: Enables bit 0 and bit 1 scale-down timing values.
				[3]	DISSCRAMBLE	1'h0	Disable Scrambling (DisScramble) Transmit request to Link Partner on next transition to Recovery or Polling.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	U2EXIT_LFPS	1'h1	U2EXIT_LFPS 0: The link treats 248ns LFPS as a valid U2 exit. 1: The link waits for 8us of LFPS before it detects a valid U2 exit. This bit is added to improve interoperability with a third-party host/device controller. This host/device controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the host/device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the host/device can stay in U2 while ignoring this glitch from the host/device controller. This bit is applicable for both host and device controller. This bit is added to improve interoperability with a third party host controller. This host controller in U2 state while performing receiver detection generates an LFPS glitch of about 4ms duration. This causes the device to exit from U2 state because the LFPS filter value is 248ns. With the new functionality enabled, the device can stay in U2 while ignoring this glitch from the host controller.
				[1]	GblHibernationEn	1'h0	GblHibernationEn This bit enables hibernation at the global level. If hibernation is not enabled through this bit, the PMU immediately accepts the D0->D3 and D3->D0 power state change requests, but does not save or restore any controller state. In addition, the PMUs never drive the PHY interfaces and let the controller continue to drive the PHY interfaces. Access: Read only.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[0]	DSBLCLKGTNG	1'h0	Disable Clock Gating (DsblClkGtng) This bit is set to 1 and the controller is in Low Power mode, internal clock gating is disabled. You can set this bit to 1'b1 after Power On Reset.
C114H	GPMSTS	W	[31:28]	PortSel	4'h0	Global Power Management Status Register, PortSel This field selects the port number.
		R	[27:17]	Reserved		
		R	[16:12]	U3Wakeup	5'h0	U3Wakeup This field gives the following USB 3.0 port wakeup conditions: Bit [12]: Overcurrent Detected Bit [13]: Resume Detected Bit [14]: Connect Detected Bit [15]: Disconnect Detected Bit [16]: Last Connection State
		R	[11:10]	Reserved		
		R	[9:0]	U2Wakeup	10'h0	U2Wakeup This field indicates the following USB 2.0 port wakeup conditions: Bit [0]: Overcurrent Detected Bit [1]: Resume Detected Bit [2]: Connect Detected Bit [3]: Disconnect Detected Bit [4]: Last Connection State Bit [5]: ID Change Detected Bit [6]: SRP Request Detected Bit [7]: ULPI Interrupt Detected Bit [8]: USB Reset Detected Bit [9]: Resume Detected Changed

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C118H	GSTS	R	[31:20]	CBELT	12'h7e8	Current BELT Value In Host mode, this field indicates the minimum value of all received device BELT values and the BELT value that is set by the Set Latency Tolerance Value command.
		R	[19:12]	Reserved		
		R	[11]	SSIC_IP	1'h0	This field is not used.
		R	[10]	OTG_IP	1'h0	This field is not used.
		R	[9]	BC_IP	1'h0	Battery Charger Interrupt Pending This field indicates that there is a pending interrupt pertaining to BC in BCEVT register.
		R	[8]	ADP_IP	1'h0	This field is not used.
		R	[7]	Host_IP	1'h0	Host Interrupt Pending This field indicates that there is a pending interrupt pertaining to xHC in the Host event queue.
		R	[6]	Device_IP	1'h0	Device Interrupt Pending This field indicates that there is a pending interrupt pertaining to peripheral (device) operation in the Device event queue.
		RW1C	[5]	CSRTimeout	1'h0	CSR Timeout When this bit is 1'b1, it indicates that the software performed a write or read to a controller register that could not be completed within USB3 CSR ACCESS TIMEOUT bus clock cycles (default: h1FFFF).

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
		RW1C	[4]	BUSERRADDRVLD	1'h0	Bus Error Address Valid (BusErrAddrVld) Indicates that the GBUSERRADDR register is valid and reports the first bus address that encounters a bus error. **Note:** Only supported in AHB and AXI configurations.
		R	[3:2]	Reserved		
		R	[1:0]	CURMOD	2'h0	Current Mode of Operation (CurMod) Indicates the current mode of operation: 2'b00: Device mode. 2'b01: Host mode.
C11CH	GUCTL1	RW	[31]	DEV_DECOUPLE_L1L2_EVT	1'h0	DEV_DECOUPLE_L1L2_EVT 0: Default behavior, no change in device events L1/L2U3 events are not decoupled (old behavior of v2.90a and before) 1: Feature enabled, L1 and L2 events are separated when operating in 2.0 mode. Separate event enable bits for L1 suspend and wake events. This bit is applicable for device mode only. If this feature is enabled, L1 suspend and wake events have individual controls to enable/mask them. Enable this feature if you want to get L1 (LPM) events separately and not combined with L2 events when operating in 2.0 speeds.
			[30]	DS_RXDET_MAX_TOUT_CTRL	1'h0	DS_RXDET_MAX_TOUT_CTRL This bit is used to control the tRxDetectTimeoutDFP timer for the SuperSpeed link. 0: Default behavior; 12ms is used as tRxDetectTime-outDFP. 1: 120ms is used as the tRxDetectTimeoutDFP. This bit is used only in host mode. For more details, refer to ECN020 for USB 3.0 Specification.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[29]	FILTER_SE0_FSLS_EOP	1'h0	FILTER_SE0_FSLS_EOP 0: Default behavior, no change in LineState check for SE0 detection in FS/LS. 1: Feature enabled, FS/LS SE0 is filtered for 2 clocks for detecting EOP. This bit is applicable for FS/LS operation. If this feature is enabled, then SE0 on the LineState is validated for 2 consecutive utmi/ulpi clock edges for EOP detection. This feature is applicable only in FS in device mode and FS/LS mode of operation in host mode. Device mode: FS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then for device LPM handshake, the controller will ignore single SE0 glitch on the LineState during transmit. Only 2 or more SE0 is considered as a valid EOP on FS. Host mode: FS/LS - If GUCTL1.FILTER_SE0_FSLS_EOP is set, then the controller will ignore single SE0 glitch on the LineState during transmit. Only 2 or more SE0 is considered as a valid EOP on FS/LS port. Enable this feature if the LineState has SE0 glitches during transmission. This bit is quasi-static, that is, it must not be changed during device operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[28]	TX_IPGAP_LINECHECK_DIS	1'h0	TX_IPGAP_LINECHECK_DIS 0: Default behavior, no change in LineState check. 1: Feature enabled, 2.0 MAC disables LineState check during HS transmit. This bit is applicable for HS operation of u2mac. If this feature is enabled, then the 2.0 mac operating in HS ignores the UTMI/ULPI LineState during the transmit of a token (during token-to-token and token-to-data IPGAP). When enabled, the controller implements a fixed 40-bit TxEndDelay after the packet is given on UTMI and ignores the LineState during this time. This feature is applicable only in HS mode of operation. Device mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then for device LPM handshake, the controller will ignore the LineState after TX and wait for fixed clocks (40 bit times equivalent) after transmitting ACK on utmi. Host mode: If GUCTL1.TX_IPGAP_LINECHECK_DIS is set, then the ipgap between (tkn to tkn/data) is added by 40 bit times of TXENDDELAY, and LineState is ignored during this 40 bit times delay. Enable this bit if the LineState will not reflect the expected line state (J) during transmission. This bit is quasi-static, that is, it must not be changed during device operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27]	DEV_TRB_OUT_SPR_IND	1'h0	DEV_TRB_OUT_SPR_IND 0: Default behavior, no change in TRB status dword. 1: Feature enabled, OUT TRB status indicates Short Packet. This bit is applicable for device mode only (and ignored in host mode). If the device application (software/hardware) wants to know if a short packet was received for an OUT in the TRB status itself, then this feature can be enabled, so that a bit is set in the TRB writeback in the buf_size dword. Bit[26] - SPR of the {trbstatus, Reserved, SPR, PCM1, bufsize} dword will be set during an OUT transfer TRB write back if this is the last TRB used for that transfer descriptor. This bit is quasi-static, that is, it must not be changed during device operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[26]	DEV_FORCE_20_CLK_FOR_30_CLK	1'h0	DEV_FORCE_20_CLK_FOR_30_CLK 0: Default behavior, Uses 3.0 clock when operating in 2.0 mode. 1: Feature enabled. This bit is applicable (and to be set) for device mode (DCFG.Speed != SS) only. In the 3.0 device controller, if the controller is programmed to operate in 2.0 only (that is, Device Speed is programmed to 2.0 speeds in DCFG[Speed]), then setting this bit makes the internal 2.0 (utmi/ulpi) clock to be routed as the 3.0 (pipe) clock. Enabling this feature allows the pipe3 clock to be not-running when forcibly operating in 2.0 device mode. **Note:** When using this feature, all pipe3 inputs must be in inactive mode. In particular, the pipe3 clocks must not be running and the pipe3_phystatus_async must be tied to 0. This bit should not be set if the controller is programmed to operate in SuperSpeed mode (even when it falls back to 2.0). This bit is quasi-static, that is, it must not be changed during operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[25]	P3_IN_U2	1'h0	P3_IN_U2 0: Default behavior, When SuperSpeed link is in U2, PowerState P2 is attempted on the PIPE Interface. 1: When SuperSpeed link is in U2, PowerState P3 is attempted if GUSB3PIPECTL[17] is set. Setting this bit enables P3 Power State when the SuperSpeed link is in U2. Another Power Saving option. Check with your PHY vendor before enabling this option. When setting this bit to 1 to enable P3 in P2, GUSB3PIPECTL[27] should be set to 0 to make sure that the U2 exit is attempted in P0. This bit should be set only when GCTL.SOFITPSYNC=1 or FLADJ.GFLADJ_REFCLK_LPM_SEL=1.
				[24]	DEV_L1_EXIT_BY_HW	1'h0	DEV_L1_EXIT_BY_HW 0: Default behavior, disables device L1 hardware exit logic. 1: Feature enabled. This bit is applicable for device mode (2.0) only. This field enables device controller sending remote wakeup for L1 if the device becomes ready for sending/accepting data when in L1 state. If the host expects the device to send remote wakeup signaling to resume after going into L1 in flow controlled state, then this bit can be set to send the remote wake signal automatically when the device controller becomes ready. This feature is applicable only to bulk and interrupt transfers, and not for Isoch/Control:

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							When control transfers are in progress, the LPM will be rejected (NYET response). Only after control transfers are completed (either with ACK/STALL), LPM will be accepted. For Isoch transfers, the host needs to do the wake-up and start the transfer. Device controller will not do remote wakeup when Isoch endpoints get ready. The device SW needs to keep the GUSB2PHYCFG[EnblSlpM] reset in order to keep the PHY clock to be running for keeping track of SOF intervals. When L1 hibernation is enabled, the controller will not do automatic exit for hibernation requests thru L1. This bit is quasi-static, that is, it must not be changed during device operation.
				[23:21]	IP_GAP_ADD_ON	3'h0	This register field is used to add on to the default inter packet gap setting in the USB 2.0 MAC. This should be programmed to a non zero value only in case where you need to increase the default inter packet delay calculations in the USB 2.0 MAC module.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[20]	DEV_LSP_TAIL_LOCK_DIS	1'h0	DEV_LSP_TAIL_LOCK_DIS 0: Default behavior, enables device lsp lock logic for tail TRB update. 1: Fix disabled. This is a bug fix for STAR 9000716195 that affects the CSP mode for OUT endpoints in device mode. The issue is that tail TRB index is not synchronized with the cache Scratchpad bytecount update. If the fast-forward request comes in-between the bytecount update on a newly fetched TRB and the tail-index write update in TPF, the RDP works on an incorrect tail index and misses the byte count decrement for the newly fetched TRB in the fast-forwarding process. This fix needs to be present all the times.
				[19]	NAK_PER_ENH_FS	1'h0	NAK_PER_ENH_FS 0: Enhancement not applied. 1: Enables performance enhancement for FS async endpoints in the presence of NAKs If a periodic endpoint is present , and if a bulk endpoint which is also active is being NAKed by the device, then this could result in a decrease in performance of other Full-Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your FullSpeed application. Setting this bit will only control, and is only required for Full Speed transfers.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[18]	NAK_PER_ENH_HS	1'h1	NAK_PER_ENH_HS 0: Enhancement not applied. 1: Enables performance enhancement for HS async endpoints in the presence of NAKs. If a periodic endpoint is present, and if a bulk endpoint which is also active is being NAKed by the device, then this could result in decrease in performance of other High Speed bulk endpoint which is ACKed by the device. Setting this bit to 1, will enable the host controller to schedule more transactions to the async endpoints (bulk/ control) and hence will improve the performance of the bulk endpoint. This control bit should be enabled only if the existing performance with the default setting is not sufficient for your HighSpeed application. Setting this bit will only control, and is only required for High Speed transfers.
				[17]	PARKMODE_DISABLE_SS	1'h0	PARKMODE_DISABLE_SS This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all SS bus instances in park mode are disabled.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[16]	PARKMODE_DISABLE_HS	1'h0	PARKMODE_DISABLE_HS This bit is used only in host mode. When this bit is set to 1 all HS bus instances park mode are disabled. To improve performance in park mode, the xHCI scheduler queues in three requests of 4 packets each for High Speed asynchronous endpoints in a micro-frame. But if a device is slow and if it NAKs more than 3 times, then it is rescheduled only in the next micro-frame. This could decrease the performance of a slow device even further. In a few high speed devices (such as Sandisk Cruzer Blade 4GB VID:1921, PID:21863 and Flex Drive VID:3744, PID:8552) when an IN request is sent within 900ns of the ACK of the previous packet, these devices send a NAK. When connected to these devices, if required, the software can disable the park mode if you see performance drop in your system. When park mode is disabled, pipelining of multiple packet is disabled and instead one packet at a time is requested by the scheduler. This allows up to 12 NAKs in a micro-frame and improves performance of these slow devices.
				[15]	PARKMODE_DISABLE_FSLS	1'h0	PARKMODE_DISABLE_FSLS This bit is used only in host mode, and is for debug purpose only. When this bit is set to 1 all FS/LS bus instances in park mode are disabled.
				[14:13]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	DisUSB2RefClkGtng	1'h1	Disable ref_clk gating for 2.0 PHY (DisUSB2RefClkGtng) If ref_clk gating is disabled, then the ref_clk input cannot be turned off to the USB 2.0 PHY and controller. This is independent of the GCTL[DisClkGtng] setting. 0: ref_clk gating enabled for USB 2.0 PHY. 1: ref_clk gating disabled for USB 2.0 PHY. Access: Read only.
				[11]	DisRefClkGtng	1'h1	Disable ref_clk gating (DisRefClkGtng) If the ref_clk gating is disabled then input ref_clk cannot be turned off to SSPHY and controller. This is independent of GCTL[DisClkGtng] setting. 0: ref_clk gating Enabled for SSPHY. 1: ref_clk gating Disabled for SSPHY. Access: Read only.
				[10]	RESUME_OPMODE_HS_HOST	1'h0	RESUME_OPMODE_HS_HOST This bit is used only in host mode, and is for USB 2.0 opmode behavior in HS Resume. 0: The UTMI/ULPI opmode will be changed to "normal" 2us after HS terminations change after EOR. This is the default behavior. 1: The UTMI/ULPI opmode will be changed to "normal" along with HS terminations after EOR. This option is to support certain legacy UTMI/ULPI PHYs.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9]	DEV_HS_NYET_BULK_SPR	1'h0	DEV_HS_NYET_BULK_SPR 0: Default behavior, no change in device response. 1: Feature enabled, HS bulk OUT short packet gets NYET response. This bit is applicable for device mode only (and ignored in host mode) to be used in 2.0 operation. If this bit is set, the device controller sends NYET response instead of ACK response for a successfully received bulk OUT short packet. If NYET is sent after receiving short packet, then the host would PING before sending the next OUT; this improves the performance as well as clears up the buffer/cache on the host side. Internal to the device controller, short packet (SPR=1) processing takes some time, and during this time, the USB is flow controlled. With NYET response instead of ACK on short packet, the host does not send another OUT-DATA without pinging in HS mode. This bit is quasi-static, that is, it must not be changed during device operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[8]	L1_SUSP_THRLD_EN_FOR_HOST	1'h1	L1_SUSP_THRLD_EN_FOR_HOST This bit is used only in host mode. The host controller asserts the utmi_l1_suspend_n and utmi_sleep_n output signals as follows: The controller asserts the utmi_l1_suspend_n signal to put the PHY into deep low-power mode in L1 when both of the following are true: - The HIRD/BESL value used is greater than or equal to the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - The HIRD/BESL value used is less than the value in L1_SUSP_THRLD_FOR_HOST field. - The L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1'b0.
				[7:4]	L1_SUSP_THRLD_FOR_HOST	4'h8	L1_SUSP_THRLD_FOR_HOST This field is effective only when the L1_SUSP_THRLD_EN_FOR_HOST bit is set to 1. For more details, refer to the description of the L1_SUSP_THRLD_EN_FOR_HOST bit.
				[3]	HC_ERRATA_ENABLE	1'h1	Host ELD Enable (HELDEn) When this bit is set to 1, it enables the Exit Latency Delta (ELD) support. This bit is used only in the host mode. This bit must be set to 1 in Host mode.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	HC_PARCHK_DISABLE	1'h0	Host Parameter Check Disable (HParChkDisable) 0: By default, the xHC checks that the input slot/EP context fields comply to the xHCI Specification. Upon detection of a parameter error during command execution, the xHC generates an event TRB with completion code indicating 'PARAMETER ERROR'. 1: The xHC does not perform parameter checks and does not generate 'PARAMETER ERROR' completion code.
				[1]	OVRLD_L1_SUSP_COM	1'h1	OVRLD_L1_SUSP_COM If this bit is set, the utmi_l1_suspend_com_n is overloaded with the utmi_sleep_n signal. This bit is usually set if the PHY stops the port clock during L1 sleep condition. **Note:** The recommended connection for the SUSPENDM/SLEEPM signals to the PHY with respect to this bit is as follows. For non-zero ports: Connect: - utmi_sleep_n[n] to SLEEPM[n]. - (utmi_suspend_n[n] & utmi_l1_suspend_n[n]) to SUSPENDM[n]. - USB2 PHYCLK[n] to utmi_clk[n] GUCTL1.OVRLD_L1_SUSP_COM impacts only Port0. For Port0: For our PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=1; With this connection, the PHY keeps PLL active so that FREECLK is always

USB Device	BASE_ADDR: 0xB200_0000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
							available irrespective of suspend/sleep. - Connect USB2 PHY COMMONONN to 0. - Connect utmi_sleep_n[0] to SLEEPM[0]. - Connect (utmi_suspend_n[0] & utmi_l1_suspend_n[0]) to SUSPENDM[0]. - Connect USB2 PHY FREECLK to utmi_clk[0]. - Leave utmi_suspend_com_n, utmi_l1_suspend_com_n unconnected. - GUCTL1.OVRLD_L1_SUSP_COM can be set to any value. For Third Party PHY, GUSB2PHYCFGn.U2_FREECLK_EXISTS=0; With this connection the PHY can shut off all the clocks when the required conditions are met (like, GUSB2PHYCFGn[8,6], GUCTL1[1], GFLADJ[23], GCTL[10], Suspend condition, HW LPM enable etc). - Connect -utmi_suspend_com_n to SUSPENDM[0] (or equivalent). - Connect -utmi_l1_suspend_com_n to SLEEPM[0] (or equivalent). - Connect PHYCLK0 (first port clock) to utmi_clk[0]. - Leave utmi_suspend_n[0], utmi_l1_suspend_ n[0], utmi_sleep_n[0] unconnected. - Set GUCTL1.OVRLD_L1_SUSP_COM to 1'b1.
				[0]	LOA_FILTER_EN	1'h0	LOA_FILTER_EN If this bit is set, the USB 2.0 port babble is checked at least three consecutive times before the port is disabled. This prevents false triggering of the babble condition when using low quality cables. This bit is valid only in host mode.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C120H	GSNPSID	R	[31:0]	ID	32'h5533330b	ID ID[31:16] indicates Core Identification Number. 0x5533 is ASCII for U3 (Horizon_usb3). ID[15:0] indicates the release number. Current Release is 3.30a. Software uses this register to configure release-specific features in the driver.
C124H	GGPIO	RW	[31:16]	GPO	16'h0	General Purpose Output The value of this field is driven out on the gp_out[15:0] output port.
		R	[15:0]	GPI	16'h0	General Purpose Input The read value of this field reflects the gp_in[15:0] input signal value. **Note:** Register bit-bash test should not check for reset value of this field since its not predictable; depends on the gp_in port.
C128H	GUID	RW	[31:0]	USERID	32'h12345678	USERID Application-programmable ID field.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C12CH	GUCTL	RW	[31:22]	REFCLKPER	10'h8	REFCLKPER This field indicates in terms of nano seconds the period of ref_clk. The default value of this register is set to 'h8 (8ns/125 MHz). This field needs to be updated during power-on initialization, if GCTL.SOFITPSYNC or GFLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. The programmable maximum value is 62ns, and the minimum value is 8ns. You must use a reference clock with a period that is an integer multiple, so that ITP can meet the jitter margin of 32ns. The allowable ref_clk frequencies whose period is not integer multiples are 16/17/19.2/24/39.7MHz. This field must not be set to 0 at any time. If you never plan to use this feature, then set this field to 'h8, the default value.
			[21]	NoExtrDl	1'h0	No Extra Delay Between SOF and the First Packet(NoExtrDl) Some HS devices misbehave when the host sends a packet immediately after a SOF. However, adding an extra delay between a SOF and the first packet can reduce the USB data rate and performance. This bit is used to control whether the host must wait for 2 microseconds before it sends the first packet after a SOF, or not. User can set this bit to one to improve the performance if those problematic devices are not a concern in the user's host environment. 0: Host waits for 2 microseconds after a SOF before it sends the first USB packet. 1: Host doesn't wait after a SOF before it sends the first USB packet.
			[20:18]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17]	SprsCtrlTransEn	1'h0	Sparse Control Transaction Enable Some devices are slow in responding to Control transfers. Scheduling multiple transactions in one microframe/frame can cause these devices to misbehave. If this bit is set to 1'b1, the host controller schedules transactions for a Control transfer in different microframes/frames.
				[16]	ResBwHSEPS	1'h0	Reserving 85% Bandwidth for HS Periodic EPs (ResBwHSEPS) By default, HC reserves 80% of the bandwidth for periodic EPs. If this bit is set, the bandwidth is relaxed to 85% to accommodate two high speed, high bandwidth ISOC EPs. USB 2.0 required 80% bandwidth allocated for ISOC traffic. If two High-bandwidth ISOC devices (HD Webcams) are connected, and if each requires 1024-bytes X 3 packets per Micro-Frame, then the bandwidth required is around 82%. If this bit is set, then it is possible to connect two Webcams of 1024bytes X 3 payload per Micro-Frame each. Otherwise, you may have to reduce the resolution of the Webcams. This bit is valid in Host and DRD configuration and is used in host mode operation only. Ignore this bit in device mode.
				[15]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[14]	USBHstInAutoRetryEn	1'h0	Host IN Auto Retry (USBHstInAutoRetryEn) When set, this field enables the Auto Retry feature. For IN transfers (non-isochronous) that encounter data packets with CRC errors or internal overrun scenarios, the auto retry feature causes the Host controller to reply to the device with a non-terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP != 0). If the Auto Retry feature is disabled (default), the controller will respond with a terminating retry ACK (that is, an ACK transaction packet with Retry = 1 and NumP = 0). 0: Auto Retry Disabled. 1: Auto Retry Enabled. **Note:** When enabling Auto Retry feature, if the system latency is large enough to cause the internal PSQ full (PSQ can be full as the result of messages not being processed because of pending fetches before flushing the TxQ due to NRDY/ERDY conditions), then the host controller can generate a transaction error.
				[13]	EnOverlapChk	1'h0	Enable Check for LFPS Overlap During Remote Ux Exit: 0: When the link exists U1/U2/U3 because of a remote exit, it does not look for an LFPS overlap. 1: The SuperSpeed link when exiting U1/U2/U3 waits for either the remote link LFPS or TS1/TS2 training symbols before it confirms that the LFPS handshake is complete. This is done to handle the case where the LFPS glitch causes the link to start exiting from the low power state. Looking for the LFPS overlap makes sure that the link partner also sees the LFPS.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	ExtCapSupptEN	1'h0	External Extended Capability Support Enable (ExtCapSuptEN) When set, this field enables extended capabilities to be implemented outside the controller. When the ExtCapSupEN is set and the Debug Capability is enabled, the Next Capability pointer in "Debug Capability" returns 16. A read to the first DWORD of the last internal extended capability (the "xHCI Supported Protocol Capability for USB 3.0" when the Debug Capability is not enabled) returns a value of 4 in the Next Capability Pointer field. This indicates to software that there is another capability four DWORDs after this capability (for example, at address N+16 where N is the address of this DWORD). If enabled, an external address decoder that snoops the xHC slave interface must be implemented. If it sees an access to N+16 or greater, the slave access is re-routed to a piece of hardware which returns the external capability pointer register of the new capability and also handles reads/writes to this new capability and the side effects. If disabled, a read to the first DWORD of the last internal extended capability returns 0 in the 'Next Capability Pointer field. This indicates there are no more capabilities.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	InsrtExtrFSBODI	1'h0	Insert Extra Delay Between FS Bulk OUT Transactions (InsrtExtrFSBODI). Some FS devices are slow to receive Bulk OUT data and can get stuck when there are consecutive Bulk OUT transactions with short inter-transaction delays. This bit is used to control whether the host inserts extra delay between consecutive Bulk OUT transactions to a FS Endpoint. 0: Host doesn't insert extra delay between consecutive. 1: Host inserts about 12us extra delay between consecutive Bulk OUT transactions to a FS Endpoint to work around the device issue. **Note:** Setting this bit to one will reduce the Bulk OUT transfer performance for most of the FS devices.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10:9]	DTCT	2'h0	Device Timeout Coarse Tuning (DTCT) This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. The controller first checks the DTCT value. If it is 0, then the timeout value is defined by the DTFT. If it is non-zero, then it uses the following timeout values: 00: 0 usec -> use DTFT value instead. 01: 500 usec. 10: 1.5 msec. 11: 6.5 msec. **Note:** When the system latency is larger than the programmed DTCT /DTFT value, if the host controller is not able to accept certain transactions on the bus (because of system bus delays), the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[8:0]	DTFT	9'h10	Device Timeout Fine Tuning (DTFT) This field is a Host mode parameter which determines how long the host waits for a response from device before considering a timeout. For the DTFT field to take effect, DTCT must be set to 2'b00. The DTFT value is the number of 125 MHz clocks * 256 to count before considering a device timeout. The minimum value of DTFT is 2. For example, if the mac3_clk is 125 MHz clk (8 ns period), this is calculated as follows: (DTFT value) * 256 * (8 ns) - If DTFT = 0x2, 2*256*8 = 4usec timeout. - If DTFT = 0x5, 5*256*8 = 10usec timeout. - If DTFT = 0xA, 10*256*8 = 20usec timeout. - If DTFT = 0x10, 16*256*8 = 32usec timeout. - If DTFT = 0x19, 25*256*8 = 51usec timeout. - If DTFT = 0x31, 49*256*8 = 100usec timeout. - If DTFT = 0x62, 98*256*8 = 200usec timeout. **Note:** When the system latency is larger than the programmed DTCT /DTFT value, if the host controller is not able to accept certain transactions on the bus (because of system bus delays), the controller may not release header credits which in turn can cause the host to report a transaction error. Therefore, program this value to be larger than your system delay.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C130H	GBUSERRADDRLO	R	[31:0]	BUSERRADDR	32'h0	Bus Address - Low (BusAddrLo) This register contains the lower 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. **Note:** Only supported in AHB and AXI configurations.
C134H	GBUSERRADDRHI	R	[31:0]	BUSERRADDR	32'h0	Bus Address - High (BusAddrHi) This register contains the higher 32 bits of the first bus address that encountered a SoC bus error. It is valid when the GSTS.BusErrAddrVld field is 1. It can only be cleared by resetting the controller. **Note:** Only supported in AHB and AXI configurations.
C138H	GPRTBIMAPLO	RW	[31:28]	BINUM8	4'h0	BINUM8: SS USB Instance Number for Port 8. Application-programmable ID field.
			[27:24]	BINUM7	4'h0	BINUM7: SS USB Instance Number for Port 7. Application-programmable ID field.
			[23:20]	BINUM6	4'h0	BINUM6: SS USB Instance Number for Port 6. Application-programmable ID field.
			[19:16]	BINUM5	4'h0	BINUM5: SS USB Instance Number for Port 5. Application-programmable ID field.
			[15:12]	BINUM4	4'h0	BINUM4: SS USB Instance Number for Port 4. Application-programmable ID field.
			[11:8]	BINUM3	4'h0	BINUM3: SS USB Instance Number for Port 3. Application-programmable ID field.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[7:4]	BINUM2	4'h0	BINUM2: SS USB Instance Number for Port 2. Application-programmable ID field.
			[3:0]	BINUM1	4'h0	BINUM1: SS USB Instance Number for Port 1. Application-programmable ID field.
C13CH	GPRTBIMAPHI	RW	[31:28]	Reserved		
			[27:24]	BINUM15	4'h0	BINUM15: SS USB Instance Number for Port 15. Application-programmable ID field.
			[23:20]	BINUM14	4'h0	BINUM14: SS USB Instance Number for Port 14. Application-programmable ID field.
			[19:16]	BINUM13	4'h0	BINUM13: SS USB Instance Number for Port 13. Application-programmable ID field.
			[15:12]	BINUM12	4'h0	BINUM12: SS USB Instance Number for Port 12. Application-programmable ID field.
			[11:8]	BINUM11	4'h0	BINUM11: SS USB Instance Number for Port 11. Application-programmable ID field.
			[7:4]	BINUM10	4'h0	BINUM10: SS USB Instance Number for Port 10. Application-programmable ID field.
			[3:0]	BINUM9	4'h0	BINUM9: SS USB Instance Number for Port 9. Application-programmable ID field.
C140H	GHWPARAMS0	R	[31:24]	ghwparams0_31_24	8'h40	USB3_AWIDTH
			[23:16]	ghwparams0_23_16	8'h20	USB3_SDWIDTH
			[15:8]	ghwparams0_15_8	8'h40	USB3_MDWIDTH
			[7:6]	ghwparams0_7_6	2'h1	USB3_SBUS_TYPE
			[5:3]	ghwparams0_5_3	3'h1	USB3_MBUS_TYPE

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[2:0]	ghwparams0_2_0	3'h2	USB3_MODE
C144H	GHWPARAMS1	R	[31]	ghwparams1_31	1'h0	USB3_EN_DBC
			[30]	ghwparams1_30	1'h0	USB3_RM_OPT_FEATURES
			[29]	ghwparams1_29	1'h0	Reserved
			[28]	ghwparams1_28	1'h0	USB3_RAM_BUS_CLKS_SYNC
			[27]	ghwparams1_27	1'h0	USB3_MAC_RAM_CLKS_SYNC
			[26]	ghwparams1_26	1'h0	USB3_MAC_PHY_CLKS_SYNC
			[25:24]	ghwparams1_25_24	2'h1	USB3_EN_PWROPT
			[23]	ghwparams1_23	1'h0	USB3_SPRAM_TYP
			[22:21]	ghwparams1_22_21	2'h3	USB3_NUM_RAMS
			[20:15]	ghwparams1_20_15	6'h1	USB3_DEVICE_NUM_INT
			[14:12]	ghwparams1_14_12	3'h4	USB3_ASPACEWIDTH
			[11:9]	ghwparams1_11_9	3'h4	USB3_REQINFOWIDTH
			[8:6]	ghwparams1_8_6	3'h4	USB3_DATAINFOWIDTH
			[5:3]	ghwparams1_5_3	3'h7	USB3_BURSTWIDTH-1
			[2:0]	ghwparams1_2_0	3'h3	USB3_IDWIDTH-1
C148H	GHWPARAMS2	R	[31:0]	ghwparams2_31_0	32'h12345678	USB3_USERID
C14CH	GHWPARAMS3	R	[31]	ghwparams3_31	1'h0	Reserved
			[30:23]	ghwparams3_30_23	8'h9	USB3_CACHE_TOTAL_XFER_RESOURCES
			[22:18]	ghwparams3_22_18	5'h6	USB3_NUM_IN_EPS
			[17:12]	ghwparams3_17_12	6'h9	USB3_NUM_EPS
			[11]	ghwparams3_11	1'h0	USB3_ULPI_CARKIT
			[10]	ghwparams3_10	1'h0	USB3_VENDOR_CTL_INTERFACE

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[9:8]	ghwparams3_9_8	2'h0	Reserved
			[7:6]	ghwparams3_7_6	2'h2	USB3_HSPHY_DWIDTH
			[5:4]	ghwparams3_5_4	2'h0	USB3_FSPHY_INTERFACE
			[3:2]	ghwparams3_3_2	2'h1	USB3_HSPHY_INTERFACE
			[1:0]	ghwparams3_1_0	2'h1	USB3_SSPHY_INTERFACE
C150H	GHWPARAMS4	R	[31:28]	ghwparams4_31_28	4'h4	USB3_BMU_LSP_DEPTH
			[27:24]	ghwparams4_27_24	4'h7	USB3_BMU_PTL_DEPTH-1
			[23]	ghwparams4_23	1'h1	USB3_EN_ISOC_SUPT
			[22]	ghwparams4_22	1'h0	Reserved
			[21]	ghwparams4_21	1'h0	USB3_EXT_BUFF_CONTROL
			[20:17]	ghwparams4_20_17	4'h1	USB3_NUM_SS_USB_INSTANCES
			[16:13]	ghwparams4_16_13	4'h1	USB3_HIBER_SCRATCHBUFS Number of external scratchpad buffers the controller requires to save its internal state in the device mode. Each buffer is assumed to be 4KB. The scratchpad buffer array must have so many buffer pointers.
			[12]	ghwparams4_12	1'h0	Reserved
			[11]	ghwparams4_11	1'h0	Reserved
			[10:9]	ghwparams4_10_9	2'h0	Reserved
			[8:7]	ghwparams4_8_7	2'h0	Reserved
			[6]	ghwparams4_6	1'h0	Reserved
			[5:0]	ghwparams4_5_0	6'h4	USB3_CACHE_TRBS_PER_TRANSFER
C154H	GHWPARAMS5	R	[31:28]	ghwparams5_31_28	4'h0	Reserved
			[27:22]	ghwparams5_27_22	6'h10	USB3_DFQ_FIFO_DEPTH

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[21:16]	ghwparams5_21_16	6'h20	USB3_DWQ_FIFO_DEPTH
			[15:10]	ghwparams5_15_10	6'h8	USB3_TXQ_FIFO_DEPTH
			[9:4]	ghwparams5_9_4	6'h8	USB3_RXQ_FIFO_DEPTH
			[3:0]	ghwparams5_3_0	4'h8	USB3_BMU_BUSGM_DEPTH
C158H	GHWPARAMS6	R	[31:16]	ghwparams6_31_16	16'h774	USB3_RAM0_DEPTH
			[15]	BusFltrsSupport	1'h1	USB3_EN_BUS_FILTERS
			[14]	BCSupport	1'h0	USB3_EN_BC
			[13]	OTG_SS_Support	1'h0	Reserved
			[12]	ADPSupport	1'h0	USB3_EN_ADP
			[11]	HNPSupport	1'h0	Reserved
			[10]	SRPSupport	1'h0	Reserved
			[9:8]	ghwparams6_9_8	2'h0	Reserved
			[7]	ghwparams6_7	1'h0	USB3_EN_FPGA
			[6]	ghwparams6_6	1'h0	USB3_EN_DBG_PORTS
			[5:0]	ghwparams6_5_0	6'h20	USB3_PSQ_FIFO_DEPTH
C15CH	GHWPARAMS7	R	[31:16]	ghwparams7_31_16	16'h308	USB3_RAM2_DEPTH
			[15:0]	ghwparams7_15_0	16'hae5	USB3_RAM1_DEPTH
C160H	GDBGFIFOSPACE	R	[31:16]	SPACE_AVAILABLE	16'h42	SPACE_AVAILABLE
		R	[15:9]	Reserved		

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
		RW	[8:0]	FIFO_QUEUE_SELECT	9'h0	FIFO/Queue Select (or) Port-Select FIFO/Queue Select[8:5] indicates the FIFO/Queue Type. FIFO/Queue Select[4:0] indicates the FIFO/Queue Number. For example, 9'b0_0010_0001 refers to RxFIFO_1 and 9'b0_0101_1110 refers to TxReqQ_30. 9'b0_0001_1111 to 9'b0_0000_0000: TxFIFO_31 to TxFI-FO_0. 9'b0_0011_1111 to 9'b0_0010_0000: RxFIFO_31 to RxFI-FO_0. 9'b0_0101_1111 to 9'b0_0100_0000: TxReqQ_31 to TxReqQ_0. 9'b0_0111_1111 to 9'b0_0110_0000: RxReqQ_31 to RxReqQ_0. 9'b0_1001_1111 to 9'b0_1000_0000: RxInfoQ_31 to RxInfoQ_0. 9'b0_1010_0000: DescFetchQ_0 (for backwards compatibility). 9'b0_1010_0001: EventQ_0 (for backwards compatibility). 9'b0_1010_0010: ProtocolStatusQ_0. 9'b0_1101_1111 to 9'b0_1110_0000: DescFetchQ_31 to DescFetchQ_0. 9'b0_1111_1111 to 9'b0_1110_0000: WriteBack/EventQ_31 to WriteBack/EventQ_0. 9'b1_0000_0111 to 9'b1_0000_0000: AuxEventQ_7 to AuxEventQ_0 (if EN_SEPARATE_DESC_QUEUES=1). Port-Select[3:0] selects the port-number when accessing GDBGLTSSM register.
C164H	GDBGLTSSM	R	[31]	Reserved		
			[30]	RxElecidle	1'h1	RxElecidle For description of RxElecIdle, see table 5-4, "Status Interface Signals" of the PIPE3 Specification.
			[29]	X3_XS_SWAPPING	1'h0	Reserved
			[28]	X3_DS_HOST_SHUTDOWN	1'h0	Reserved

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[27]	PRTDIRECTION	1'h0	Reserved
			[26]	LTDBTIMEOUT	1'h0	LTDB Timeout (LTDBTimeout)
			[25:22]	LTDBLINKSTATE	4'h4	LTDB Link State (LTDBLinkState)
			[21:18]	LTDBSUBSTATE	4'h0	LTDB Sub-State (LTDBSubState)
			[17]	ELASTICBUFFERMODE	1'h0	Elastic Buffer Mode (ElasticBufferMode) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[16]	TXELECLDLE	1'h1	Tx Elec Idle (TxElecIdle) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[15]	RXPOLARITY	1'h0	Rx Polarity (RxPolarity) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[14]	TxDetRxLoopback	1'h0	Tx Detect Rx/Loopback (TxDetRxLoopback) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[13:11]	LTDBPhyCmdState	3'h0	LTSSM PHY command State (LTDBPhyCmdState) 000: PHY_IDLE (PHY command state is in IDLE. No PHY request pending). 001: PHY_DET (Request to start Receiver detection). 010: PHY_DET_3 (Wait for Phy_Status (Receiver detection)). 011: PHY_PWR_DLY (Delay Pipe3_PowerDown P0 -> P1/P2/P3 request). 100: PHY_PWR_A (Delay for internal logic). 101: PHY_PWR_B (Wait for Phy_Status(Power state change request)).
			[10:9]	POWERDOWN	2'h2	POWERDOWN (PowerDown) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[8]	RXEQTRAIN	1'h0	RxEq Train For field definition, refer to Table 5-3 of the PIPE3 specification.

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[7:6]	TXDEEMPHASIS	2'h1	TXDEEMPHASIS (TxDeemphasis) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[5:3]	LTDBClkState	3'h0	LTSSM Clock State (LTDBClkState) In multi-port host configuration, the port number is defined by Port-Select[3:0] field in the GDBGFIFOSPACE register. **Note:** GDBGLTSSM register is not applicable for USB 2.0-only mode. 000: CLK_NORM (PHY is in non-P3 state and PCLK is running). 001: CLK_TO_P3 (P3 entry request to PHY). 010: CLK_WAIT1 (Wait for Phy_Status (P3 request)). 011: CLK_P3 (PHY is in P3 and PCLK is not running). 100: CLK_TO_P0 (P3 exit request to PHY). 101: CLK_WAIT2 (Wait for Phy_Status (P3 exit request)).
			[2]	TXSWING	1'h0	Tx Swing (TxSwing) For field definition, refer to Table 5-3 of the PIPE3 specification.
			[1]	RXTERMINATION	1'h0	Rx Termination (RxTermination)
			[0]	TXONESZEROS	1'h0	Tx Ones/Zeros (TxOnesZeros) For field definition, refer to Table 5-3 of the PIPE3 specification.
C168H	GDBGLNMCC	R	[31:9]	Reserved		
			[8:0]	LNMCC_BERC	9'h0	This field indicates the bit error rate information for the port selected in the GDBGFIFOSPACE.PortSelect field. This field is for debug purposes only.
C16CH	GDBGBMU	R	[31:8]	BMU_BCU	24'h0	BMU_BCU Debug information
			[7:4]	BMU_DCU	4'h0	BMU_DCU Debug information
			[3:0]	BMU_CCU	4'h0	BMU_CCU Debug information
C170H	GDBGLSPMUX_HS_	RW	[31:24]	Reserved		

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	I		[23:16]	logic_analyzer_trace	8'h3f	logic_analyzer_trace Port MUX Select Currently only bits[21:16] are used. A value of 6'h3F drives 0s on the logic_analyzer_trace signal. If you plan to OR (instead using a mux) this signal with other trace signals in your system to generate a common trace signal, you can use this feature.
			[15:14]	Reserved		
			[13:0]	HOSTSELECT	14'h0	Device LSP Select Selects the LSP debug information presented in the GDBGLSP register in host mode.
C174H	GDBGLSP	R	[31:0]	LSPDEBUG	32'h0	LSP Debug Information
C178H	GDBGEPINFO0	R	[31:0]	EPDEBUG	32'h0	Endpoint Debug Information, bits[31:0]
C17CH	GDBGEPINFO1	R	[31:0]	EPDEBUG	32'h800000	Endpoint Debug Information, bits[63:32]
C180H	GPRTBIMAP_HSLO	RW	[31:28]	BINUM8	4'h0	BINUM8: HS USB Instance Number for Port 8. Application-programmable ID field.
			[27:24]	BINUM7	4'h0	BINUM7: HS USB Instance Number for Port 7. Application-programmable ID field.
			[23:20]	BINUM6	4'h0	BINUM6 USB Instance Number for Port 6. Application-programmable ID field.
			[19:16]	BINUM5	4'h0	BINUM5: HS USB Instance Number for Port 5. Application-programmable ID field.
			[15:12]	BINUM4	4'h0	BINUM4: HS USB Instance Number for Port 4. Application-programmable ID field.
			[11:8]	BINUM3	4'h0	BINUM3: HS USB Instance Number for Port 3. Application-programmable ID field.

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[7:4]	BINUM2	4'h0	BINUM2: HS USB Instance Number for Port 2. Application-programmable ID field.
			[3:0]	BINUM1	4'h0	BINUM1: HS USB Instance Number for Port 1. Application-programmable ID field.
C184H	GPRTBIMAP_HSHI	RW	[31:28]	Reserved		
			[27:24]	BINUM15	4'h0	BINUM15: HS USB Instance Number for Port 15. Application-programmable ID field.
			[23:20]	BINUM14	4'h0	BINUM14: HS USB Instance Number for Port 14. Application-programmable ID field.
			[19:16]	BINUM13	4'h0	BINUM13: HS USB Instance Number for Port 13. Application-programmable ID field.
			[15:12]	BINUM12	4'h0	BINUM12: HS USB Instance Number for Port 12. Application-programmable ID field.
			[11:8]	BINUM11	4'h0	BINUM11: HS USB Instance Number for 11. Application-programmable ID field.
			[7:4]	BINUM10	4'h0	BINUM10: HS USB Instance Number for Port 10. Application-programmable ID field.
			[3:0]	BINUM9	4'h0	BINUM9: HS USB Instance Number for Port 9. Application-programmable ID field.
C188H	GPRTBIMAP_FSLO	RW	[31:28]	BINUM8	4'h0	BINUM8: FS USB Instance Number for Port 8. Application-programmable ID field.
			[27:24]	BINUM7	4'h0	BINUM7: FS USB Instance Number for Port 7. Application-programmable ID field.
			[23:20]	BINUM6	4'h0	BINUM6: FS USB Instance Number for Port 6. Application-programmable ID field.

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[19:16]	BINUM5	4'h0	BINUM5: FS USB Instance Number for Port 5. Application-programmable ID field.
			[15:12]	BINUM4	4'h0	BINUM4: FS USB Instance Number for Port 4. Application-programmable ID field.
			[11:8]	BINUM3	4'h0	BINUM3: FS USB Instance Number for Port 3. Application-programmable ID field.
			[7:4]	BINUM2	4'h0	BINUM2: FS USB Instance Number for Port 2. Application-programmable ID field.
			[3:0]	BINUM1	4'h0	BINUM1: FS USB Instance Number for Port 1. Application-programmable ID field.
C18CH	GPRTBIMAP_FSHI	RW	[31:28]	Reserved		
			[27:24]	BINUM15	4'h0	BINUM15: FS USB Instance Number for Port 15. Application-programmable ID field.
			[23:20]	BINUM14	4'h0	BINUM14: FS USB Instance Number for Port 14. Application-programmable ID field.
			[19:16]	BINUM13	4'h0	BINUM13: FS USB Instance Number for Port 13. Application-programmable ID field.
			[15:12]	BINUM12	4'h0	BINUM12: FS USB Instance Number for Port 12. Application-programmable ID field.
			[11:8]	BINUM11	4'h0	BINUM11: FS USB Instance Number for Port 11. Application-programmable ID field.
			[7:4]	BINUM10	4'h0	BINUM10: FS USB Instance Number for Port 10. Application-programmable ID field.
			[3:0]	BINUM9	4'h0	BINUM9: FS USB Instance Number for Port 9. Application-programmable ID field.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C19CH	GUCTL2	RW	[31:26]	Reserved		
			[25:19]	EN_HP_PM_TIMER	7'h33	This register field is used to set new HP and PM timers. To enable PM timer, set GUCTL2[19] bit as 1. To enable HP timer, set GUCTL2[20] bit as 1. Default value of HP timer is 4us when HP PM timer is not enabled; when new HP timer is enabled default value is 12us. Use GUCTL2[25:21] to specify HP timer value in microseconds.
			[18:15]	NOLOWPWRDUR	4'h0	No Low Power Duration (NOLOWPWRDUR) After starting a transfer on a SS ISOC endpoint, the application must program these bits to prevent the device to lose frame synchronization over a period of time. Based on this count-down counter, the device will wake itself from U1/U2 low power states. After entering to U0 state and receiving two ITPs (which will sync up the host and the device), U1/U2 low power entry is allowed. Each count represents the duration in terms of milliseconds. For example, a value of 3 represents 3ms. To disable this feature, set this field to 4'b0. These bits are applicable only in device mode and ignored in host mode. Some xHCI hosts do not send ITPs when performing ISOC transfers when the link enters U1/U2 low power states. This causes the device to lose frame synchronization over a period of time resulting in ISOC packets being dropped.
			[14]	Rst_actbitlater	1'h0	Enable clearing of the command active bit for the ENDXFER command after the command execution is completed. This bit is valid in device mode only.
			[13]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	EnableEpCacheEvict	1'h0	Enable Evicting Endpoint cache after Flow Control for bulk endpoints. In 3.00a release, a performance enhancement was done to keep the non-stream capable bulk IN endpoint in cache after flow control. Setting this bit will disable this enhancement. This should be set only for debug purpose.
				[11]	DisableCFC	1'h0	Disable xHCI Errata Feature Contiguous Frame ID Capability This field controls the xHCI Errata feature Contiguous FrameID capability. When set, the xHCI HCCPARAMS1 bit 11 will be set to 0 indicating that CFC is not supported. Disable this feature only if your application cannot tolerate Missed Service Error events for Isoc transfers, and your system latencies are large to cause Missed Service errors even if the software is following the Isochronous Thresholding rules.
				[10:5]	RxPingDuration	6'h20	Receive Ping Maximum Duration This field is relevant to Host mode and controls the maximum duration of received LFPS to be treated as a Ping LFPS. The Max duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 32 indicates 256 ns.
				[4:0]	TxPingDuration	5'hd	Transmit Ping Maximum Duration This field is relevant to Device mode and controls the maximum duration for which the controller should instruct the PHY to transmit a Ping LFPS. The duration of the Ping LFPS is controlled by programming this value and is in terms of 8 ns granularity. Eg: A value of 13 indicates 104 ns.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C200H	GUSB2PHYCFG	RW	[31]	PHYSOFTRST	1'h0	UTMI PHY Soft Reset (PHYSoftRst) Causes the usb2phy_reset signal to be asserted to reset a UTMI PHY. Not applicable to ULPI, and the controller automatically writes to this register when the controller is reset.
		RW	[30]	U2_FREECLK_EXISTS	1'h1	U2_FREECLK_EXISTS Specifies whether your USB 2.0 PHY provides a free-running PHY clock, which is active when the clock control input is active. If your USB 2.0 PHY provides a free-running PHY clock, it must be connected to the utmi_clk[0] input. The remaining utmi_clk[n] must be connected to the respective port clocks. The controller uses the Port-0 clock for generating the internal mac2 clock. 0: USB 2.0 free clock does not exist. 1: USB 2.0 free clock exists. **Note:** When the controller is configured as device-only, do not set this bit to 1.
		RW	[29]	ULPI_LPM_WITH_OPMODE_CHK	1'h0	ULPI_LPM_WITH_OPMODE_CHK Support the LPM over ULPI without NOPID token to the ULPI PHY. If this bit is set, the ULPI PHY is expected to qualify the EXT PID with OPMODE=2'b00 for LPM and not treat it as a NOPID. Check with your PHY vendor about your PHY behavior. 0: A NOPID is sent before sending an EXTPID for LPM. 1: An EXTPID is sent without previously sending a NOPID. **Note:** This bit is valid only in host mode. This bit should be 0 for our PHY.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[28:27]	HSIC_CON_WIDTH_ADJ	2'h0	HSIC_CON_WIDTH_ADJ This bit is used in the HSIC device mode of operation. By default, the connect duration for the HSIC device controller is thrice the strobe period. You can change this duration to 4, 5, or 6 times the strobe period by setting the value of this field to 1, 2, or 3. This value is added to the default connect duration.
			R	[26]	INV_SEL_HSIC	1'h0	INV_SEL_HSIC The application driver uses this bit to control the HSIC enable /disable function. When set to 1, this bit overrides and functionally inverts the "if_select_hsic" input signal. If {INV_SEL_HSIC, if_select_hsic} is: 00: HSIC Capability is disabled. 01: HSIC Capability is enabled. 10: HSIC Capability is enabled. 11: HSIC Capability is disabled. If the controller operates as non-HSIC-capable, it can only connect to non-HSIC-capable PHYs. If it operates as HSIC-capable, it can connect to HSIC-capable PHYs. When selecting the HSIC feature, set the host side to HSIC mode first, then set the device mode side. If the device side is set to HSIC mode first and if the host does not see a connection in HSIC mode, then you must de-select the device HSIC mode and select it again using the if_select_hsic setting or bit GUSB2PHYCFGn[26] to ensure that the device can connect to the host.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[25]	OVRD_FSLS_DISC_TIME	1'h0	Overriding the FS/LS disconnect time to 32us. 0: The FS/LS disconnect time is set to 2.5us as per the USB specification. 1: The disconnect detection time is set to 32us. Normally, this value is set to 0. However, if the USB 2.0 PHYs introduce noise on the UTMI LineState and cause SE0 glitches longer than 2.5us, then a false disconnect condition may get triggered. To avoid interoperability issues with these PHYs, this bit can be set to 1.
			RW	[24:22]	LSTRD	3'h0	LS Turnaround Time (LSTRDTIM) This field indicates the value of the Rx-to-Tx packet gap for LS devices. The encoding is as follows: 0: 2 bit times. 1: 2.5 bit times. 2: 3 bit times. 3: 3.5 bit times. 4: 4 bit times. 5: 4.5 bit times. 6: 5 bit times. 7: 5.5 bit times. This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h0 (2 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the Open LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the device's delay requirement.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[21:19]	LSIPD	3'h2	LS Inter-Packet Time (LSIPD) This field indicates the value of Tx-to-Tx packet gap for LS devices. The encoding is as follows: 0: 2 bit times. 1: 2.5 bit times. 2: 3 bit times. 3: 3.5 bit times. 4: 4 bit times. 5: 4.5 bit times. 6: 5 bit times. 7: 5.5 bit times. This field is applicable only in Host mode. For normal operation (to work with most LS devices), set the default value of this field to 3'h2 (3 bit times). The programmable LS device inter-packet gap and turnaround delays are provided to support some legacy LS devices that might require different delays than the default/fixed ones. For instance, the AOpen LS mouse requires 3 bit times of inter-packet gap to work correctly. Include your PHY delays when programming the LSIPD/LSTRDTIM values. For example, if your PHY's TxEndDelay in LS mode is 30 UTMI/ULPI CLKs, then subtract this delay (~1 LS bit time) from the device's delay requirement.
			RW	[18]	ULPIEXTVBUSINDICTOR	1'h0	ULPI External VBUS Indicator (ULPIExtVbusIndicator) Indicates the ULPI PHY VBUS over-current indicator. 0: PHY uses an internal VBUS valid comparator. 1: PHY uses an external VBUS valid comparator.
			RW	[17]	ULPIEXTVBUSDRV	1'h0	ULPI External VBUS Drive (ULPIExtVbusDrv) Selects supply source to drive 5V on VBUS, in the ULPI PHY. 0: PHY drives VBUS with internal charge pump (default). 1: PHY drives VBUS with an external supply.
			R	[16]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[15]	ULPIAUTORES	1'h0	ULPI Auto Resume (ULPIAutoRes) Sets the AutoResume bit in Interface Control register on the ULPI PHY. 0: PHY does not use the AutoResume feature. 1: PHY uses the AutoResume feature.
			R	[14]	Reserved		
			RW	[13:10]	USBTRDTIM	4'h9	USB 2.0 Turnaround Time (USBTrdTim) Sets the turnaround time in PHY clocks. Specifies the response time for a MAC request to the Packet FIFO Controller (PFC) to fetch data from the DFIFO (SPRAM). The following are the required values for the minimum SoC bus frequency of 60 MHz. USB turnaround time is a critical certification criteria when using long cables and five hub levels. The required values for this field: 4'h5: When the MAC interface is 16-bit UTMI+. 4'h9: When the MAC interface is 8-bit UTMI+/ULPI. If SoC bus clock is less than 60 MHz, and USB turnaround time is not critical, this field can be set to a larger value. This field is valid only in device mode.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[9]	XCVRDLY	1'h0	Transceiver Delay: Enables a delay between the assertion of the UTMI/ULPI Transceiver Select signal (for HS) and the assertion of the TxValid signal during a HS Chirp. When this bit is set to 1, a delay (of approximately 2.5 us) is introduced from the time when the Transceiver Select is set to 2'b00 (HS) to the time the TxValid is driven to 0 for sending the chirp-K. This delay is required for some UTMI/ULPI PHYs. If you enable the hibernation feature when the device controller comes out of power-off, you must re-initialize this bit with the appropriate value because the controller does not save and restore this bit value during hibernation. This bit is valid only in device mode.
			RW	[8]	ENBLSLPM	1'h0	Enable utmi_sleep_n and utmi_l1_suspend_n (EnblSlpM) The application uses this bit to control utmi_sleep_n and utmi_l1_suspend_n assertion to the PHY in the L1 state. 0: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is not transferred to the external PHY. 1: utmi_sleep_n and utmi_l1_suspend_n assertion from the controller is transferred to the external PHY. **Note:** This bit must be set high for Port0 if our PHY is used. In Device mode - Before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. Without disabling this bit, if a command is issued when the device is in L1 state and if mac2_clk (utmi_clk /ulpi_clk) is gated off, the command will not get completed.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W	[7]	PHYSEL	1'h0	USB 2.0 High-Speed PHY or USB 1.1 Full-Speed Serial Transceiver Select The application uses this bit to select a high-speed PHY or a full-speed transceiver. 0: USB 2.0 high-speed UTMI+ or ULPI PHY. This bit is always 0, with Write Only access. 1: USB 1.1 full-speed serial transceiver. This bit is always 1, with Write Only access. If both interface types are selected in coreConsultant the application uses this bit to select the active interface is active, with Read-Write bit access. **Note:** USB 1.1 full-serial transceiver is not supported. This bit always reads as 1'b0.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[6]	SUSPENDUSB20	1'h0	Suspend USB2.0 HS/FS/LS PHY (SusPHY) When set, USB2.0 PHY enters Suspend mode if Suspend conditions are valid. For DRD configurations, it is recommended that this bit is set to 0 during coreConsultant configuration. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the controller initialization completes. For all other configurations, this bit can be set to 1 during controller configuration. **Note:** In host mode, on reset, this bit is set to 1. Software can override this bit after reset. In device mode, before issuing any device endpoint command when operating in 2.0 speeds, disable this bit and enable it after the command completes. If you issue a command without disabling this bit when the device is in L2 state and if mac2_clk (utmi_clk/ulpi_clk) is gated off, the command will not get completed.
			R	[5]	FSINTF	1'h0	Full-Speed Serial Interface Select (FSIntf) The application uses this bit to select a unidirectional or bidirectional USB 1.1 full-speed serial transceiver interface. 0: 6-pin unidirectional full-speed serial interface. This bit is set to 0 with Read Only access. 1: 3-pin bidirectional full-speed serial interface. This bit is set to 0 with Read Only access. **Note:** USB 1.1 full-speed serial interface is not supported. This bit always reads as 1'b0.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[4]	ULPI_UTMI_Sel	1'h0	ULPI or UTMI+ Select (ULPI_UTMI_Sel) The application uses this bit to select a UTMI+ or ULPI Interface. 0: UTMI+ Interface. 1: ULPI Interface. This bit is writable only if UTMI+ and ULPI is specified for High-Speed PHY Interface(s). Otherwise, this bit is read-only.
			RW	[3]	PHYIF	1'h0	PHY Interface (PHYIf) If UTMI+ is selected, the application uses this bit to configure the controller to support a UTMI+ PHY with an 8- or 16-bit interface. 0: 8 bits. 1: 16 bits. ULPI Mode: 1'b0 **Note:** - All the enabled 2.0 ports must have the same clock frequency as Port0 clock frequency (utmi_clk[0]). - The UTMI 8-bit and 16-bit modes cannot be used together for different ports at the same time (that is, all the ports must be in 8-bit mode, or all of them must be in 16-bit mode, at a time). - If any of the USB 2.0 ports is selected as ULPI port for operation, then all the USB 2.0 ports must be operating at 60 MHz.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
		RW	[2:0]	TOutCal	3'h0	HS/FS Timeout Calibration (TOutCal) The number of PHY clocks, as indicated by the application in this field, is multiplied by a bit-time factor; this factor is added to the high-speed/full-speed interpacket timeout duration in the controller to account for additional delays introduced by the PHY. This may be required, since the delay introduced by the PHY in generating the LineState condition may vary among PHYs. The USB standard timeout value for high-speed operation is 736 to 816 (inclusive) bit times. The USB standard timeout value for full-speed operation is 16 to 18 (inclusive) bit times. The application must program this field based on the speed of connection. The number of bit times added per PHY clock are: High-speed operation: - One 30-MHz PHY clock = 16 bit times. - One 60-MHz PHY clock = 8 bit times. Full-speed operation: - One 30-MHz PHY clock = 0.4 bit times. - One 60-MHz PHY clock = 0.2 bit times. - One 48-MHz PHY clock = 0.25 bit times.
C240H	GUSB2I2CCTL	R	[31:0]	Reserved		
C280H	GUSB2PHYACC_ULPI	R	[31:27]	Reserved		
			[26]	DISUIPIDRVR	1'h0	DISUIPIDRVR
			[25]	NEWREGREQ	1'h0	New Register Request The application sets this bit for a new vendor control access. Setting this bit to 1 asserts the utmi_vcontrolload_n (1'b0) on the UTMI interface.
			[24]	VSTSDONE	1'h0	VSTSDONE

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23]	VSTSBSY	1'h0	VSTSBSY
				[22]	REGWR	1'h0	Register Write The application sets this bit for register writes and clears it for register reads. **Note:** This bit is applicable for ULPI register read/write access only.
				[21:16]	REGADDR	6'h0	Register Address The 6-bit PHY register address for immediate PHY Register Set access. Set to 6'h2F for Extended PHY Register Set access. **Note:** These bits are applicable for ULPI only.
				[15:8]	EXTREGADDR	8'h0	EXTREGADDR
				[7:0]	REGDATA	8'h0	REGDATA
	C2C0H	GUSB3PIPECTL	RW	[31]	PHYSoftRst	1'h0	USB3 PHY Soft Reset After setting this bit to 1, the software needs to clear this bit.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[30]	HstPrtCmpl	1'h0	HstPrtCmpl This feature tests the PIPE PHY compliance patterns without having to have a test fixture on the USB 3.0 cable. This bit enables placing the SS port link into a compliance state. By default, this bit must be set to 1'b0. In compliance lab testing, the SS port link enters compliance after failing the first polling sequence after power on. Set this bit to 0, when you run compliance tests. The sequence for using this functionality is as follows: 1. Disconnect any plugged in devices. 2. Perform USBCMD.HCRST or power-on-chip reset. 3. Set PORTSC.PLS=0xA. 4. Set PORTSC.PP=0. 5. Set GUSB3PIPECTL. HstPrtCmpl=1. This places the link into compliance state. To advance the compliance pattern, follow this sequence (toggle the set GUSB3PIPECTL. HstPrtCmpl): 1. Set GUSB3PIPECTL.HstPrtCmpl=0. 2. Set GUSB3PIPECTL.HstPrtCmpl=1. This advances the link to the next compliance pattern. To exit from the compliance state perform USBCMD.HCRST or power-on-chip reset.
			RW	[29]	U2P3ok	1'h0	P3 OK for SSInactive (SSIP3ok) 0: During link state SS.Inactive, put PHY in P2 (Default) 1: During link state SS.Inactive, put PHY in P3.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[28]	DisRxDetP3	1'h0	Disabled receiver detection in P3 (DisRxDetP3) 0: If PHY is in P3 and controller needs to perform receiver detection, The controller performs receiver detection in P3 (Default). 1: If PHY is in P3 and controller needs to perform receiver detection, The controller changes the PHY power state to P2 and then performs receiver detection. After receiver detection, the cores changes PHY power state to P3.
			RW	[27]	Ux_exit_in_Px	1'h0	Ux Exit in Px (Ux_exit_in_Px) 0: The controller does U1/U2/U3 exit in PHY power state P0 (default). 1: The controller does U1/U2/U3 exit in PHY power state P1/P2/P3 respectively. **Note:** This bit is used by third-party SS PHY. It must be set to 0 for our PHY.
			RW	[26]	ping_enhancement_en	1'h0	Ping Enhancement Enable (ping_enhancement_en) When set, the Downstream port U1 ping receive timeout becomes 500 ms instead of 300 ms. Minimum Ping.LFPS receive duration is 8 ns (one mac3_clk). This field is valid for the downstream port only. **Note:** This bit is used by third-party SS PHY. It must be set to 0 for our PHY.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[25]	u1u2exitfail_to_recov	1'h0	U1U2exitfail to Recovery (u1u2exitfail_to_recov) When set, and U1/U2 LFPS handshake fails, the LTSSM transitions from U1/U2 to Recovery instead of SS Inactive. If Recovery fails, then the LTSSM can enter SS.Inactive. This is an enhancement only. It prevents interoperability issue if the remote link does not do proper handshake.
			RW	[24]	request_p1p2p3	1'h1	Always Request P1/P2/P3 for U1/U2/U3 (request_p1p2p3) When set, the controller always requests PHY power change from P0 to P1/P2/P3 during U0 to U1/U2/U3 transition. If this bit is 0, and immediate Ux exit (remotely initiated, or locally initiated) happens, the controller does not request P1/P2/P3 power state change. **Note:** This bit must be set to 1 for Our PHY. For third-party SS PHY, check with your PHY vendor.
			W	[23]	StartRxDetU3RxDet	1'h0	Start Receiver Detection in U3/Rx.Detect (StartRxdetU3RxDet) This feature must not be enabled for normal operation.
			RW	[22]	DisRxDetU3RxDet	1'h0	Disable Receiver Detection in U3/Rx.Det When set, the controller does not handle receiver detection in either U3 or Rx.Detect states. This feature must not be enabled for normal operation.
			RW	[21:19]	DelayP1P2P3	3'h1	Delay P1P2P3 Delay P0 to P1/P2/P3 request when entering U1/U2/U3 until (USB3_GUSB3PIPECTL_INIT[21:19]*8) 8B10B error occurs, or Pipe3_RxValid drops to 0.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[18]	DELAYP1TRANS	1'h1	Delay PHY power change from P0 to P1/P2/P3 when link state changing from U0 to U1/U2/U3 respectively. 0: When entering U1/U2/U3, transition to P1/P2/P3 without checking for Pipe3_RxElecIdle and pipe3_RxValid. 1: When entering U1/U2/U3, delay the transition to P1/P2/P3 until the pipe3 signals, Pipe3_RxElecIdle is 1 and pipe3_RxValid is 0. **Note:** You need to check with your PHY vendor for recommendation on setting this bit.
			RW	[17]	SUSPENDENABLE	1'h0	Suspend USB3.0 SS PHY (Suspend_en) When set, and if Suspend conditions are valid, the USB 3.0 PHY enters Suspend mode. For DRD configurations, it is recommended that this bit is set to 0 during coreConsultant configuration. If it is set to 1, then the application must clear this bit after power-on reset. Application needs to set it to 1 after the controller initialization is completed. For all other configurations, this bit can be set to 1 during controller configuration.
			R	[16:15]	DATWIDTH	2'h0	PIPE Data Width (DatWidth) 00: 32 bits. 01: 16 bits. One clock after reset, these bits receive the value seen on the pipe3_DataBusWidth. **Note:** 8-bit data width is not supported.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[14]	AbortRxDetInU2	1'h0	Abort Rx Detect in U2 (AbortRxDetInU2) When set and the link state is U2, the controller will abort receiver detection if it receives U2 exit LFPS from the remote link partner. This bit is for the downstream port only. **Note:** This bit is used by third-party SS PHY. It must be set to 0 for our PHY.
			RW	[13]	SkipRxDet	1'h0	Skip Rx Detect: When set, the controller skips Rx Detection if pipe3_RxElecIdle is low. Skip is defined as waiting for the appropriate timeout, then repeating the operation.
			RW	[12]	LFPSP0Algn	1'h0	LFPS P0 Align When set, - The controller deasserts LFPS transmission on the clock edge that it requests Phy power state 0 when exiting U1, U2, or U3 low power states. Otherwise, LFPS transmission is asserted one clock earlier. - The controller requests symbol transmission two pipe3_rx_pclks periods after the PHY asserts PhyStatus as a result of the PHY switching from P1 or P2 state to P0 state. Currently, this bit is only used in USB 3.0 HUB with our PHY. For other USB 3.0 Host, Device, and DRD cores, this bit is not required.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[11]	P3P2TranOK	1'h0	P3 P2 Transitions OK (P3P2TranOK) When set, the controller transitions directly from Phy power state P2 to P3 or from state P3 to P2. When not set, P0 is always entered as an intermediate state during transitions between P2 and P3, as defined in the PIPE3 Specification. According to the PIPE3 Specification, any direct transition between P3 and P2 is illegal. **Note:** This bit is used by third-party SS PHY. It must be set to 0 for our PHY.
			RW	[10]	P3ExSigP2	1'h0	P3 Exit Signal in P2 (P3ExSigP2) When this bit is set, the controller always changes the PHY power state to P2, before attempting a U3 exit handshake. This bit is used only for some third-party PHYs that cannot do LFPS in P3. **Note:** This bit is used by third-party SS PHY. It must be set to 0 for our PHY.
			RW	[9]	LFPSFILTER	1'h0	LFPS Filter (LFPSFilt) When set, filter LFPS reception with pipe3_RxValid in PHY power state P0, that is, ignore LFPS reception from the PHY unless both pipe3_Rxelecidle and pipe3_RxValid are deasserted.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
		RW	[8]	RX_DETECT_to_Polling_LFPS_Control	1'h0	RX_DETECT to Polling.LFPS Control 0 (Default): Enables a 400us delay to start Polling LFPS after RX_DETECT. This allows VCM offset to settle to a proper level. 1: Disables the 400us delay to start Polling LFPS after RX_DETECT. During controller certification with third party PHY it is observed that the PHY is not able to meet the Tx AC common mode voltage active (VTX-CM-ACPP_ACTIVE <100mv) if the link starts polling within 80us from the time rx.detect is performed. To meet this VTX-CM-ACPP_ACTIVE specification, the polling must be delayed further. If the PHY does not have issue then they can set this bit to 1 which allows polling to start within 80us.
		RW	[7]	SSICEn	1'h0	This field is not used.
		RW	[6]	TX_SWING	1'h0	Tx Swing (TxSwing) Refer to the PIPE3 specification.
		RW	[5:3]	TX_MARGIN	3'h0	Tx Margin[2:0] (TxMargin) Refer to Table 5-3 of the PIPE3 Specification.
		RW	[2:1]	SS_TX_DE_EMPHASIS	2'h1	Tx Deemphasis (TxDeemphasis) The value driven to the PHY is controlled by the LTSSM during USB3 Compliance mode. (Refer to Table 5-3 of the PIPE3 specification.)
		RW	[0]	ELASTIC_BUFFER_MODE	1'h0	Elastic Buffer Mode (ElasticBufferMode) (Refer to Table 5-3 of the PIPE3 specification.)
C300H	GTXFIFOSIZ0	RW	[31:16]	TXFSTADDR_N	16'h0	Transmit FIFO0 RAM Start Address This field contains the memory start address for TxFIFO0 in MDWIDTH-bit words.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	TXFDEP_N	16'h42	TxFIFO Depth This field contains the depth of TxFIFO0 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768
C304H	GTXFIFOSIZ1	RW	[31:16]	TXFSTADDR_N	16'h42	Transmit FIFO1 RAM Start Address This field contains the memory start address for TxFIFO1 in MDWIDTH-bit words.
			[15:0]	TXFDEP_N	16'h307	TxFIFO Depth This field contains the depth of TxFIFO1 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768
C308H	GTXFIFOSIZ2	RW	[31:16]	TXFSTADDR_N	16'h349	Transmit FIFO2 RAM Start Address This field contains the memory start address for TxFIFO2 in MDWIDTH-bit words.
			[15:0]	TXFDEP_N	16'h307	TxFIFO Depth This field contains the depth of TxFIFO2 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768
C30CH	GTXFIFOSIZ3	RW	[31:16]	TXFSTADDR_N	16'h650	Transmit FIFO3 RAM Start Address This field contains the memory start address for TxFIFO3 in MDWIDTH-bit words.
			[15:0]	TXFDEP_N	16'h187	TxFIFO Depth This field contains the depth of TxFIFO3 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
C310H	GTXFIFOSIZ4	RW	[31:16]	TXFSTADDR_N	16'h7d7	Transmit FIFO4 RAM Start Address This field contains the memory start address for TxFIFO4 in MDWIDTH-bit words.
			[15:0]	TXFDEP_N	16'h187	TxFIFO Depth This field contains the depth of TxFIFO4 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768
C314H	GTXFIFOSIZ5	RW	[31:16]	TXFSTADDR_N	16'h95e	Transmit FIFO5 RAM Start Address This field contains the memory start address for TxFIFO5 in MDWIDTH-bit words.
			[15:0]	TXFDEP_N	16'h187	TxFIFO Depth This field contains the depth of TxFIFO5 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 32,768
C380H	GRXFIFOSIZ0	RW	[31:16]	RXFSTADDR_N	16'h0	RxFIFO0 RAM Start Address (RxFStAddr_n) This field contains the memory start address for RxFIFO0 in MDWIDTH-bit words.
			[15:0]	RXFDEP_N	16'h305	RxFIFO Depth (RxFDep_n) This field contains the depth of RxFIFO0 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 16,384
C384H	GRXFIFOSIZ1	RW	[31:16]	RXFSTADDR_N	16'h305	RxFIFO1 RAM Start Address (RxFStAddr_n) This field contains the memory start address for RxFIFO1 in MDWIDTH-bit words.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	RXFDEP_N	16'h0	RxFIFO Depth (RxFDep_n) This field contains the depth of RxFIFO1 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 16,384
C388H	GRXFIFOSIZ2	RW	[31:16]	RXFSTADDR_N	16'h305	RxFIFO2 RAM Start Address (RxFStAddr_n) This field contains the memory start address for RxFIFO2 in MDWIDTH-bit words.
			[15:0]	RXFDEP_N	16'h0	RxFIFO Depth (RxFDep_n) This field contains the depth of RxFIFO2 in MDWIDTH-bit words. Minimum value: 32 Maximum value: 16,384
C400H	GEVNTADRLO	RW	[31:0]	EVNTADRLO	32'h0	Event Buffer Address (EvntAdrLo) Holds the lower 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.
C404H	GEVNTADRHI	RW	[31:0]	EVNTADRHI	32'h0	Event Buffer Address (EvntAdrHi) Holds the higher 32 bits of start address of the external memory for the Event Buffer. During operation, hardware does not update this address.
C408H	GEVNTSIZ	RW	[31]	EVNTINTRPTMASK	1'h0	Event Interrupt Mask (EvntIntMask). When set to 1, this prevents the interrupt from being generated. However, even when the mask is set, the events are queued.
			[30:16]	Reserved		
			[15:0]	EVENTSIZ	16'h0	Event Buffer Size in bytes (EVNTSiz) Holds the size of the Event Buffer in bytes; must be a multiple of four. This is programmed by software once during initialization. The minimum size of the event buffer is 32 bytes.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
C40CH	GEVNTCOUNT	RW	[31]	EVNT_HANDLER_BUSY	1'h0	Event Handler Busy Device software event handler busy indication. The controller sets this bit when the interrupt line is asserted due to pending events. Software clears this bit (with 1'b1) when it has finished processing the events (along with updating the EVNTCOUNT in this register). The controller does not raise the interrupt line for a new event unless this bit is cleared. **Note:** When Interrupt moderation is disabled (that is, DEVICE_IMODI = 0), this bit is ignored.
			[30:16]	Reserved		
			[15:0]	EVNTCOUNT	16'h0	Event Count (EVNTCount) When read, returns the number of valid events in the Event Buffer (in bytes). When written, hardware decrements the count by the value written. When Interrupt moderation is enabled (that is, DEVICE_IMODI!= 0), the interrupt line gets de-asserted when the first write happens on this register to decrement the count. When Interrupt moderation is disabled (that is, DEVICE_IMODI = 0), the Interrupt line continues to get asserted until the event count becomes zero (no-moderation behavior).
C600H	GHWPARAMS8	R	[31:0]	ghwparams8_32_0	32'h774	USB3_DCACHE_DEPTH_INFO
C60CH	GUCTL3	RW	[31:17]	Reserved		
			[16]	Sch_Ping_early	1'h1	Enable SuperSpeed Ping Transaction Packet scheduling early in the microframe. This bit is valid in Host mode only.

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	Reserved		
C610H	GTXFIFOPRIDEV	RW	[x:0]	gtxfifopridev	6'h0	Device TxFIFO priority
C618H	GTXFIFOPRIHST	RW	[x:0]	gtxfifoprihst	3'h0	Host TxFIFO priority
C61CH	GRXFIFOPRIHST	RW	[x:0]	grxfifoprihst	3'h0	Host RxFIFO priority
C624H	GDMAHLRATIO	RW	[31:13]	Reserved		
			[12:8]	hstrxfifo	5'h8	Host RXFIFO DMA High-Low Priority
			[7:5]	Reserved		
			[4:0]	hsttxfifo	5'h8	Host TXFIFO DMA High-Low Priority

C630H	GFLADJ	RW	[31]	GFLADJ_REFCLK_240MHZDECR_PLS1	1'h0	GFLADJ_REFCLK_240MHZDECR_PLS1
						This field indicates that the decrement value that the controller applies for each ref_clk must be GFLADJ_REFCLK_240MHZ_DECR and GFLADJ_REFCLK_240MHZ_DECR +1 alternatively on each ref_clk.
						Set this bit to a 1 only if GFLADJ_REFCLK_LPM_SEL is set to 1 and the fractional component of 240/ref_frequency is greater than or equal to 0.5.
						Examples:
						If the ref_clk is 19.2 MHz then
						- GUCTL.REF_CLK_PERIOD = 52.
						- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/19.2) = 12.5.
						- GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 1.
						If the ref_clk is 24 MHz then
						- GUCTL.REF_CLK_PERIOD = 41.
						- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = (240/24) = 10.
						- GFLADJ.GFLADJ_REFCLK_240MHZDECR_PLS1 = 0.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description

				[30:24]	GFLADJ_REFCLK_240MHZ_DECR	7'h0	This field indicates the decrement value that the controller applies for each ref_clk in order to derive a frame timer in terms of a 240-MHz clock.
							This field must be programmed to a non-zero value only if GFLADJ_REFCLK_LPM_SEL is set to 1.
							The value is derived as follows:
							GFLADJ_REFCLK_240MHZ_DECR = 240/ref_clk_frequency
							Examples: If the ref_clk is 24 MHz then
							- GUCTL.REF_CLK_PERIOD = 41.
							- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/24 = 10.
							If the ref_clk is 48 MHz then
							- GUCTL.REF_CLK_PERIOD = 20.
							- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/48 = 5.
							If the ref_clk is 17 MHz then
							- GUCTL.REF_CLK_PERIOD = 58.
							- GFLADJ.GFLADJ_REFCLK_240MHZ_DECR = 240/17 = 14.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23]	GFLADJ_REFCLK_LPM_SEL	1'h0	This bit enables the functionality of running SOF/ITP counters on the ref_clk. This bit must not be set to 1 if GCTL.SOFITPSYNC bit is set to 1. Similarly, if GFLADJ_REFCLK_LPM_SEL set to 1, GCTL.SOFITPSYNC must not be set to 1. In device mode, setting this bit to 1 enables SOF tracking using ref_clk. When GFLADJ_REFCLK_LPM_SEL is set to 1 the overloading of the suspend control of the USB 2.0 first port PHY (UTMI/ULPI) with USB 3.0 port states is removed. For example, for our PHY, the COMMONONN signal can be tied to 1. **Note:** The ref_clk frequencies supported in this mode are 16/17/19.2 /20/24/39.7/40 MHz. The utmi_clk[0] signal of the controller must be connected to the FREECLK of the PHY. If you set this bit to 1, the GUSB2PHYCFG.U2_FREECLK_EXISTS bit must be set to 0.
				[22]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[21:8]	GFLADJ_REFCLK_FLADJ	14'h0	This field indicates the frame length adjustment to be applied when SOF/ITP counter is running on the ref_clk. This register value is used to adjust the ITP interval when GCTL[SOFITPSYNC] is set to 1; SOF and ITP interval when GLADJ.GFLADJ_REFCLK_LPM_SEL is set to 1. This field must be programmed to a non-zero value only if GFLADJ _REFCLK_LPM_SEL is set to 1 or GCTL.SOFITPSYNC is set to 1. The value is derived as follows: FLADJ_REF_CLK_FLADJ=((125000/ref_clk_period_integer)-(125000/ref_clk_period)) * ref_clk_period where - the ref_clk_period_integer is the integer value of the ref_clk period got by truncating the decimal (fractional) value that is programmed in the GUCTL.REF_CLK_PERIOD field. - the ref_clk_period is the ref_clk period including the fractional value. Examples: If the ref_clk is 24 MHz then - GUCTL.REF_CLK_PERIOD = 41. - GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/41)-(125000/41.6666))*41.6666 = 2032. If the ref_clk is 48 MHz then - GUCTL.REF_CLK_PERIOD = 20. - GFLADJ.GLADJ_REFCLK_FLADJ = ((125000/20)-(125000/20.8333))*20.8333 = 5208.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[7]	GFLADJ_30MHZ_SDBND_SEL	1'h0	GFLADJ_30MHZ_SDBND_SEL This field selects whether to use the input signal fladj_30mhz_reg or the GFLADJ.GFLADJ_30MHZ to adjust the frame length for the SOF/ITP. 0: The controller uses the input signal fladj_30mhz_reg value. 1: The controller uses the register field GFLADJ.GFLAD-J_30MHZ value.
			[6]	Reserved		
			[5:0]	GFLADJ_30MHZ	6'h0	GFLADJ_30MHZ This field indicates the value that is used for frame length adjustment instead of considering from the sideband input signal fladj_30mhz_reg. This enables post-silicon frame length adjustment in case the input signal fladj_30mhz_reg is connected to a wrong value or is not valid.
C640H	GUSB2RHBCTL	RW	[31:4]	Reserved		
			[3:0]	OVRD_L1TIMEOUT	4'h0	Overriding the driver programmed L1TIMEOUT value. If this value is 0, the L1 Timeout value is taken from the xHCI PORTHLPMC register. If this value is non-0, then this will override the L1 Timeout value programmed in the xHCI PORTHLPMC register. In that case the actual L1 Timeout would be 2 ^ <OVRD_L1TIMEOUT-1> * 8us. (1=8us, 2=16us, 3=32us etc).
C700H	DCFG	RW	[31:25]	Reserved		
			[24]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23]	IgnStrmPP	1'h0	IgnoreStreamPP This bit only affects stream-capable bulk endpoints. When this bit is set to 0 and the controller receives a Data Packet with the Packet Pending (PP) bit set to 0 for OUT endpoints, or it receives an ACK with the NumP field set to 0 and PP set to 0 for IN endpoints, the controller attempts to search for another stream (CStream) to initiate to the host. However, there are two situations where this behavior is not optimal: - When the host is setting PP=0 even though it has not finished the stream, or - When the endpoint on the device is configured with one transfer resource and therefore does not have any other streams to initiate to the host. When this bit is set to 1, the controller ignores the Packet Pending bit for the purposes of stream selection and does not search for another stream when it receives DP(PP=0) or ACK(NumP=0, PP=0). This can enhance the performance when the device system bus bandwidth is low or the host responds to the controller's ERDY transmission very quickly.
				[22]	LPMCAP	1'h0	LPM Capable The application uses this bit to control the LPM capabilities of the DWC_usb3 controller. If the controller operates as a non-LPM-capable device, it cannot respond to LPM transactions. 0: LPM capability is not enabled. 1: LPM capability is enabled.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[21:17]	NUMP	5'h4	Number of Receive Buffers. This bit indicates the number of receive buffers to be reported in the ACK TP. The usb3 controller uses this field for non-control endpoints if GRXTHRCFG.UsbRxPktCntSel is set to 0. The application can program this value based on RxFIFO size, buffer sizes programmed in descriptors, and system latency. For an OUT endpoint, this field controls the number of receive buffers reported in the NumP field of the ACK TP transmitted by the controller. **Note:** This bit is used in host mode when Debug Capability is enabled.
				[16:12]	INTRNUM	5'h0	Interrupt number Indicates interrupt/EventQ number on which non-endpoint-specific device-related interrupts (see DEVT) are generated.
				[11:10]	Reserved		
				[9:3]	DEVADDR	7'h0	Device Address. The application must perform the following: - Program this field after every SetAddress request. - Reset this field to zero after USB reset.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[2:0]	DEVSPD	3'h4	Device Speed. Indicates the speed at which the application requires the controller to connect, or the maximum speed the application can support. However, the actual bus speed is determined only after the chirp sequence is completed, and is based on the speed of the USB host to which the controller is connected. 100: SuperSpeed (USB 3.0 PHY clock is 125 MHz or 250 MHz). 000: High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz). 001: Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz). Values: 0x4 (SuperSpeed): SuperSpeed (USB 3.0 PHY clock is 125 MHz or 250 MHz). 0x0 (HighSpeed): High-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz). 0x1 (FullSpeed): Full-speed (USB 2.0 PHY clock is 30 MHz or 60 MHz).

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	C704H	DCTL	RW	[31]	RUN_STOP	1'h0	Run/Stop The software writes 1 to this bit to start the device controller operation. To stop the device controller operation, the software must remove any active transfers and write 0 to this bit. When the controller is stopped, it sets the DSTS.DevCtrlHlt bit when the controller is idle and the lower layer finishes the disconnect process. The Run/Stop bit must be used in following cases as specified: - After power-on reset and CSR initialization, the software must write 1 to this bit to start the device controller. The controller does not signal connect to the host until this bit is set. - The software uses this bit to control the device controller to perform a soft disconnect. When the software writes 0 to this bit, the host does not see that the device is connected. The device controller stays in the disconnected state until the software writes 1 to this bit. The minimum duration of keeping this bit cleared is specified in the Note below. If the software attempts a connect after the soft disconnect or detects a disconnect event, it must

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							set DCTL[8:5] to 5 before reasserting the Run/Stop bit. - When the USB or Link is in a lower power state and the Two Power Rails configuration is selected, software writes 0 to this bit to indicate that it is going to turn off the Core Power Rail. After the software turns on the Core Power Rail again and re-initializes the device controller, it must set this bit to start the device controller. **Note:** The following is the minimum duration under various conditions for which the soft disconnect (SftDiscon) bit must be set for the USB host to detect a device disconnect: 30ms: - For SuperSpeed, when the device state is Suspended, Idle, Transmit, or Receive. 10ms: - For high-speed, when the device state is Suspended, Idle, or not Idle/Suspended (performing transactions) - For full-speed/low-speed, when the device state is Suspended, Idle, or not Idle/Supended (performing transactions) To accommodate clock jitter, it is recommended that the application add extra delay to the specified minimum duration.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
		RW1S	[30]	CSFTRST	1'h0	Core Soft Reset Resets the all clock domains as follows: - This bit clears the interrupts and all the CSRs except GSTS, GSNPSID, GGPIO, GUID, GUSB2PHYCFG, GUSB3PIPECTL, DCFG, DCTL, DEVTEN, and DSTS registers. - All module state machines (except the SoC Bus Slave Unit) are reset to the IDLE state, and all the TxFIFOs and the RxFIFO are flushed. - Any transactions on the SoC bus Master are terminated as soon as possible, after gracefully completing the last data phase of a SoC bus transfer. Any transactions on the USB are terminated immediately. The application can write this bit at any time to reset the controller. This is a self-clearing bit; the controller clears this bit after all necessary logic is reset in the controller, which may take several clocks depending on the current state of the controller. Once this bit is cleared, the software must wait at least 3 PHY clocks before accessing the PHY domain (synchronization delay). Typically, software reset is used during software development and also when you dynamically change the PHY selection bits in the USB configuration registers listed above. When you change the PHY, the corresponding clock for the PHY is selected and used in the PHY domain. Once a new clock is selected, the PHY domain must be reset for proper operation. **Note:** Programming this field with random data causes side effect . Bit Bash register testing is not recommended.
		R	[29]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[28:24]	HIRDTHRES	5'h0	HIRD Threshold (HIRD_Thres) The controller asserts output signals utmi_l1_suspend_n and utmi_sleep_n on the basis of this signal: The controller asserts utmi_l1_suspend_n to put the PHY into Deep Low-Power mode in L1 when both of the following are true: - HIRD value is greater than or equal to the value in DCTL.HIRD_Thres[3:0]. - HIRD_Thres[4] is set to 1'b1. The controller asserts utmi_sleep_n on L1 when one of the following is true: - If the HIRD value is less than HIRD_Thres[3:0] or - HIRD_Thres[4] is set to 1'b0. **Note:** This field must be set to 0 during SuperSpeed mode of operation.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[23:20]	LPM_NYET_thres	4'hf	LPM NYET Threshold When LPM Errata is enabled: Bits [23:20]: LPM NYET Response Threshold (LPM_NYET_thres) Handshake response to LPM token specified by device application. Response depends on DCFG.LPMCap. DCFG.LPMCap is 1'b0 - The controller always responds with Timeout (that is, no response). DCFG.LPMCap is 1'b1 - The controller responds with an ACK on successful LPM transaction, which requires that all of the following are satisfied: - There are no PID or CRC5 errors in both the EXT token and the LPM token (if not true, inactivity results in a timeout ERROR). - No data is pending in the TxFIFO and RxFIFO is empty (else NYET). - The BESL value in the LPM token is less than or equal to LPM_NYET_thres[3:0].

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[19]	KeepConnect	1'h0	Keep Connect When 1, this bit enables the save and restore programming model by preventing the controller from disconnecting from the host when DCTL.RunStop is set to 0. It also enables the Hibernation Request Event to be generated when the link goes to U3 or L2. The device controller disconnects from the host when DCTL.RunStop is set to 0. This bit indicates whether to preserve this behavior (0), or if the controller must not disconnect when RunStop is set to 0 (1). This bit also prevents the LTSSM from automatically going to U0/L0 when the host requests resume from U3/L2. **Note:** If Hibernation is disabled, that is, GCTL[1] (GblHibernationEn) = 0, this bit is tied to zero.
			RW	[18]	L1HibernationEn	1'h0	L1HibernationEn When this bit is set along with KeepConnect, the device controller generates a Hibernation Request Event if L1 is enabled and the HIRD value in the LPM token is larger than the threshold programmed in DCTL.HIRD_Thres. The controller does not exit the LPM L1 state until software writes Recovery into the DCTL.ULStChngReq field. This prevents corner cases where the device is entering hibernation at the same time the host is attempting to exit L1. **Note:** If Hibernation is disabled, that is, GCTL[1] (GblHibernationEn) = 0, this bit is tied to zero.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[17]	CRS	1'h0	Controller Restore State (CRS) This command is similar to the USBCMD.CRS bit in host mode and initiates the restore process. When software sets this bit to 1, the controller immediately sets DSTS.RSS to 1. When the controller has finished the restore process, it sets DSTS.RSS to 0. When read, this field always returns 0.
			RW	[16]	CSS	1'h0	Controller Save State (CSS) This command is similar to the USBCMD.CSS bit in host mode and initiates the save process. When software sets this bit to 1, the controller immediately sets DSTS.SSS to 1. When the controller has finished the save process, it sets DSTS.SSS to 0. When read, this field always returns 0.
			R	[15:13]	Reserved		
			RW	[12]	INITU2ENA	1'h0	Initiate U2 Enable 0: May not initiate U2 (default). 1: May initiate U2. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature(U2_ENABLE), and clears this bit when ClearFeature(U2_ENABLE) is received. If DCTL[11] (AcceptU2Ena) is 0, the link immediately exits U2 state.
			RW	[11]	ACCEPTU2ENA	1'h0	Accept U2 Enable 0: Rejects U2 except when Force_LinkPM_Accept bit is set (default). 1: Controller accepts transition to U2 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[10]	INITU1ENA	1'h0	Initiate U1 Enable 0: May not initiate U1 (default). 1: May initiate U1. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving SetFeature(U1_ENABLE), and clears this bit when ClearFeature(U1_ENABLE) is received. If DCTL[9] (AcceptU1Ena) is 0, the link immediately exits U1 state.
			RW	[9]	ACCEPTU1ENA	1'h0	Accept U1 Enable 0: Controller rejects U1 except when Force_LinkPM_Accept bit is set (default). 1: Controller accepts transition to U1 state if nothing is pending on the application side. On USB reset, hardware clears this bit to 0. Software sets this bit after receiving a SetConfiguration command.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			W	[8:5]	ULSTCHNGREQ	4'h0	ULSTCHNGREQ Software writes this field to issue a USB/Link state change request. A change in this field indicates a new request to the controller. If software wants to issue the same request back-to-back, it must write a 0 to this field between the two requests. The result of the state change request is reflected in the USB/Link State in DSTS. These bits are self-cleared on the MAC Layer exiting suspended state. If software is updating other fields of the DCTL register and not intending to force any link state change, then it must write a 0 to this field. SS Compliance mode is normally entered and controlled by the remote link partner. Refer to the USB 3.0 specification. Alternatively, you can force the local link directly into compliance mode, by resetting the SS link with the RUN/STOP bit set to zero. If you write '10' to the USB/Link State Change field and 1 to

USB Device

BASE_ADDR: 0xB200_0000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
						RUN/STOP, the link goes to compliance mode. Once you are in compliance, you may alternately write zero and '10' to this field to advance the compliance pattern. In SS mode, value requested Link state transition/action: 0: No Action. 4: SS.Disabled. 5: Rx.Detect. 6: SS.Inactive. 8: U3 exit request. 0: Compliance. Others: Reserved. In HS/FS/LS mode, value requested USB state transition: 8: Remote wakeup request. Others: Reserved. The Remote wakeup request must be issued 2us after the device goes into suspend state (DSTS[21:18] is 3). **Note:** After coming out of hibernation, software must write 8 (Recovery) into this field to confirm exit from the suspended state.
		RW	[4:1]	TSTCTL	4'h0	Test Control 4'b000: Test mode disabled. 4'b001: Test_J mode. 4'b010: Test_K mode. 4'b011: Test_SE0_NAK mode. 4'b100: Test_Packet mode. 4'b101: Test_Force_Enable. Others: Reserved.
		R	[0]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	C708H	DEVTEN	R	[31:17]	Reserved		
			R	[16]	ECCERREN	1'h0	ECC Error Enable. If this bit is set to 1, the controller reports an ECC error to the software when an uncorrectable ECC occurs internally.
			R	[15]	Reserved		
			RW	[14]	L1WKUPEVTEN	1'h0	L1 Resume Detected Event Enable. **Note:** If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for L1 Resume Detected Event Enable.
			RW	[13]	Reserved		
			RW	[12]	VENDEVTSTRCVDEN	1'h0	Vendor Device Test LMP Received Event (VndrDevTstRcvedEn)
			R	[11:10]	Reserved		
			RW	[9]	ERRTICERREVTEN	1'h0	Erratic Error Event Enable
			RW	[8]	L1SUSPEN	1'h0	L1 Suspend Event Enable **Note:** Only if GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, this bit is for L1 Suspend Event Enable.
			RW	[7]	SOFTEVTEN	1'h0	Start of (u)frame
			RW	[6]	U3L2L1SuspEn	1'h0	U3/L2 or U3/L2L1 Suspend Event Enable. If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Suspend Event Enable. If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Suspend Event Enable.
			RW	[5]	HibernationReqEvtEn	1'h0	This bit enables/disables the generation of the Hibernation Request Event.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[4]	WKUPEVTEN	1'h0	U3/L2 or U3/L2L1 Resume Detected Event Enable. If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is enabled, then this bit is for U3/L2 Resume Detected Event Enable. If GUCTL1[DEV_DECOUPLE_L1L2_EVT] is not enabled, then this bit is for U3/L2L1 Resume Detected Event Enable.
			RW	[3]	ULSTCNGEN	1'h0	USB/Link State Change Event Enable
			RW	[2]	CONNECTDONEEVTEN	1'h0	Connection Done Enable
			RW	[1]	USBRSTEVTEN	1'h0	USB Reset Enable
			RW	[0]	DISSCONNEVTEN	1'h0	Disconnect Detected Event Enable
	C70CH	DSTS	R	[31:30]	Reserved		
			R	[29]	DCNRD	1'h0	Device Controller Not Ready The bit indicates that the controller is in the process of completing the state transitions after exiting from hibernation. To complete the state transitions, it takes 256 bus clock cycles from the time DCTL[31].Run/Stop is set. During hibernation, if the UTMI/ULPI PHY is in suspended state, then the 256-bus clock cycle delay starts after the PHY exited suspended state. Software must set DCTL[31].Run/Stop to 1 and wait for this bit to be de-asserted to zero before processing DSTS.USBLnkSt. This bit is valid only when USB3_EN_PWROPT is set to 2 and GCTL[1].GblHibernationEn =1.
			RW1C	[28]	SRE	1'h0	Save Restore Error. Currently not supported.
			R	[27:26]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[25]	RSS	1'h0	RSS Restore State Status This bit is similar to the USBSTS.RSS in host mode. When the controller has finished the restore process, it completes the command by setting DSTS.RSS to 0.
			R	[24]	SSS	1'h0	SSS Save State Status This bit is similar to the USBSTS.SSS in host mode. When the controller has finished the save process, it completes the command by setting DSTS.SSS to 0.
			R	[23]	COREIDLE	1'h1	Core Idle The bit indicates that the controller finished transferring all RxFIFO data to system memory, writing out all completed descriptors, and all Event Counts are zero. **Note:** While testing for Reset values, mask out the read value. This bit represents the changing state of the controller and does not hold a static value.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[22]	DEVCTRLHLT	1'h1	Device Controller Halted This bit is set to 0 when the Run/Stop bit in the DCTL register is set to 1. The controller sets this bit to 1, after SW sets Run/Stop to 0, the controller is idle and the lower layer finishes the disconnect process. When Halted=1, the controller does not generate Device events. **Note:** The controller does not set this bit to 1 if GEVNTCOUNT has some valid value. Software needs to acknowledge the events that are generated (by writing to GEVNTCOUNT) while it is waiting for this bit to be set to 1. When Interrupt Moderation is enabled, there could be delay in raising the interrupt line when the event count is non-zero. Software should read the GEVNTCOUNT register directly and acknowledge them.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			R	[21:18]	USBLNKST	4'h4	USB/Link State In SS mode: LTSSM State. 4'h0: U0. 4'h1: U1. 4'h2: U2. 4'h3: U3. 4'h4: SS_DIS. 4'h5: RX_DET. 4'h6: SS_INACT. 4'h7: POLL. 4'h8: RECOV. 4'h9: HRESET. 4'ha: CMPLY. 4'hb: LPBK. 4'hf: Resume/Reset In HS/FS/LS mode: 4'h0: On state. 4'h2: Sleep (L1) state. 4'h3: Suspend (L2) state 4'h4: Disconnected state (Default state) 4'h5: Early Suspend state (valid only when Hibernation is disabled, GCTL[1].GblHibernationEn = 0) 4'he: Reset (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) 4'hf: Resume (valid only when Hibernation is enabled, GCTL[1].GblHibernationEn = 1) The link state Resume/Reset indicates that the controller received a resume or USB reset request from the host while the link was in hibernation. Software must write '8' (Recovery) to the DCTL.ULStChngReq field to acknowledge the resume/reset request.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							When Hibernation is enabled, GCTL[1].GblHibernationEn = 1, this field USBLnkSt is valid only when DCTL[31].Run/Stop set to 1 and DSTS[29].DCNRD = 0. The Early Suspend link state is an early indication of device suspend in HS/FS. The link state changes to Early Suspend after detecting bus idle for 3ms. In HS operation, this is an indication that the USB bus (that is, LineState) has been in idle (SE0) for 3ms. However, it does not confirm whether the next process is Suspend or Reset. The device checks the bus again after pull up enable delay and if the line state indicates Suspend (full speed J), then the device waits for an additional time (~3ms) to indicate the actual Suspend state. In FS operation, this is an indication that the USB bus (that is, LineState) has been in idle (J) for 3ms. The device waits for an additional time (~3ms of Idle) to indicate the actual Suspend state.
			R	[17]	RXFIFOEMPTY	1'h1	RxFIFO Empty.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
		R	[16:3]	SOFFN	14'h0	Frame/Microframe Number of the Received SOF. When the controller is operating at SuperSpeed, [16:3] indicates the uframe/ITP number. When the controller is operating at high-speed, [16:6] indicates the frame number, [5:3] indicates the microframe number. When the controller is operating at full-speed, [16:14] is not used. Software can ignore these 3 bits. [13:3] indicates the frame number. **Note:** After power-on reset, the controller generates the microframe number internally for every 125us if the USB host has not issued SOF/ITP yet. During P3 state, the duration of SOFFN is based on the suspend_clk frequency.
		R	[2:0]	CONNECTSPD	3'h4	Connected Speed (ConnectSpd) Indicates the speed at which the DWC_usb3 controller has come up after speed detection through a chirp sequence. 100: SuperSpeed (PHY clock is running at 125 or 250 MHz). 000: High-speed (PHY clock is running at 30 or 60 MHz). 001: Full-speed (PHY clock is running at 30 or 60 MHz). Low-speed is not supported for devices using a UTMI+ PHY. Values: 0x4 (SuperSpeed): SuperSpeed (PHY clock is running at 125 or 250 MHz). 0x0 (HighSpeed): High-speed (PHY clock is running at 30 or 60 MHz). 0x1 (FullSpeed): Full-speed (PHY clock is running at 30 or 60 MHz).
C710H	DGCMDPAR	RW	[31:0]	PARAMETER	32'h0	PARAMETER

USB Device	BASE_ADDR: 0xB200_0000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
	C714H	DGCMD	R	[31:16]	Reserved		
			R	[15:12]	CMDSTATUS	4'h0	Command Status 0: Indicates command success. 1: CmdErr: Indicates that the device controller encountered an error while processing the command.
			R	[11]	Reserved		
			RW1S	[10]	CMDACT	1'h0	Command Active The software sets this bit to 1 to enable the device controller to execute the generic command. The device controller sets this bit to 0 after executing the command.
			R	[9]	Reserved		
			RW	[8]	CMDIOC	1'h0	Command Interrupt on Complete When this bit is set, the device controller issues a Generic Command Completion event after executing the command. This interrupt is mapped to DCFG.IntrNum. **Note:** This field must not set to 1 if the DCTL.RunStop field is 0.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[7:0]	CMDTYP	8'h0	Generic Command Type Specifies the type of generic command the software driver is requesting the controller to perform. 02h: Set Periodic Parameters. 04h: Set Scratchpad Buffer Array Address Lo. 05h: Set Scratchpad Buffer Array Address Hi. 07h: Transmit Device Notification. 09h: Selected FIFO Flush. 0Ah: All FIFO Flush. 0Ch: Set Endpoint NRDY. 10h: Run SoC Bus LoopBack Test. 11h: Restart After Disconnect. All other values are reserved.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
C720H	DALEPENA	RW	[31:0]	USBACTEP	32'h0	USB Active Endpoints (USBActEP) This field indicates if a USB endpoint is active in the current configuration and interface. It applies to USB IN endpoints 0.15 and OUT endpoints 0.15, with one bit for each of the 32 possible endpoints. Even numbers are for USB OUT endpoints, and odd numbers are for USB IN endpoints, as follows: Bit[0]: USB EP0-OUT. Bit[1]: USB EP0-IN. Bit[2]: USB EP1-OUT. Bit[3]: USB EP1-IN. The entity programming this register must set bits 0 and 1 because they enable control endpoints that map to physical endpoints (resources) after USBReset. Hardware clears these bits for all endpoints (other than EP0-OUT and EP0-IN) after detecting a USB reset event. After receiving SetConfiguration and SetInterface requests, the application must program endpoint registers accordingly and set these bits.
C724H	Reserved	R	[31:0]	Reserved		
C800H	DEPCMDPAR2	RW	[31:0]	PARAMETER	32'h0	PARAMETER
C804H	DEPCMDPAR1	RW	[31:0]	PARAMETER	32'h0	PARAMETER
C808H	DEPCMDPAR0	RW	[31:0]	PARAMETER	32'h0	PARAMETER

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	C80CH	DEPCMD	RW	[31:16]	COMMANDPARAM	16'h0	Command Parameters or Event Parameters Command Parameters (CommandParam), when this register is written: For Start Transfer command: [31:16]: StreamID. The USB StreamID assigned to this transfer. For Start Transfer command applied to an isochronous endpoint: [31:16]: StartMicroFramNum: Indicates the (micro)frame number to which the first TRB applies. For Update Transfer, End Transfer, and Start New Configuration commands [22:16]: Transfer Resource Index (XferRscIdx). The hardware-assigned transfer resource index for the transfer, which was returned in response to the Start Transfer command. The application software-assigned transfer resource index for a Start New Configuration command.
				[15:12]	CMDSTATUS	4'h0	Command Completion Status (CmdStatus) Additional information about the completion of this command is available in this field. The information is in the same format as bits[15:12] of the Endpoint Command Complete event.
				[11]	HIPRI_FORCERM	1'h0	HighPriority/ForceRM (HiPri_ForceRM) HighPriority: Only valid for Start Transfer command. ForceRM: Only valid for End Transfer command. ClearPendIN: Only valid for Clear Stall command . Software sets this bit to clear any pending IN transaction (on that endpoint) stuck at the lower layers when a Clear Stall command is issued.

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10]	CMDACT	1'h0	Command Active (CmdAct) Software sets this bit to 1 to enable the device endpoint controller to execute the generic command. The device controller sets this bit to 0 when the CmdStatus field is valid and the endpoint is ready to accept another command. This does not imply that all the effects of the previously-issued command have taken place.
				[9]	Reserved		
				[8]	CMDIOC	1'h0	Command Interrupt on Complete (CmdIOC) When this bit is set, the device controller issues a generic Endpoint Command Complete event after executing the command. This interrupt is mapped to DEPCFG.IntrNum. When the DEPCFG command is executed, the command interrupt on completion goes to the interrupt pointed by the DEPCFG.IntrNum in the current command. **Note:** This field must not set to 1 if the DCTL.RunStop field is 0.
				[7:4]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3:0]	CMDTYP	4'h0	Command Type Specifies the type of command the software driver is requesting the controller to perform. 00h: Reserved. 01h: Set Endpoint Configuration - -64 or 96-bit Parameter. 02h: Set Endpoint Transfer Resource Configuration - 32-bit Parameter. 03h: Get Endpoint State - No Parameter Needed. 04h: Set Stall - No Parameter Needed. 05h: Clear Stall - No Parameter Needed. 06h: Start Transfer - 64-bit Parameter. 07h: Update Transfer - No Parameter Needed. 08h: End Transfer - No Parameter Needed. 09h: Start New Configuration - No Parameter Needed.
	CA00H	DEV_IMOD	RW	[31:16]	DEVICE_IMODC	16'h0	Interrupt Moderation Down Counter Loaded with the DEVICE_IMODI value, whenever the hardware interrupt(n) line is de-asserted from the asserted state, counts down to 0, and stops. The interrupt(n) is signaled whenever this counter is 0, EVNT_HANDLER_BUSY is 0, and there are pending events (that is, event count is non-zero). This counter may be directly written by software at any time to alter the interrupt rate.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[15:0]	DEVICE_IMODI	16'h0	Moderation Interval (DEVICE_IMODI) This field holds the minimum inter-interrupt interval between events. The interval is specified in terms of 250ns increments. A value of 0 disables the interrupt throttling logic and interrupts are generated immediately if event count becomes non-zero. In scaledown simulation mode, 4 ram clocks are used to time 250ns.
D000H	LU1LFPSRXTIM	RW	[31:16]	Reserved		
			[15:8]	u1u2_lfps_exit_rx_clk	8'h1f	Programmable U1U2 LFPS EXIT RX CLKS Applicable to Remote Partner initiated Ux exit: Time to recognize valid Ux exit request from the remote partner. This field is encoded as the pipe clk (8ns) count for the LFPS. 1: 8ns. 2: 16ns. 3: 24ns, and so on.
			[7:0]	u1u2_exit_rsp_rx_clk	8'h1f	Programmable U1U2 EXIT RESP RX CLKS Applicable to locally initiated Ux exit: Minimum LFPS reception from remote to consider Ux exit handshake is successful. This field is encoded as the pipe clk (8ns) count for the LFPS. 1: 8ns. 2: 16ns. 3: 24ns, and so on.
D020H	LINK_SETTINGS	RW	[31]	Reserved		Reserved
			[30:28]	u1_resid_timer_us	3'h4	Programmable U1 MIN RESIDENCY TIMER This field specifies U1 MIN RESIDENCY TIMER value in us. A value of 0 disables the timer.
			[27]	Reserved		

USB Device	BASE_ADDR: 0xB200_0000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[26:24]	pm_lc_timer_us	3'h5	Programmable PM_LC_TIMER This field specifies PM_LC_TIMER value in us.
				[23:20]	pm_entry_timer_us	4'h9	Programmable PM_ENTRY_TIMER This field specifies PM_ENTRY_TIMER value in us.
				[19:0]	Reserved		
	D024H	LLUCTL		[31:30]	Reserved		
				[29]	support_p4_pg	1'h0	PHY P4 Power gate mode (PG) is enabled. Set this bit if the PHY supports PG mode in P4. This bit is used only for our PHY.
				[28]	support_p4	1'h0	Support PHY P3.CPM and P4 Power States When this bit is set, the controller puts the PHY in P3.CPM or P4 in certain states. This bit is used only for our PHY.
				[27:24]	Reserved		
				[23]	DisRxDet_LTSSM_Timer_Ovrrd	1'h1	DisRxDet_LTSSM_Timer_Ovrrd When DisRxDetU3RxDet is asserted in Polling or U1, the timeout expires immediately.
				[22:13]	Reserved		
				[12]	U2P3CPMok	1'h0	P3CPM OK for U2/SSInactive (U2P3CPMok) 0: During link state U2/SS.Inactive, put PHY in P2 (Default). 1: During link state U2/SS.Inactive, put PHY in P3CPM. **Note:** For a port, if both GUCTL1[25]=1 and LUCTL[12]=1, LUCTL[12]=1 takes priority.

USB Device

BASE_ADDR: 0xB200_0000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[11]	en_reset_pipe_after_phy_mux	1'h0	en_reset_pipe_after_phy_mux The controller issues USB 3.0 PHY reset after DisRxDetU3RxDet is de-asserted.
			[10:8]	Reserved		
			[7]	mask_pipe_reset	1'h1	Mask pipe reset If this bit is set, controller blocks pipe_reset_n from going to the PHY when DisRxDetU3RxDet=1.
			[6]	Reserved		
			[5]	no_ux_exit_p0_trans	1'h0	no_ux_exit_p0_trans Link LTSSM detects Ux_exit LFPS when P0 transition is on-going by default. If this bit is set, Link LTSSM may miss Ux_exit LFPS when P0 transition is happening.
			[4:0]	Reserved		
D028H	LPTMDPDELAY	RW	[31:22]	Reserved		
			[21:10]	p3cpmp4_residency	12'h3	p3cpmp4 residency timer value Minimum number of suspend_clk periods that the controller needs to stay in P3.CPM or P4 before exiting P3.CPM or P4. This field is used only for our PHY.
			[9:0]	Reserved		
D800H	U3RHBDBG	RW	[31:4]	Reserved		
			[3]	tpcfg_tout_ctrl	1'h0	tpcfg_tout_ctrl This bit controls the USB 3.0 port configuration timeout duration. 0: The port configuration timeout counter does not reset if the link enters recovery or exits U0. 1: The port configuration timeout counter resets when the link is not in U0.

USB Device	BASE_ADDR: 0xB200_0000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
				[2:0]	Reserved		