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Horizon Robotics

Sunrise 3 Hardware Reference Design Errata

Rev. 0.4

July 12, 2021

Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
V 0.1	2020-11-12	Initial Draft for VAA ramp up rate issue and reset circuit
V0.2	2020-11-25	Add Design note for CNN power supply
V0.3	2021-01-28	Add Section 2.4 USB device hot plug support.
V0.4	2021-07-12	Add Section 2.5 EFUSE_VDD Connection

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1 Scope

This document describes the potential problems found during the verification of the Sunrise 3 DVB. The documents is applicable to the following Sunrise 3 DVB schematic and PCB layout revision.

Table 1-1 applicable reference design revision

Design	Filename	
Schematic	SC-2510-2-2a-dv-sm-01a_20200826a SC-2510-3-2a-dv-sm-01b_20200826a SC-2510-6-2A-DV-SM-01C_20200907	
PCB	LO-2510-2-2A-DV-SM-01A_11221500 LO-2510-3-2A-DV-SM-01B_ddr4_202001201530 LO-2510-6-2A-DV-SM-01C_20200828	

2 Schematic Design Note

2.1 DDR PHY power rail ramp up rate

Issue description:

Some of the Power rails of Sunrise 3 integrate a typical ESD protection circuit depicted by the following figure.

When VDD ramp up too fast (ESD transient), the RC delay circuit will keep Vrc low and Vg high, then Mesd will be opened to sink the ESD transient to VSS。

However, if normal power up event has too fast ramp up rate, it will mis-trigger the Mesd and has the very small potential to damage the Mesd after numerous power-up events.

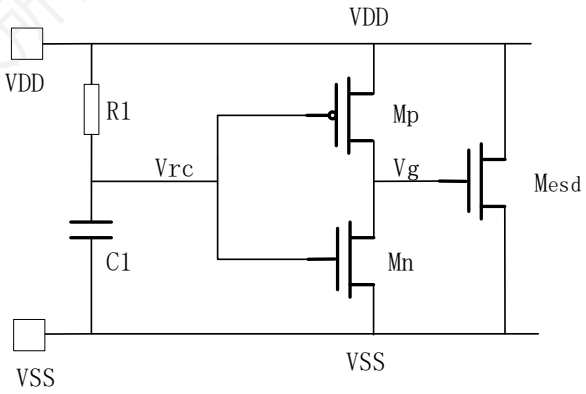

Figure 2-1 Sunrise 3 integrated ESD protection

The following table summarizes the requirements on the ramp up rate of Sunrise 3 's power rails.

Table 2-1 Sunrise 3 power ramp up rate requirements

Power rail	VDDQ_DDR VDDQLP_DDR VAA	VP_MIPI VPH_MIPI	VDD_USB VP_USB VPH_USB	EFUSE_VDD	ARMPLL_VDDPST ARMPLL_VDDHV ARMPLL_VDDREF	**Others**
Ramp up rate	<5mV/us	<100mV/us	<100mV/us	<60mV/us	No requirement	<18mV/us

Regarding the Sunrise 3 reference design, the failed power rail is VAA and PVT_VDDA_TAVDD. The actual measured ramp up rate is around 25mV/us.

Workaround:

There are two options to eliminate the potential risk.

- One option is to use a discrete LDO power supply which has < 5mv/us ramp up rate.
- The 2nd option is to use the following soft start circuit between the LDO output and VAA.

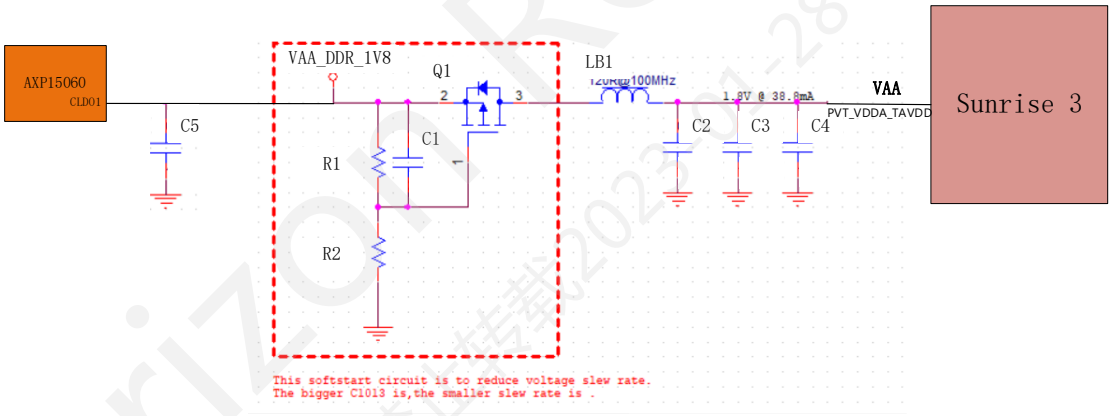

Figure 2-2 DDR PHY VAA ramp up rate control circuit

The following table describes the recommended value for passive components.

Table 2-2 passive components value recommendation

Ref.	Value	Vendor	Part number	Notes
C1	2.2uF	-	-	3
C2	10uF	-	-	-
C3	1uF	-	-	-
C4	0.1uF	-	-	-
C5	4.7uF	-	-	-
R1	100K Ohm	-	-	-

R2	10K Ohm	-	-	-
Q1	-	NEXPERIA	PMV160UP	1,2
LB1	120Ohm@100Mhz	-	-	-

Notes：

1. select Q1 with small Rdson (<200mOhm) and continuous Id drain current > 200mA
2. Make sure voltage feed into VAA still meets the ripple requirement (1.8V+/- 2.5%)
3. Adjust the value of C1 to achieve < 5mV/us ramp up rate.

2.2 Reset Circuit

Sunrise 3 needs external Power-On-Reset (POR) input through RSTN pin to reset the entire chip. The RSTN should be stable more than 10ms after all the power groups (1/2/3/4) achieve target value and 24MHz main clock is active and stable.

Figure 2-3 shows the recommended connection of external POR circuit.

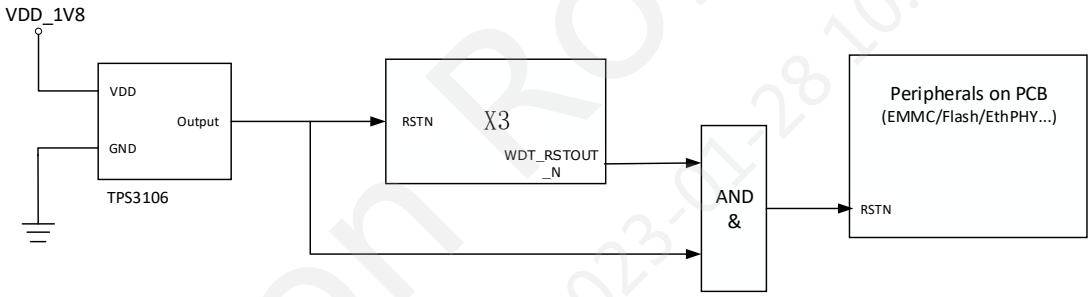

Figure 2-3 External POR reset circuit

WDT_RSTOUT_N is an active-low reset output signal and generated by X3 watchdog timeout event, it is used to reset peripherals on the board, EMMC, Flash, Ethernet PHY, etc.

***Note**:* WDT_RSTOUT_N signal needs to be sent to peripherals on the board especially memory devices (EMMC and Flash) and can't be sent back to X3's RSTN input signal via PCB trace.

2.3 CNN Power supply

Issue description:

Because Sunrise3's CNN behavior causes much higher di/dt (current variation over time) than other core power supply, the power supply to CNN core needs to have better transient load response performance. Otherwise, transient voltage drop will occur on VRM's output. Please check the following figure for this phenomenon.

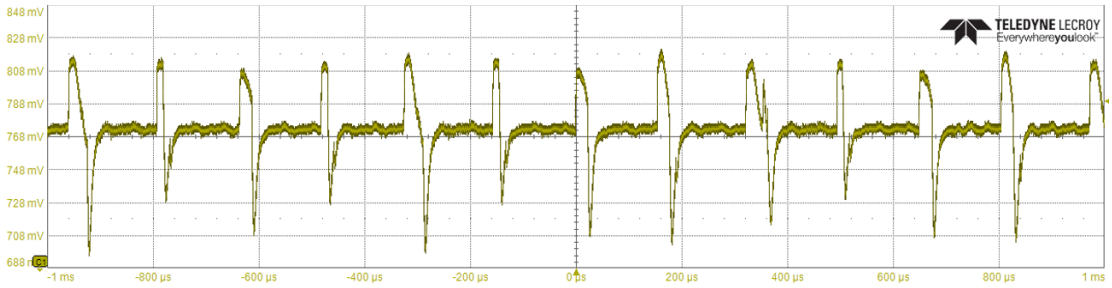

Figure 2-4 CNN Power supply transient voltage drop

Workaround:

To mitigate the potential problem caused by the voltage drop, there are 2 ways to improve the situation.

- First way is to choose a DCDC/PMIC with better transient load response performance, the following table depict a reference requirement for DCDC/PMIC transient load response.

Table 2-3 Reference DCDC/PMIC transient load response requirement

Transient load regulation	Undershoot	Overshoot
Under typical Cout **Iload (di/dt) = 2A/us**	Vout – 25mV	Vout + 25mV

- 2nd way is to increase Cout to BIGGER value if the PCB space could accommodate the extra component. The following table gives some reference part number which could be used. Customer could choose their own part number with enough capacitance and small ESR.

Table 2-4 Suggested Bulk Capacitor Part Number

Vendor	Part Number	Value	ESR
Panasonic	EEFSX0D331XE	330uF	6 mΩ max
Panasonic	EEFSX0D471ER	470uF	9 mΩ max

NOTE: Balance the DCDC/PMIC selection and Bulk capacitor selection to achieve the result depicted by following table. Be noted that the measurement should be done under customer typical scenario with BPU in maximum loading.

Table 2-5 CNN0/1 power supply

Power rail	Typical voltage	V peak to peak
VDD_CNN0/1	0.82V	*< 82mV (+/-5%)*

2.4 USB Device mode Hot-plug Support

Issue description:

When Sunrise3 acts as USB device, extra consideration should be taken to support the Hot-plug feature.

USB_VBUS pin is not functional available at the package ball. The 30KΩ pull up resistor is no longer needed, and the VBUS detection is also not available through USB_VBUS pin.

Workaround:

Solution A: use a separate GPIO to detect the VBUS insertion. Please refer to the Figure 2-5 for the detail connection. Dedicated software thread is needed for GPIO status polling.

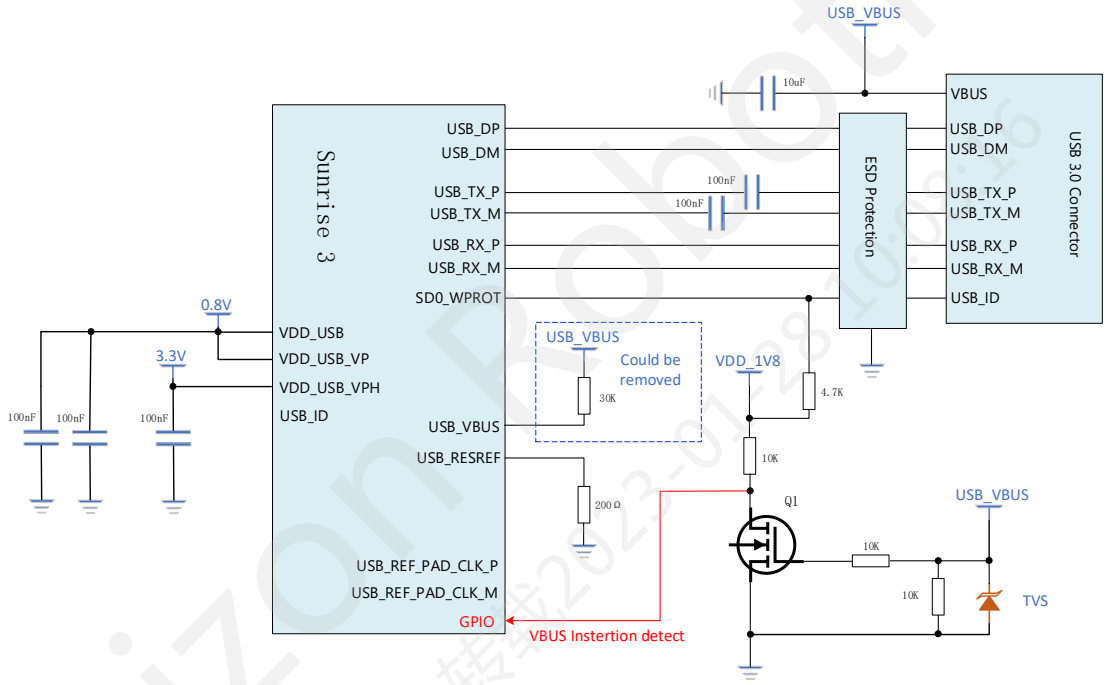

Figure 2-5 VBUS Insertion Detection Solution

Solution B: Use USB_VBUS as enable signal to the X3's PMIC output. X3 will not power up without USB_VBUS inserted. This is common in Smart USB Camera scenario. Please refer to the Figure 2-6 for this solution.

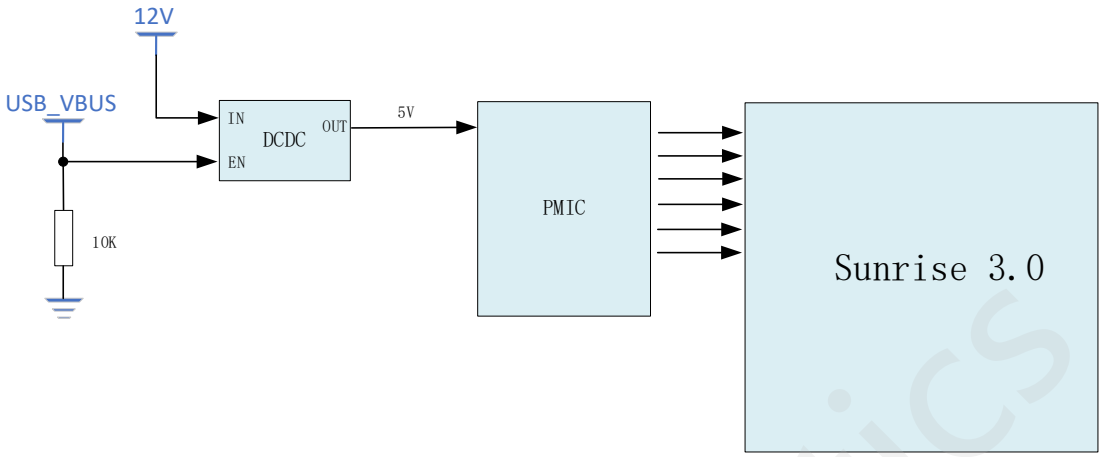

Figure 2-6 USB VBUS Controlled Power up for X3

2.5 EFUSE_VDD Connection

Issue description:

EFUSE_VDD is default powered up by 1.8V LDO output. EFUSE_VDD needs only to be powered up while burning X3 EFUSE, and it should be connected to ground or left floating in all other situation except burning EFUSE. Otherwise, there is very small chance that the EFUSE content is mistakenly changed.

Workaround:

Connect EFUSE_VDD to the test pad instead of 1.8V.

EFUSE_VDD will be floating in customer normal scenario. When customer needs to change the content of EFUSE in production line, use production jig to short the EFUSE_VDD to 1.8V.

The short behavior needs to be controlled by SW to make sure that the EFUSE_VDD on/off sequence describe in Figure 2-8 is fulfilled.

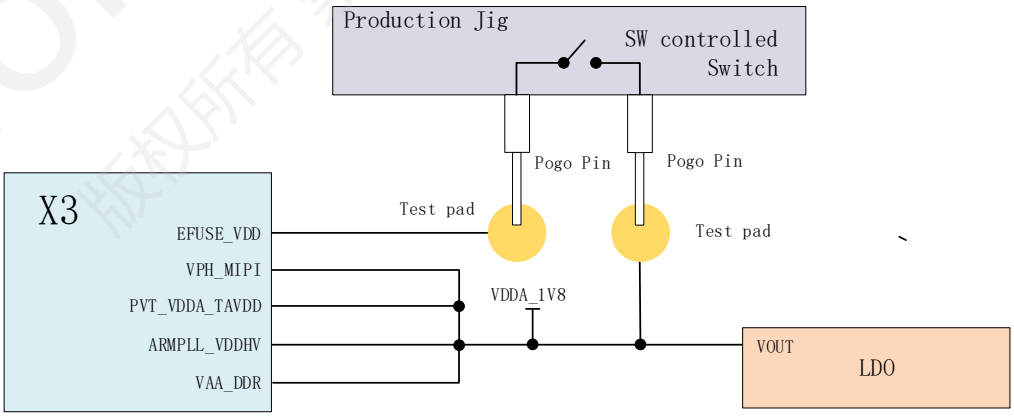

Figure 2-7 EFUSE VDD Connection

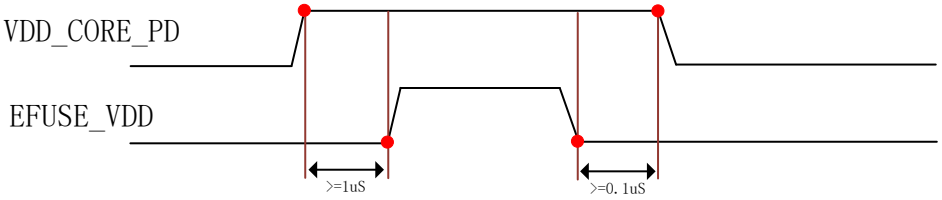

Figure 2-8 EFUSE_VDD on/off Sequence