X3M Register Reference Manual GPIO/PIN Group

Revision History

Revision	Date	Description
1.0	July-03-2020	Initial Release
1.1		 Corrected the register name from QSPI_MOSI_IO1 to QSPI_MISO_IO1. Corrected the bit field name from QSPI_MOSI_IO1_XX to QSPI_MISO_IO1_XX. Corrected the register name from QSPI_MOSI_IO2 to QSPI_WP_IO2. Corrected the bit field name from QSPI_MOSI_IO2_XX to QSPI_WP_IO2_XX. Corrected the register name from QSPI_MOSI_IO3 to QSPI_HOLD_IO3.
	NOT.	Corrected the bit field name from QSPI_MOSI_IO3_XX to QSPI_HOLD_IO3_XX.



BASE_ADE	DR:0xA600_3000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
008H	GPIO0_OUTPUT_CTR	RW	[31:16]	GPIO0_DIR	16'h0	GPIO0 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO0_OUTPUT_VALU E	16'h0	GPIO0 output register. 0: Output 0. 1: Output 1.
00CH	GPIO0_INPUT_VALU	RO	[31:16]	Reserved		9
	E		[15:0]	GPIO0_INPUT_VALUE	16'h0	GPIO0 pin value. 0: Input 0. 1: Input 1.
018H	GPIO1_OUTPUT_CTR	RW	[31:16]	GPIO1_DIR	16'h0	GPIO1 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO1_OUTPUT_VALU E		GPIO1 output register. 0: Output 0. 1: Output 1.
01CH	GPIO1_INPUT_VALU	RO	[31:16]	Reserved	×X	
	E		[15:0]	GPIO1_INPUT_VALUE	16'h0	GPIO1 pin value. 0: Input 0. 1: Input 1.
028H	GPIO2_OUTPUT_CTR	RW	[31:16]	GPIO2_DIR	16'h0	GPIO2 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO2_OUTPUT_VALU E	16'h0	GPIO2 output register. 0: Output 0. 1: Output 1.
02CH	GPIO2_INPUT_VALU	RO	[31:16]	Reserved		



BASE_ADI	DR:0xA600_3000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	E		[15:0]	GPIO2_INPUT_VALUE	16'h0	GPIO2 pin value. 0: Input 0. 1: Input 1.
038H	GPIO3_OUTPUT_CTR	RW	[31:16]	GPIO3_DIR	16'h0	GPIO3 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO3_OUTPUT_VALU E	16'h0	GPIO3 output register. 0: Output 0. 1: Output 1.
03CH	GPIO3_INPUT_VALU	RO	[31:16]	Reserved		1.0
	E		[15:0]	GPIO3_INPUT_VALUE	16'h0	GPIO3 pin value. 0: Input 0. 1: Input 1.
048H	GPIO4_OUTPUT_CTR	RW	[31:16]	GPIO4_DIR	16'h0	GPIO4 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO4_OUTPUT_VALU E	16'h0	GPIO4 output register. 0: Output 0. 1: Output 1.
04CH	GPIO4_INPUT_VALU	RO	[31:16]	Reserved	1. The second se	
	E	. ([15:0]	GPIO4_INPUT_VALUE	16'h0	GPIO4 pin value. 0: Input 0. 1: Input 1.
058H	GPIO5_OUTPUT_CTR	RW	[31:16]	GPIO5_DIR	16'h0	GPIO5 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO5_OUTPUT_VALU E	16'h0	GPIO5 output register. 0: Output 0. 1: Output 1.
05CH	GPIO5_INPUT_VALU	RO	[31:16]	Reserved		



BASE_ADI	DR:0xA600_3000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	E		[15:0]	GPIO5_INPUT_VALUE	16'h0	GPIO5 pin value. 0: Input 0. 1: Input 1.
068H	GPIO6_OUTPUT_CTR L	RW	[31:16]	GPIO6_DIR	16'h0	GPIO6 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO6_OUTPUT_VALU E		GPIO6 output register. 0: Output 0. 1: Output 1.
06CH	GPIO6_INPUT_VALU	RO	[31:16]	Reserved		
	E		[15:0]	GPIO6_INPUT_VALUE	16'h0	GPIO6 pin value. 0: Input 0. 1: Input 1.
078H	GPIO7_OUTPUT_CTR	RW	[31:25]	Reserved	2	
	L		[24:16]	GPIO7_DIR	9'h0	GPIO7 pin direction. 0: Input. 1: Output.
			[8:0]	GPIO7_OUTPUT_VALU E		GPIO7 output register. 0: Output 0. 1: Output 1.
07CH	GPIO7_INPUT_VALU	RO	[31:9]	Reserved		
	E		[8:0]	GPIO7_INPUT_VALUE	9'h0	GPIO7 pin value. 0: Input 0. 1: Input 1.
100H	GPIO_INT_MUX_SEL	RW	[31]	Reserved		



CDIO	BASE_ADDR:0xA600_3000												
GPIO	Offset	Register Name	Access	Bits	Field Name	Default Value	Description						
				[30:24]	GPIO_INT3_MUX_SEL	7'h0	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 3. 7'd00: GPIO0. 7'd01: GPIO1 7'd120: GPIO120. 7'd121~7'd127: 1'b0.						
				[23]	Reserved								
				[22:16]	GPIO_INT2_MUX_SEL		GPIO interrupt 2 mux selection. The specific GPIO that will generate interrupt 2. 7'd00: GPIO0. 7'd01: GPIO1 7'd120: GPIO120. 7'd121~7'd127: 1'b0.						
				[15]	Reserved								
					GPIO_INT1_MUX_SEL	()_ '	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 1. 7'd00: GPIO0. 7'd01: GPIO1 7'd120: GPIO120. 7'd121~7'd127: 1'b0.						
				[7]	Reserved								
					GPIO_INT0_MUX_SEL	7'h0	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 0. 7'd00: GPIO0. 7'd01: GPIO1 7'd120: GPIO120. 7'd121~7'd127: 1'b0.						
	104H	GPIO_INTE	RW	[31:4]	Reserved								



BASE_AD	DR:0xA600_3000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[3:0]	GPIO_INTE	4'h0	GPIO interrupt enable. The specific bit that enables interrupt generation for corresponding input GPIO. Interrupt can be enabled only when GPIO_DIR is configured to input.
108H	GPIO_INT_POS	RW	[31:4]	Reserved		
			[3:0]	GPIO_INT_POS	4'hf	GPIO positive edge interrupt flag. The specific bit indicates the corresponding bit has positive/negtive edge interrupt. 0: Disabled. 1: Enabled.
10CH	GPIO_INT_NEG	RW	[31:4]	Reserved		
			[3:0]	GPIO_INT_NEG	4'hf	GPIO negtive edge interrupt flag. The specific bit indicates the corresponding bit has positive/negtive edge interrupt. 0: Disabled. 1: Enabled.
110H	GPIO_INT_WIDTH	RW	[31:0]	GPIO_INT_WIDTH	32'h1	Valid input holding width for GPIO interrupt generation, the holding time is calculated as 2 * (GPIO_INT_WIDTH + 1) * padc_mclk Period.
120H	GPIO_INTMASK	RO	[31:4]	Reserved		
			[3:0]	GPIO_INTMASK	4'h0	0: Unmasked. 1: Masked.
124H	GPIO_SETMASK	WO	[31:4]	Reserved		
			[3:0]	GPIO_SETMASK	4'h0	Writing setmask[i] = 1 means mask bit i. 0: Unmasked. 1: Masked.
128H	GPIO_UNMASK	WO	[31:4]	Reserved		
			[3:0]	GPIO_UNMASK	4'h0	Writing unmask[i] = 1 means unmask bit i. 0: Unmasked. 1: Unmasked.
12CH	GPIO_SRCPND	W1C	[31:4]	Reserved		



CDIO	BASE_ADDI	R:0xA600_3000					
GPIO	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3:0]	GPIO_SRCPND	4'h0	For read: 0: Interrupt source inactive. 1: Interrupt source active.
							For write: 0: No effect. 1: Clears corresponding source.
	130H	IRQOUT_CTRL	RW	[31:21]	Reserved		
				[20]	IRQOUT_TRIG	1'b0	X2A_IRQOUT_N edge type interrupt trigger. SW should configure IRQOUT_POL before IRQOUT_TRIG. 1'b0: No effect. 1'b1: Triggers interrupt.
				[19:17]	Reserved		10.
				[16]	IRQOUT_POL	1'b0	X2A_IRQOUT_N edge type interrupt polority: 1'b0: Low active. 1'b1: High active.
				[15:0]	IRQOUT_PERIOD	16'h20	X2A_IRQOUT_N edge type interrupt pulse width. The width is IRQ_PERIOD 24MHz cycles.
	140H	STRAP_PIN	RO	[31:17]	Reserved		
				[16]	SW_STRAP[16]	1'b0	Reserved.
				[15]	SW_STRAP[15]	1'b0	Reserved.
				[14]	SW_STRAP[14]	1'b0	Reserved.
				[13]	SW_STRAP[13]	1'b0	0: SPI NAND has 1 plane, you do not need to set plane selection for 03H command.1: SPI NAND has 2 planes, you need to set plane selection for 03H command.
				[12]	SW_STRAP[12]	1'b0	Whether dummy byte is inserted when SPI NAND reading ID: 0: Inserts dummy byte when SPI NAND flash reading device ID (9FH command). 1: No dummy byte inserted when SPI NAND flash reading device ID (9FH command).



CDIC	BASE_ADI	DR:0xA600_3000					
GPIO	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	SW_STRAP[11]	1'b0	Watchdog disable: 0: Enables WatchDog to protect clock switch. Triggers system reset if system hangs in the process of clock switch. 1: Disables WatchDog. Enable watchdog before clock switch to PLL, and disable watchdog after the success of clock switch.
				[10]	SW_STRAP[10]	1'b0	SPI flash reset is only valid if 2NDBOOT=SPI FLASH. 0: No operation. 1: Triggers a flash reset command before reading NAND/NOR FLASH.
				[9]	SW_STRAP[9]	1'b0	When Warm boot: 0: Load SPL from SRAM. 1: Load SPL from flash/emmc/uart/bifspi/usb.
				[8]	SW_STRAP[8]	1'b0	Reserved.
				[7]	SW_STRAP[7]	1'b0	UART baud rate: 0: 921600 bps. 1: 115200 bps.
				[6:5]	SW_STRAP[6:5]	2'b0	Fast boot selection, CPU/BUS frequency selection: 00: cpu_clk=1.2G, ace_aclk=sys_noc_aclk=600M, sys_ap_aclk=400M, sys_pclk=cx_dbgclk=300M. 01: cpu_clk=600M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M, sys_pclk=cx_dbgclk=150M. 10: cpu_clk=300M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M, sys_pclk=cx_dbgclk=150M. 11: No clock switch to high freq, cpu_clk=24M, ace_aclk=sys_noc_aclk=12M, sys_pclk=4.8M, sys_ap_aclk=cx_dbgclk=8M.



10	BASE_ADD	R:0xA600_3000					
10	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	SW_STRAP[4]	1'b0	Device mode. When 2NDBOOT=EMMC: 0: DRV CLK phase shift 180°, falling edge launch and rising edge capture. 1: DRV CLK no phase shift, rising edge launch and rising edge capture. When 2NDBOOT_SEL=SPI NAND FLASH: 0: 2KB Page Size. 1: 4KB Page Size. When 2NDBOOT_SEL=SPI NOR FLASH: 0: 32-bit addr mode. 1: 24-bit addr mode.
				[3:1]	SW_STRAP[3:1]	3'b0	000: 2NDBOOT from EMMC 001: 2NDBOOT from SPI FLASH(SPI NAND FLASH) 010: 2NDBOOT from AP BIFSPI 011: 2NDBOOT from UART XMODEM 100: 2NDBOOT from USB, Normal boot 101: 2NDBOOT from SPI FLASH(SPI NOR FLASH) 110: 2NDBOOT from USB with program 111: RESERVED (2NDBOOT from UART) Note: 100 or 110 (USB boot or USB program) will detect USB ID pin (GPIO[65], SD0_WPROT) 0: The chip is playing as a USB host, perform USB host operation 1: The chip is playing as a USB device, perform UART boot
				[0]	SW_STRAP[0]	1'b0	Reserved.
	170H	SD_MODE_CTRL	RW	[31:4]	Reserved		
				[3]	SD2_MODE_SEL	1'b0	SD2 mode selector 0: 3.0V mode 1: 1.8V mode
				[2]	SD1_MODE_SEL	1'b0	SD1 mode selector 0: 3.0V mode 1: 1.8V mode



10	BASE_ADDR	0xA600_3000					
IU	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	SD0_MODE_SEL_DOM AIN1		SD0 mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[0]	SD0_MODE_SEL_DOM AIN0		SD0 mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
	174H	IO_MODE_CTRL	RW	[31:12]	Reserved		
				[11]	RGMII_MODE_SEL_DO MAIN1		RGMII I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[10]	RGMII_MODE_SEL_DO MAIN0		RGMII I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
				[9]	I2C2_MODE_SEL	1'b0	I2C2/I2C3 I/O mode selector 0: 3.0V mode 1: 1.8V mode
				[8]	I2C0_MODE_SEL	1'b0	I2C0/Sensor2_MCLK/Sensor3_MCLK I/O mode selector 0: 3.0V mode 1: 1.8V mode
				[7]	Reserved	1	
				[6]	BT1120_MODE_SEL_D OMAIN2		BT1120 I/O mode selector in SD domain 2 0: 3.0V mode 1: 1.8V mode
				[5]	BT1120_MODE_SEL_D OMAIN1		BT1120 I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[4]	BT1120_MODE_SEL_D OMAIN0		BT1120 I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode



BASE_ADI	DR:0xA600_3000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[3]	BIFSD_MODE_SEL_DO MAIN1		BIFSD I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
			[2]	BIFSD_MODE_SEL_DO MAIN0		BIFSD I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
			[1]	BIFSPI_MODE_SEL	1'b0	BIFSPI I/O mode selector 0: 3.0V mode 1: 1.8V mode
			[0]	JTG_MODE_SEL	1'b0	JTAG I/O mode selector 0: 3.0V mode 1: 1.8V mode
180H	GPIO_TS_SEL	RW	[31:7]	Reserved		
			[6:0]	GPIO_TS_SEL	7'h0	GPIO mux selection for timestamp trigger source The specific which GPIO will be sent to vio subsys 7'd00: GPIO0 7'd01: GPIO1 7'd120: GPIO120 7'd121~7'd127: 1'b0
200H	DUMMY0	RW	[31:0]	DUMMY0	32'h0	Dummy register 0.
204H	DUMMY1	RW	[31:0]	DUMMY1		Dummy register 1.



IN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO	
	0000H	EN_VDD_CORE	RW				PIN configuration register		
				[31:9]	Reserved				
				[8]	EN_VDD_CORE_ST	1'h0	PIN Schmitt trigger enable		
							0: Disabled		
							1: Enabled		
				[7]	EN_VDD_CORE_PS	1'h0	PIN pull selector		
							0: Pull down		
							1: Pull up		
				[6]	EN_VDD_CORE_PE	1'h0	Pin pull enable		
							0: Pull function is disabled	GPIO0	
							1: Pull function is enabled		
				[5:2]	EN_VDD_CORE_DS	4'h0	PIN Driving selector (typical value)		
							0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA		
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	EN_VDD_CORE_FS	2'h0	PIN function selection		
							00: Normal function		
							01: N/A		
							10: N/A		
	000411	EN_VDD_CNN0	RW				11: GPIO		
	0004H	EN_VDD_CNN0	KVV	[24.0]	Reserved		PIN configuration register		
				[31:9]		1'h0	DINI Schmitt trigger enable		
				[O]	EN_VDD_CNN0_ST	1110	PIN Schmitt trigger enable 0: Disabled		
							1: Enabled		
				[7]	EN_VDD_CNN0_PS	1'h0	PIN pull selector		
				[,]	LIV_VDD_CIVIVO_IS	×	0: Pull down		
						**	1: Pull up		
				[6]	EN_VDD_CNN0_PE	1'h0	Pin pull enable		
YSTEM				[0]			0: Pull function is disabled	GPIO0	
						X	1: Pull function is enabled		
				[5:2]	EN_VDD_CNN0_DS	4'h0	PIN Driving selector (typical value)		
					\		0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA		
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	EN_VDD_CNN0_FS	2'h0	PIN function selection		
							00: Normal function		
							01: N/A		
							10: N/A		
				11: GPIO					
	H8000	EN_VDD_CNN1	RW				PIN configuration register		



I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[31:9]	Reserved			
				[8]	EN_VDD_CNN1_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[7]	EN_VDD_CNN1_PS	1'h0	PIN pull selector	
				1 1			0: Pull down	
							1: Pull up	
				[6]	EN_VDD_CNN1_PE	1'h0	Pin pull enable	
							0: Pull function is disabled	GPIO
							1: Pull function is enabled	
				[5:2]	EN_VDD_CNN1_DS	4'h0	PIN Driving selector (typical value)	-
				[3.2]		1110	0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EN_VDD_CNN1_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	000CH	JTG_TCK	RW				PIN configuration register	
				[31:10]	Reserved	411.4		
				[9]	JTG_TCK_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled 1: Enabled	
							.Ş. /	
				[8]	JTG_TCK_PU	1'h0	PIN pull up enable	
							0: Disabled 1: Enabled	
				F-71	ITC TCV DD	all a		
				[7]	JTG_TCK_PD	1'h1	Pin pull down enable 0: Disabled	
							1: Enabled	GPIO
				[6]	Reserved		1. Endoted	
				[5:2]	JTG_TCK_DS	4'h1	PIN Driving selector (typical value)	
				[5.2]	JIG_ICK_DS	4 111	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TCK_FS	2'h0	PIN function selection	
							00: Normal function	
							01: SPI1_SCLK	
							10: N/A	
							11: GPIO	
	0010H	JTG_TRSTN	RW				PIN configuration register	



I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GP
				[31:10]	Reserved			
				[9]	JTG_TRSTN_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	JTG_TRSTN_PU	1'h0	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	JTG_TRSTN_PD	1'h1	Pin pull down enable	
							0: Disabled	CDIC
							1: Enabled	GPIC
				[6]	Reserved			
				[5:2]	JTG_TRSTN_DS	4'h1	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TRSTN_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: PWM0	
	004.411	LTC THE	D) 4 /				11: GPIO	
	0014H	JTG_TMS	RW				PIN configuration register	
		[31:10] Reserved [9] JTG_TMS_ST 1'h0 PIN Schmitt trigger enable						
				[9]	JTG_TMS_ST	1'n0	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				[0]	ITC TMC DIL	1151	XZ.VX ¹	
				[8]	JTG_TMS_PU	1'h1	PIN pull up enable 0: Disabled	
						X	1: Enabled	
				[7]	JTG_TMS_PD	1'h0	Pin pull down enable	
				[,,]	710_11VI3_11D	1110	0: Disabled	
TAG				·		2012.	1: Enabled	GPIC
				[6]	Reserved	Kil		
				[5:2]	JTG_TMS_DS	4'h1	PIN Driving selector (typical value)	
				[5,2]			0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TMS_FS	2'h0	PIN function selection	
							00: Normal function	
							01: SPI1_CSN	
							10: N/A	
							11: GPIO	



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
	0018H	JTG_TDI	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	JTG_TDI_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TDI_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TDI_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPI00[6
				[6]	Reserved			
				[5:2]	JTG_TDI_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TDI_FS	2'h0	PIN function selection 00: Normal function 01: SPI1_MOSI 10: N/A 11: GPIO	
	001CH	JTG_TDO	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	JTG_TDO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TDO_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TDO_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO0[7]
				[6]	Reserved			
				[5:2]	JTG_TDO_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	



Group	Offset	Register Name	Access	Rits	Field Name	Default Value	Description	GP	
	Oliset	Register Name	Access			2'h0	PIN function selection	GF	
				[1:0]	JTG_TDO_FS	2 nu	00: Normal function		
							01: SPI1_MISO		
							10: N/A		
							11: GPIO		
	0020H	I2C0_SCL	RW				PIN configuration register		
				[31:10] Reserved					
				[9]	I2C0_SCL_ST	1'h0	PIN Schmitt trigger enable		
							0: Disabled		
							1: Enabled		
				[8]	I2C0_SCL_PU	1'h1	PIN pull up enable		
							0: Disabled		
							1: Enabled		
				[7]	1200 001 00	111.0			
				[7]	I2C0_SCL_PD	1'h0	Pin pull down enable		
							0: Disabled	GPIC	
							1: Enabled		
				[6]	Reserved				
				[5:2]	I2C0_SCL_DS	4'h1	PIN Driving selector (typical value)		
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA		
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	I2C0_SCL_FS	2'h3	PIN function selection		
							00: Normal function		
							01: N/A		
							10: N/A		
							11: GPIO		
12 C 0	0024H	I2C0_SDA	RW			<u> </u>	PIN configuration register		
		1.200_0271		[31:10]	Reserved	1/1			
				[9]	I2C0_SDA_ST	1'h0	PIN Schmitt trigger enable		
					1200_307_31	1110	0: Disabled		
						/X+	1: Enabled		
				[8]	I2C0_SDA_PU	1'h1	PIN pull up enable		
							0: Disabled		
							1: Enabled		
				[7]	I2C0_SDA_PD	1'h0	Pin pull down enable		
							0: Disabled	CDIC	
							1: Enabled	GPIO	
				[6]	Reserved				

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I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIC	
				[5:2]	I2C0_SDA_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	I2C0_SDA_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO		
	0028H	I2C1_SCL	RW				PIN configuration register		
				[31:9]	Reserved				
				[8]	I2C1_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled		
				[7]	I2C1_SCL_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up		
				[6]	I2C1_SCL_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO0	
				[5:2]	I2C1_SCL_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
12C1				[1:0]	I2C1_SCL_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO		
1201	002CH	I2C1_SDA	RW			180	PIN configuration register		
				[31:9]	Reserved				
				[8]	I2C1_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled		
			[7	[7	[7]	I2C1_SDA_PU	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2C1_SDA_PD	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO0	



IN Group		BASE_ADDR: 0xA						
Отобр	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[5:2]	I2C1_SDA_DS	4'h0	PIN Driving selector (typical value)	
							0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C1_SDA_FS	2'h3	PIN function selection	
				, ,			00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	0030H	I2C2_SCL	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	I2C2_SCL_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[0]	1262 661 811	411.4		
				[8]	I2C2_SCL_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	I2C2_SCL_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIC
							1: Enabled	0.10
				[6]	Reserved			
				[5:2]	I2C2_SCL_DS	4'h1	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C2_SCL_FS	2'h3	PIN function selection	
				[]			00: Normal function	
							01: SPI2_MOSI	
							10: PWM7	
						***	11: GPIO	
12C2	0034H	I2C2_SDA	RW			1/2	PIN configuration register	
				[31:10]	Reserved			
				[9]	I2C2_SDA_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
					\ \frac{1}{2}		1: Enabled	
				[8]	I2C2_SDA_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	I2C2_SDA_PD	1'h0	Pin pull down enable	
							0: Disabled	
							1: Enabled	GPIC
				[6]	Reserved			
				[6]	Neserveu			



IN Group		BASE_ADDR: 0xA						
пч Огоир	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[5:2]	I2C2_SDA_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C2_SDA_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_MISO 10: PWM8 11: GPIO	
	0038H	I2C3_SCL	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	I2C3_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C3_SCL_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C3_SCL_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO0
				[6]	Reserved			
				[5:2]	I2C3_SCL_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C3_SCL_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_SCLK 10: N/A 11: GPIO	
I2C3	003CH	I2C3_SDA	RW				PIN configuration register	
				[31:10]	Reserved	, O'S'		
				[9]	I2C3_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	[8]	I2C3_SDA_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled
				[7]	I2C3_SDA_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO0



N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI		
				[6]	Reserved					
				[5:2]	I2C3_SDA_DS	4'h1	PIN Driving selector (typical value)			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	I2C3_SDA_FS	2'h3	PIN function selection			
							00: Normal function			
							01: SPI2_CSN			
							10: N/A			
							11: GPIO			
	0040H	SPI0_CSN	RW				PIN configuration register			
				[31:9]	Reserved					
				[8]	SPI0_CSN_ST	1'h0	PIN Schmitt trigger enable			
							0: Disabled			
							1: Enabled			
				[7]	SPI0_CSN_PS	1'h1	PIN pull selector			
							0: Pull down			
							1: Pull up			
				[6]	SPIO_CSN_PE	1'h1	Pin pull enable			
							0: Pull function is disabled	GPIO		
							1: Pull function is enabled			
						[5:2]	SPI0_CSN_DS	4'h0	PIN Driving selector (typical value)	
						0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA				
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	SPI0_CSN_FS	2'h3	PIN function selection			
							00: Normal function			
							01: I2C4_SDA			
						术》	10: N/A			
						X	11: GPIO			
	0044H	SPI0_SCLK	RW				PIN configuration register			
				[31:9]	Reserved	201,				
				[8]	SPI0_SCLK_ST	1'h0	PIN Schmitt trigger enable			
					X		0: Disabled			
							1: Enabled			
				[7]	SPI0_SCLK_PS	1'h1	PIN pull selector			
							0: Pull down			
							1: Pull up			
				[6]	SPI0_SCLK_PE	1'h1	Pin pull enable			
							0: Pull function is disabled	GPIO		
							1: Pull function is enabled			



N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[5:2]	SPI0_SCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
				[1:0]	SPI0_SCLK_FS	2'h3	1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA PIN function selection 00: Normal function	
							01: I2C4_SCL 10: N/A 11: GPIO	
SPI0	0048H	SPI0_MOSI	RW				PIN configuration register	
	0040П	SPIO_IVIOSI	NVV	[21:0]	Reserved		Fin Configuration register	
				[31:9]	SPI0_MOSI_ST	1'h0	PIN Schmitt trigger enable	
				[о]	3F10_IVIO3I_31	1110	0: Disabled 1: Enabled	
				[7]	SPI0_MOSI_PS	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[6]	SPI0_MOSI_PE	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO
				[5:2]	SPI0_MOSI_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_MOSI_FS	2'h3	PIN function selection 00: Normal function 01: I2C5_SDA 10: PWM5 11: GPIO	
	004CH	SPI0_MISO	RW			1/2	PIN configuration register	
	004011	31 10_111130	IXVV	[31:9]	Reserved		The Configuration register	
				[8]	SPI0_MISO_ST	1'h0	PIN Schmitt trigger enable	
				[O]	31 10_WI3O_31	110	0: Disabled 1: Enabled	
				[7]	SPI0_MISO_PS	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[6]	SPI0_MISO_PE	1'h1	Pin pull down enable 0: Disabled	GPIO



Group of	ffset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[5:2]	SPI0_MISO_DS	4'h1	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_MISO_FS	2'h3	PIN function selection	
				[1.0]	3PIU_IVII3U_F3	2 113	00: Normal function	
							01: I2C5_SCL	
							10: PWM6	
							11: GPIO	
00	050H	BIFSD_CLK	RW				PIN configuration register	
	05011	DII 3D_CER	100	[31:10]	Reserved		The configuration register	
				[9]	BIFSD_CLK_ST	1'h1	PIN Schmitt trigger enable	
					DII 3D_CEK_31		0: Disabled	
							1: Enabled	
				[0]	DIECD CLK DIL	411.0		
				[8]	BIFSD_CLK_PU	1'h0	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	BIFSD_CLK_PD	1'h1	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	0.10
				[6]	Reserved			
				[5:2]	BIFSD_CLK_DS	4'h1	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_CLK_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
						X)	10: RGB_VSYNC	
						XX	11: GPIO	
00	054H	BIFSD_CMD	RW				PIN configuration register	
				[31:10]	Reserved	307		
				[9]	BIFSD_CMD_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_CMD_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	BIFSD_CMD_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	Grio



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GP
				[6]	Reserved			
				[5:2]	BIFSD_CMD_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_CMD_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: RGB_HSYNC	
							11: GPIO	
	0058H	BIFSD_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA0_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_DATA0_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	BIFSD_DATA0_PD	1'h0	Pin pull down enable	
							0: Disabled	CDIO
							1: Enabled	GPIO
				[6]	Reserved			
				[5:2]	BIFSD_DATA0_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA0_FS	2'h0	PIN function selection	
						木工	00: Normal function	
						1	01: PWM1	
							10: RGB_DAT16	
				1		M.	11: GPIO	
	005CH	BIFSD_DATA1	RW			07/	PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA1_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_DATA1_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	



N Group	Offset	Register Name	Acces	ss Bits	Field Name	Default Value	Description	GPIC
				[7]	BIFSD_DATA1_PD	1'h0	Pin pull down enable	
							0: Disabled	
BIFSD							1: Enabled	GPIO1[
				[6]	Reserved			
				[5:2]	BIFSD_DATA1_DS	4'h6	PIN Driving selector (typical value)	
				[3.2]	DII 3D_DATAT_D3	4110	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA1_FS	2'h0	PIN function selection	
							00: Normal function	
							01: PWM2	
							10: RGB_DAT17	
							11: GPIO	
	0060H	BIFSD_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA2_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_DATA2_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	BIFSD_DATA2_PD	1'h0	Pin pull down enable	
							0: Disabled	GDIO1
							1: Enabled	GPIO1[
				[6]	Reserved			
				[5:2]	BIFSD_DATA2_DS	4'h6	PIN Driving selector (typical value)	
						X/2	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA2_FS	2'h0	PIN function selection	
						**	00: Normal function	
						85,	01: PWM3	
							10: RGB_DAT18	
							11: GPIO	
	0064H	BIFSD_DATA3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA3_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	

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N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description Description	GPIO
				[8]	BIFSD_DATA3_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1
				[6]	Reserved			
				[5:2]	BIFSD_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA3_FS	2'h0	PIN function selection 00: Normal function 01: PWM4 10: RGB_DAT19 11: GPIO	
	0068H	BIFSD_RSTN	RW				PIN configuration register	
				[31:10]	Reserved		PIN configuration register 1'h1 PIN Schmitt trigger enable 0: Disabled	
				[9]	BIFSD_RSTN_ST	1'h1		
				[8]	BIFSD_RSTN_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_RSTN_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1
				[6]	Reserved	100		
			[5:2]	BIFSD_RSTN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	BIFSD_RSTN_FS	2'h0	PIN function selection 00: Normal function 01: PPS_TRIG_IN 10: RGB_DE 11: GPIO	
	006CH	BIFSPI_CSN	RW				PIN configuration register	
				[31:10]	Reserved			



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIC
				[9]	BIFSPI_CSN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_CSN_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_CSN_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1
				[6]	Reserved			
				[5:2]	BIFSPI_CSN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_CSN_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0070H	BIFSPI_SCLK	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSPI_SCLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_SCLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_SCLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO1
				[6]	Reserved	73EP,		
				[5:2]	BIFSPI_SCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_SCLK_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0074H	BIFSPI_MOSI	RW				PIN configuration register	



DIN Group	PIN_REG	BASE_ADDR: 0xA60	00_4000							
PIN Group	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIC		
				[31:10]	Reserved					
				[9]	BIFSPI_MOSI_ST	1'h0	PIN Schmitt trigger enable			
							0: Disabled			
							1: Enabled			
				[8]	BIFSPI_MOSI_PU	1'h1	PIN pull up enable			
							0: Disabled			
							1: Enabled			
				[7]	BIFSPI_MOSI_PD	1'h0	Pin pull down enable			
DIECDI							0: Disabled	20104		
BIFSPI							1: Enabled	GPIO1		
				[6]	Reserved					
				[5:2]	BIFSPI_MOSI_DS	4'h1	PIN Driving selector (typical value)			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	BIFSPI_MOSI_FS	2'h0	PIN function selection			
							00: Normal function			
							01: N/A			
							10: N/A			
							11: GPIO			
	0078H	BIFSPI_MISO	RW				PIN configuration register			
				[31:10]	Reserved					
				[9]	BIFSPI_MISO_ST	1'h0				
							0: Disabled			
							1: Enabled			
				[8]	BIFSPI_MISO_PU	1'h1	PIN pull up enable			
						*	0: Disabled			
						\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	1: Enabled			
				[7]	BIFSPI_MISO_PD	1'h0	Pin pull down enable			
							0: Disabled	GPIO ⁻		
						13 E) .	1: Enabled	0.10		
				[6]	Reserved	19-1				
				[5:2]	BIFSPI_MISO_DS	4'h1	PIN Driving selector (typical value)			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	BIFSPI_MISO_FS	2'h0	PIN function selection			
							00: Normal function			
							01: N/A			
							10: N/A			
							11: GPIO			



Group	Offset	Register Name	Access	s Bits	Field Name	Default Value	Description	GPI
	007CH	BIFSPI_RSTN	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSPI_RSTN_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSPI_RSTN_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7] BIF	BIFSPI_RSTN_PD	1'h0	Pin pull down enable	
							0: Disabled	CDIO
							1: Enabled	GPIO
				[6]	Reserved			
				[5:2]	BIFSPI_RSTN_DS	4'h1	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_RSTN_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	H0800	QSPI_CSN	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	QSPI_CSN_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled 1: Enabled	
							y 'X	
				[7]	QSPI_CSN_PS	1'h1	PIN pull selector	
						1/4	0: Pull down	
							1: Pull up	
				[6]	QSPI_CSN_PE	1'h1	Pin pull enable	CDIO
						/X * * * * * * * * * * * * * * * * * * *	0: Pull function is disabled 1: Pull function is enabled	GPIO
								_
				[5:2]	QSPI_CSN_DS	4'h0	PIN Driving selector (typical value)	
							0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_CSN_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A 10: N/A	
							11(): N1/A	



roup	_	BASE_ADDR: 0xA						
	Offset	Register Name	Access	Bits	Field Name	Default Value	·	GF
	0084H	QSPI_SCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	QSPI_SCLK_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[7]	QSPI_SCLK_PS	1'h1	PIN pull selector	
							0: Pull down	
							1: Pull up	
				[6]	QSPI_SCLK_PE	1'h1	Pin pull enable	
							0: Pull function is disabled	GPIC
							1: Pull function is enabled	
				[5:2]	QSPI_SCLK_DS	4'h2	PIN Driving selector (typical value)	
							0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_SCLK_FS	2'h0	PIN function selection	
				[]	4 0. 2 0.02.2.0		00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	0088H	QSPI_MOSI_IO0	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	QSPI_MOSI_IO0_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[7]	QSPI_MOSI_IO0_PS	1'h1	PIN pull selector	
						*	0: Pull down	
						· 大力	1: Pull up	
				[6]	QSPI_MOSI_IO0_PE	1'h1	Pin pull enable	
							0: Pull function is disabled	GPI
						×37,	1: Pull function is enabled	
				[5:2]	QSPI_MOSI_IO0_DS	4'h1	PIN Driving selector (typical value)	
						100	0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_MOSI_IO0_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
PI								



roup		BASE_ADDR: 0xA60						
	Offset	Register Name	Access		Field Name	Default Value	Description	
				[31:9]	Reserved QSPI_MISO_IO1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_MISO_IO1_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_MISO_IO1_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GI
				[5:2]	QSPI_MISO_IO1_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_MISO_IO1_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0090H	QSPI_WP_IO2	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	QSPI_WP_IO2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_WP_IO2_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
			[€	[6]	QSPI_WP_IO2_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GI
				[5:2]	2] QSPI_WP_IO2_DS 4'h1	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_WP_IO2_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0094H	QSPI HOLD 103	RW				PIN configuration register	
	005-11	QSPI_HOLD_IO3 RW						



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIC
				[8]	QSPI_HOLD_IO3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_HOLD_IO3_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_HOLD_IO3_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO2
				[5:2]	QSPI_HOLD_IO3_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_HOLD_IO3_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0098H	EPHY_CLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	EPHY_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	EPHY_CLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	EPHY_CLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO2
				[5:2]	EPHY_CLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EPHY_CLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	009CH	MDCK	RW				PIN configuration register	
				I				



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[8]	MDCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	MDCK_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	MDCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	MDCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	MDCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00A0H	MDIO	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	MDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	MDIO_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	MDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO2
		[ř	[5:2]	MDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
		[1:0]	[1:0]	MDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO		
	00A4H	RGMII_RX_CLK	RW				PIN configuration register	
		GIVIII_KA_CLK RI		[31:10]	Reserved			



roup	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIO
				[9]	RGMII_RX_CLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RX_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RX_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO2[
				[6]	Reserved			
				[5:2]	RGMII_RX_CLK_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RX_CLK_FS	2'h3	PIN function selection 00: Normal function (RGMII_RX_CLK or RMII_REF_CLK_IN) 01: N/A 10: N/A 11: GPIO	
	00A8H	RGMII_RXD0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	RGMII_RXD0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RXD0_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RXD0_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO2
				[6]	Reserved	357		
				[5:2]	RGMII_RXD0_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD0_FS	2'h3	PIN function selection 00: Normal function (RGMII_RXD0 or RMII_RXD0) 01: N/A 10: N/A 11: GPIO	
	00ACH	RGMII_RXD1	RW				PIN configuration register	



I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[31:10]	Reserved			
				[9]	RGMII_RXD1_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	RGMII_RXD1_PU	1'h0	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	RGMII_RXD1_PD	1'h1	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	G. 10
				[6]	Reserved			
				[5:2]	RGMII_RXD1_DS	4'h0	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD1_FS	2'h3	PIN function selection	
							00: Normal function (RGMII_RXD1 or RMII_RXD1)	
							01: N/A	
							10: N/A 11: GPIO	
	00B0H	RGMII_RXD2	RW				PIN configuration register	
	ООВОП	KGIVIII_KXD2	IN V V	[31:10]	Reserved		Fin Configuration register	_
				[9]	RGMII_RXD2_ST	1'h0	PINI Schmitt trigger enable	
					INGIVIII_IONDE_51	1110	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				[8]	RGMII_RXD2_PU	1'h0	PIN pull up enable	
				[0]			0: Disabled	
						***	1: Enabled	
				[7]	RGMII_RXD2_PD	1'h1	Pin pull down enable	
							0: Disabled	CDIC
						7577,	1: Enabled	GPIC
				[6]	Reserved			
			[5:2]	RGMII_RXD2_DS	4'h0	PIN Driving selector (typical value)		
						0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA		
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD2_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
						11: GPIO		



DIN Group	PIN_REG	BASE_ADDR: 0xA	600_4000							
PIN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO		
	00B4H	RGMII_RXD3	RW				PIN configuration register			
				[31:10]	Reserved					
				[9]	RGMII_RXD3_ST	1'h0	PIN Schmitt trigger enable			
							0: Disabled			
							1: Enabled			
				[8]	RGMII_RXD3_PU	1'h0	PIN pull up enable			
				[7]	RGMII_RXD3_PD	1'h1	Pin pull down enable			
								GPIO2[13]		
							1: Enabled			
Ethernet MAC				[6]	Reserved					
				[5:2]	RGMII_RXD3_DS	4'h0				
				[1:0]	RGMII_RXD3_FS	2'h3				
							0: Disabled 1: Enabled PIN pull up enable 0: Disabled 1: Enabled			
	00B8H	RGMII_RX_DV	RW				PIN configuration register			
				[31:10]	Reserved					
				[9]	RGMII_RX_DV_ST	1'h0	PIN Schmitt trigger enable			
						杉	1: Enabled			
				[8]	RGMII_RX_DV_PU	1'h0	PIN pull up enable			
							0: Disabled			
						327	1: Enabled			
				[7]	RGMII_RX_DV_PD	1'h1	Pin pull down enable			
					X		0: Disabled 1: Enabled PIN Driving selector (typical value) 0000: 6mA			
							1: Enabled	GPIO2[14]		
				[6]	Reserved					
				[5:2]	RGMII_RX_DV_DS	4'h0				
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			



Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPI
Onoot	rtogiotor rtaino	AGGGG	[1:0]	RGMII_RX_DV_FS	2'h3	PIN function selection	3 . 1
			[1.0]		2113	00: Normal function (RGMII_RX_DV or RMII_CRS_DV)	
						01: N/A	
						10: N/A	
						11: GPIO	
00BCH	RGMII_TX_CLK	RW				PIN configuration register	
			[31:10]	Reserved			
			[9]	RGMII_TX_CLK_ST	1'h0	PIN Schmitt trigger enable	
						0: Disabled	
						1: Enabled	
			[8]	RGMII_TX_CLK_PU	1'h0	PIN pull up enable	
						0: Disabled	
						1: Enabled	
			[7]	RGMII_TX_CLK_PD	1'h1	Pin pull down enable	
						0: Disabled	GPIC
						1: Enabled	GFIC
			[6]	Reserved		8	
			[5:2]	RGMII_TX_CLK_DS	4'h3	PIN Driving selector (typical value)	
						0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
			1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1	1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
			[1:0]	RGMII_TX_CLK_FS	2'h3	PIN function selection	
						00: Normal function (RGMII_TX_CLK or RMII_REF_CLK_OUT)	
						01: N/A	
						10: N/A	
						11: GPIO	
00C0H	RGMII_TXD0	RW			**	PIN configuration register	
			[31:10]	Reserved			
			[9]	RGMII_TXD0_ST	1'h0	PIN Schmitt trigger enable	
					2011,	0: Disabled	
					1: Enabled		
		[8]	RGMII_TXD0_PU	1'h0	PIN pull up enable		
					0: Disabled		
					1: Enabled		
		[7]	RGMII_TXD0_PD	1'h1	Pin pull down enable		
						0: Disabled	GPIC
						1: Enabled	GFIO
			[6]	Reserved			



PIN_REC	BASE_ADDR: 0xA	4600_4000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
			[5:2]	RGMII_TXD0_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1:0]	RGMII_TXD0_FS	2'h3	PIN function selection 00: Normal function (RGMII_TXD0 or RMII_TXD0) 01: N/A 10: N/A 11: GPIO	
00C4H	RGMII_TXD1	RW				PIN configuration register	
			[31:10]	Reserved			
			[9]	RGMII_TXD1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
			[8]	RGMII_TXD1_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
			[7]	RGMII_TXD1_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[1]
			[6]	Reserved			
			[5:2]	RGMII_TXD1_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1:0]	RGMII_TXD1_FS	2'h3	PIN function selection 00: Normal function (RGMII_TXD1 or RMII_TXD1) 01: N/A 10: N/A 11: GPIO	
00C8H	RGMII_TXD2	RW				PIN configuration register	
			[31:10]	Reserved	103,		
			[9]	RGMII_TXD2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
			[8]	RGMII_TXD2_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
			[7]	RGMII_TXD2_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[2]



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI		
				[6]	Reserved					
				[5:2]	RGMII_TXD2_DS	4'h3	PIN Driving selector (typical value)			
				[5.2]			0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	RGMII_TXD2_FS	2'h3	PIN function selection			
							00: Normal function			
							01: N/A			
							10: N/A			
							11: GPIO			
	00CCH	RGMII_TXD3	RW				PIN configuration register			
				[31:10]	Reserved					
				[9]	RGMII_TXD3_ST	1'h0	PIN Schmitt trigger enable			
							0: Disabled			
							1: Enabled			
				[8]	RGMII_TXD3_PU	1'h0	PIN pull up enable			
							0: Disabled			
							1: Enabled			
				[7]	RGMII_TXD3_PD	1'h1	Pin pull down enable			
							0: Disabled	GPIO3		
							1: Enabled	Gi ios		
				[6]	Reserved					
				[5:2]	RGMII_TXD3_DS	4'h3	PIN Driving selector (typical value)			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	RGMII_TXD3_FS	2'h3	PIN function selection			
						术》	00: Normal function			
						X	01: N/A			
							10: N/A			
				•		POL,	11: GPIO			
	00D0H	RGMII_TX_EN	RW			0	PIN configuration register			
				[31:10]	Reserved					
				[9]	RGMII_TX_EN_ST	1'h0	PIN Schmitt trigger enable			
							0: Disabled			
							PIN Driving selector (typical value) 2000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 2000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA 21N function selection 20: Normal function 20: N/A 20: N/A 21: GPIO 21N configuration register 21N Schmitt trigger enable 2: Disabled 3: Enabled			
				[8]	RGMII_TX_EN_PU	1'h0	PIN pull up enable			
							0: Disabled			
							1: Enabled			



N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[7]	RGMII_TX_EN_PD	1'h1	Pin pull down enable	
							0: Disabled	
							1: Enabled	GPIO3[
				[6]	Reserved			
				[5:2]	RGMII_TX_EN_DS	4'h3	PIN Driving selector (typical value)	
				[3.2]	KGIVIII_TX_EIV_D3	4113	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TX_EN_FS	2'h3	PIN function selection	
							00: Normal function (RGMII_TX_EN or RMII_TX_EN)	
							01: N/A	
							10: N/A	
							11: GPIO	
	00D4H	SD0_CLK	RW				PIN configuration register	
				[31:10]	Reserved		4.3	
				[9]	SD0_CLK_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD0_CLK_PU	1'h0	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	SD0_CLK_PD	1'h1	Pin pull down enable	
							0: Disabled	CDIO31
							1: Enabled	GPIO3[
				[6]	Reserved			
				[5:2]	SD0_CLK_DS	4'h6	PIN Driving selector (typical value)	
						不	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
						,1/2	1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_CLK_FS	2'h3	PIN function selection	
						75/7,	00: Normal function	
						0,7	01: N/A	
							10: N/A	
							11: GPIO	
	00D8H	SD0_CMD	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_CMD_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	



Group	Offset	Register Name	Access	s Bits	Field Name	Default Value	Description Description	GPI
				[8]	SD0_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3
				[6]	Reserved			
				[5:2]	SD0_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_CMD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00DCH	SD0_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_DATA0_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3
				[6]	Reserved	1400		
			[5:2]	SD0_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	SD0_DATA0_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E0H	SD0_DATA1	RW				PIN configuration register	
				[31:10]	Reserved			

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I Omercia	PIN_REG	BASE_ADDR: 0xA6	600_4000					
d (iroun	Offset	Register Name	Access		Field Name	Default Value	Description	GPI
				[9]	SD0_DATA1_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA1_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA1_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3
				[6]	Reserved			
				[5:2]	SD0_DATA1_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA1_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E4H	SD0_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_DATA2_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA2_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA2_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3
				[6]	Reserved			
				[5:2]	SD0_DATA2_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E8H	SD0_DATA3	RW				PIN configuration register	
				_				



DIN Croup	PIN_REG	BASE_ADDR: 0xA	600_4000					
PIN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	SD0_DATA3_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
					1'h1	PIN pull up enable 0: Disabled 1: Enabled		
				[7]	SD0_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[10
				[6]	Reserved			
					SD0_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00ECH	SD0_DATA4	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_DATA4_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA4_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
SD0				[7]	SD0_DATA4_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[11
				[6]	Reserved	,32°		
				[5:2]	SD0_DATA4_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
	[1:0] SD0_DATA4_FS 2'h3 PIN function selection 00: Normal function 01: N/A 10: N/A					00: Normal function 01: N/A		
	00F0H	SD0_DATA5	RW				PIN configuration register	



l Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[31:10]	Reserved			
				[9]	SD0_DATA5_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD0_DATA5_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	SD0_DATA5_PD	1'h0	Pin pull down enable	
							0: Disabled	CDIO
							1: Enabled	GPIO
				[6]	Reserved			
				[5:2]	SD0_DATA5_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA5_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	00F4H	SD0_DATA6	RW				PIN configuration register	
				[31:10]	Reserved		3	
				[9]	SD0_DATA6_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD0_DATA6_PU	1'h1	PIN pull up enable	
							0: Disabled	
						下/	1: Enabled	
				[7]	SD0_DATA6_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	
				[6]	Reserved	18.		
				[5:2]	SD0_DATA6_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA6_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	



Group	Offset	Register Name	Access	s Bits	Field Name	Default Value	Description	GPIO			
	00F8H	SD0_DATA7	RW				PIN configuration register				
				[31:10]	Reserved						
				[9]	SD0_DATA7_ST	1'h1	PIN Schmitt trigger enable				
							0: Disabled				
							1: Enabled				
				[8]	SD0_DATA7_PU	1'h1	PIN pull up enable				
							0: Disabled				
							1: Enabled				
				[7]	SD0_DATA7_PD	1'h0	Pin pull down enable				
							0: Disabled	GPIO3[14]			
							1: Enabled				
				[6]	Reserved						
				[5:2]	SD0_DATA7_DS	4'h6	PIN Driving selector (typical value)				
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA				
				[1:0]	SD0_DATA7_FS	2'h3	PIN function selection				
	00FCH	SD0_DATA_STRB	RW								
				[31:10]	Reserved						
				[9]	SD0_DATA_STRB_ST	1'h1	PIN Schmitt trigger enable				
							0: Disabled				
						***	1: Enabled				
				[8]	SD0_DATA_STRB_PU	1'h0	PIN pull up enable				
							0: Disabled				
						OZ,	1: Enabled				
				[7]	SD0_DATA_STRB_PD	1'h1	Pin pull down enable				
					(4)		0: Disabled	GPIO3[15]			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111: 27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111: 45mA PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO PIN configuration register PIN Schmitt trigger enable 0: Disabled 1: Enabled PIN pull up enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled				
				[6]	Reserved						
				[5:2]	SD0_DATA_STRB_DS	4'h6	PIN Driving selector (typical value)				
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA				
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA				



Offset	Register Name	Access	Bits	Field Name	Default Value	Description	G
011001	Trogistor Humo	7,00000	[1:0]	SD0_DATA_STRB_FS	2'h3	PIN function selection	
Offset 0100H			[1.0]	JDO_DATA_STRU_TS	2113	00: Normal function	
						01: N/A	
						10: N/A	
						11: GPIO	
0100⊔	SD0_DET_EN	RW				PIN configuration register	
01000	3DO_DET_EN	NVV	[31:9]	Reserved		Fin Configuration register	
					1'h1	DINI Schmitt tringer enable	
			[8]	SD0_DET_EN_ST	l n i		
			[7]	SD0_DET_EN_PS	1'h1	PIN pull selector	
						0: Pull down	
						1: Pull up	
			[6]	SD0_DET_EN_PE	1'h1	Pin pull enable	
						0: Pull function is disabled	GP
						1: Pull function is enabled	
			[5:2]	SD0_DET_EN_DS	4'h0	PIN Driving selector (typical value)	
						0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
					1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
			[1:0]	SD0_DET_EN_FS	2'h3	PIN function selection	
						11: GPIO	
0104H	1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA						
			[31:9]	Reserved		0: Pull down 1: Pull up Pin pull enable 0: Pull function is disabled 1: Pull function is enabled PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
			[8]	SD0_WPROT_ST	1'h1	PIN Schmitt trigger enable	
					100		
						1: Enabled	
			[7]	SD0_WPROT_PS	1'h0	PIN pull selector	
					2.	1: Pull up	
			[6]	SD0_WPROT_PE	1'h1	Pin pull enable	
							GP
			[5:2]	SD0_WPROT_DS	4'h0	PIN Driving selector (typical value)	
			الع.دا	350_**** 1.01_53	110		
			-1			10000, SHIR OOU LOHIN OO IO, SHIR OO II, IEHIM O IOO, ITHIM O IO I, EUHM O I IO, EEHIM O I I I.EJIHM	

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Offset	Register Name	Access	s Bits	Field Name	Default Value	Description	GPIC
Onoot	Trogistor Hamo	7,0000	[1:0]	SD0_WPROT_FS	2'h3	PIN function selection	011
			[1.0]	3D0_W1 NO1_13	2113	00: Normal function	
						01: N/A	
						10: N/A	
						11: GPIO	
 0108H	SD1_CLK	RW				PIN configuration register	
0 10011	JD I_CLK	IXVV	[31:10]	Reserved		The configuration register	
			[9]	SD1_CLK_ST	1'h0	PIN Schmitt trigger enable	_
				SD1_CLK_S1	1110	0: Disabled	
						1: Enabled	
			[8]	SD1_CLK_PU	1'h0	PIN pull up enable	
						0: Disabled	
						1: Enabled	
			[7]	SD1_CLK_PD	1'h1	Pin pull down enable	
						0: Disabled	GPIO4
						1: Enabled	GP104
			[6]	Reserved		8	
			[5:2]	SD1_CLK_DS	4'h6	PIN Driving selector (typical value)	
						0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
						1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1:0]	SD1_CLK_FS	2'h3	PIN function selection	
						00: Normal function	
						01: N/A	
						10: N/A	
						11: GPIO	
010CH	SD1_CMD	RW			X)	PIN configuration register	
			[31:10]	Reserved	XX		
			[9]	SD1_CMD_ST	1'h0	PIN Schmitt trigger enable	
						0: Disabled	
					4	1: Enabled	
			[8]	SD1_CMD_PU	1'h1	PIN pull up enable	
						0: Disabled	
						1: Enabled	
	[7]	[7]	SD1_CMD_PD	1'h0	Pin pull down enable		
		=			0: Disabled		
						1: Enabled	GPIO4[



Group		BASE_ADDR: 0x4	1000_7000					
Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	G
				[5:2]	SD1_CMD_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_CMD_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	0110H	SD1_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD1_DATA0_ST	1'h1	PIN Schmitt trigger enable	
				[[0]			0: Disabled	
							1: Enabled	
				[8]	SD1_DATA0_PU	1'h1	PIN pull up enable	
				[[0]	55 1_57 (17 (5_1 6		0: Disabled	
							1: Enabled	
					CD 4 D 4 T 4 0 DD	411.0		
				[7]	SD1_DATA0_PD	1'h0	Pin pull down enable	
							0: Disabled	GP
							1: Enabled	
				[6]	Reserved			
				[5:2]	SD1_DATA0_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA0_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
						A T	10: N/A	
						1/2/4	11: GPIO	
SD1	0114H	SD1_DATA1	RW				PIN configuration register	
				[31:10]	Reserved	307,		
				[9]	SD1_DATA1_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD1_DATA1_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	SD1_DATA1_PD	1'h0	Pin pull down enable	
							0: Disabled	CE
							1: Enabled	GPI



I Group	Offset	Register Name	Access	s Bits	Field Name	Default Value	Description	GPI
				[6]	Reserved			
				[5:2]	SD1_DATA1_DS	4'h6	PIN Driving selector (typical value)	
				[5.2]		1	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA1_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	0118H	SD1_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD1_DATA2_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD1_DATA2_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	SD1_DATA2_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO-
							1: Enabled	G. 10-
				[6]	Reserved			
				[5:2]	SD1_DATA2_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA2_FS	2'h3	PIN function selection	
						不少	00: Normal function	
							01: N/A	
							10: N/A	
				•		102,	11: GPIO	
	011CH	SD1_DATA3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD1_DATA3_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD1_DATA3_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	



l Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIC		
				[7]	SD1_DATA3_PD	1'h0	Pin pull down enable			
				,			0: Disabled			
							1: Enabled	GPIO4[
				161	D 1					
				[6]	Reserved					
				[5:2]	SD1_DATA3_DS	4'h6	PIN Driving selector (typical value)			
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA			
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	SD1_DATA3_FS	2'h3	PIN function selection			
							00: Normal function			
							01: N/A			
							10: N/A			
							11: GPIO			
	0120H	SD2_CLK	RW				PIN configuration register			
				[31:10]	Reserved			_		
				[9]	SD2_CLK_ST	1'h0	DINI Schmitt trigger enable			
					3D2_CLK_31	1 110				
				[8]	SD2_CLK_PU	1'h0				
							1: Enabled			
				[7]	SD2_CLK_PD	1'h1	Pin pull down enable			
					3D2_CEI_I D					
							1: Enabled	GPIO4[
				[6]	Reserved		XXL	_		
				[5:2]	SD2_CLK_DS	4'h6	PIN Driving coloctor (typical value)			
				[3.2]	3DZ_CLK_D3	4110	A. y			
						/ 1/4				
				[1:0]	SD2_CLK_FS	2'h3				
						(X)				
							11: GPIO			
	0124H	SD2_CMD	RW				PIN configuration register			
				[31:10]	Reserved		11: GPIO PIN configuration register PIN Schmitt trigger enable 0: Disabled 1: Enabled PIN pull up enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO			
				[9]	SD2_CMD_ST	1'h0	PIN Schmitt trigger enable			



I Group	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIC
				[8]	SD2_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO4
				[6]	Reserved			
				[5:2]	SD2_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_CMD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0128H	SD2_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD2_DATA0_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD2_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO4
				[6]	Reserved	100		
				[5:2]	SD2_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
SD2				[1:0]	SD2_DATA0_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
302	012CH	SD2_DATA1	RW				PIN configuration register	
				[31:10]	Reserved			



roup	Offset	BASE_ADDR: 0xA		Rite	Field Name	Default Value	Description	GF
	Offset	Register Name	Access				·	GI
				[9]	SD2_DATA1_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD2_DATA1_PU	1'h1	PIN pull up enable	
				1			0: Disabled	
							1: Enabled	
					600 04744 00	411.0		
				[7]	SD2_DATA1_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIC
							1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_DATA1_DS	4'h6	PIN Driving selector (typical value)	
				[5.2]	65 <u>_</u> 5756	1	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA1_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	0130H	SD2_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD2_DATA2_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD2_DATA2_PU	1'h1	PIN pull up enable	
				[O]	JUZ_UATAZ_T		0: Disabled	
							1: Enabled	
				[7]	SD2_DATA2_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIC
							1: Enabled	0.10
				[6]	Reserved	1387,		
				[5:2]	SD2_DATA2_DS	4'h6	PIN Driving selector (typical value)	
				[5.2]	352_37(17(2_53		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
						au -		
				[1:0]	SD2_DATA2_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	



N Group	PIN_REG	BASE_ADDR: 0xA60	00_4000					
N Group	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIC
				[31:10]	Reserved			
				[9]	SD2_DATA3_ST	1'h1	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SD2_DATA3_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	SD2_DATA3_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO4
							1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_DATA3_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA3_FS	2'h3	PIN function selection	
							00: Normal function	
							01: N/A 10: N/A	
							11: GPIO	
	0138H	RT1120 OUT CLK	D\A/				PIN configuration register	
	013011	H BT1120_OUT_CLK RW	IXVV	[21:10]	Reserved		The configuration register	_
				[31:10]	BT1120_OUT_CLK_ST	1'h1	PIN Schmitt trigger enable	
				[9]	B11120_OO1_CLK_31		0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_CLK_PU	1'h0	PIN pull up enable	
					D11120_001_CER_1 0		0: Disabled	
						×	1: Enabled	
				[7]	BT1120_OUT_CLK_PD	1'h1	Pin pull down enable	
				[,]	D11120_001_01K_1 D		0: Disabled	
							1: Enabled	GPIO4
				[6]	Reserved	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ 		
				[5:2]	BT1120_OUT_CLK_DS	4'h3	PIN Driving selector (typical value)	
				[3.2]	D11120_001_01K_D3		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
						1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
				[1:0]	BT1120_OUT_CLK_FS	2'h3	PIN function selection	_
				[]			00: Normal function (BT1120_OUT_CLK or BT656_OUT_CLK)	
						01: DVP_IN_PCLK		
							10: RGB_CLK	
							11: GPIO	
	013CH	BT1120_OUT_DAT0	RW				PIN configuration register	



Group	Offset	Register Name	00_4000 Access	Rite	Field Name	Default Value	Description	GP
	Oliset	Register Name	Access		Reserved	Delault Value	Description	Gi
				[31:10]		1160	DINI Cohmitt trigger enable	
				[9]	BT1120_OUT_DAT0_ST	I no	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_DAT0_P	1'h0	PIN pull up enable	
					U		0: Disabled	
							1: Enabled	
				[7]	BT1120_OUT_DAT0_P	1'h1	Pin pull down enable	
					D		0: Disabled	GPIC
							1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT0_D	4'h3	PIN Driving selector (typical value)	
					S		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT0_FS	2'h3	PIN function selection	
				,			00: Normal function (BT1120_OUT_DAT0 or BT656_DAT0)	
							01: DVP_IN_VSYNC	
							10: RGB_DAT0	
							11: GPIO	
	0140H	BT1120_OUT_DAT1	RW				PIN configuration register	
				[31:10]	Reserved		-3	
				[9]	BT1120_OUT_DAT1_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_DAT1_P	1'h0	PIN pull up enable	
					U		0: Disabled	
						本人	1: Enabled	
				[7]	BT1120_OUT_DAT1_P	1'h1	Pin pull down enable	
					D		0: Disabled	
						DZ,	1: Enabled	GPIC
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT1_D	4'h3	PIN Driving selector (typical value)	
				[5.2]	S		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
						1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA		
			[1:0]	BT1120_OUT_DAT1_FS	12'h3	PIN function selection		
			[1.0]	BTTTZU_OUT_DATT_F3	, , , , , , , , , , , , , , , , , , , ,	00: Normal function (BT1120_OUT_DAT1 or BT656_DAT1)		
							01: DVP_IN_HSYNC	
							10: RGB_DAT1	



Group	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIO
	0144H	BT1120_OUT_DAT2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled Pin pull up enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27m 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45m PIN function selection 00: Normal function (BT1120_OUT_DAT2 or BT656_DAT2) 01: DVP_IN_DATA0 10: RGB_DAT2 11: GPIO PIN configuration register PIN Schmitt trigger enable 0: Disabled 1: Enabled PIN pull up enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled 1: Enabled Pin pull down enable 0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_DAT2_P	1'h0	PIN pull up enable	
					U			
							1: Enabled	
				[7]	BT1120_OUT_DAT2_P	1'h1		
					D			GPIO5[
							1: Enabled	
				[6]	Reserved		20	
				[5:2]	BT1120_OUT_DAT2_D	4'h3		
					S			
				[1:0]	BT1120_OUT_DAT2_FS	[2'h3		
	0148H	BT1120_OUT_DAT3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT3_ST	1'h0	PIN Schmitt trigger enable	
						X		
						*//		
				[8]	BT1120_OUT_DAT3_P	1'h0		
					U			
				[7]	BT1120_OUT_DAT3_P	1'h1		
					D		Pin pull down enable 0: Disabled 1: Enabled PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27m/ 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA PIN function selection 00: Normal function (BT1120_OUT_DAT2 or BT656_DAT2) 01: DVP_IN_DATA0 10: RGB_DAT2 11: GPIO PIN configuration register PIN Schmitt trigger enable 0: Disabled 1: Enabled PIN pull up enable 0: Disabled 1: Enabled Pin pull down enable	
				[C]	Deserved		T. Eliablea	
				[6]	Reserved	4'b2	DIN Driving coloctor (typical value)	
				[5:2]	BT1120_OUT_DAT3_D	4113		



Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GI
Onset	Tregister Name	Access	[1:0]	BT1120_OUT_DAT3_FS		PIN function selection	O.
			[1.0]	D11120_001_DA13_13	2113	00: Normal function (BT1120_OUT_DAT3 or BT656_DAT3)	
						01: DVP_IN_DATA1	
						10: RGB_DAT3	
						11: GPIO	
014CH	BT1120_OUT_DAT4	RW				PIN configuration register	
			[31:10]	Reserved			
			[9]	BT1120_OUT_DAT4_ST	1'h0	PIN Schmitt trigger enable	
						0: Disabled	
						1: Enabled	
			[8]	BT1120_OUT_DAT4_P	1'h0	PIN pull up enable	
				U		0: Disabled	
						1: Enabled	
			[7]	BT1120_OUT_DAT4_P	1'h1	Pin pull down enable	
				D		0: Disabled	GP
						1: Enabled	
			[6]	Reserved			
			[5:2]	BT1120_OUT_DAT4_D	4'h3	PIN Driving selector (typical value)	
				S		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
						1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1:0]	BT1120_OUT_DAT4_FS	2'h3	PIN function selection	
						00: Normal function (BT1120_OUT_DAT4 or BT656_DAT4)	
						01: DVP_IN_DATA2	
						10: RGB_DAT4	
						11: GPIO	
0150H	BT1120_OUT_DAT5	RW			· KI	PIN configuration register	_
			[31:10]	Reserved			
			[9]	BT1120_OUT_DAT5_ST	1'h0	PIN Schmitt trigger enable	
					<i>5</i> 7.	0: Disabled	
						1: Enabled	
		[8]	BT1120_OUT_DAT5_P	1'h0	PIN pull up enable		
				U		0: Disabled	
						1: Enabled	
			[7]	BT1120_OUT_DAT5_P	1'h1	Pin pull down enable	
				D		0: Disabled	GP
						1: Enabled	
			[6]	Reserved			



DIN Croup	PIN_REG	BASE_ADDR: 0xA60	0_4000					
PIN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	BT1120_OUT_DAT5_D S	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT5_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT5 or BT656_DAT5) 01: DVP_IN_DATA3 10: RGB_DAT5 11: GPIO	
	0154H	BT1120_OUT_DAT6	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT6_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT6_P U	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT6_P D	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[5]
I				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT6_D S	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT6_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT6 or BT656_DAT6) 01: DVP_IN_DATA4 10: RGB_DAT6 11: GPIO	
I	0158H	BT1120_OUT_DAT7	RW			XX	PIN configuration register	
I				[31:10]	Reserved	ST,		
				[9]	BT1120_OUT_DAT7_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT7_P U	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
BT1120_OUT				[7]	BT1120_OUT_DAT7_P D	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[6]



DIM Croup	PIN_REG	BASE_ADDR: 0xA60	0_4000					
PIN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT7_D	4'h3	PIN Driving selector (typical value)	
					S		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT7_FS	2'h3	PIN function selection	
							00: Normal function (BT1120_OUT_DAT7 or BT656_DAT7)	
							01: DVP_IN_DATA5	
							10: RGB_DAT7 11: GPIO	
	015611	DT1120 OLIT DATO	DVA					
	015CH	BT1120_OUT_DAT8	RW	[24 40]	Daganiad		PIN configuration register	
				[31:10]	Reserved	111.0	DIAL Calabating the control of the c	
				[9]	BT1120_OUT_DAT8_ST	1'n0	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				101	DT1120 OUT DATO D	111.0		
				[8]	BT1120_OUT_DAT8_P	1'h0	PIN pull up enable 0: Disabled	
					O		1: Enabled	
				[7]	DT1120 OLIT DATO D	411.4		
				[7]	BT1120_OUT_DAT8_P	I'nı	Pin pull down enable 0: Disabled	
					D		1: Enabled	GPIO5[7]
				[6]	Reserved			
				[6]		4'b2	DIN Driving coloctor (typical value)	
				[5:2]	BT1120_OUT_DAT8_D S	4 N3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1.0]	DT1120 OUT DATE OF	2162	PIN function selection	
				[1:0]	BT1120_OUT_DAT8_FS	12 113	00: Normal function (BT1120_OUT_DAT8 or BT656_DAT0)	
						1/2	01: DVP_IN_DATA6	
							10: RGB_DAT8	
						VIGIT.	11: GPIO	
	0160H	BT1120_OUT_DAT9	RW			V	PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT9_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_DAT9_P	1'h0	PIN pull up enable	
					U		0: Disabled	
							1: Enabled	



Group	Offset	Register Name	Acces	s Bits	Field Name	Default Value	Description	GPIC
				[7]	BT1120_OUT_DAT9_P	1'h1	Pin pull down enable	
					D		0: Disabled	
							1: Enabled	GPIO5[
				[6]	Reserved			
				[6]		411.2		
				[5:2]	BT1120_OUT_DAT9_D	4 ⁻ n3	PIN Driving selector (typical value)	
					S		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT9_FS	2'h3	PIN function selection	
							00: Normal function (BT1120_OUT_DAT9 or BT656_DAT1)	
							01: DVP_IN_DATA7	
							10: RGB_DAT9	
							11: GPIO	
	0164H	BT1120_OUT_DAT10	RW				PIN configuration register	
		D11120_001_D1110		[31:10]	Reserved		i ii t comigaration registo.	
				[9]	BT1120_OUT_DAT10_S	1'h0	PIN Schmitt trigger enable	
				[2]	T		0: Disabled	
					1		1: Enabled	
				[8]	BT1120_OUT_DAT10_	1'h0	PIN pull up enable	
					PU		0: Disabled	
							1: Enabled	
				[7]	BT1120_OUT_DAT10_	1'h1	Pin pull down enable	
					PD		0: Disabled	
							1: Enabled	GPIO5[
				[6]	Reserved		XXXI	
				[5:2]	BT1120_OUT_DAT10_	1'h3	PIN Driving selector (typical value)	
				[5.2]	DS	4113	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
					D3	1/1	1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT10_F	2'h3	PIN function selection	
					S	7	00: Normal function (BT1120_OUT_DAT10 or BT656_DAT2)	
							01: DVP_IN_DATA8	
							10: RGB_DAT10	
							11: GPIO	
	0168H	BT1120_OUT_DAT11	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT11_S	1'h0	PIN Schmitt trigger enable	
					T		0: Disabled	
							1: Enabled	

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Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	BT1120_OUT_DAT11_ PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT11_ PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT11_ DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT11_F	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT11 or BT656_DAT3) 01: DVP_IN_DATA9 10: RGB_DAT11 11: GPIO	
	016CH	BT1120_OUT_DAT12	RW				PIN configuration register	
				[31:10]	Reserved		387	
				[9]	BT1120_OUT_DAT12_S T	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT12_ PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT12_ PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT12_ DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT12_F S	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT12 or BT656_DAT4) 01: DVP_IN_DATA10 10: RGB_DAT12 11: GPIO	
	0170H	BT1120_OUT_DAT13	RW				PIN configuration register	
				[31:10]	Reserved			



roup	Offset	BASE_ADDR: 0xA60	_	Dita	Field Name	Default Value	Description	CP
	Offset	Register Name	Access					GP
				[9]	BT1120_OUT_DAT13_S	o i nu	PIN Schmitt trigger enable 0: Disabled	
					I		1: Enabled	
							i. Ellabled	
				[8]	BT1120_OUT_DAT13_	1'h0	PIN pull up enable	
					PU		0: Disabled	
							1: Enabled	
				[7]	BT1120_OUT_DAT13_	1'h1	Pin pull down enable	
					PD		0: Disabled	CDIO
							1: Enabled	GPIO
				[6]	Reserved			-
				[5:2]	BT1120_OUT_DAT13_	1'h3	PIN Driving selector (typical value)	
				[5.2]	DS	4113	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[4 O]	DT4420 OLIT 5 1742 F	211.2		
				[1:0]	BT1120_OUT_DAT13_F	2'h3	PIN function selection	
					5		00: Normal function (BT1120_OUT_DAT13 or BT656_DAT5)	
							01: DVP_IN_DATA11 10: RGB_DAT13	
							11: GPIO	
	0174H	BT1120_OUT_DAT14	RW				PIN configuration register	
	01740	B11120_001_DA114	LVV	[31:10]	Reserved		File Configuration register	
					BT1120_OUT_DAT14_S	1160	DINI Schmitt trigger enable	
				[9]	T BITI20_OUT_DAT14_3	I no	PIN Schmitt trigger enable 0: Disabled	
					1		1: Enabled	
							57. Z	
				[8]	BT1120_OUT_DAT14_	1'h0	PIN pull up enable	
					PU		0: Disabled	
						*	1: Enabled	
				[7]	BT1120_OUT_DAT14_	1'h1	Pin pull down enable	
					PD	100	0: Disabled	GPIO
							1: Enabled	GF10.
				[6]	Reserved	<i>3</i> 7,		
				[5:2]	BT1120_OUT_DAT14_	4'h3	PIN Driving selector (typical value)	
					DS		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT14_F	2'h3	PIN function selection	
				[]	S		00: Normal function (BT1120_OUT_DAT14 or BT656_DAT6)	
							01: N/A	
							10: RGB_DAT14	
							11: GPIO	
		1						



N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT15_S	1'h0	PIN Schmitt trigger enable	
					Т		0: Disabled	
							1: Enabled	
				[8]	BT1120_OUT_DAT15_	1'h0	PIN pull up enable	
					PU		0: Disabled	
							1: Enabled	
				[7]	BT1120_OUT_DAT15_	1'h1	Pin pull down enable	
					PD		0: Disabled	CDIO
							1: Enabled	GPIO:
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT15_	4'h3	PIN Driving selector (typical value)	
					DS		0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT15_F	2'h3	PIN function selection	
					S		00: Normal function (BT1120_OUT_DAT15 or BT656_DAT7)	
							01: N/A	
							10: RGB_DAT15	
	017611	LIADTO TVD	RW				11: GPIO	
	017CH	UART0_TXD	KVV	[21.0]	Reserved		PIN configuration register	
				[31:9]		1'h0	DINI Schmitt trigger enable	
				[O]	UART0_TXD_ST	1110	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				[7]	UARTO_TXD_PS	1'h1	PIN pull selector	
				[[,]	OAKTO_TXD_T3	1111	0: Pull down	
						· A	1: Pull up	
				[6]	UARTO_TXD_PE	1'h1	Pin pull enable	
							0: Pull function is disabled	GPIO
						<i>5</i> 72,	1: Pull function is enabled	
				[5:2]	UARTO_TXD_DS	4'h0	PIN Driving selector (typical value)	
					1		0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
							1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART0_TXD_FS	2'h0	PIN function selection	
							00: Normal function	
							01: N/A	
							10: N/A	
JARTO							11: GPIO	
	0180H	UARTO_RXD	RW				PIN configuration register	



Group	PIN_REG	BASE_ADDR: 0xA6	00_4000					
Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[31:9] [8]	Reserved UARTO_RXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UARTO_RXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UARTO_RXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	UARTO_RXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART0_RXD_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0184H	UART1_TXD	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	UART1_TXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_TXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_TXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6
				[5:2]	UART1_TXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_TXD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0188H	UART1_RXD	RW				PIN configuration register	
		UART1_RXD		[31:9]	Reserved			



PIN Group		BASE_ADDR: 0xA			•			
пт Огоар	Offset	Register Name	Access	Bits	Field Name	Default Value	Description Description	GPIC
				[8]	UART1_RXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_RXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_RXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6
				[5:2]	UART1_RXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
UART1				[1:0]	UART1_RXD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	018CH	UART1_RTSN	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	UART1_RTSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_RTSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_RTSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6
				[5:2]	UART1_RTSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_RTSN_FS	2'h3	PIN function selection 00: Normal function 01: UART2_TXD 10: N/A 11: GPIO	
	0190H	UART1_CTSN	RW				PIN configuration register	



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[8]	UART1_CTSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_CTSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_CTSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	UART1_CTSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_CTSN_FS	2'h3	PIN function selection 00: Normal function 01: UART2_RXD 10: N/A 11: GPIO	
	0194H	I2S0_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S0_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S0_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S0_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	I2S0_MCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0198H	I2S0_BCLK	RW				PIN configuration register	
		I2SO_BCLK R		[31:9]	Reserved			



I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GP
				[8]	I2S0_BCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S0_BCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2SO_BCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIC
				[5:2]	I2SO_BCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
1250				[1:0]	I2S0_BCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	019CH	I2S0_LRCK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S0_LRCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2SO_LRCK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2SO_LRCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIC
				[5:2]	I2S0_LRCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_LRCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A0H	I2S0_SDIO	RW				PIN configuration register	
				[31:9]	Reserved			



Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
				[8]	I2S0_SDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2SO_SDIO_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2SO_SDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	I2S0_SDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_SDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A4H	I2S1_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S1_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPI06
				[5:2]	I2S1_MCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A8H	I2S1_BCLK	RW				PIN configuration register	
		I2S1_BCLK		[31:9]	Reserved		•	



N Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPI
	Offset	Register Name	Access	[8]	I2S1_BCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_BCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_BCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	I2S1_BCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
I2 S 1				[1:0]	I2S1_BCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01ACH	I2S1_LRCK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S1_LRCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_LRCK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_LRCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	I2S1_LRCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1	[1:0]	I2S1_LRCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B0H	I2S1_SDIO	RW				PIN configuration register	
				[31:9]	Reserved			



INI Cuavia	PIN_REG	BASE_ADDR: 0xA6	00_4000					
IN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	I2S1_SDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_SDIO_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_SDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[1
				[5:2]	I2S1_SDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_SDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B4H	SENSOR0_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	SENSOR0_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SENSOR0_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SENSOR0_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[13
				[5:2]	SENSOR0_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR0_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B8H	SENSOR1_MCLK	RW				PIN configuration register	
		SENSOR1_MCLK R		[31:9]	Reserved			



DIN Crous	PIN_REG	BASE_ADDR: 0xA6	600_4000					
PIN Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	SENSOR1_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SENSOR1_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SENSOR1_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[14
				[5:2]	SENSOR1_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR1_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
SENSOR	01BCH SE	SENSOR2_MCLK	RW				PIN configuration register	
SENSOR				[31:10]	Reserved			
				[9]	SENSOR2_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SENSOR2_MCLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SENSOR2_MCLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO6[15
				[6]	Reserved			
				[5:2]	SENSOR2_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
			[1:0] SENSOR2_MCLK_FS 2'h3 PIN function selection 00: Normal function 01: UART3_TXD 10: N/A 11: GPIO	00: Normal function 01: UART3_TXD				
	01C0H	SENSOR3_MCLK	RW				PIN configuration register	
				[31:10]	Reserved			



Proup		BASE_ADDR: 0xA6						
•	Offset	Register Name	Access		Field Name	Default Value		GF
				[9]	SENSOR3_MCLK_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	SENSOR3_MCLK_PU	1'h0	PIN pull up enable	
				[[0]			0: Disabled	
							1: Enabled	
				[7]	SENSOR3_MCLK_PD	1'h1	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	
				[6]	Reserved			
				[5:2]	SENSOR3_MCLK_DS	4'h1	PIN Driving selector (typical value)	
				[5.2]	SENSONS_INICEN_DS	7	0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR3_MCLK_FS	2'h3	PIN function selection	
							00: Normal function	
							01: UART3_RXD	
							10: N/A	
							11: GPIO	
	01C4H \	WDT_RSTOUT_N	RW				PIN configuration register	GPIC
				[31:9]	Reserved			
				[8]	WDT_RSTOUT_N_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[7]	WDT_RSTOUT_N_PS	1'h1	PIN pull selector	
				[,]	WD1_K31001_N_13		0: Pull down	
							1: Pull up	
						<u> </u>		
				[6]	WDT_RSTOUT_N_PE	1'h1	Pin pull enable	
							0: Pull function is disabled	GPIO
							1: Pull function is enabled	
				[5:2]	WDT_RSTOUT_N_DS	4'h1	PIN Driving selector (typical value)	
							0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA	
						N.	1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	WDT_RSTOUT_N_FS	2'h0	PIN function selection	
				[[1.0]	ראירויראיוראין וחאורא	2110	00: Normal function	
							01: N/A	
							10: N/A	
							11: GPIO	
	01C8H	X2A_WKUPIN_N	RW				PIN configuration register	
		X2A_WKUPIN_N		[31:9]	Reserved			



I Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GP
				[8]	X2A_WKUPIN_N_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	X2A_WKUPIN_N_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
MISC				[6]	X2A_WKUPIN_N_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO
				[5:2]	X2A_WKUPIN_N_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	X2A_WKUPIN_N_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
0	01CCH	X2A_IRQOUT_N	RW				PIN configuration register	
			[31:9] Reserved					
				[8]	X2A_IRQOUT_N_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	X2A_IRQOUT_N_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	X2A_IRQOUT_N_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIC
				[5:2]	X2A_IRQOUT_N_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	X2A_IRQOUT_N_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01D0H	BIFSD_DATA4	RW				PIN configuration register	
				[31:10]	Reserved			



I Group		BASE_ADDR: 0xA						
- Стобр	Offset	Register Name	Access		Field Name	Default Value		GP
				[9]	BIFSD_DATA4_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_DATA4_PU	1'h1	PIN pull up enable	
				1			0: Disabled	
							1: Enabled	
				[7]	DIECD DATA A DD	111.0		
				[7]	BIFSD_DATA4_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA4_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA4_FS	2'h0	PIN function selection	-
				[1.0]	טווטט_טאוא-	2110	00: Normal function	
							01: LPWM0	
							10: RGB_DAT20	
							11: GPIO	
	01D4H	BIFSD_DATA5	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA5_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[0]	DICCO DATAE DIL	1'h1	57. 1	
				[8]	BIFSD_DATA5_PU		PIN pull up enable 0: Disabled	
							1: Enabled	
						<u> </u>		
				[7]	BIFSD_DATA5_PD	1'h0	Pin pull down enable	
							0: Disabled	GPIO
							1: Enabled	
				[6]	Reserved	184		
				[5:2]	BIFSD_DATA5_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA5_FS	2'h0	PIN function selection	
							00: Normal function	
							01: LPWM1	
							10: RGB_DAT21	
							11: GPIO	
BIFSD	01D8H	BIFSD_DATA6	RW				PIN configuration register	



l Group	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GP
				[31:10]	Reserved			
				[9]	BIFSD_DATA6_ST	1'h0	PIN Schmitt trigger enable	
							0: Disabled	
							1: Enabled	
				[8]	BIFSD_DATA6_PU	1'h1	PIN pull up enable	
							0: Disabled	
							1: Enabled	
				[7]	BIFSD_DATA6_PD	1'h0	Pin pull down enable	
							0: Disabled	ani
							1: Enabled	GPIC
				[6]	Reserved			
				[5:2]	BIFSD_DATA6_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA6_FS	2'h0	PIN function selection	
							00: Normal function	
							01: LPWM2	
							10: RGB_DAT22	
	045611	DIECO DATAZ	DVA				11: GPIO	
	01DCH	BIFSD_DATA7	RW	524.401	Decembed		PIN configuration register	
				[31:10]	Reserved	411.0	PINIC L. W. C. L. L.	
				[9]	BIFSD_DATA7_ST	1'h0	PIN Schmitt trigger enable 0: Disabled	
							1: Enabled	
				[0]	DIECD DATAZ DI	1151	3X2/9X1	
				[8]	BIFSD_DATA7_PU	1'h1	PIN pull up enable 0: Disabled	
						***	1: Enabled	
				[7]	BIFSD_DATA7_PD	1'h0	Pin pull down enable	
				[,]	B.11 35 _57 (17 (1 _1 5	1110	0: Disabled	
						107.	1: Enabled	GPIC
				[6]	Reserved			
				[5:2]	BIFSD_DATA7_DS	4'h6	PIN Driving selector (typical value)	
							0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA	
							1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA7_FS	2'h0	PIN function selection	
							00: Normal function	
							01: LPWM3	
							10: RGB_DAT23	
							11: GPIO	



PIN Group	PIN_REG BASE_ADDR: 0xA600_4000									
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO		
QSPI	01E0H	QSPI_CSN1	RW				PIN configuration register	GPIO7[8]		
			[31:9 [8] [7] [6] [1:0]	[31:9]	Reserved					
				[8]	QSPI_CSN1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled			
				[7]	QSPI_CSN1_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up			
				[6]	QSPI_CSN1_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled			
				[5:2]	QSPI_CSN1_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA			
				[1:0]	QSPI_CSN1_FS	2'h3	PIN function selection 00: Normal function 01: SPI0_CSN1 10: N/A 11: GPIO			