X3M Register Reference Manual
I2C

Revision History

Revision	Date	Description
1.0	July-02-2020	Initial Release

I2Cx (x = 0, 1, 2, 3, 4, 5)	BASE_ADDR: 0xA5009000, 0xA500A000, 0xA500B000, 0xA500C000, 0xA5016000, 0xA5017000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
	00H	CONFIGURE	RW				I2C Configuration Register This register is used to configure the module enable signal and the internal sampling signal.
				[31:19]	Reserved		
				[18]	ACK	1'b0	ACK bit for non-transaction mode. When the TRANS_EN bit is set to 0, the I2C master works in non-transaction mode. This bit is used to respond with ACK/NACK to the slaves.
				[17]	DIR_RD	1'b0	Read operation without any subaddress write during transaction mode. When this bit is enabled, the RD bit of the Control register should be also enabled. For the EEPROM or sensor, the RD operation starts with a write to subaddress then followed by a read. When I2C communicates with such slaves, this bit should be set to 0.
				[16:12]	Reserved		
				[11]	TO_EN	1'h0	Timeout Check Enable. 0: Timeout check disabled. 1: Timeout check enabled.
				[10]	Reserved		
				[9]	TRANS_EN	1'b0	Transaction Mode Enable. 0: I2C master works in non-transaction mode. 1: I2C master works in transaction mode. Software is required to configure the register based on the selected transaction mode to prevent frequent interrupts.
				[8]	EN	1'h0	I2C Module Enable. 0: I2C module disabled. 1: I2C module enabled. The EN bit is cleared only when no transfer is in progress, for example, after a STOP command, or when the Control register has the STO bit set. If setting the EN bit to 0 when a transfer is ongoing, the I2C module will release the bus.
				[7:0]	SCL8F	8'h1d	The value for dividing i2c_mclk to generate SCL. SCL8F = f(i2c_mclk)/ (8 * f(SCL)) -1 The default frequency of i2c_mclk is 187.5MHz. It can be changed only when the EN bit is set to 0.
	04H	SLAVEADDR	RW				Slave Address Register This register is used to specify the I2C module 7-bit addresses or first 7-bit of 10-bit addresses for the I2C operations.
				[31:12]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	TEN_ADDR	1'h0	This bit is used to enable 10-bit addressing. 0: 7-bit addressing mode enabled. 1: 10-bit addressing mode enabled.
				[10:1]	SLAVEADDR	10'h0	Slave Address. The low bits[7:1] are for 7-bit addressing, and the bits[10:1] are for 10-bit addressing.
				[0]	Reserved		
	08H	DCOUNT	RW				Data Count Register This register is used to control the number of bytes in the I2C data transfer.
				[31:16]	RDCOUNT	16'h0	Read Data Count. The maximum data read count is 65535. 0 means no data to be read.
				[15:0]	WDCOUNT	16'h0	Write Data Count. The maximum is 65535. 0 means no data to be written.
	0CH	CONTROL	RW				Control Register The I2C module can respond to new commands only when the EN bit of the CONFIGURE register is set to 1.
				[31:8]	Reserved		
				[7]	TXFIFO_CLR	1'h0	This bit is used to clear the TX FIFO in transaction mode. This bit automatically clears itself after the TX FIFO is cleared.
				[6]	RXFIFO_CLR	1'h0	This bit is used to clear the RX FIFO in transaction mode. This bit automatically clears itself after the RX FIFO is cleared.
				[5]	STA	1'h0	Start Condition. 0: No start (S) condition generated and detected on the bus. 1: Start (S) condition generated and detected on the bus. This bit automatically clears itself after the programmed start condition on the bus is generated and detected. It works only when the EN bit is enabled.
				[4]	STO	1'h0	Stop Condition. 0: No stop (P) condition generated and detected on the bus. 1: Stop (P) condition generated and detected on the bus. This bit automatically clears itself after the programmed stop condition on the bus is generated and detected. It works only when the EN bit is enabled.
				[3]	WR	1'h0	Write Operation. This bit is set when I2C write operations are required. This bit automatically clears itself after the write operation is complete. It works only when the EN bit is enabled.

I2Cx (x = 0, 1, 2, 3, 4, 5)

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[2]	RD	1'h0	Read Operation. This bit is set when I2C read operations are required. When the DIR_RD bit of the CONFIGURE register is enabled, the RD bit should be enabled. This bit automatically clears itself after the write read operation is complete. It works only when the EN bit is enabled.
			[1:0]	Reserved		
10H	TX_DATA	RW				Transmit Data Register
			[31:8]	Reserved		
			[7:0]	TX_DATA	8'h0	Transmit Data. For non-transaction mode, it is the I2C TX DATA sent. For transaction mode: It is the end point/entry point for ARM to write data to FIFO. Writing to a full FIFO will return an error.
14H	RX_DATA	RO				Receive Data Register
			[31:8]	Reserved		
			[7:0]	RX_DATA	8'h0	Receive data. For non-transaction mode, it is the I2C RX DATA received. For transaction mode: This register is the end point/entry point for ARM to read data from FIFO. Reading from an empty FIFO (i.e. at reset) will return an error.
18H	STATUS	RO				Status Register
			[31:7]	Reserved		
			[6]	TXFIFO_EMPTY	1'h1	Status of TX FIFO empty. 0: Inactive. 1: Active.
			[5]	TXFIFO_FULL	1'h0	Status of TX FIFO full. 0: Inactive. 1: Active.
			[4]	RXFIFO_EMPTY	1'h1	Status of RX FIFO empty. 0: Inactive. 1: Active.
			[3]	RXFIFO_FULL	1'h0	Status of RX FIFO full. 0: Inactive. 1: Active.
			[2]	AL	1'h0	Status of arbitration lost. 0: Inactive. 1: Active.

I2Cx (x = 0, 1, 2, 3, 4, 5)

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[1]	RXACK	1'h1	RX ACK from slave. 0: Inactive. 1: Active.
			[0]	BB	1'h0	Status of bus busy. This bit reflects the status of I2C bus that is determined by all the devices on the I2C bus. This bit is set to 1 when a START condition on the bus is detected, and is set to 0 when a STOP condition on the bus is detected.
1CH	TO_COUNT	RW				Timeout Counter Register
			[31:16]	Reserved		
			[15:0]	TO_COUNT	16'hFFFF	If the I2C master detects the SCK has been pulled down for the TO_COUNT bit, an timeout interrupt will be generated. This bit only works when the TO_EN bit of the CONFIGURE register is set to 1.
20H	SRCPND	W1C				Interrupt Source Pending Register
			[31:8]	Reserved		
			[7]	STERR	1'h0	Stop Error. **Note:** This bit is applicable to both normal transaction mode and non-transaction mode. This bit is set to 1 when a STOP condition is sent out but the SDA and SCK read back don't show the STOP status. In that case, the SDA is held by the slave and software need to overdrive the SDA and SCK to HIGH to return the STOP condition. 0: No STOP error occurred. 1: STOP error interrupt occurred.
			[6]	TO	1'h0	Timeout. This bit is set to 1 when a transaction cannot be completed in the specified time. 0: No timeout error occurred. 1: Timeout error interrupt occurred.
			[5]	AERR	1'h0	Access Error. This bit is set to 1 if any of the following occurs: - A write access to the TX DATA register is performed by software while the TX FIFO is full. - A read access to the RX DATA register is performed by software while the RX FIFO is empty. A read to the empty RX FIFO returns the previous data read value. A write to the full TX FIFO is ignored. It is cleared to 0 after software writing 1 to this bit.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	XRDY	1'h0	Transmit Data Ready. This bit is set to 1 when the TX FIFO is changed to empty from non-empty status. This bit must be cleared after TX FIFO has loaded all the data. It is cleared to 0 after software writing 1 to this bit.
				[3]	RRDY	1'h0	Receive Data Ready. This bit is set to 1 when the RX FIFO is changed to full from non-full status. This bit must be cleared after the RX FIFO is empty. It is cleared to 0 after software writing 1 to this bit.
				[2]	TR_DONE	1'h0	Transaction/Byte Transfer Done. This bit is set to 1 when previous transaction is completed in transaction mode. This bit is set to 1 when previous byte transfer is finished in non-transaction mode. It is cleared to 0 after software writing 1 to this bit.
				[1]	NACK	1'h0	Non-acknowledgment. This bit is set to 1 when a non-acknowledgment has been received. The transfer is automatically ended by generating a stop condition on the bus. The TX and RX FIFOs must be cleared. The STA and STO are cleared by hardware. It is cleared to 0 after software writing 1 to this bit.
				[0]	Reserved		
	24H	INTMASK	RO				Interrupt Mask Register
				[31:8]	Reserved		
				[7]	STERR_MASK	1'h1	Mask for the stop error interrupt. 0: Unmasked. 1: Masked.
				[6]	TO_MASK	1'h1	Mask for the timeout interrupt. 0: Unmasked. 1: Masked.
				[5]	AERR_MASK	1'h1	Mask for the access error interrupt. 0: Unmasked. 1: Masked.
				[4]	XRDY_MASK	1'h1	Mask for the transmit data ready interrupt. 0: Unmasked. 1: Masked.
				[3]	RRDY_MASK	1'h1	Mask for the receive data ready interrupt. 0: Unmasked. 1: Masked.
				[2]	TR_DONE_MASK	1'h1	Mask for the transaction done interrupt. 0: Unmasked. 1: Masked.

I2Cx (x = 0, 1, 2, 3, 4, 5)

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[1]	NACK_MASK	1'h1	Mask for the non-acknowledgment interrupt. 0: Unmasked. 1: Masked.
			[0]	AL_MASK	1'h1	Mask the arbitration Lost interrupt. 0: Unmasked. 1: Masked.
28H	INTSETMASK	WO				Interrupt Set Mask Register
			[31:8]	Reserved		
			[7]	STERR_SETMASK	1'h0	Sets mask for the stop error interrupt. 0: No effect. 1: Masks the stop error interrupt.
			[6]	TO_SETMASK	1'h0	Sets mask for the timeout interrupt. 0: No effect. 1: Masks the timeout interrupt.
			[5]	AERR_SETMASK	1'h0	Sets mask for the access error interrupt. 0: No effect. 1: Masks the access error interrupt.
			[4]	XRDY_SETMASK	1'h0	Sets mask for the transmit data ready interrupt. 0: No effect. 1: Masks the transmit data ready interrupt.
			[3]	RRDY_SETMASK	1'h0	Sets mask for the receive data ready interrupt. 0: No effect. 1: Masks the receive data ready interrupt.
			[2]	TR_DONE_SETMASK	1'h0	Sets mask for the transaction/byte transfer done interrupt. 0: No effect. 1: Masks the transaction/byte transfer done interrupt.
			[1]	NACK_SETMASK	1'h0	Sets mask for the non-acknowledgement interrupt. 0: No effect. 1: Masks the non-acknowledgement interrupt.
			[0]	Reserved		
2CH	INTUNMASK	WO				Interrupt Unmask Register
			[31:8]	Reserved		
			[7]	STERR_UNMASK	1'h0	Used to unmask the stop error interrupt. 0: No effect. 1: Unmasks the stop error interrupt.

I2Cx (x = 0, 1, 2, 3, 4, 5)	BASE_ADDR: 0xA5009000, 0xA500A000, 0xA500B000, 0xA500C000, 0xA5016000, 0xA5017000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6]	TO_UNMASK	1'h0	Used to unmask the timeout interrupt. 0: No effect. 1: Unmasks the timeout interrupt.
				[5]	AERR_UNMASK	1'h0	Used to unmask the access error interrupt. 0: No effect. 1: Unmasks the access error interrupt.
				[4]	XRDY_UNMASK	1'h0	Used to unmask the transmit data ready interrupt. 0: No effect. 1: Unmasks the transmit data ready interrupt.
				[3]	RRDY_UNMASK	1'h0	Used to unmask the receive data ready interrupt. 0: No effect. 1: Unmasks the receive data ready interrupt.
				[2]	TR_DONE_UNMASK	1'h0	Used to unmask the transaction/byte transfer done interrupt. 0: No effect. 1: Unmasks the transaction/byte transfer done interrupt.
				[1]	NACK_UNMASK	1'h0	Used to unmask the non-acknowledgement interrupt. 0: No effect. 1: Unmasks the non-acknowledgement interrupt.
				[0]	Reserved		
	34H	FIFO_CTRL	RW				FIFO Control Register This register is used for system debugging.
				[31:2]	Reserved		
				[1]	RX_FULL_HOLD	1'b0	Holds the RX FIFO full signal to stall the I2C until the RX FIFO is read out. 1: The RX FIFO Full signal is held. 0: The RX FIFO Full signal is released.
				[0]	TX_EMPTY_HOLD	1'b0	Holds the TX FIFO empty signal to stall the I2C until the TX FIFO is filled. 1: The TX FIFO empty signal is held. 0: The TX FIFO empty signal is released.