X3M Register Reference Manual
I2S

Revision History

Revision	Date	Description
1.0	August-31-2020	Initial Release

I2Sx (x = 0, 1) RX Function

BASE_ADDR: 0xA5007000, 0xA5008000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	AUD_CTL	RW				Control information register
			[31]	rx_test	1'h0	Enable Test. Receiver test mode is used to test if it works normally. When enabling test mode, audio must be configured as follows: - I2S_mode. - 16-bit. - 4 channels at maximum. - 2nd edge.
			[30:3]	Reserved		
			[2]	imem_clear	1'h0	Clear internal memory (SRAM). It lasts for only 1 bit clock cycle and then cleared by hardware automatically. It is used to protect from incorrect operation: 0: No effect. 1: Clears internal buffer.
			[1]	imem_en	1'h0	Internal memory (SRAM) is enabled or disabled to store received audio data in Receiver (fetch of audio data in Transmitter): 0: Disabled. 1: Enabled.
			[0]	enable	1'h0	Receiver/Transmitter enable. Transmitter/Receiver is not working if this bit is set to 0, SW can set 1 to this bit after configuring AUD_MODE, AUD_WS_DIV, AUD_MEM_FORMAT, AUD_ADDR* and AUD_BUF* registers: 0: Audio RX is disabled, I2S bus data will be ignored by RX. 1: Audio RX is enabled.
04H	AUD_MODE	RW				I2S/DSP interface mode selection register
			[31:8]	Reserved		
			[7]	lr_ws	1'h0	Polarity of ws signal on I2S Serial Interface to embedded audio codec: 0: ws low level indicates left channel, and ws high level indicates right channel. 1: ws low level indicates right channel, and ws high level indicates left channel. **Note:** For DSP Serial Interface, set lr_ws_in must equals 1'b0.
			[6]	first_edge	1'h0	For both master and slave modes, this bit indicates when to capture the first serial data on I2S/DSP Serial Interface: 0: Begins to capture serial data on the 2nd serial clk edge after ws transition. 1: Begins to capture serial data on the 1st serial clk edge after ws transition.
			[5]	word_len	1'h0	Word length of serial data on I2S/DSP Serial Interface： 0: 8-bit. 1: 16-bit.

I2Sx (x = 0, 1) RX Function

BASE_ADDR: 0xA5007000, 0xA5008000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[4:2]	ch_num	3'h00	Channel number: 3'b000: 2 channels. 3'b001: 4 channels. 3'b010: 8 channels. 3'b011: 16 channels. 3'b100: 1 channel.
			[1]	i2s_dsp_mode	1'h0	I2S/DSP mode selection: 0: I2S mode. 1: DSP mode.
			[0]	ms_mode	1'h0	Master or slave mode selection: 0: Master mode. 1: Slave mode.
08H	AUD_DIV_WS	RW				Divider of ws on I2S/PCM Serial Interface. **Note:** Sample Rate = Fws = Fsclk/(div_ws_l+div_ws_h+2) For I2S Serial Interface: div_ws_l+1 = div_ws_h+1 and greater than or equal to word_len*chn/2 is a basic requirement. div_ws_l = div_ws_h = 127 is a recommended configuration (Fsclk=256*Fws). For DSP Serial Interface: div_ws_h = 0, div_ws_l+2 greater than or equal to word_len*chn is a basic requirement. div_ws_h = 0, div_ws_l = 254 is a recommended configuration (Fsclk=256*Fws).
			[31:16]	Reserved		
			[15:8]	div_ws_h	8'h7f	High level of ws lasts (div_ws_h+1) sclk cycles in one ws period.
			[7:0]	div_ws_l	8'h7f	Low level of ws lasts (div_ws_l+1) sclk cycles in one ws period.
0CH	AUD_CH_EN	RW				Channel enable register for storing to system memory - For AUD0, [15:0] is used, [31:16] is reserved. - For AUD1/2/3, [3:0] is used, [31:4] is reserved. - For AUD4, [1:0] is used, [31:2] is reserved.
			[31:16]	Reserved		

I2Sx (x = 0, 1) RX Function	BASE_ADDR: 0xA5007000, 0xA5008000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:0]	chxx_en	1'h0	This bit indicates whether channel n is enabled, if disabled, it will be discarded: 0: Disabled. 1: Enabled. Bit[n] means channel n: [15]: Channel 15. [14]: Channel 14. ... [0]: Channel 0.
	20H	AUD_BUF_SIZE	RW				Buffer size register for each channel
				[31:0]	buf_size	31'h0	Buffer size in system memory allocated for each channel, its unit is Byte. (16 byte boundary)
	24H	AUD_BUF0_ADDR	RW				BUF0 start address register
				[31:0]	buf0_addr		BUF0 start address in system memory.
	28H	AUD_BUF0_RDY	RW				BUF0 ready indicator register
				[31:1]	Reserved	16'h0	
				[0]	buf0_rdy	16'h0	Ready indicator for buffer 0 in system memory, active high: 0: Not ready. 1: Ready.
	2CH	AUD_BUF1_ADDR	RW				Buffer 1 start address register
				[31:0]	buf1_addr		Buffer 1 start address in system memory.
	30H	AUD_BUF1_RDY	RW				Buffer 1 ready indicator register
				[31:1]	Reserved	16'h0	
				[0]	buf1_rdy	16'h0	Ready indicator for buffer 1 in system memory, active high: 0: Not ready. 1: Ready.
	34H	AUD_BUF_CUR_ADDR	RO				Start address of current buffer register
				[31:0]	buf_cur_addr	16'h0	Start address of current buffer in system memory.
	38H	AUD_CH_ERROR	RO				Overflow error indicator for channel 0 to channel 15
				[31:16]	Reserved	16'h0	

I2Sx (x = 0, 1) RX Function

BASE_ADDR: 0xA5007000, 0xA5008000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	chxx_error	1'h0	Overflow error indicator for channel 0 to channel 15: 0: No error. 1: Error. Bit[n] means channel n: [15]: Channel 15. [14]: Channel 14. ... [0]: Channel 0.
3CH	AUD_CH0_FRAME_LEN	RW				Channel 0 frame length register
			[31:0]	ch0_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio recover reaches the length of channel 0.
40H	AUD_CH1_FRAME_LEN	RW				Channel 1 frame length register
			[31:0]	ch1_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 1.
44H	AUD_CH2_FRAME_LEN	RW				Channel 2 frame length register
			[31:0]	ch2_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 2.
48H	AUD_CH3_FRAME_LEN	RW				Channel 3 frame length register
			[31:0]	ch3_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 3.
4CH	AUD_CH4_FRAME_LEN	RW				Channel 4 frame length register
			[31:0]	ch4_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 4.
50H	AUD_CH5_FRAME_LEN	RW				Channel 5 frame length register
			[31:0]	ch5_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 5.
54H	AUD_CH6_FRAME_LEN	RW				Channel 6 frame length register
			[31:0]	ch6_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 6.
58H	AUD_CH7_FRAME_LEN	RW				Channel 7 frame length register
			[31:0]	ch7_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 7.
5CH	AUD_CH8_FRAME_	RW				Channel 8 frame length register

I2Sx (x = 0, 1) RX Function

BASE_ADDR: 0xA5007000, 0xA5008000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	LEN		[31:0]	ch8_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 8.
60H	AUD_CH9_FRAME_LEN	RW				Channel 9 frame length register
			[31:0]	ch9_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 9.
64H	AUD_CH10_FRAME_LEN	RW				Channel 10 frame length register
			[31:0]	ch10_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 10.
68H	AUD_CH11_FRAME_LEN	RW				Channel 11 frame length register
			[31:0]	ch11_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 11.
6CH	AUD_CH12_FRAME_LEN	RW				Channel 12 frame length register
			[31:0]	ch12_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 12.
70H	AUD_CH13_FRAME_LEN	RW				Channel 13 frame length register
			[31:0]	ch13_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 13.
74H	AUD_CH14_FRAME_LEN	RW				Channel 14 frame length register
			[31:0]	ch14_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 14.
78H	AUD_CH15_FRAME_LEN	RW				Channel 15 frame length register
			[31:0]	ch15_frame_len	32'h0	Audio receiver will inform AVSYNC to record the PTS value, when the transmitted data to memory though audio receiver reaches the length of channel 15.
80H	AUD_SRCPND	RW				Interrupt status register
			[31:4]	Reserved		
			[3]	rx_buf1_trf_done	1'h0	Data transfer done interrupt from AUD(*) indicates all channels of AUD0 have been stored to the buffer 1 in system memory, active high. Writing 1'b1 will clear the corresponding bit.
			[2]	rx_buf0_trf_done	1'h0	Data transfer done interrupt from AUD(*) indicates all channels of AUD0 have been stored to the buffer 0 in system memory, active high. Writing 1'b1 will clear the corresponding bit.
			[1]	rx_overflow	1'h0	Buffer 0 and buffer 1 of AUD(*) are filled with more data than its fixed size, and are not able send all enabled audio channels in time, active high. Writing 1'b1 will clear the corresponding bit.

I2Sx (x = 0, 1) RX Function	BASE_ADDR: 0xA5007000, 0xA5008000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	rx_not_ready	1'h0	Buffer 0 and buffer 1 of AUD(*) are overflow because the buffer is not ready, active high. Writing 1'b1 will clear the corresponding bit.
	84H	AUD_INTMASK	RO				Interrupt mask status register
				[31:4]	Reserved		
				[3:0]	intmask	4'hf	Interrupt mask status of AUD_SRCPND. AUD_INTMASK[i] indicates the current mask status of AUD_SRCPND[i]. Each bit: 0: Unmasked. 1: Masked.
	88H	AUD_SETMASK	WO				Interrupt setmask register
				[31:4]	Reserved		
				[3:0]	setmask		Unmasks the interrupt of AUD_SRCPND. Writing 1'b1 to AUD_SETMASK[i] will mask AUD_SRCPND[i] to prevent the 2nd-level interrupts to IRQ Controller. Writing 1'b0 to AUD_SETMASK[i] will take no effect. Each bit: 0: No effect. 1: Masks the corresponding interrupt.
	8CH	AUD_UNMASK	WO				Interrupt unmask register
				[31:4]	Reserved		
				[3:0]	unmask		Unmasks the interrupt of AUD_SRCPND. Writing 1'b1 to AUD_UNMASK[i] will unmask AUD_SRCPND[i] to allow the 2nd-level interrupts to IRQ Controller. Writing 1'b0 to AUD_UNMASK[i] will take no effect. Each bit: 0: No effect. 1: Unmasks the corresponding interrupt.

I2Sx (x = 0, 1) TX Function

BASE_ADDR: 0xA5007500, 0xA5008500

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	AUD_CTL	RW				Control information register
			[31:3]	Reserved		
			[2]	imem_clear	1'h0	Clear internal memory (SRAM). It lasts for only 1 bit clock cycle and then cleared by hardware automatically. It is used to protect from incorrect operation. 0: No effect. 1: Clears internal buffer.
			[1]	imem_en	1'h0	Internal memory (SRAM) is enabled or disabled to store received audio data in Receiver (fetch of audio data in Transmitter). 0: Disabled. 1: Enabled.
			[0]	enable	1'h0	Control Receiver/Transmitter enable. Transmitter/Receiver is not working if this bit is set to 0, SW can set 1 to this bit after configuring AUD_MODE, AUD_WS_DIV, AUD_MEM_FORMAT, AUD_ADDR* and AUD_BUF* registers. 0: Audio TX is disabled, TX will not send data to I2S bus. 1: Audio TX is enabled.
04H	AUD_MODE	RW				I2S/DSP interface mode register
			[31:10]	Reserved		
			[9]	clk_edge	1'h0	Clock edge selection for capturing ws. Horizon recommends using default value for master mode, and setting this bit to '1' for slave mode. 0: clkn is used. 1: clk is used.
			[8]	copy_zero_sel	1'h0	For the disabled channel by ch_en, when ch_num equals two channels, this bit means the audio interface data of disabled channel is copied to the enabled channel or treated as zero. 0: Zero 1: Copy
			[7]	lr_ws	1'h0	Polarity of ws signal on I2S Serial Interface to embedded audio codec: 0: ws low level indicates left channel, and ws high level indicates right channel. 1: ws low level indicates right channel, and ws high level indicates left channel. **Note:** For DSP Serial Interface, set lr_ws_in must equals 1'b0.
			[6]	first_edge	1'h0	For both master and slave modes, this bit indicates when to capture the first serial data on I2S/DSP Serial Interface: 0: Begins to capture serial data on the 2nd serial clk edge after ws transition. 1: Begins to capture serial data on the 1st serial clk edge after ws transition.

I2Sx (x = 0, 1) TX Function

BASE_ADDR: 0xA5007500, 0xA5008500

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[5]	word_len	1'h0	Word length of serial data on I2S/DSP Serial Interface: 0: 8-bit. 1: 16-bit.
			[4:3]	Reserved	2'h00	
			[2]	ch_num	1'h0	Channel number: 0: 2 channels. 1: 1 channel.
			[1]	i2s_dsp_mode	1'h0	I2S/DSP mode selection: 0: I2S mode. 1: DSP mode.
			[0]	ms_mode	1'h0	Master or slave mode selection: 0: Master mode. 1: Slave mode.
08H	AUD_DIV_WS	RW				Divider of ws on I2S/PCM Serial Interface. **Note:** Sample Rate = Fws = Fsclk/(div_ws_l+div_ws_h+2) For I2S Serial Interface: div_ws_l+1 = div_ws_h+1 and greater than or equal to word_len*chn/2 is a basic requirement. div_ws_l = div_ws_h = 127 is a recommended configuration (Fsclk=256*Fws). For DSP Serial Interface: div_ws_h = 0, div_ws_l+2 greater than or equal to word_len*chn is a basic requirement. div_ws_h = 0, div_ws_l = 254 is a recommended configuration (Fsclk=256*Fws).
			[31:16]	Reserved		
			[15:8]	div_ws_h	8'h7f	High level of ws lasts (div_ws_h+1) sclk cycles in one ws period.
			[7:0]	div_ws_l	8'h7f	Low level of ws lasts (div_ws_l+1) sclk cycles in one ws period.
0CH	AUD_CH_EN	RW				Channel enable register for storing to system memory
			[31:2]	Reserved		
			[1]	ch1_en	1'h0	This bit indicates whether channel 1 is enabled, if disabled, it will be discarded. 0: Disabled. 1: Enabled.
			[0]	ch0_en	1'h0	This bit indicates whether channel 0 is enabled, if disabled, it will be discarded. 0: Disabled. 1: Enabled.
20H	AUD_BUF_SIZE	RW				Buffer size register for each channel

I2Sx (x = 0, 1) TX Function

BASE_ADDR: 0xA5007500, 0xA5008500						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[31:0]	buf_size	31'h0	Buffer size in system memory allocated for each channel, its unit is Byte. (16 byte boundary)
24H	AUD_BUF0_ADDR	RW				Buffer 0 start address register
			[31:0]	buf0_addr		Buffer 0 start address in system memory.
28H	AUD_BUF0_RDY	RW				Buffer 0 ready indicator register
			[31:1]	Reserved		
			[0]	buf0_rdy	1'h0	Ready indicator for buffer 0 in system memory, active high: 0: Not ready. 1: Ready.
2CH	AUD_BUF1_ADDR	RW				Buffer1 start address register
			[31:0]	buf1_addr		Buffer1 start address in system memory.
30H	AUD_BUF1_RDY	RW				Buffer1 ready indicator register
			[31:1]	Reserved		
			[0]	buf1_rdy	1'h0	Ready indicator for buffer 1 in system memory, active high: 0: Not ready. 1: Ready.
34H	AUD_BUF_CUR_ADDR	RO				Start address of current buffer register
			[31:0]	buf_cur_addr	32'h0	Start address of current buffer in system memory.
38H	AUD_ERROR	RO				Underflow error indicator register
			[31:2]	Reserved		
			[1]	ch1_error	1'h0	Underflow error indicator for channel 1: 0: No error. 1: Error.
			[0]	ch0_error	1'h0	Underflow error indicator for channel 0: 0: No error. 1: Error.
80H	AUD_SRCPND	RW				Interrupt status register
			[31:4]	Reserved		
			[3]	tx_buf1_trf_done	1'h0	Data transfer done interrupt indicator from AUD6 indicates all channels of AUD5 have fetched out data from the buffer 1 in system memory, active high. Writing 1'b1 will clear the corresponding bit.
			[2]	tx_buf0_trf_done	1'h0	Data transfer done interrupt indicator from AUD6 indicates all channels of AUD5 have fetched out data from the buffer 0 in system memory, active high. Writing 1'b1 will clear the corresponding bit.

I2Sx (x = 0, 1) TX Function	BASE_ADDR: 0xA5007500, 0xA5008500						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	tx_buf_underflow	1'h0	Buffer 0 and buffer 1 of AUD(*) are empty after audio is enabled, active high. Writing 1'b1 will clear the corresponding bit.
				[0]	tx_buf_not_ready	1'h0	Buffer 0 and buffer 1 of AUD(*) are overflow because the buffer is not ready, active high. Writing 1'b1 will clear the corresponding bit.
	84H	AUD_INTMASK	RO				Interrupt mask status register
				[31:4]	Reserved		
				[3:0]	intmask	4'hf	Interrupt mask status of AUD_SRCPND. AUD_INTMASK[i] indicates the current mask status of AUD_SRCPND[i]. Each bit: 0: Unmasked. 1: Masked.
	88H	AUD_SETMASK	WO				Interrupt setmask register
				[31:4]	Reserved		
				[3:0]	setmask		Unmasks the interrupt of AUD_SRCPND. Writing 1'b1 to AUD_SETMASK[i] will mask AUD_SRCPND[i] to prevent the 2nd-level interrupts to IRQ Controller. Writing 1'b0 to AUD_SETMASK[i] will take no effect. Each bit: 0: No effect. 1: Masks the corresponding interrupt.
	8CH	AUD_UNMASK	WO				Interrupt unmask register
				[31:4]	Reserved		
				[3:0]	unmask		Unmasks the interrupt of AUD_SRCPND. Writing 1'b1 to AUD_UNMASK[i] will unmask AUD_SRCPND[i] to allow the 2nd-level interrupts to IRQ Controller. Writing 1'b0 to AUD_UNMASK[i] will take no effect. Each bit: 0: No effect. 1: Unmasks the corresponding interrupt.