X3M Register Reference Manual
SPI

Revision History

Revision	Date	Description
1.0	July-15-2020	Initial Release.
1.1	April-27-2021	In the DMA_CTRL1register, updated the descritpion of the RX_DMA_ABORT bit.

SPIx (x = 0, 1, 2)

BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	TX	WO				Data Transmit Register
			[31:16]	Reserved		
			[15:0]	TX	8'h0	SPI TX data sent.
04H	RX	RO				Data Receive Register
			[31:16]	Reserved		
			[15:0]	RX	8'h0	SPI RX data received.
08H	CTRL	RW				SPI Control Register
			[31]	Reserved		
			[30]	SLAVE_SEL	1'h0	SPI Slave Select. This bit is used to select which slave to send data to. 0: Selects slave0, default. 1: Selects slave1. **Note:** SPI0 supports 2 slaves. SPI1 and SPI2 currently only support 1 slave.
			[29:28]	SAMP_CNT	2'h0	Sampling Delay Count. It is used to select the number of the delayed spi_clk samplings. 00: 1 delayed spi_clk sampling. 01: 2 delayed spi_clk sampling. 10: 3 delayed spi_clk sampling. 11: 4 delayed spi_clk sampling.
			[27]	SAMP_SEL	1'h1	Sampling Delay Select. 0: Data is sampled using SPI protocol in Master mode. Data is sent out right after the TX sampling edge in Slave mode. 1: Data is sampled using sampling delay method in Master Mode. Data is sent out right after the RX sampling edge in Slave mode.
			[26]	DW_SEL	1'h0	Data width for LSB or MSB in master mode only. When 16-bit width is selected, the TX and RX registers will also be 16-bit width. 0: 8-bit width. 1: 16-bit width.
			[25]	TX_FIFOE	1'h0	Enables transmit data to come from FIFO. 0: The transmitted data is feeded through APB with the TX register. 1: The transmitted data comes from TX FIFO.
			[24]	RX_FIFOE	1'h0	Enables the received data to be written to the RX FIFO. 0: The received data is stored in the RX register. 1: The received data is written to the RX FIFO.
			[23]	TX_DIS	1'h1	Transmit Empty Control. 0: The transmission stops when the TX FIFO is empty. 1: The transmission continues when the TX FIFO is empty.
			[22]	RX_DIS	1'h1	Receive Ready Control. 0: The receiving stops when the RX ready occurs. 1: The receiving continues when the RX ready occurs.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[21]	MS_MODE	1'h0	This bit is used to select Master/Slave mode. 0: Master mode. 1: Slave mode.
				[20]	PHASE	1'h0	0: The first edge of SCLK after the SSN high-to-low transition is the capture edge. 1: The second edge of SCLK after the SSN high-to-low transition is the capture edge.
				[19]	POLARITY	1'h0	This bit is used to set SCLK polarity. 0: SCLK keeps low when SSN is invalid. 1: SCLK keeps high when SSN is invalid.
				[18]	LSB	1'h0	This bit is used to select LSB first or MSB first. If this bit is set, the LSB of the TX register (TX[0] bit) is sent first to the line, and the first bit received from the line is put in the LSB of the RX register (RX[0] bit). If this bit is cleared, the MSB is transmitted/received first. 0: MSB first. 1: LSB first.
				[17]	SSAL	1'h0	This bit indicates the active level of SSN. 0: SSN is active low. 1: SSN is active high.
				[16]	SPI_EN	1'h0	SPI Core Enable. 0: SPI logic disabled. 1: SPI logic enabled.
				[15:0]	DIVIDER	16'h0	The divider value for SPI clock. It is the frequency divider value of SPI_CLK to generate the SCLK in master mode. The desired SCLK frequency is calculated as follows: FSCLK = FSPI_CLK/(2*(Divider+1)).
	0CH	SS	RW				SSN Limit Configure Register This register is only used in master mode. This register cannot be written when SPI is transferring data. This register can only be written when the TIP bit of the SFSR register is 0.
				[31:12]	Reserved		
				[11:8]	PRE_LIMIT	4'h4	The number of SCLK cycles from SSN being active to the first edge of SCLK.
				[7:4]	POS_LIMIT	4'h4	The number of SCLK cycles from the last edge of SCLK to SSN being inactive.
				[3:0]	SSH_LIMIT	4'h4	The number of SCLK cycles from SSN being inactive to SSN being active.
	10H	SFSR	RO				SPI Status Register
				[31:16]	Reserved		
				[17]	TX_RST_DONE	1'h0	Asynchronous TX FIFO Reset Done. 0: No effect. 1: Done.
				[16]	RX_RST_DONE	1'h0	Asynchronous RX FIFO Reset Done. 0: No effect. 1: Done.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15]	TX_QUE_DONE	1'h0	TX query for DMA TX_SIZE operation done. 0: No effect. 1: Done.
				[14]	TX_TER_DONE	1'h0	TX Termination Done. It indicates the TX_DMA_ABORT operation has completed. 0: No effect. 1: Done.
				[13]	RX_QUE_DONE	1'h0	RX Query for DMA RX_SIZE Operation Done. 0: No effect. 1: Done.
				[12]	RX_FLUSH_DONE	1'h0	RX Flush Done. It indicates the RX_FLUSH operation is done. 0: No effect. 1: Done.1: Done.
				[11]	RX_TER_DONE	1'h0	RX Termination Done. It indicates the RX_DMA_ABORT operation has completed. 0: No effect. 1: Done.
				[10]	TX_BG_INDEX	1'h0	Current Buffer Group Index for TX DMA with Ping-Pong buffering.
				[9]	RX_BG_INDEX	1'h0	Current Buffer Group Index for RX DMA with Ping-Pong buffering.
				[8]	TIP	1'h0	SPI Transfer in Progress Flag. 0: SPI is in idle state. 1: SPI is transferring data. Software should check this bit before starting SPI transfer.
				[7]	TXDON	1'h0	SPI Transmit DMA Request Enable. 0: No effect. 1: SPI transmitter is sending a DMA request, but has not gotten a reply from AXI.
				[6]	RXDON	1'h0	SPI Receive DMA Request Enable. 0: No effect. 1: SPI receiver is sending a DMA request, but has not gotten a reply from AXI.
				[5]	TF_EMPTY	1'h1	Transmit Register Empty Flag. 0: Transmit register is not empty. 1: Transmit register is empty. If the SPI_EN bit of the CTRL register is set to 0, this bit will be forced to 1.
				[4]	DATA_RDY	1'h0	The value 1 indicates the received data ready in the receiver register. This bit is changed to 0 after software reads the RX register. This bit is set to 1 when the received data is loaded from the shift register to the RX register.
				[3:0]	Reserved		
	14H	RFTO	RW				Receiver Timeout Threshold Register This register cannot be written when SPI is transferring data. This register can only be written when the TIP bit of the SFSR register is set to 0.

SPIx (x = 0, 1, 2)

BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[31:15]	Reserved		
			[16:0]	RFTO	17'hfffff	[16]: Receiver timeout enable. 0: RX timeout disabled. 1: RX timeout enabled. [15:0]: Sets the threshold of receiver timeout. When the SPI_EN bit of the CTRL register and the RX timeout enable bit of the RFTO register is set to 1, if SPI doesn't receive any data within the threshold time, then the receiver timeout occurs. The threshold time = RFTO * spi_clk. If timeout occurs, SPI will generate an RX_TIMEOUT interrupt. **Note:** RFTO*spi_clk should be greater than the period of SCLK and the period between sampling SCLK edge and the SSN asserting/disasserting edge.
18H	TLEN	RW				Transfer Length Register This register is only used in master mode. This register cannot be written when SPI is transferring data. This register can only be written when the TIP bit of the SFSR register is set to 0.
			[31:24]	Reserved		
			[23:0]	TLEN	24'h8	The number of bits will be transferred in one transfer. SSN being active once means one transfer. The maximum transfer length of one transfer is 2M bytes. **Note:** The instruction bits are not included in TLEN. If TLEN is not a length of multiples of 8, software should handle the last few bits handling. TLEN is only updated by writing to the CTRL register.
1CH	INSTRUCT	RW				Instruction Register This register cannot be written when SPI is transferring data. This register can only be written when the TIP bit of the SFSR register is set to 0.
			[31:0]	INSTRUCT	32'h0	The instruction before received or transmitted data. The instruction data must be aligned to the MSB of the register, for example, if the transmit instruction is 13'b0011_1100_0101_0, the register should be set to 32'b0011_1100_0101_0XXX_XXXX_XXXX_XXXX_XXXX. The X means 0 or 1. The length of the instruction is variable, please refer to the INST_MASK register.
20H	INST_MASK	RW				Instruction Mask Register This register cannot be written when SPI is transferring data. This register can only be written when the TIP bit of the SFSR register is set to 0.
			[31:0]	INST_MASK	32'hffff_ffff	Mask for the INSTRUCT register. 0: Unmasked. 1: Masked. For example, if the transmit instruction is '13b'0011_1100_0101_0', the INST_MASK register should be set to 32'h0007_FFFF.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	24H	SPI_SRCPND	W1C				SPI Interrupt Source Pending Register
				[31:11]	Reserved		
				[10]	DMA_TRDONE	1'h0	DMA Transaction Done. When the TLEN bits have been transmitted or received, this interrupt is generated in Master mode. In Slave mode, the interrupt will be generated once the master terminates the transfer by pulling up SSN. 0: DMA transaction is ongoing. 1: DMA transaction done.
				[9]	TX_BGDONE	1'h0	TX Buffer Group Done. It is only used for Ping-Pong buffering. When the TX_BGDONE interrupt occurs, software should fill the memory if there are more data to transfer. 0: No TX buffer group done interrupt occurred. 1: TX current buffer memory transfer done.
				[8]	RX_BGDONE	1'h0	RX Buffer Group Done. It is only used for Ping-Pong buffering. When the RX current buffer memory done occurs, software should read received data from memory. 0: No buffer memory transfer done interrupt occurred. 1: RX current buffer memory transfer done.
				[7]	TX_EMPTY	1'h0	Synchronous TX FIFO Empty. When the data left in the synchronous TX FIFO is not greater than the threshold defined by TX_TH, the corresponding interrupt is generated. 0: No synchronous TX FIFO empty interrupt occurred. 1: Synchronous TX FIFO empty interrupt occurred.
				[6]	RX_FULL	1'h0	Synchronous RX FIFO Full. When the data filled in the synchronous RX FIFO is not less than the threshold defined by RX_TH, the corresponding interrupt is generated. 0: No synchronous RX FIFO full interrupt occurred. 1: Synchronous RX FIFO full interrupt occurred.
				[5]	RX_TIMEOUT	1'h0	Receiver Timeout. When no data is received for time threshold defined by RFTO, the receiver timeout interrupt is generated. In DMA mode, this signal triggers the FIFO flush and is generated after the FIFO flush done. 0: No RX timeout interrupt occurred.
				[4]	TX_DMA_ERR	1'h0	DMA error interrupt for transmission (from memory to SPI). 0: No TX DMA error occurred. 1: TX DMA error occurred.
				[3]	RX_DMA_ERR	1'h0	DMA error interrupt for receiving (from SPI to memory). 0: No RX DMA error occurred. 1: RX DMA error occurred.
				[2]	TEMPTY	1'h1	TX register empty indicator source pending. 0: No TX empty interrupt occurred. 1: TX empty interrupt occurred. Writing 1 to this register clears this bit.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	OE	1'h0	Overrun error indicator source pending. 0: No overrun occurred since last register reset. 1: When there are characters in the receiver buffer and shift register, if another character is starting to arrive, it will overwrite the data in the shift register and generate an OE interrupt, but the data in buffer will remain intact. Writing 1 to this register clears this bit.
				[0]	DR	1'h0	Data Ready (DR) Indicator. 0: No characters in the RX buffer. 1: At least one character has been received and is in the RX register and RX buffer. Writing 1 to this bit clears this bit.
	28H	SPI_INTMASK	RO				SPI Interrupt Mask Register
				[31:11]	Reserved		
				[10]	DMA_TRDONE	1'h1	Mask for the DMA transaction done interrupt. 0: Unmasked. 1: Masked.
				[9]	TX_BGDONE	1'h1	Mask for the TX DMA buffer group done interrupt. 0: Unmasked. 1: Masked.
				[8]	RX_BGDONE	1'h1	Mask for the RX DMA buffer group done interrupt. 0: Unmasked. 1: Masked.
				[7]	TX_EMPTY	1'h1	Mask for the TX FIFO empty interrupt. 0: Unmasked. 1: Masked.
				[6]	RX_FULL	1'h1	Mask for the RX FIFO full interrupt. 0: Unmasked. 1: Masked.
				[5]	RX_TIMEOUT	1'h1	Mask for the RX timeout interrupt. 0: Unmasked. 1: Masked.
				[4]	TX_DMA_ERR	1'h1	Mask for the TX DMA error interrupt. 0: Unmasked. 1: Masked.
				[3]	RX_DMA_ERR	1'h1	Mask for the RX DMA error interrupt. 0: Unmasked. 1: Masked.
				[2]	TEMPTY	1'h1	Mask for the TX register empty interrupt. 0: Unmasked. 1: Masked.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	OE	1'h1	Mask for the overrun error interrupt. 0: Unmasked. 1: Masked.
				[0]	DR	1'h1	Mask for the RX data ready interrupt. 0: Unmasked. 1: Masked.
	2CH	SPI_INTSETMASK	WO				SPI Interrupt Set Mask Register
				[31:11]	Reserved		
				[10]	DMA_TRDONE	1'h0	Sets mask for the DMA transaction done interrupt. 0: No effect. 1: Masks the DMA transaction done interrupt.
				[9]	TX_BGDONE	1'h0	Sets mask for the TX DMA buffer group done interrupt. 0: No effect. 1: Masks the TX DMA buffer group done interrupt.
				[8]	RX_BGDONE	1'h0	Sets mask for the RX DMA buffer group done interrupt. 0: No effect. 1: Masks the RX DMA buffer group done interrupt.
				[7]	TX_EMPTY	1'h0	Sets mask for the TX FIFO empty interrupt. 0: No effect. 1: Masks the TX FIFO empty interrupt.
				[6]	RX_FULL	1'h0	Sets mask for the RX FIFO full interrupt. 0: No effect. 1: Masks the RX FIFO full interrupt.
				[5]	RX_TIMEOUT	1'h0	Sets mask for the RX timeout interrupt. 0: No effect. 1: Masks the RX timeout interrupt.
				[4]	TX_DMA_ERR	1'h0	Sets mask for the TX DMA error interrupt. 0: No effect. 1: Masks the TX DMA error interrupt.
				[3]	RX_DMA_ERR	1'h0	Sets mask for the RX DMA interrupt. 0: No effect. 1: Masks the RX DMA interrupt.
				[2]	TEMPTY	1'h0	Sets mask for the TX register empty interrupt. 0: No effect. 1: Masks the TX register empty interrupt.
				[1]	OE	1'h0	Sets mask for the overrun error interrupt. 0: No effect. 1: Masks the overrun error interrupt.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	DR	1'h0	Sets mask for the RX data ready interrupt. 0: No effect. 1: Masks the RX data ready interrupt.
	30H	SPI_INTUNMASK	WO				SPI Interrupt Unmask Register
				[31:11]	Reserved		
				[10]	DMA_TRDONE	1'h0	Used to unmask the DMA transaction done interrupt. 0: No effect. 1: Unmasks the DMA transaction done interrupt.
				[9]	TX_BGDONE	1'h0	Used to unmask the TX DMA buffer group done interrupt. 0: No effect. 1: Unmasks the TX DMA buffer group done interrupt.
				[8]	RX_BGDONE	1'h0	Used to unmask the RX DMA buffer group done interrupt. 0: No effect. 1: Unmasks the RX DMA buffer group done interrupt.
				[7]	TX_EMPTY	1'h0	Used to unmask the TX FIFO empty interrupt. 0: No effect. 1: Unmasks the RX DMA group done interrupt.
				[6]	RX_FULL	1'h0	Used to unmask the RX FIFO full interrupt. 0: No effect. 1: Unmasks the RX FIFO full interrupt.
				[5]	RX_TIMEOUT	1'h0	Used to unmask the RX timeout interrupt. 0: No effect. 1: Unmasks the RX timeout interrupt.
				[4]	TX_DMA_ERR	1'h0	Used to unmask the TX DMA error interrupt. 0: No effect. 1: Unmasks the TX DMA error interrupt.
				[3]	RX_DMA_ERR	1'h0	Used to unmask the RX DMA error interrupt. 0: No effect. 1: Unmasks the RX DMA error interrupt.
				[2]	TEMPTY	1'h0	Used to unmask the TX register empty interrupt. 0: No effect. 1: Unmasks the TX register empty interrupt.
				[1]	OE	1'h0	Used to unmask the overrun error interrupt. 0: No effect. 1: Unmasks the overrun error interrupt.
				[0]	DR	1'h0	Used to unmask the RX data ready interrupt. 0: No effect. 1: Unmasks the RX data ready interrupt.
	34H	DMA_CTRL0	RW				DMA Control Register

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[31:18]	Reserved		
				[17:16]	Reserved		
				[15]	TX_APBSEL	1'h0	APB TX FIFO Access Select. This bit is used to enable the APB access to the TX FIFO directly. In this mode, the AXI interface is disabled and APB can directly write TX FIFO. 0: APB TX FIFO access disabled. 1: APB TX FIFO access enabled.
				[14]	TX_BG	1'h0	Buffer Group for TX Channel. If Ping-Pong buffering is required, this bit is set to 1. In that case, the two buffers have a size of TX_DMA_SIZE0 and TX_DMA_SIZE1 with start address of TX_DMA_ADDR0 and TX_DMA_ADDR1. 0: Single buffer group. 1: Two buffer groups if Ping-Pong buffering is required. **Note:** Do NOT change the TX_BG value during DMA transfer.
				[13:12]	TX_MAXOS	2'h1	Maximum outstanding transaction number for TX DMA mode. 00: 1. 01: 2. 10: 3. 11: 4. **Note:** Do NOT change the TX_MAXOS value during DMA transfer.
				[11]	TX_AL	1'h0	TX DMA Ping-Pong Buffering Auto Link. 0: Ping-Pong buffering is configured by software. 1: Ping-Pong buffering auto link.
				[10:9]	TX_BURST_LEN	2'h0	These bits specify the preferred burst length for the DMA TX (memory to SPI) transfer. Software doesn't need to reconfigure these bits even if the transfer_length isn't a length of multiples of BURST_LEN, the internal DMA can issue a request for AXI bus with the preferred burst length, and automatically adjust the burst length to complete the last data transfer. (a word equals 4 bytes) 00: 1-word. 01: 2-word. 10: 4-word. 11: 4-word. **Note:** Do NOT change the TX_BURST_LEN value during DMA transfer.
				[8:7]	Reserved	2'h0	
				[6]	RX_APBSEL	1'h0	APB RX Access FIFO Mode Select. This mode is used to enable the APB access the RX FIFO directly. In this mode, the AXI interface is disabled and APB can direclty write RX FIFO. 0: APB RX FIFO access disabled. 1: APB RX FIFO access enabled.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5]	RX_BG	1'h0	Buffer group for RX Channel. If Ping-Pong buffering is required, this register is set to 1. In that case, the two buffers have a size of RX_DMA_SIZE0 and RX_DMA_SIZE1 with start address of RX_DMA_ADDR0 and RX_DMA_ADDR1. 0: Single buffer group. 1: Two buffer groups if Ping-Pong buffering is required. Note: Do NOT change the RX_BG value during DMA transfer.
				[4:3]	RX_MAXOS	2'h1	Maximum outstanding transaction number for RX DMA mode. 00b: 1. 01b: 2. 10b: 3. 11b: 4. **Note:** Do NOT change the RX_MAXOS value during DMA transfer.
				[2]	RX_AL	1'h0	RX DMA Ping-Pong Buffering Auto Link. 0: Ping-Pong buffering is configured by software. 1: Ping-Pong buffering auto link.
				[1:0]	RX_BURST_LEN	2'h0	These bits specify the preferred burst length for DMA RX(SPI to memory) transfer. Software doesn't need to reconfigure these bits even if the transfer_length isn't a length of multiples of BURST_LEN, the internal DMA can issue a request for AXI bus with the preferred burst length, and automatically adjust the burst length to complete the last data transfer. (a word equals 4 bytes) 00: 1-word. 01: 2-word. 10: 4-word. 11: 4-word. **Note:** Do NOT change this register during DMA transfer.
	38H	DMA_CTRL1	RW				DMA Control Register
				[31:9]	Reserved		
				[8]	TX_DMA_ABORT	1'h0	This bit is used to abort the internal TX DMA transfer. Software writes 1 to this bit to trigger the host controller to abort the current data transfer, and then the host should write the TXFIFO_CLEAR bit of the FIFO_RESET register to reset the FIFO pointer. 0: No effect. 1: The internal TX DMA transfer is aborted.
				[7]	TX_DMA_STOP	1'h0	This bit is used to stop the TX DMA operation for Ping-Pong buffering mode. The current buffer is the final buffer. 0: No effect. 1: The TX DMA operation is stopped. The bit automatically clears itself after being stopped.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6]	TX_DMA_CFG	1'h0	This bit is used to configure the TX DMA address and size for a transfer. 0: No effect. 1: The TX DMA parameters are configured. The bit automatically clears itself after being set.
				[5]	TX_DMA_START	1'h0	This bit is used to start the SPI TX DMA operation. 0: No effect. 1: The TX DMA operation is started. This bit is set by CPU and cleared by SPI.
				[4]	RX_DMA_FLUSH	1'h0	This bit is used to flush the data into the memory if the transfer needs to be ended. 0: No effect. 1: RX FIFO is flushed. This bit is cleared by hardware after the RX DMA flush is done.
				[3]	RX_DMA_ABORT	1'h0	This bit is used to abort the internal RX DMA transfer. Software writes 1 to this bit to trigger the host controller to abort the current data transfer, and then the host should write the RXFIFO_CLEAR bit of the FIFO_RESET register to reset the FIFO pointer. 0: No effect. 1: The internal RX DMA transfer is aborted. This bit is cleared by hardware after the RX DMA termination is done.
				[2]	RX_DMA_STOP	1'h0	This bit is used to stop the RX DMA operation for Ping-Pong buffering mode. The current buffer is the final buffer. 0: No effect. 1: The RX DMA operation is stopped. The bit automatically clears itself after being stopped.
				[1]	RX_DMA_CFG	1'h0	This bit is used to configure the DMA address and size for a transfer. 0: No effect. 1: The RX DMA parameters are configured. The bit automatically clears itself after being set.
				[0]	RX_DMA_START	1'h0	This bit used to start the SPI RX DMA operation. 0: No effect. 1: The RX DMA operation is started. This bit is set by CPU and cleared by SPI.
	3CH	TX_DMA_ADDR0	RW	[31:0]	TX_DMA_ADDR0	32'h0	The memory start address of the TX DMA transfer (from memory to SPI) for Ping-Pong buffer group 0 . It can be changed when DMA accesses buffer group 1.
	40H	TX_DMA_SIZE0	RW	[31:24]	Reserved		
				[20:0]	TX_DMA_SIZE0	21'h0	The memory buffer size of the TX DMA transfer (from memory to SPI) for Ping-Pong buffer group 0. It is byte-aligned. It can be changed when DMA accesses buffer group 1.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	44H	TX_DMA_ADDR1	RW	[31:0]	TX_DMA_ADDR1	32'h0	The memory start address of the TX DMA transfer (from memory to SPI) for Ping-Pong buffer group 1. It can be changed when DMA accesses buffer group 0.
	48H	TX_DMA_SIZE1	RW	[31:24]	Reserved		
				[20:0]	TX_DMA_SIZE1	21'h0	The memory buffer size of the TX DMA transfer (from memory to SPI) for Ping-Pong buffer group 1. It is byte-aligned. It can be changed when DMA accesses buffer group 0.
	4CH	RX_DMA_ADDR0	RW	[31:0]	RX_DMA_ADDR0	32'h0	The memory start address of the RX DMA transfer (from SPI to memory) for Ping-Pong buffer group 0. It can be changed when DMA accesses buffer group 1.
	50H	RX_DMA_SIZE0	RW	[31:24]	Reserved		
				[20:0]	RX_DMA_SIZE0	21'h0	The memory buffer size of the RX DMA transfer (from SPI to memory) for Ping-Pong buffer group 0. It is byte-aligned. It can be changed when DMA access buffer group 1.
	54H	RX_DMA_ADDR1	RW	[31:0]	RX_DMA_ADDR1	32'h0	The memory start address of the RX DMA transfer (from SPI to memory) for Ping-Pong buffer group 1. It can be changed when DMA accesses buffer group 0.
	58H	RX_DMA_SIZE1	RW	[31:24]	Reserved		
				[20:0]	RX_DMA_SIZE1	21'h0	The memory buffer size of RX DMA transfer (from SPI to memory) for Ping-Pong buffer group 1. It is byte-aligned. It can be changed when DMA accesses buffer group 0.
	5CH	TX_SIZE	RO	[31:24]	Reserved		
				[20:0]	TX_SIZE	21'h0	The size of the current TX transfer. It is used to indicate how much data has been read from memory.
	60H	RX_SIZE	RO	[31:24]	Reserved		
				[20:0]	RX_SIZE	21'h0	The size of the current RX transfer. It is used to indicate how much data has been written to memory.
	64H	FIFO_RESET	RW				FIFO Soft Reset Register
				[31:9]	Reserved		
				[8]	SPI_ABORT	1'h0	SPI Transfer Abort. Writing 1 to this bit terminates the SPI transfer. It only lasts for 1 module clock cycle, and then is cleared by hardware automatically.
				[7]	TX_FIFOINT_DIS	1'h0	This bit is used to clear the synchronous TX FIFO empty interrupt. Writing 1 to this bit clears the TX FIFO empty interrupt. It only lasts for 1 module clock cycle, and then is cleared by hardware automatically.
				[6]	RX_FIFOINT_DIS	1'h0	This bit is used to clear the synchronous RX FIFO full interrupt. Writing 1 to this bit clears the RX FIFO full interrupt. It only lasts for 1 module clock cycle, and then is cleared by hardware automatically.

SPIx (x = 0, 1, 2)	BASE_ADDR: 0xA5004000, 0xA5005000, 0xA5006000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5]	RX_QUERY_EN	1'h0	This bit is used to query the RX_SIZE for the DMA transfer. 0: No effect. 1: Queries the RX_SIZE of the DMA transfer. It only lasts for 1 module clock cycle, and then is cleared by hardware automatically.
				[4]	TX_QUERY_EN	1'h0	This bit is used to query the TX_SIZE for the DMA transfer. 0: No effect. 1: Queries RX_SIZE of the DMA transfer. It only lasts for 1 module clock cycle, and then is cleared by hardware automatically.
				[3]	RXFIFO_SCLEAR	1'h0	This bit is used to reset the synchronous RX FIFO when an error occurs in the data read transfer. It only lasts for 1 module clock cycle, and then cleared by hardware automatically. 0: No effect. 1: Clears the synchronous RX FIFO.
				[2]	TXFIFO_SCLEAR	1'h0	This bit is used to reset the synchronous TX FIFO when an error occurs in the data write transfer. 0: No effect. 1: Clears the synchronous TX FIFO. It only lasts for 1 module clock cycle, and then cleared by hardware automatically.
				[1]	RXFIFO_CLEAR	1'h0	This bit is used to reset the RX FIFO when an error occurs in the data read transfer. 0: No effect. 1: Clears the RX FIFO. It only lasts for 1 module clock cycle, and then cleared by hardware automatically.
				[0]	TXFIFO_CLEAR	1'h0	This bit is used to reset the TX FIFO when an error occurs in the data write transfer. 0: No effect. 1: Clears the TX FIFO. It only lasts for 1 module clock cycle, and then cleared by hardware automatically.
	68H	TX_DMA_SIZE	RW	[31:21]	Reserved		
				[20:0]	TX_DMA_SIZE	21'h0	These bits are used to set total transfer size for SPI TX in Ping-Pong buffering mode. The SPI TX buffer is byte-aligned.
	6CH	RX_DMA_SIZE	RW	[31:21]	Reserved		
				[20:0]	RX_DMA_SIZE	21'h0	These bits are used to set total transfer size for SPI RX Ping-Pong buffering mode. The SPI RX buffer is byte-aligned.