X3M Register Reference Manual
Timer

Revision History

Revision	Date	Description
1.0	September-18-2020	Initial Release

Timer

BASE_ADDR: 0xA1002000, 0xA1003000, 0xA1004000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	TMREN	RO				Timer Status Register
			[31:3]	Reserved		
			[2]	Tmr2_enable	1'h0	Timer2 status signal: 0: Idle 1: Running
			[1]	Tmr1_enable	1'h0	Timer1 status signal: 0: Idle 1: Running
			[0]	Tmr0_enable	1'h0	Timer0 status signal: 0: Idle 1: Running
04H	TMRSTART	WO				Timer Start Register
			[31:3]	Reserved		
			[2]	Tmr2start	1'h0	Start timer2 Writing 1 to this bit will start the corresponding timer.
			[1]	Tmr1start	1'h0	Start timer1 Writing 1 to this bit will start the corresponding timer.
			[0]	Tmr0start	1'h0	Start timer0 Writing 1 to this bit will start the corresponding timer.
08H	TMRSTOP	WO				Timer Stop Register
			[31:3]	Reserved		
			[2]	Tmr2stop	1'h0	Stop timer2 Writing 1 to this bit will stop the corresponding timer.
			[1]	Tmr1stop	1'h0	Stop timer1 Writing 1 to this bit will stop the corresponding timer.
			[0]	Tmr0stop	1'h0	Stop timer0 Writing 1 to this bit will stop the corresponding timer.
0CH	TMRMODE	RW				Timer Mode Control Register 4 bits for each timer

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BASE_ADDR: 0xA1002000, 0xA1003000, 0xA1004000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[31:12]	Reserved		
			[11:8]	Tmr2_mode	4'h0	Timer2 mode 4'h0000: One-time mode (32-bit general-purpose timer) 4'h0001: Periodical mode (32-bit general-purpose timer) 4'h0010: Continuous mode (32-bit general-purpose timer) Others: Watchdog mode
			[7:4]	Tmr1_mode	4'h0	Timer1 mode 4'h0000: One-time mode (32-bit general-purpose timer) 4'h0001: Periodical mode (32-bit general-purpose timer) 4'h0010: Continuous mode (32-bit general-purpose timer) Others: Watchdog mode
			[3:0]	Tmr0_mode	4'h0	Timer0 mode 4'h0000: One-time mode (32-bit general-purpose timer) 4'h0001: Periodical mode (32-bit general-purpose timer) 4'h0010: Continuous mode (32-bit general-purpose timer) Others: Watchdog mode
10H	TMR0TGTL	RW				Timer0 Lower 32-bit Target Value Register
			[31:0]	Tmr0tgtl	32'hffffffff	Timer0 lower 32-bit target value
14H	TMR0TGTH	RW				Timer0 Upper 32-bit Target Value Register
			[31:0]	Tmr0tgth	32'hffffffff	Timer0 upper 32-bit target value
18H	TMR0DL	RO				Timer0 Lower 32-bit Current Value Register
			[31:0]	Tmr0dl	32'h0	Timer0 lower 32-bit current value
1CH	TMR0DH	RO				Timer0 Upper 32-bit Current Value Register
			[31:0]	Tmr0dh	32'h0	Timer0 upper 32-bit current value
20H	TMR1TGT	RW				Timer1 Target Value Register
			[31:0]	Tmr1tgt	32'hffffffff	Timer1 target value
24H	TMR1D	RO				Timer1 Current Value Register
			[31:0]	Tmr1d	32'h0	Timer1 current value
28H	WDTGT	RW				Timer2 TMR_W1 Target Value Register
			[31:0]	WD1tgt	32'hffffffff	Timer2 TMR_W1 target value

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BASE_ADDR: 0xA1002000, 0xA1003000, 0xA1004000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
2CH	WDWAIT	RW				Timer2 TMR_W2 Target Value Register
			[31:0]	WD2tgt	32'hffffffff	Timer2 TMR_W2 target value
30H	WD1D	RO				Timer2 TMR_W1 Current Value Register
			[31:0]	WD1d	32'h0	Timer2 TMR_W1 current value
34H	WD2D	RO				Timer2 TMR_W2 Current Value Register
			[31:0]	WD2d	32'h0	Timer2 TMR_W2 current value
38H	WDCLR	WO				Watchdog Clear Register
			[31:1]	Reserved		
			[0]	WDogclr	1'h0	Watchdog clear Writing 1 to this bit will clear the watchdog. The watchdog will be reset and another round will start.
3CH	TMR_SRCPND	W1C				Timer Interrupt Source Pending Register
			[31:3]	Reserved		
			[2]	Tmr2srcpnd	1'h0	This bit indicates whether the timer2 interrupt source is pending: 0: The timer2 interrupt source is inactive. 1: The timer2 interrupt source is active. Writing 1 to this bit will clear the corresponding interrupt source.
			[1]	Tmr1srcpnd	1'h0	This bit indicates whether the timer1 interrupt source is pending: 0: The timer1 interrupt source is inactive. 1: The timer1 interrupt source is active. Writing 1 to this bit will clear the corresponding interrupt source.
			[0]	Tmr0srcpnd	1'h0	This bit indicates whether the timer0 interrupt source is pending: 0: The timer0 interrupt source is inactive. 1: The timer0 interrupt source is active. Writing 1 to this bit will clear the corresponding interrupt source.
40H	TMR_INTMASK	RO				Timer Interrupt Mask Status Register
			[31:3]	Reserved		
			[2]	Tmr_intmask2	1'h1	Interrupt mask for timer2: 0: Unmasked. 1: Masked

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	Tmr_intmask1	1'h1	Interrupt mask for timer1: 0: Unmasked. 1: Masked
				[0]	Tmr_intmask0	1'h1	Interrupt mask for timer0: 0: Unmasked. 1: Masked
	44H	TMR_SETMASK	WO				This register is used to set interrupt mask of TMR_SRCPND.
				[31:3]	Reserved		
				[2]	Tmr_setmask2	1'h0	Sets mask for the timer2 alarm interrupt. Writing 1 to this bit will mask TMR_SRCPND[2] to prevent the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Masks the timer2 alarm interrupt.
				[1]	Tmr_setmask1	1'h0	Sets mask for the timer1 alarm interrupt. Writing 1 to this bit will mask TMR_SRCPND[1] to prevent the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Masks the timer1 alarm interrupt.
				[0]	Tmr_setmask0	1'h0	Sets mask for the timer0 alarm interrupt. Writing 1 to this bit will mask TMR_SRCPND[0] to prevent the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Masks the timer0 alarm interrupt.
	48H	TMR_UNMASK	WO				This register is used to set interrupt unmask of TMR_SRCPND.
				[31:3]	Reserved		

Timer	BASE_ADDR: 0xA1002000, 0xA1003000, 0xA1004000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	Tmr_unmask2	1'h0	Unmask for the timer2 alarm interrupt. Writing 1 to this bit will unmask TMR_SRCPND[2] to allow the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Unmasks the timer2 alarm interrupt.
				[1]	Tmr_unmask1	1'h0	Unmask for the timer1 alarm interrupt. Writing 1 to this bit will unmask TMR_SRCPND[1] to allow the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Unmasks the timer1 alarm interrupt.
				[0]	Tmr_unmask0	1'h0	Unmask for the timer0 alarm interrupt. Writing 1 to this bit will unmask TMR_SRCPND[0] to allow the 2nd-level interrupts to IRQ Controller. Writing 0 to this bit will take no effect. 0: No effect. 1: Unmasks the timer0 alarm interrupt.