X3M Register Reference Manual
BIFSPI

Revision History

Revision	Date	Description
1.0	September-1-2020	Initial Release

BIFSPI

BASE_ADDR: 0xA1006000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0000H	SHARE_REG_00	RW				Share register 0
			[31:0]	Share_reg00	32'h0	Share register 0
0004H	SHARE_REG_01	RW				Share register 1
			[31:0]	Share_reg01	32'h0	Share register 1
0008H	SHARE_REG_02	RW				Share register 2
			[31:0]	Share_reg02	32'h0	Share register 2
000CH	SHARE_REG_03	RW				Share register 3
			[31:0]	Share_reg03	32'h0	Share register 3
0010H	SHARE_REG_04	RW				Share register 4
			[31:0]	Share_reg04	32'h0	Share register 4
0014H	SHARE_REG_05	RW				Share register 5
			[31:0]	Share_reg05	32'h0	Share register 5
0018H	SHARE_REG_06	RW				Share register 6
			[31:0]	Share_reg06	32'h0	Share register 6
001CH	SHARE_REG_07	RW				Share register 7
			[31:0]	Share_reg07	32'h0	Share register 7
0020H	SHARE_REG_08	RW				Share register 8
			[31:0]	Share_reg08	32'h0	Share register 8
0024H	SHARE_REG_09	RW				Share register 9
			[31:0]	Share_reg09	32'h0	Share register 9
0028H	SHARE_REG_10	RW				Share register 10
			[31:0]	Share_reg10	32'h0	Share register 10
002CH	SHARE_REG_11	RW				Share register 11
			[31:0]	Share_reg11	32'h0	Share register 11

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0030H	SHARE_REG_12	RW				Share register 12
			[31:0]	Share_reg12	32'h0	Share register 12
0034H	SHARE_REG_13	RW				Share register 13
			[31:0]	Share_reg13	32'h0	Share register 13
0038H	SHARE_REG_14	RW				Share register 14
			[31:0]	Share_reg14	32'h0	Share register 14
003CH	SHARE_REG_15	RW				Share register 15
			[31:0]	Share_reg15	32'h0	Share register 15
0040H	SHARE_REG_16	RW				Share register 16
			[31:0]	Share_reg16	32'h0	Share register 16
0044H	SHARE_REG_17	RW				Share register 17
			[31:0]	Share_reg17	32'h0	Share register 17
0048H	SHARE_REG_18	RW				Share register 18
			[31:0]	Share_reg18	32'h0	Share register 18
004CH	SHARE_REG_19	RW				Share register 19
			[31:0]	Share_reg19	32'h0	Share register 19
0050H	SHARE_REG_20	RW				Share register 20
			[31:0]	Share_reg20	32'h0	Share register 20
0054H	SHARE_REG_21	RW				Share register 21
			[31:0]	Share_reg21	32'h0	Share register 21
0058H	SHARE_REG_22	RW				Share register 22
			[31:0]	Share_reg22	32'h0	Share register 22
005CH	SHARE_REG_23	RW				Share register 23
			[31:0]	Share_reg23	32'h0	Share register 23
0060H	SHARE_REG_24	RW				Share register 24

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[31:0]	Share_reg24	32'h0	Share register 24
0064H	SHARE_REG_25	RW				Share register 25
			[31:0]	Share_reg25	32'h0	Share register 25
0068H	SHARE_REG_26	RW				Share register 26
			[31:0]	Share_reg26	32'h0	Share register 26
006CH	SHARE_REG_27	RW				Share register 27
			[31:0]	Share_reg27	32'h0	Share register 27
0070H	SHARE_REG_28	RW				Share register 28
			[31:0]	Share_reg28	32'h0	Share register 28
0074H	SHARE_REG_29	RW				Share register 29
			[31:0]	Share_reg29	32'h0	Share register 29
0078H	SHARE_REG_30	RW				Share register 30
			[31:0]	Share_reg30	32'h0	Share register 30
007CH	SHARE_REG_31	RO				Share register 31
			[31:16]	Bif_test_data	16'h5a5a	BIF test data
			[15:8]	Bif_version	8'h02	BIF version
			[7:2]	Reserved		
			[1]	Bus_write_state	1'h0	Bus write status: 0: Idle 1: Busy
			[0]	Bus_read_state	1'h0	Bus read status: 0: Idle 1: Busy
0100H	SPI_CFG	RW				SPI configuration register
			[31:3]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	Chk_mode	1'h1	Check mode: 0: Normal check 1: Delay check
				[1]	CPOL	1'h0	SPI clock polarity: 0: High active 1: Low active
				[0]	CPHA	1'h0	SPI sample phase: 0: First edge sample 1: Second edge sample
	0104H	INT_EN_CLEAR	RW				Interrupt clear and enable signal register
				[31:12]	Reserved		
				[11]	Int_clr_6	1'h0	Interrupt clear signal, high active.
				[10]	Int_clr_5	1'h0	Interrupt clear signal, high active.
				[9]	Int_clr_4	1'h0	Interrupt clear signal, high active.
				[8]	Int_clr_3	1'h0	Interrupt clear signal, high active.
				[7]	Int_clr_2	1'h0	Interrupt clear signal, high active.
				[6]	Int_clr_1	1'h0	Interrupt clear signal, high active.
				[5]	Int_en_6	1'h0	Interrupt enable signal, high active.
				[4]	Int_en_5	1'h0	Interrupt enable signal, high active.
				[3]	Int_en_4	1'h0	Interrupt enable signal, high active.
				[2]	Int_en_3	1'h0	Interrupt enable signal, high active.
				[1]	Int_en_2	1'h0	Interrupt enable signal, high active.
				[0]	Int_en_1	1'h0	Interrupt enable signal, high active.
	0108H	INT_STATE	RO				Interrupt status register
				[31:6]	Reserved		
				[5]	Wr_same_sharereg	1'h0	AP CP write the same Share register address.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	Ap_access_outof_limit	1'h0	AP access address out of the limit.
				[3]	Read_buffer_empty	1'h0	Read cmd but buffer empty (underflow).
				[2]	Read_buffer_full	1'h0	Read cmd but buffer full.
				[1]	Check_cmd_err	1'h0	Check cmd is not the cmd we use.
				[0]	Write_buffer_full	1'h0	Write cmd but all buffer full.
	010CH	BUFFER_CLEAR	RW				Command data buffer clear register
				[31:2]	Reserved		
				[1]	Buf_clear_1	1'h0	Buffer 2 clear
				[0]	Buf_clear_2	1'h0	Buffer 1 clear
	0110H	AP_ACCESS_FIRST_ADD	RW				AP access address limit first address register
				[31:0]	AP_access_first_address	32'h0	AP access address limit first address
	0114H	AP_ACCESS_LAST_ADD	RW				AP access address limit last address register
				[31:0]	AP_access_last_address	32'hFFFFFFFF	AP access address limit last address
	0118H	DDR_FIRST_ADD	RW				DDR first address register
				[31:0]	DDR_first_address	32'h0	DDR first address
	011CH	DDR_LAST_ADD	RW				DDR last address register
				[31:0]	DDR_last_address	32'h80FFFFFF	DDR last address
	0120H	LEN_BYTE_UNIT	RW				Command data length unit register
				[31:6]	Reserved		
				[5]	Len_unit_128B	1'h0	Data length unit 128-Byte: 1: 128-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	Len_unit_64B	1'h0	Data length unit 64-Byte: 1: 64-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.
				[3]	Len_unit_32B	1'h0	Data length unit 32-Byte: 1: 32-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.
				[2]	Len_unit_16B	1'h0	Data length unit 16-Byte: 1: 16-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.
				[1]	Len_unit_8B	1'h0	Data length unit 8-Byte: 1: 8-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.
				[0]	Len_unit_4B	1'h0	Data length unit 4-Byte: 1: 4-Byte In one hot mode, only one bit of bits[5:0] can be set to 1'h1. All zero means 16-Byte unit.
	0124H	AXI_ID	RW				AXI read and write id register
				[31:16]	Reserved		
				[15:8]	AXI_aw_wid	8'h01	AXI awid and wid
				[7:0]	AXI_arid	8'h01	AXI arid