X3M Register Reference Manual
UART

Revision History

Revision	Date	Description
1.0	July-15-2020	Initial Release

URATx (x = 0, 1, 2, 3)

BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0000H	UART_RDR	RO				UART Receive Data Register
			[31:8]	Reserved		
			[7:0]	UART_RXD	8'h0	UART Receive Data. In 7-bit data mode, the most significant bit (MSB) is forced to 0. In 8-bit data mode, all bits are active.
0004H	UART_TDR	WO				UART Transmit Data Register. **Note:** You can write data to this register when the UART_TXRDY bit of the UART_LSR register is 0, otherwise you will overwrite it.
			[31:8]	Reserved		
			[7:0]	UART_TXD	8'h0	UART Transmit Data. In 7-bit data mode, the most significant bit (MSB) is forced to 0. In 8-bit data mode, all bits are active.
0008H	UART_LCR	RW				UART Line Control Register **Note:** You can change the UART_LCR bit of the UART_LSR register, when the UART is disabled or the UART is in idle state.
			[31:13]	Reserved		
			[12]	UART_IREN	1'h0	0: Standard Non-Return-to-Zero operation. 1: Others. **Note:** Do NOT change the configuration value 0.
			[11:8]	UART_TOI	4'h2	UART Timeout Condition Check Interval. This bit is used for checking timeout condition by frame time intervals. 1-Frame time interval = (1 start bit time + 7/8 data bit time + 1 parity bit time + 1/2 stop bit time) 0: 1-Frame time interval. 1: 2-Frame time interval. 2: 4-Frame time interval. 3: 8-Frame time interval. 4: 16-Frame time interval. 5: 32-Frame time interval. 6: 64-Frame time interval. 7: 128-Frame time interval. 8: 256-Frame time interval. 9: 512-Frame time interval. 10: 1024-Frame time interval. 11: 2048-Frame time interval. 12: 4096-Frame time interval. Other: Reserved.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	UART_SFCEN	1'h0	UART Software Flow Control (XON/XOFF) Enable. 0: UART software flow control (XON/XOFF) disabled. 1: UART software flow control (XON/XOFF) enabled. **Note:** If you want to use CTS/RTS flow control, you must disable the software flow control (XON/XOFF).
				[6]	UART_RTSEN	1'h0	UART Automatic Receiver Hardware Flow Control Enable. 0: UART auto-RTS flow control disabled. If the receive FIFO is overrun, the received data is probably discarded and an interrupt is generated. 1: UART auto-RTS flow control enabled. The receiver sets output uart_rts_n to 1, when it detects pending RX FIFO overrun.
				[5]	UART_CTSEN	1'h0	UART Automatic Transmitter Hardware Flow Control Enable. 0: UART auto-CTS flow control disabled. The transmitter sends bytes of data whenever the data is available in transmit FIFO. 1: UART auto-CTS flow control enabled. The transmitter waits until uart_cts_n is changed to 0 before transmitting bytes of data.
				[4]	UART_SP	1'h0	Stick Parity Select. 0: Stick parity disabled. 1: Stick parity enabled. The parity bit is forced to a defined state, depending on the UART_PEN and UART_EPS settings in the same register: - If both UART_PEN and UART_EPS are 1, the parity bit is transmitted and checked as 0. - If UART_PEN is 1 and UART_EPS is 0, the parity bit is transmitted and checked as 1.
				[3]	UART_EPS	1'h0	Parity Mode Selection. 0: Odd parity. An odd number of 1 is transmitted and checked in each word. In other words, if the data has an odd number of 1 in it, then the parity bit is 0. 1: Even parity. An even number of 1 is transmitted and checked in each word. In other words, if the data has an even number of 1 in it, then the parity bit is 0.
				[2]	UART_PEN	1'h0	UART Parity Enable. 0: No parity. 1: The parity bit is generated in each outgoing data and checked on each incoming data.
				[1]	UART_STP	1'h0	UART Stop Bit. 0: 1 stop bit. 1: 2 stop bits.
				[0]	UART_BIT	1'h0	UART Data Bit. 0: 7 data bits. 1: 8 data bits.
	000CH	UART_ENR	RW				UART Enable Regsiter
				[31:3]	Reserved		

URATx (x = 0, 1, 2, 3)

BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[2]	UART_TEN	1'h0	Transmitter Enable. 0: Transmitter disabled. 1: Transmitter enabled. This bit must be set to 1 for the transmitter to work. **Note:** If you disable the UART transmitter, the UART will terminate the current transmit DMA transfer firstly, and the entire procedure will probably last for a longer time. UART cannot restart the currrent transmit DMA automatically when the UART transmitter is re-enabled again, software must restart the transmit DMA based on the last one.
			[1]	UART_REN	1'h0	Receiver Enable. 0: Receiver disabled. 1: Receiver enabled. This bit must be set to 1 for the receiver to work. **Note:** If you disable the UART receiver, the UART will terminate the current receive DMA transfer firstly, the entire procedure will probably last for a longer time. UART cannot restart the currrent receive DMA automatically when the UART receiver is re-enabled again, software must restart the receive DMA based on the last one.
			[0]	UART_EN	1'h0	UART Enable. 0: UART disabled. 1: UART enabled.
0010H	UART_BCR	RW				UART BAUD Rate Configuration Register **Note:** You can change the UART_BCR, when the UART is disabled or the UART is in the idle state.
			[31:30]	Reserved		
			[29:28]	UART_BRDIV_MODE	2'h0	UART Baud Rate Generation Mode. 0: 16x Baud Rate clock for low-speed mode. 1: 8x Baud Rate clock for medium-speed mode. 2: 4x Baud Rate clock for high-speed mode. 3: Reserved.
			[27:26]	Reserved		
			[25:16]	UART_BRDIV_FRAC	10'h0	UART Fractional Baud Rate Divisor. This is the fractional part of the baud rate divisor value. Baud rate divisor = UART_BRDIV_INT + UART_BRDIV_FRAC/1024.
			[15:0]	UART_BRDIV_INT	16'h0	UART Integer Baud Rate Divisor. This is the integer part of the baud rate divisor value.
0014H	UART_MCR	RW				UART Modem Control Register
			[31:24]	Reserved		
			[23:16]	UART_XOFF	8'h0	Character to stop UART transmission. In software flow control mode, when the UART receiver sends the XOFF character, the transmitter stops
			[15:8]	UART_XON	8'h0	Character to resume UART transmission. In software flow control mode, after the UART transmitter receives the XON character, it resumes transmission.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:4]	Reserved		
				[3:2]	UART_LMD	2'h0	UART Line Mode. This bit is used to indicate which pins are used. 0: Two-Line Port Mode. The TXD and RXD pins are used. The RTS, CTS, DSR, DCD, RI and DTR pins are not used. 1: Four-Line Port Mode. The TXD, RXD, RTS and CTS pins are used. The DSR, DCD, RI and DTR pins are not used. 2: Seven-Line Port Mode. The TXD, RXD, RTS, CTS, DSR, DCD and RI pins are used. The DTR pin is not used. 3: Eight-Line Port Mode. The TXD, RXD, RTS, CTS, DSR, DCD, RI and DTR pins are used. **Note:** The accurate state of UART must be set, otherwise the UART won't know which pins are being used.
				[1]	UART_RTSN	1'h0	UART_RTS_N. For modem control, when the UART_RTSEN bit of the UART_LCR register is set to 0, this bit controls the output port uart_rts_n. The RTS pin is active low. 0: Sets RTS pin to 0, default. 1: Sets RTS pin to 1.
				[0]	UART_DTRN	1'h0	UART_DTR_N. For modem control, this bit controls the output port uart_dtr_n. The DTS pin is active low. 0: Sets DTR pin to 0, default. 1: Sets DTR pin to 1.
	0018H	UART_TCR	RW				UART Test Control Register
				[31:4]	Reserved		
				[3]	UART_BRK	1'h0	Break Control. 0: Break transmission disabled. 1: Break transmission enabled. The uart_txd output pin is forced to the break state (logic 0). Setting this bit is set to 1 forces the transmitter to insert the break interrupt.
				[2]	UART_FPE	1'h0	Force Parity Error. 0: No parity error generated. 1: Generates the inverted parity error. This bit is used for system debugging. Setting this bit to 1 forces the transmitter to generate the parity error if the parity is enabled.
				[1]	UART_FFE	1'h0	Force Framing Error. 0: No framing error generated. 1: Generates the framing error. This bit is used for system debugging. Setting this bit to 1 forces the transmitter to generate the framing error.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000					
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[0]	UART_LB	1'h0	UART Loopback Mode Enable. 0: Normal receiver operation. 1: The transmitter output internally connected to the receiver input. This bit is used for system debugging. When this bit is set to 1, the transmit output is internally connected to the receive input. In this case, the uart_rxd pin is bypassed, but the uart_txd pin isn't affected.
001CH	UART_FCR	RW				UART FIFO Configuration Register
			[31:29]	Reserved		
			[28:24]	UART_TFTRL	5'h8	UART Transmit FIFO Empty Trigger Level. The value can be from 0 to 15. It cannot be set to 16. The TX FIFO width is 32-bit. The unit of one TX FIFO entry is 1 word that contains 4 bytes. Thus, the total bytes = UART_TFRTL * 4. For example, UART_TFRTL is set to 8, and the total bytes equals 32-byte (8 words).
			[23:21]	Reserved		
			[20:16]	UART_RFTRL	5'h8	UART Receive FIFO Full Trigger Level. The value can be from 1 to 16. It cannot be set to 0. The RX FIFO width is 32-bit. The unit of one RX FIFO entry is 1 word that contains 4 bytes. Thus, the total bytes = UART_RFRTL * 4. For example, UART_RFRTL is set to 8, and the total bytes equals 32-byte (8 words).
			[15:4]	Reserved		
			[3]	UART_TFRST	1'h0	UART Transmit FIFO Reset. 0: No UART transmit FIFO reset. 1: Clears UART transmit FIFO. **Note:** This bit is automatically cleared by UART. To reset the TX FIFO, you must terminate the TX DMA firstly, then reset the UART TX FIFO, and the entire procedure will probably last for a longer time. After resetting the TX FIFO, UART cannot restart the TX DMA automatically, software must restart the TX DMA based on the last one.
			[2]	UART_RFRST	1'h0	UART Receive FIFO Reset. 0: No UART receive FIFO reset. 1: Clears UART receive FIFO. **Note:** UART_RFRST is auto-cleared by UART. To reset the RX FIFO, you must terminate the RX DMA firstly, then reset the UART RX FIFO, and the entire procedure will probably last for a longer time. After resetting the RX FIFO, the UART cannot restart the RX DMA automatically, software must restart the RX DMA based on the last one.
			[1]	UART_TFEN	1'h0	UART Transmit DMA Enable. 0: Transmit DMA disabled. 1: Transmit DMA enabled.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	UART_RFEN	1'h0	UART Receive DMA Enable. 0: Receive DMA disabled. 1: Receive DMA enabled.
	0020H	UART_LSR	RO				UART Line Status Register
				[31:13]	Reserved		
				[12]	UART_TXEPT	1'h1	Transmitter Empty. 0: Either the transmit FIFO or transmitter shift register is not empty. 1: Both the transmit FIFO and transmitter shift register are empty. This bit is cleared when the data is shifted into shift register.
				[11]	UART_TFEPT	1'h1	Transmit FIFO Empty. 0: The transmit FIFO is not empty. 1: The transmit FIFO is empty. This bit is cleared when the data is written to the transmit FIFO.
				[10]	UART_TFTRLR	1'h1	Transmit FIFO Trigger Level Reached. 0: The number of the characters in the FIFO is greater than the transmit trigger level. 1: The number of the characters in the FIFO is not greater than the transmit trigger level. Generates the corresponding interrupt through the UART_TXEPT_int. This bit is cleared when characters are written to the transmit FIFO and the number of the characters in the FIFO is greater than the transmit trigger level.
				[9]	UART_TXRDY	1'h1	Transmit register is ready to be written. 0: Transmit register data is not empty. 1: Transmit register data is empty.
				[8]	UART_TXBUSY	1'h0	UART Transmitter Busy. 0: UART transmitter is not busy. 1: UART is transmitting characters.
				[7]	UART_RFTRLR	1'h0	Receive FIFO Trigger Level Reached. 0: The number of the characters in the FIFO is less than the receive trigger level. 1: The number of the characters in the FIFO is not less than the receive trigger level. Generates the corresponding interrupt through the UART_RXFUL_int. The bit is cleared when characters are read from the receiver FIFO and the number of the characters in the FIFO is less than the receive trigger level.
				[6]	UART_RXTO	1'h0	Receive FIFO timeout. 0: No timeout occurred. 1: A character timeout is detected when all the following conditions are met: 1) At least one character is in the FIFO or the current DMA transfer hasn't completed until now. 2) The most recently received character was received more than UART_TOI (programmable by software) times ago. 3) The most recent FIFO read was performed more than UART_TOI times ago. **Note:** Before generating the UART_RXTO interrupt, the UART must flush out all of the remaining data into memory. Reading this register automatically clears this bit.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5]	UART_RXOE	1'h0	UART Receiver Overrun Error. 0: No overrun occurred since the last reset of this register. 1: Overrun error occurred. The Receive FIFO is full and another character has been received in the receiver shift register. If another character is starting to arrive, it will overwrite the last character but the FIFO will remain intact. Reading this register automatically clears this bit.
				[4]	UART_BI	1'h0	Break Interrupt. 0: No break condition occurred since the last reset of this register. 1: The bit is set when a break condition has been reached in the current character. The break condition occurs when the line is held in 0 at least for a time of one character (start bit + data + parity + stop bit). In this case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. Reading this register automatically clears this bit.
				[3]	UART_FE	1'h0	Framing Error. 0: No framing error occurred since the last reset of this register. 1: The bit is set when the received character did not have a valid stop bit. Generally, any data transmitted during this time gets corrupted. Reading this register automatically clears this bit.
				[2]	UART_PE	1'h0	Parity Error. 0: No parity error occurred since the last reset of this register. 1: This bit is set when the received character comes with parity error. Reading this register automatically clears this bit.
				[1]	UART_RXRDY	1'h0	RX Reg is ready to be read. 0: Receive Reg data is empty. 1: Receive Reg data is not empty.
				[0]	UART_RXBUSY	1'h0	UART Receiver Busy. 0: UART Receiver is not busy. 1: UART is receiving characters.
	0024H	UART_MSR	RO				UART Modem Status Register
				[31:8]	Reserved		
				[7]	UART_RI_C	1'h0	UART Ring Indicator Change. 0: The status on RI pin hasn't changed since last read of UART_MSR. 1: The status on RI pin has changed since last read of UART_MSR. Reading this register automatically clears this bit.
				[6]	UART_DCD_C	1'h0	UART Data Carrier Detect Change. 0: The status on DCD pin hasn't changed since last read of UART_MSR. 1: The status on DCD pin has changed since last read of UART_MSR. Reading this register automatically clears this bit.
				[5]	UART_DSR_C	1'h0	UART Data Set Ready Change. 0: The status on DSR pin hasn't changed since last read of UART_MSR. 1: The status on DSR pin has changed since last read of UART_MSR. Reading this register automatically clears this bit.

URATx (x = 0, 1, 2, 3)

BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[4]	UART_CTS_C	1'h0	UART Clear to Send Change. 0: The status on CTS pin hasn't changed since last read of UART_MSR. 1: The status on CTS pin has changed since last read of UART_MSR. Reading this register automatically clears this bit.
			[3]	UART_RI_N	1'h1	UART Ring Indicator Status. The RI pin is active low. 0: RI pin is 0. 1: RI pin is 1.
			[2]	UART_DCD_N	1'h0	UART Data Carrier Detect status. The DCD pin is active low. 0: DCD pin is 0. 1: DCD pin is 1.
			[1]	UART_DSR_N	1'h0	UART Data Set Ready status. The DSR pin is active low. 0: DSR pin is 0. 1: DSR pin is 1.
			[0]	UART_CTS_N	1'h0	UART Clear To Send status. The CTS pin is active low. 0: CTS pin is 0. 1: CTS pin is 1.
0028H	UART_RXADDR	RW				UART Receive DMA Base Address Register **Note:** Do NOT change the UART_RXADDR value until the current receive DMA transfer has completed.
			[31:0]	UART_RXADDR	32'h0	UART receive memory base address. Do NOT change the UART_RXADDR value until the current receive DMA has completed.
002CH	UART_RXSIZE	RW				UART Receive DMA Size Register.
			[31:24]			
			[23:0]	UART_RXSIZE	24'h0	The Bytes of characters to receive. The value can be from 0 to 16MB. The value 0 means no characters to receive. Write: The CPU sets the receive DMA size. Read: The size of current DMA transfer is returned. **Note:** Do NOT change the UART_RXSIZE value until the current receive DMA transfer has completed.
0030H	UART_RXDMA	RW				UART Receive DMA Control Register
			[31:16]	Reserved		

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
				[15:12]	UART_RXTHD	4'h0	UART Receive DMA Threshold. 0: UART RX DMA threshold disabled. 1: Every 64-byte operation generates an interrupt. 2: Every 128-byte operation generates an interrupt. 3: Every 256-byte operation generates an interrupt. 4: Every 512-byte operation generates an interrupt. 5: Every 1K-byte operation generates an interrupt. 6: Every 2K-byte operation generates an interrupt. 7: Every 4K-byte operation generates an interrupt. 8: Every 8K-byte operation generates an interrupt. 9: Every 16K-byte operation generates an interrupt. 10: Every 32K-byte operation generates an interrupt. 11: Every 64K-byte operation generates an interrupt. 12: Every 128K-byte operation generates an interrupt. 13: Every 256K-byte operation generates an interrupt. 14: Every 512K-byte operation generates an interrupt. 15: Every 1M-byte operation generates an interrupt.
				[11:8]	UART_RXMOS	4'h4	UART receive DMA maximum outstanding number. It is used for DMA transfer. The value can be from 1 to 15. Its default value is 4. **Note:** Do NOT change the UART_RXMOS value until the current receive DMA transfer has completed.
				[7:4]	UART_RXLEN	4'h3	UART receive DMA preferred burst length. It is used for every burst in AXI DMA transfer. The value can be from 0 to 15. The preferred burst length should be selected before starting the DMA transfer and keep it stable throughout the DMA transfer. The width of AXI-DMA bus is 32-bit, a unit is one word that contains 4 bytes. Thus, the total bytes can be calculated as follows: Total bytes = (UART_RXLEN+1) * 4. For example, it is set to 7, and the total bytes are 32 bytes ((7+1)*4 = 32 = 8 words). **Note:** Do NOT change the UART_RXLEN value until the current transmit DMA has completed. When UART RX is in the hardware auto-flow control mode, please make sure that UART_RXLEN +1<= UART_RFTRL.
				[3]	UART_RXAE	1'h0	UART Receive DMA Address Error. 0: No error. 1: DMA address error occurred. Reading this register automatically clears this bit.
				[2]	UART_RXWRAP	1'h0	UART Receive Wrap Mode Enable. 0: Receive Wrap Mode disabled. 1: Receive Wrap Mode enabled. **Note:** Do NOT change UART_RXWRAP until the current receive DMA has completed.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	UART_RXSTP	1'h0	This bit is used to stop the UART receive DMA operation. If some errors occur in transmission, the CPU can terminate the current DMA operation. 0: Not stopped. 1: Stops the current transmit DMA operation. It is cleared by UART. This bit automatically clears itself after being written. **Note:** You can terminate the RX DMA transfer, but you must restart the receive DMA operation until this bit is changed to 0.
				[0]	UART_RXSTA	1'h0	This bit is used to start the UART receive DMA operation. 0: No started. 1: Starts the receive DMA operation. It is set by CPU and cleared by UART. If the current DMA is not in wrap mode, this bit is cleared by UART after the current DMA transfer has completed. If the current DMA is in wrap mode, this bit is cleared by UART after software terminates the current wrap DMA transfer. When all characters have been received by UART, an interrupt is generated to CPU.
	0034H	UART_TXADDR	RW				UART Transmit DMA Base Address Register **Note:** Do NOT change the UART_TXADDR value until the current transmit DMA transfer has completed.
				[31:0]	UART_TXADDR	32'h0	UART Transmit Memory Base Address. **Note:** Do NOT change the UART_TXADDR value until the current transmit DMA has completed.
	0038H	UART_TXSIZE	RW				UART Transmit DMA Size Register **Note:** Do NOT change the UART_TXSIZE value until the current transmit DMA transfer has completed.
				[31:24]			
				[23:0]	UART_TXSIZE	24'h0	The Bytes of characters to transmit. The value can be from 0 to 16MB. The value 0 means no characters to transmit. Write: The CPU sets the transmit DMA size. Read: The size of current DMA transfer is returned. **Note:** Do NOT change the UART_TXSIZE value until the current TX DMA transfer has completed.
	003CH	UART_TXDMA	RW				UART Transmit DMA Control Register
				[31:16]	Reserved		

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000					
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
				[15:12]	UART_TXTHD	4'h0	UART Transmit DMA Threshold. 0: UART TX DMA threshold disabled. 1: Every 64-byte operation generates an interrupt. 2: Every 128-byte operation generates an interrupt. 3: Every 256-byte operation generates an interrupt. 4: Every 512-byte operation generates an interrupt. 5: Every 1K-byte operation generates an interrupt. 6: Every 2K-byte operation generates an interrupt. 7: Every 4K-byte operation generates an interrupt. 8: Every 8K-byte operation generates an interrupt. 9: Every 16K-byte operation generates an interrupt. 10: Every 32K-byte operation generates an interrupt. 11: Every 64K-byte operation generates an interrupt. 12: Every 128K-byte operation generates an interrupt. 13: Every 256K-byte operation generates an interrupt. 14: Every 512K-byte operation generates an interrupt. 15: Every 1M-byte operation generates an interrupt.
				[11:8]	UART_TXMOS	4'h4	UART transmit DMA maximum outstanding number. It is only used for DMA transfer. The value can be from 1 to 15. Its default value is 4. **Note:** Do NOT change the UART_TXMOS value until the current transmit DMA has completed.
				[7:4]	UART_TXLEN	4'h3	UART transmit DMA preferred burst length. It is used for every burst in AXI DMA transfer. The value can be from 0 to 15. The preferred burst length should be selected before starting the DMA transfer and keep it stable throughout the DMA transfer. The width of AXI-DMA bus is 32-bit, a unit is one word that contains 4 bytes. Thus, the total bytes can be calculated as follows: Total bytes = (UART_TXLEN+1) * 4. For example, it is set to 7, and the total bytes are 32 bytes ((7+1)*4 = 32 = 8 words). **Note:** Do NOT change the UART_TXLEN value until the current transmit DMA has completed.
				[3]	UART_TXAE	1'h0	UART Transmit DMA Address Error. 0: No Error. 1: DMA Address Error occurred. This bit is automatically cleared by reading UART_TXDMA.
				[2]	UART_TXWRAP	1'h0	UART Transmit Wrap Mode Enable. 0: Transmit Wrap Mode disabled. 1: Transmit Wrap Mode enabled. **Note:** Do NOT change the UART_TXWRAP value until the current transmit DMA has completed.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	UART_TXSTP	1'h0	This bit is used to stop the UART transmit DMA operation. If some errors occur in transmission, the CPU can terminate the current DMA operation. 0: Not stopped. 1: Stops the current transmit DMA operation. It is cleared by UART. **Note:** You can terminate the TX DMA transfer, but you must restart the transmit DMA operation until this bit is changed to 0.
				[0]	UART_TXSTA	1'h0	This bit is used to start the UART transmit DMA operation. 0: Not started. 1: Starts the transmit DMA operation. It is set by CPU and cleared by UART. When all characters have been transmitted by UART, an interrupt is generated to CPU.
	0040H	UART_SRC_PND	W1C				UART Interrupt Source Pending Register
				[31:15]	Reserved		
				[14]	UART_TXEPT	1'h0	This bit indicates whether the UART transmit FIFO Empty/TX reg ready interrupt source is pending. Read : 0: The UART transmit FIFO empty/TX reg ready interrupt source is inactive. 1: The UART transmit FIFO empty/TX reg ready interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[13]	UART_TXTHD	1'h0	This bit indicates whether the UART transmit DMA threshold interrupt source is pending. Read : 0: The UART transmit DMA threshold interrupt source is inactive. 1: The UART transmit DMA threshold interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[12]	UART_TXDON	1'h0	This bit indicates whether the UART transmit DMA Finish interrupt source is pending. Read : 0: The UART transmit DMA finish interrupt source is inactive. 1: The UART transmit DMA finish interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[11]	UART_RXFUL	1'h0	This bit indicates whether the UART receive FIFO Full/RX reg ready interrupt source is pending. Read : 0: The UART receive FIFO full interrupt/RX reg ready source is inactive. 1: The UART receive FIFO full interrupt/RX reg ready source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10]	UART_RXTO	1'h0	This bit indicates whether the UART receiver timeout error interrupt source is pending. Read : 0: The UART receiver timeout error interrupt source is inactive. 1: The UART receiver timeout error interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[9]	UART_RXOE	1'h0	This bit indicates whether the UART receiver overrun error interrupt source is pending. Read : 0: The UART overrun error interrupt source is inactive. 1: The UART overrun error interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[8]	UART_BI	1'h0	This bit indicates whether the UART break interrupt source is pending. Read : 0: The UART break interrupt source is inactive. 1: The UART break interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[7]	UART_FE	1'h0	This bit indicates whether the UART framing error interrupt source is pending. Read : 0: The UART framing error interrupt source is inactive. 1: The UART framing error interrupt source is active. Write: 0: No effect. 1: Clears the corresponding source.
				[6]	UART_PE	1'h0	This bit indicates whether the UART parity error interrupt source is pending. Read : 0: The UART parity error interrupt source is inactive. 1: The UART parity error interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
				[5]	UART_RXTHD	1'h0	This bit indicates whether the UART receive DMA threshold interrupt source is pending. Read : 0: The UART receive DMA threshold interrupt source is inactive. 1: The UART receive DMA threshold interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.

URATx (x = 0, 1, 2, 3)

BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[4]	UART_RXDON	1'h0	This bit indicates whether the UART receive DMA finish interrupt source is pending. Read : 0: The UART receive DMA finish interrupt source is inactive. 1: The UART receive DMA finish interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
			[3]	UART_RIC	1'h0	This bit indicates whether the UART RI changed interrupt source is pending. Read : 0: The UART RI changed interrupt source is inactive. 1: The UART RI changed interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
			[2]	UART_DCDC	1'h0	This bit indicates whether the UART DCD changed interrupt source is pending. Read : 0: The UART DCD changed interrupt source is inactive. 1: The UART DCD changed interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
			[1]	UART_DSRC	1'h0	This bit indicates whether the UART DSR changed interrupt source is pending. Read : 0: The UART DSR changed interrupt source is inactive. 1: The UART DSR changed interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
			[0]	UART_CTSC	1'h0	This bit indicates whether the UART CTS changed interrupt source is pending. Read : 0: The UART CTS changed interrupt source is inactive. 1: The UART CTS changed interrupt source is active. Write: 0: No effect. 1: Clears the corresponding interrupt source.
0044H	UART_INT_MASK	RO				UART Interrupt Mask Register
			[31:15]	Reserved		
			[14]	UART_TXEPT	1'h1	Mask for the UART transmit FIFO empty/TX reg ready interrupt. 0: Unmasked. 1: Masked.
			[13]	UART_TXTHD	1'h1	Mask for the UART transmit DMA threshold interrupt. 0: Unmasked. 1: Masked.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	UART_TXDON	1'h1	Mask for the UART transmit DMA finish interrupt. 0: Unmasked. 1: Masked.
				[11]	UART_RXFUL	1'h1	Mask for the UART receive FIFO Full/RX reg ready interrupt. 0: Unmasked. 1: Masked.
				[10]	UART_RXTO	1'h1	Mask for the UART receiver timeout error interrupt. 0: Unmasked. 1: Masked.
				[9]	UART_RXOE	1'h1	Mask for the UART overrun error interrupt. 0: Unmasked. 1: Masked.
				[8]	UART_BI	1'h1	Mask for the UART break interrupt. 0: Unmasked. 1: Masked.
				[7]	UART_FE	1'h1	Mask for the UART framing error interrupt. 0: Unmasked. 1: Masked.
				[6]	UART_PE	1'h1	Mask for the UART parity error interrupt. 0: Unmasked. 1: Masked.
				[5]	UART_RXTHD	1'h1	Mask for the UART receive DMA threshold interrupt. 0: Unmasked. 1: Masked.
				[4]	UART_RXDON	1'h1	Mask for the UART receive DMA finish interrupt. 0: Unmasked. 1: Masked.
				[3]	UART_RIC	1'h1	Mask for the UART RI changed interrupt. 0: Unmasked. 1: Masked.
				[2]	UART_DCDC	1'h1	Mask for the UART DCD changed interrupt. 0: Unmasked. 1: Masked.
				[1]	UART_DSRC	1'h1	Mask for the UART DSR changed interrupt. 0: Unmasked. 1: Masked.
				[0]	UART_CTSC	1'h1	Mask for the UART CTS changed interrupt. 0: Unmasked. 1: Masked.
	0048H	UART_INT_SETMASK	WO				UART Interrupt Set Mask Register

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[31:15]	Reserved		
				[14]	UART_TXEPT	1'h0	Sets mask for the UART transmit FIFO empty/TX reg ready interrupt. 0: No effect. 1: Masks the UART transmit FIFO empty/TX reg ready interrupt.
				[13]	UART_TXTHD	1'h0	Sets mask for the UART transmit DMA threshold interrupt. 0: No effect. 1: Masks the UART transmit DMA threshold interrupt.
				[12]	UART_TXDON	1'h0	Sets mask for the UART transmit DMA finish interrupt. 0: No effect. 1: Masks the UART transmit DMA finish interrupt.
				[11]	UART_RXFUL	1'h0	Sets mask for the UART receive FIFO full/RX reg ready interrupt. 0: No effect. 1: Masks the UART receive FIFO full/RX reg ready interrupt.
				[10]	UART_RXTO	1'h0	Sets mask for the UART receiver timeout error interrupt. 0: No effect. 1: Masks the UART receiver timeout error interrupt.
				[9]	UART_RXOE	1'h0	Sets mask for the UART receiver overrun error interrupt. 0: No effect. 1: Masks the UART receiver overrun error interrupt.
				[8]	UART_BI	1'h0	Sets mask for the UART break interrupt. 0: No effect. 1: Masks the UART Break interrupt.
				[7]	UART_FE	1'h0	Sets mask for the UART framing error interrupt. 0: No effect. 1: Masks the UART framing error interrupt.
				[6]	UART_PE	1'h0	Sets mask for the UART parity error interrupt. 0: No effect. 1: Masks the UART parity error interrupt.
				[5]	UART_RXTHD	1'h0	Sets mask for the UART receive DMA threshold interrupt. 0: No effect. 1: Masks the UART receive DMA threshold interrupt.
				[4]	UART_RXDON	1'h0	Sets mask for the UART receive DMA finish interrupt. 0: No effect. 1: Masks the UART receive DMA finish interrupt.
				[3]	UART_RIC	1'h0	Sets mask for the UART RI changed interrupt. 0: No effect. 1: Masks the UART RI changed interrupt.
				[2]	UART_DCDC	1'h0	Sets mask for the UART DCD changed interrupt. 0: No effect. 1: Masks the UART DCD changed interrupt.

URATx (x = 0, 1, 2, 3)

BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[1]	UART_DSRC	1'h0	Sets mask for the UART DSR changed interrupt. 0: No effect. 1: Masks the UART DSR changed interrupt.
			[0]	UART_CTSC	1'h0	Sets mask for the UART CTS changed interrupt. 0: No effect. 1: Masks the UART CTS changed interrupt.
004CH	UART_INT_UNMASK	WO				UART Interrupt Unmask Register
			[31:15]	Reserved		
			[14]	UART_TXEPT	1'h0	Used to unmask the UART transmit FIFO empty/TX reg ready interrupt. 0: No effect. 1: Unmasks the UART transmit FIFO empty/TX reg ready interrupt.
			[13]	UART_TXTHD	1'h0	Used to unmask the UART transmit DMA threshold interrupt. 0: No effect. 1: Unmasks the UART transmit DMA threshold interrupt.
			[12]	UART_TXDON	1'h0	Used to unmask the UART transmit DMA finish interrupt. 0: No effect. 1: Unmasks the UART transmit DMA finish interrupt.
			[11]	UART_RXFUL	1'h0	Used to unmask the UART receive FIFO full/RX reg ready interrupt. 0: No effect. 1: Unmasks the UART receive FIFO full/RX reg ready interrupt.
			[10]	UART_RXTO	1'h0	Used to unmask the UART receiver timeout error interrupt. 0: No effect. 1: Unmasks the UART receiver timeout error interrupt.
			[9]	UART_RXOE	1'h0	Used to unmask the UART receiver overrun error interrupt. 0: No effect. 1: Unmasks the UART receiver overrun error interrupt.
			[8]	UART_BI	1'h0	Used to unmask the UART break interrupt. 0: No effect. 1: Unmasks the UART break interrupt.
			[7]	UART_FE	1'h0	Used to unmask the UART framing error interrupt. 0: No effect. 1: Unmasks the UART framing error interrupt.
			[6]	UART_PE	1'h0	Used to unmask the UART parity error interrupt. 0: No effect. 1: Unmasks the UART parity error interrupt.
			[5]	UART_RXTHD	1'h0	Used to unmask the UART receive DMA threshold interrupt. 0: No effect. 1: Unmasks the receive DMA threshold interrupt.

URATx (x = 0, 1, 2, 3)	BASE_ADDR: 0xA5000000, 0xA5001000, 0xA5002000, 0xA5003000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	UART_RXDON	1'h0	Used to unmask the UART receive DMA finish interrupt. 0: No effect. 1: Unmasks the receive DMA finish interrupt.
				[3]	UART_RIC	1'h0	Used to unmask the UART RI changed interrupt. 0: No effect. 1: Unmasks the UART RI changed interrupt.
				[2]	UART_DCDC	1'h0	Used to unmask the UART DCD changed interrupt. 0: No effect. 1: Unmasks the UART DCD changed interrupt.
				[1]	UART_DSRC	1'h0	Used to unmask the UART DSR changed interrupt. 0: No effect. 1: Unmasks the UART DSR changed interrupt.
				[0]	UART_CTSC	1'h0	Used to unmask the UART CTS changed interrupt. 0: No effect. 1: Unmasks the UART CTS changed interrupt.