Horizon Robotics

Sunrise 3.0

PLL/SD/EMAC Clock Structure

Rev. 1.2

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
1.0	2021-01-06	Initial release.
1.1	2021-01-12	• Updated the base address of each control register. • Updated the bits information, default value and description of the DIV2_SEL bit filed in the EMAC Clock Control register.
1.2	2021-01-14	• Added Section 3 SD1 Clock Structure. • Added Section 4 SD2 Clock Structure. • Added Section 5 I2S0 Clock Structure. • Added Section 6 I2S1 Clock Structure.

Contents

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Tables

1 PLL Frequency Configurations

The PLL frequency configurations are as follows:

Fout = (Fref * FBDIV) / (REFDIV * POSTDIV1 * POSTDIV2), where POSTDIV1 > POSTDIV2.

PLL Frequency Control Register (0xA100_0000 + PLL_offset)

Table 1-1 PLL Frequency Configurations

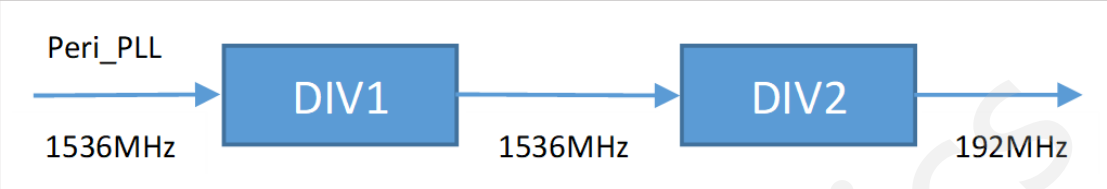
Register Name	PLL_offset	Bits	Field Name	Default Value	PLL Output Freq. (MHz)
ARMPLL	0x0	[26:24]	POSTDIV2	1	Fout=24*100/1*2*1=1,200
		[22:20]	POSTDIV1	2	
		[17:12]	REFDIV	1	
		[11:0]	FBDIV	100	
SYSPLL	0x10	[26:24]	POSTDIV2	1	Fout=24*125/1*2*1=1,500
		[22:20]	POSTDIV1	2	
		[17:12]	REFDIV	1	
		[11:0]	FBDIV	1	
CNNPLL	0x20	[26:24]	POSTDIV2	1	Fout=24*250/3*2*1=1,000
		[22:20]	POSTDIV1	2	
		[17:12]	REFDIV	3	
		[11:0]	FBDIV	250	
DDRPLL	0x30	[26:24]	POSTDIV2	1	Fout=24*55/1*1*1=1,320
		[22:20]	POSTDIV1	1	
		[17:12]	REFDIV	1	
		[11:0]	FBDIV	55	
VIOPLL	0x40	[26:24]	POSTDIV2	1	Fout=24*64/1*1*1=1,632
		[22:20]	POSTDIV1	1	
		[17:12]	REFDIV	1	
		[11:0]	FBDIV	68	
PERIPHPLL	0x50	[26:24]	POSTDIV2	1	Fout=24*100/1*2*1=1,536
		[22:20]	POSTDIV1	1	
		[17:12]	REFDIV	1	
		[11:0]	FBDIV	64	
VIOPLL2	0xB0	[26:24]	POSTDIV2	1	Fout=24*99/1*1*1=2,376
		[22:20]	POSTDIV1	1	
		[17:12]	REFDIV	1	

Register Name	PLL_offset	Bits	Field Name	Default Value	PLL Output Freq. (MHz)
		[11:0]	FBDIV	99	

2 SD0 Clock Structure

The SD0 module clock structure is as shown in Figure 2-1.

Figure 2-1 SD0 Clock Structure



SD0 Clock Control Register (0xA100_0000 + 0x320)

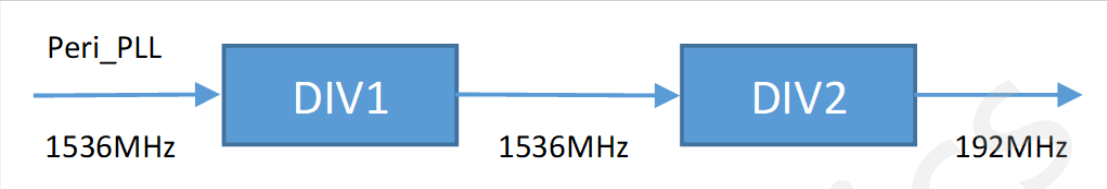
Table 2-1 SD0 Clock Control Register

Bits	Field Name	Default Value	Description
[3:0]	DIV1_SEL	4'h0	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16
[7:4]	DIV2_SEL	4'h7	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16

3 SD1 Clock Structure

The SD1 module clock structure is as shown in Figure 3-1.

Figure 3-1 SD1 Clock Structure



SD1 Clock Control Register (0xA100_0000 + 0x330)

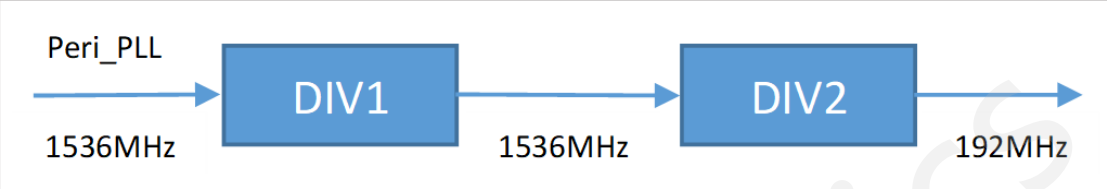
Table 3-1 SD1 Clock Control Register

Bits	Field Name	Default Value	Description
[3:0]	DIV1_SEL	4'h0	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16
[7:4]	DIV2_SEL	4'h7	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16

4 SD2 Clock Structure

The SD2 module clock structure is as shown in Figure 4-1.

Figure 4-1 SD2 Clock Structure



SD2 Clock Control Register (0xA100_0000 + 0x340)

Table 4-1 SD2 Clock Control Register

Bits	Field Name	Default Value	Description
[3:0]	DIV1_SEL	4'h0	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16
[7:4]	DIV2_SEL	4'h7	Divider select: 4'h0: refclk/1 4'h1: refclk/2 … 4'h9: refclk/10 … 4'hE: refclk/15 4'hF: refclk/16

5 I2S0 Clock Structure

The I2S0 module clock structure is as shown in Figure 5-1.

Figure 5-1 I2S0 Clock Structure

I2S0 Clock Control Register (0xA100_0000 + 0x350)

Table 5-1 I2S0 Clock Control Register

Bits	Field Name	Default Value	Description
[4:0]	DIV1_SEL	5'd24	Divider select: 5'd0: refclk/1 5'd1: refclk/2 … 5'd24: refclk/25 … 5'd30: refclk/31 5'h31: refclk/32
[12:8]	DIV2_SEL	5'd4	Divider select: 5'd0: refclk/1 5'd1: refclk/2 … 5'd4: refclk/5 … 5'd30: refclk/31 5'h31: refclk/32
[18:16]	DIV3_SEL	3'd3	Divider select: 3'd0: refclk/1 3'd1: refclk/2 3'd2: refclk/3 3'd3: refclk/4 3'd4: refclk/5 3'd5: refclk/6 3'd6: refclk/7 3'd7: refclk/8

6 I2S1 Clock Structure

The I2S1 module clock structure is as shown in Figure 6-1.

Figure 6-1 I2S1 Clock Structure

I2S1 Clock Control Register (0xA100_0000 + 0x360)

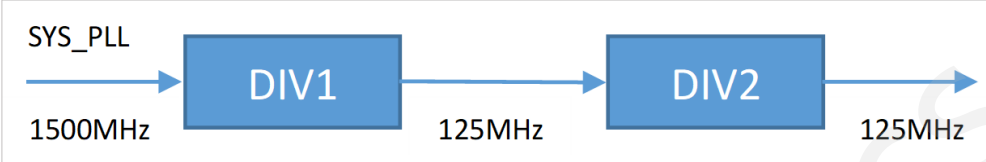
Table 6-1 I2S1 Clock Control Register

Bits	Field Name	Default Value	Description
[4:0]	DIV1_SEL	5'd24	Divider select: 5'd0: refclk/1 5'd1: refclk/2 … 5'd24: refclk/25 … 5'd30: refclk/31 5'h31: refclk/32
[12:8]	DIV2_SEL	5'd4	Divider select: 5'd0: refclk/1 5'd1: refclk/2 … 5'd4: refclk/5 … 5'd30: refclk/31 5'h31: refclk/32
[18:16]	DIV3_SEL	3'd3	Divider select: 3'd0: refclk/1 3'd1: refclk/2 3'd2: refclk/3 3'd3: refclk/4 3'd4: refclk/5 3'd5: refclk/6 3'd6: refclk/7 3'd7: refclk/8

7 EMAC Clock Structure

The EMAC module clock structure is as shown in Figure 7-1.

Figure 7-1 EMAC Clock Structure



EMAC Clock Control Register (0xA100_0000 + 0x380)

Table 7-1 EMAC Clock Control Register

Bits	Field name	Default Value	Description
[4:0]	DIV1_SEL	5'd11	Divider select: 5'd0: refclk/1 5'd1: refclk/2 … 5'd11: refclk/12(1500/12=125MHz) … 5'd29: refclk/30 5'd30: refclk/31 5'd31: refclk/32
[10:8]	DIV2_SEL	3'd0	Divider select: 3'd0: refclk/1 3'd1: refclk/2 3'd2: refclk/3 3'd3: refclk/4 3'd4: refclk/5 3'd5: refclk/6 3'd6: refclk/7 3'd7: refclk/8