X3M Register Reference Manual
LPWM

Revision History

Revision	Date	Description
1.0	January-26-2021	Initial Release

LPWM	BASE_ADDR: 0xA501_8000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	00H	LPWM_EN	RW	[31:6]	Reserved	26'h0	
				[5]	MODE_SEL	1'h0	Mode selection for LPWM enable trigger: 0: SW trigger mode. 1: PPS_trigger in mode (from GPIO source).
				[4]	INT_EN	1'h0	The interrupt is only valid for PPS_trigger in mode (MODE_SEL =1). 0: The LPWM interrupt is disabled. 1: The LPWM interrupt is enabled.
				[3]	LPWM3_EN	1'h0	0: LPWM3 channel is disabled, outputs LOW level. 1: LPWM3 channel is enabled.
				[2]	LPWM2_EN	1'h0	0: LPWM2 channel is disabled, outputs LOW level. 1: LPWM2 channel is enabled.
				[1]	LPWM1_EN	1'h0	0: LPWM1 channel is disabled, outputs LOW level. 1: LPWM1 channel is enabled.
				[0]	LPWM0_EN	1'h0	0: LPWM0 channel is disabled, outputs LOW level. 1: LPWM0 channel is enabled.
	04H	LPWM0_CFG	RW	[31:28]	Reserved	4'h0	
				[27:24]	LPWM0_HIGH	4'h0	The pulse high width of LPWM0. This pulse high width is 0.01ms*(HIGH+1).
				[23:12]	LPWM0_PERIOD	12'h084	The pulse period of LPWM0. This period time is 0.01ms*(PERIOOD+1).
				[11:0]	LPWM0_OFFSET	12'h000	The first pulse offset of LPWM0 for the trigger in signal. This offset time is 0.01ms*(OFFSET+1).
	08H	LPWM1_CFG	RW	[31:28]	Reserved	4'h0	
				[27:24]	LPWM1_HIGH	4'h0	The pulse high width of LPWM1. This pulse high width is 0.01ms*(HIGH+1).
				[23:12]	LPWM1_PERIOD	12'h084	The pulse period of LPWM1. This period time is 0.01ms*(PERIOOD+1).
				[11:0]	LPWM1_OFFSET	12'h000	The first pulse offset of LPWM1 for the trigger in signal. This offset time is 0.01ms*(OFFSET+1).
	0CH	LPWM2_CFG	RW	[31:28]	Reserved	4'h0	
				[27:24]	LPWM2_HIGH	4'h0	The pulse high width of LPWM2. This pulse high width is 0.01ms*(HIGH+1).
				[23:12]	LPWM2_PERIOD	12'h084	The pulse period of LPWM2. This period time is 0.01ms*(PERIOOD+1).
				[11:0]	LPWM2_OFFSET	12'h000	The first pulse offset of LPWM2 for the trigger in signal. This offset time is 0.01ms*(OFFSET+1).
	10H	LPWM3_CFG	RW	[31:28]	Reserved	4'h0	
				[27:24]	LPWM3_HIGH	4'h0	The pulse high width of LPWM3. This pulse high width is 0.01ms*(HIGH+1).
				[23:12]	LPWM3_PERIOD	12'h084	The pulse period of LPWM3. This period time is 0.01ms*(PERIOOD+1).
				[11:0]	LPWM3_OFFSET	12'h000	The first pulse offset of LPWM3 for the trigger in signal. This offset time is 0.01ms*(OFFSET+1).
	14H	SW_TRIG	WO	[31:0]	SW_TRIG	32'h0	In SW trigger mode (MODE_SEL = 0), writing any value to this register will trigger the LPWM function.
	20H	LPWM_RST	WO	[31:1]	Reserved	31'h0	
				[0]	LPWM_RST	1'h0	Writing 1 to this bit will reset all registers.