X3M Register Reference Manual
QSPI

Revision History

Revision	Date	Description
1.0	September-8-2020	Initial Release.
1.1	April-27-2021	In the SCLK_CON register, updated the equations of Divisor and Prescaler.

QSPI	BASE_ADDR: 0xB0000000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	00H	TX_DAT	WO	[31:0]	TX_DAT	32'h0	Transmit Data Buffer The TX_DAT bits holds the data to be transmitted in the next transaction. A read operation to these bits will return the value of RX_DAT because these two registers share the same address range.
		RX_DAT	RO	[31:0]	RX_DAT	32'h0	Received Data Buffer The RX_DAT bits holds the value of received data of the last transfer. A write operation to these bits will change the value of TX_DAT because these two registers share the same address range.
	04H	SCLK_CON	RW				This register is used for Baud-rate control while working as a master.
				[31:8]	Reserved		
				[7:4]	Divisor	4'h0	Divisor used in baud rate calculation. - It is only used in Master Mode. - The baud rate is calculated according to the following equations: Baud Rate Divisor = (Prescaler+1) * $2^{(Divisor+1)}$ Baud Rate = PCLK/Baud Rate Divisor So the baud rate ranges from 38.15Hz to 20MHz provided the PCLK is 40MHz.
				[3:0]	Prescaler	4'h0	Prescaler used in baud rate calculation. The baud rate is calculated according to the following equations: Baud Rate Divisor = (Prescaler+1) * $2^{(Divisor+1)}$ Baud Rate = PCLK/Baud Rate Divisor So the baud rate ranges from 38.15Hz to 20MHz provided the PCLK is 40MHz.
	08H	SPI_CTL1	RW				SPI Working Mode Configuration Register
				[31:8]	Reserved		
				[7]	Rx_mask	1'h0	0: The RX direction is not working. 1: The RX direction is working.
				[6]	LSB_first	1'h0	0: MSB is transferred first on SPI bus. 1: LSB is transferred first on SPI bus.
				[5]	CPHA	1'h0	0: Data sampling occurs at odd edges (1, 3, 5, ..., 15) of the SCLK clock. 1: Data sampling occurs at even edges (2, 4, 6, ..., 16) of the SCLK clock.
				[4]	CPOL	1'h0	0: Active-high clocks are selected. In idle state SCLK is low. 1: Active-low clocks are selected. In idle state SCLK is high.

QSPI	BASE_ADDR: 0xB0000000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	Tx_mask	1'h0	0: The TX direction is not working. 1: The TX direction is working.
				[2]	Mst_mode	1'h1	0: SPI works in slave mode. 1: SPI works in master mode (default).
				[1:0]	FIFO_width	1'h0	0: 8-bit. It means only the lower 8-bit in data bus is valid. 1: 16-bit. It means only the lower 16-bit in databus is valid. 2: 32-bit. It means all the 32-bit in databus is valid. 3: Reserved. This indicates the valid data-width while accessing the TX_DAT or RX_DAT register. Any change to this field will clear the write and read pointers of TX_FIFO and RX_FIFO. Data length is defined by the BATCH_CNT register and it should match the fifo_width, which means the remainder of calculation batch_cnt*8/fifo_width(8/16/32) should be 0.
	0CH	SPI_CTL2	RW				This register is used to enable the SPI interrupt.
				[31:8]	Reserved		
				[7]	Batch_tint_en	1'h0	0: Disables the SPI batch transfer interrupt. 1: Enables the SPI batch transfer interrupt. This bit can be used in both large amount of data or few data transfer.
				[6]	Batch_rint_en	1'h0	1: Enables the SPI batch transfer interrupt. 0: Disables the SPI batch transfer interrupt. This bit can be used in both large amount of data or few data transfer.
				[5:4]	Reserved	1'h0	
				[3]	MODFEN	1'h0	1: Enables the mode fault detection in ssn0_i. 0: Disables the mode fault detection in ssn0_i.
				[2]	Err_inte	1'h0	0: Disables the spi_wr_full or spi_rd_ept error interrupt. 1: Enables the spi_wr_full or spi_rd_ept error interrupt.
				[1]	Tx_int_en	1'h0	0: Disables the interrupt of TX. 1: Enables the interrupt of TX.
				[0]	Rx_int_en	1'h0	0: Disables the interrupt of RX. 1: Enables the interrupt of RX.
	10H	SPI_CTL3	RW				This register is used to reset the SPI software and enable DMA.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[31:5]	Reserved		
				[4]	Batch_disable	1'h0	0: Enable batch_cnt and batch operation. 1: Disable batch_cnt and batch operation. When Batch_disable is 0, data is received using Batch_rcnt, and Batch_rdone goes high when batch transfer is finished. Batch_rdone and Rx_mask both need be cleared for next batch RX transfer. When Batch_disable is 1, Batch_rcnt and batch_rdone are not used. In master mode, " 0" should be written to Tx_fifo to generate sclk. The sclk is generated when Tx_fifo is not empty. 1 byte "0" generates 1 byte sclk. Tx_mask needn't be set when receiving data. If XIP is defined in RTL, the default value of Batch_disable is XIP_remap(pin)&&XIP_cfg[1](reg).
				[3]	Dma_tdq_en	1'h0	Supports the flow controlled by DMA, but not SPI. 0: DMA TX transfer mode is disabled 1: DMA TX transfer mode is enabled
				[2]	Dma_rdq_en	1'h0	Supports the flow controlled by DMA, but not SPI. 0: DMA RX transfer mode is disabled 1: DMA RX transfer mode is enabled
				[1]	SW_RST_TX	1'h0	Soft reset for TX link, high active.
				[0]	SW_RST_RX	1'h0	Soft reset for RX link, high active.
	14H	DEVICE_CS	RW				This register is used to control the device select output.
				[31:8]	Reserved		
				[7:0]	Device_CS	8'h0	These bits map the corresponding device's select output ssn_o[7:0]. Set one bit will deassert the corresponding device's select signal. The mode fault detection is only available in bit 0. This register should be written last in master mode, data transfer will start immediately after writing. If other register configurations should be changed between different transfer stages in master mode, this register should be written again (either changed or unchanged) to trigger next transfer stage. This register is not used in slave mode.

QSPI	BASE_ADDR: 0xB0000000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	18H	STATUS					Work Status Report Register 1 The Tx_mask and Rx_mask are used to mark direction for the data transfer. If Tx_mask and Rx_mask are all set, it means both directions should be considered.
			RO	[31:6]	Reserved		
			R/W1C	[5]	Batch_tdone	1'h0	This bit is set after the exact number of data, which is specified by BATCH_CNT, has been shifted out from shift_reg or received by RX_FIFO. It may interrupt CPU if Batch_int_en is set. This bit should be cleared by CPU writing 1 to it when batch transfer is finished, or it retains 1 when next batch is processed. This register is effective when ctl3 [4] is set to 0.
			R/W1C	[4]	Batch_rdone	1'h0	This bit is set after the exact number of data, which is specified by BATCH_CNT, has been shifted out from shift_reg or received by RX_FIFO. It may interrupt the CPU if batch_int_en is set. This bit should be cleared by CPU writing 1 to it when batch transfer is finished, or it retains 1 when next batch is processed. This register is effective when ctl3 [4] is set to 0.
			R/W1C	[3]	MODF	1'h0	This bit is set if the SPI is configured as master and the DEVICES_CS[0] is not set but the input of device select(ssn0_i) becomes low. When it happens, the SPI is forced to slave mode and the serial data output is disabled also. It may interrupt CPU if MODFEN is set. This bit is cleared by CPU writing 1 to this bit.
			RO	[2]	Reserved	1'h0	
			RO	[1]	Tx_almost_empty	1'h1	This bit is set while data in tx_fifo is less than (fifo_txtrig_lvl) bytes.
			RO	[0]	Rx_almost_full	1'h0	This bit is set while data in rx_fifo is more than or equal to (fifo_rxtrig_lvl) bytes.
	1CH	STATUS2					Work Status Report Register 2
			RO	[31:8]	Reserved		
			RO	[7]	ssn_in	1'h1	This bit reflects the status of ssn_in.
			RO	[6]	Reserved	1'h0	
			RO	[5]	Tx_full	1'h0	This bit is cleared while there is remained space for data in TX_FIFO. It means CPU can write data to TX_FIFO. This bit reflects the TX_FIFO status in any time.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RO	[4]	Rx_empty	1'h1	This bit indicates there is no data (unit: byte) in RX_FIFO. In word mode, Rx_empty_flag keeps high until there are 4 bytes data in FIFO. In half-word mode, Rx_empty_flag keeps high until there are 2 bytes data in FIFO. In byte mode, Rx_empty_flag keeps high until there is 1 byte data in FIFO. This bit reflects the RX_FIFO status in any time.
			R/W1C	[3]	Slv_txrd_empty	1'h0	This bit is set when spi reads an empty tx_fifo, which generates a spi transfer error. It may interrupt CPU if Err_inte is set. This bit is cleared by writing 1 to this bit.
			R/W1C	[2]	Slv_rxwr_full	1'h0	This bit is set when spi writes data to an already full rx_fifo, which generates a spi error. It may interrupt CPU if Err_inte is set. This bit is cleared by writing 1 to this bit.
			RO	[1]	Tx_empty	1'h1	0: There is still data in TX_FIFO or in TX shift register. 1: There is no data in TX_FIFO and TX shift register.
			RO	[0]	Rx_full	1'h0	0: RX_FIFO is not full. 1: RX_FIFO is full, (FIFO depth) ready to be read by CPU or DMA.
	20H	BATCH_CNT_RX	RW				This register is used to hold the data number for RX batch transfer.
				[31:16]	Reserved		
				[15:0]	Tx_Batch_Number	16'h1	This is used to hold the number of data which is going to be transmitted or received on SPI bus. During the specified amount of data transfer, CPU is not interfered with interrupt request. Value 0 indicates 256 bytes. BATCH_CNT_T/RX should better be 1 or a multiple of (Fifo_rxtrig_lvl). If BATCH_CNT_T/RX is not 1 or a multiple of (Fifo_rxtrig_lvl), tail num data should be considered.
	24H	BATCH_CNT_TX	RW				This register is used to hold the data number for TX batch transfer. 1. When value 1 is set, every byte of transfer will generate a interrupt if Batch_int_en is enabled. 2. BATCH_CNT_T/RX should be 1 or times of (Fifo_depth/2). 3. When batch RX finishes, sclk is masked off. When read RX FIFO finishes, Rx_mask should go to low to clear off sclk mask, otherwise, when batch RX is processed next time, sclk is still masked off. Batch TX does not require to clear off Tx_mask. 4. If CTL3 [4] is set to 1, Batch_mode is not used, and BATCH_CNT_T/RX need be set.
				[31:16]	Reserved		

QSPI	BASE_ADDR: 0xB0000000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:0]	Rx_Batch_Number	16'h1	This is used to hold the number of data which is going to be transmitted or received on SPI bus. During the specified amount of data transfer, CPU is not interfered with interrupt request. Value 0 indicates 256 bytes.
	28H	FIFO_RXTRIG_LVL	RW				RX FIFO Trigger Level Register SPI works as QUAD spi. If hclk>=100m and sclk>=50m, Rx_trig_lvl should be set less than 0xc.
				[31:8]	Reserved		
				[7:0]	Fifo_rxtrig_lvl	Fifo_ depth	Fifo_rxtrig_lvl is used to initiate Rx_trig when receiving data (Rx_trig triggers Spi_int or Dma_rx_req). Rx_trig = Level_rfifo >= Fifo_rxtrig_lvl (Level_rfifo is the data number in RX_FIFO). Fifo_rxtrig_lvl: 0x0: Not used. 0x1: Rx_trig goes high when 1 byte of data received in TX_FIFO. ..... 0x10: Rx_full triggers Rx_trig.
	2CH	FIFO_TXTRIG_LVL	RW				TX FIFO Trigger Level Register
				[31:8]	Reserved		
				[7:0]	Fifo_txtrig_lvl	8'h0	Fifo_txtrig_lvl is used to initiate Tx_trig when transmit data (Tx_trig triggers Spi_int or Dma_tx_req). Tx_trig = Level_tfifo <= Fifo_txtrig_lvl (Level_tfifo is the data number in TX_FIFO). Fifo_txtrig_lvl: 0x0: Tx_fifo_empty triggers Tx_trig 0x1: Tx_trig goes high when only one byte data left in TX_FIFO. ... 0xf: Tx_trig high when 15 bytes data left in TX_FIFO, that is, when one byte data was read away from TX_FIFO. 0x10: Not used.
	30H	DUAL_QUAD_MODE	RW				Dual, Quad Flash Operation Enable Register This register exists only when DUAL_QUAD_MODE has been defined in RTL. Please refer to the SPI-flash data sheet for detailed information about Dual/Quad Output Read, Dual/Quad IO Read. QSPI needs only 2 cycles to transfer 8 bits of data.
				[31:8]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	Hold_o_byreg	1'h0	Hold_o reg value.
				[6]	Hold_oe_byreg	1'h1	Hold_oe reg value.
				[5]	Hold_reg_ctrled	1'h0	0: Hold pin not controlled by register. 1: Hold pin controlled by register.
				[4]	Wp_o_byreg	1'h0	Wp_o reg value.
				[3]	Wp_oe_byreg	1'h1	Wp_oe reg value.
				[2]	Wp_reg_ctrled	1'h0	0: Wp not controlled by register. 1: Wp controlled by register.
				[1]	Qual_spi	1'h0	0: Disables quad SPI mode. 1: Enables quad SPI mode.
				[0]	Dual_spi	1'h0	0: Disables dual SPI mode. 1: Enables dual SPI mode.
	34H	XIP_CFG (Optional)	RW				XIP Configuration Register This register exists only when XIP has been defined in RTL.
				[31:8]	Reserved		
				[7:5]	Dummy_cycle	3'h2	Sets the number of dummy clock cycles. Unit: sclk_num_byte. Quad spi: sclk_num_byte=2 sclk; Dual SPI: sclk_num_byte=4 sclk. Stand SPI: sclk_num _byte=8 sclk. 000: No dummy cycle. 001: 1* sclk_num_byte. ..... 111: 7* sclk_num_byte.
				[4]	Ctnu mode	1'h0	1: Continuous read (Ctnu) mode is used for XIP flash read. Dummy_cycle is not applicable to continuous read (Ctnu) mode, so don’t care data cycle.
				[3:2]	Reserved		
				[1]	XIP_remap_enable	1'h1	0: If XIP_CFG[0]=1, soft XIP is enabled, otherwise normal SPI is enabled. 1: Enables hardware XIP_remapt pin. If the XIP_remap pin is high, hardware XIP boot is enabled, otherwise, SPI function is decided by XIP_CFG[0].

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	Soft_XIP_en	1'h1	0: If XIP_CFG[1] & XIP_remap=1, XIP boot is enabled, otherwise normal SPI is enabled. 1: If XIP_CFG[1] & XIP_remap=0, flash address is directly read through SPI interface, CMD is not required. If XIP_CFG[1] & XIP_remap=1, SPI XIP boot is enabled.