X3M Register Reference Manual
MIPI CSI-2 Host & Device & DSI Host

Revision History

Revision	Date	Description
1.0	July-15-2020	Initial Release

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MIPI CSI-2 Host

BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	VERSION	RO	[31:0]	version	0x3134302a	This field indicates the version of the mipi_csi2_host.
04H	N_LANES	RW	[31:3]	Reserved		
			[2:0]	n_lanes	3	Number of active data lanes: 000: 1 Data Lane 001: 2 Data Lanes 010: 3 Data Lanes 011: 4 Data Lanes 100: 5 Data Lanes 101: 6 Data Lanes 110: 7 Data Lanes 111: 8 Data Lanes This can only be updated when the PHY lane is in stop state.
08H	CSI2_RESETN	RW	[31:1]	Reserved		
			[0]	csi2_resetn	0x0	The mipi_csi2_host reset output. Active Low.
0CH	INT_ST_MAIN	RO	[31:22]	Reserved		
			[21]	status_int_ipi4	0x0	Status of int_st_ipi4.
			[20]	status_int_ipi3	0x0	Status of int_st_ipi3.
			[19]	status_int_ipi2	0x0	Status of int_st_ipi2.
			[18]	status_int_ipi	0x0	Status of int_st_ipi.
			[17]	status_int_line	0x0	Status of int_st_line.
			[16]	status_int_phy	0x0	Status of int_st_phy.
			[15:3]	Reserved		
			[2]	status_int_frame_fatal	0x0	Status of int_st_frame_fatal.
			[1]	status_int_pkt_fatal	0x0	Status of int_st_pkt_fatal.
			[0]	status_int_phy_fatal	0x0	Status of int_st_phy_fatal.
40H	PHY_SHUTDOWNZ	RW	[31:1]	Reserved	0x0	
			[0]	phy_shutdownz	0x0	Shutdown input. This line is used to place the complete macro in power down. All analog blocks are in power down mode and digital logic is cleared. Active Low.
44H	DPHY_RSTZ	RW	[31:1]	Reserved		
			[0]	dphy_rstz	0x0	PHY reset output. Active Low.
48H	PHY_RX	RO	[31:18]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17]	phy_rxclkactivehs	0x0	Indicates that D-PHY clock lane is actively receiving a DDR clock.
				[16]	phy_rxulpsclknot	0x0	Active Low. This signal indicates that D-PHY Clock Lane module has entered the Ultra Low Power state.
				[15:4]	Reserved		
				[3]	phy_rxulpsesc_3	0x0	Lane module 3 has entered the Ultra Low Power mode.
				[2]	phy_rxulpsesc_2	0x0	Lane module 2 has entered the Ultra Low Power mode.
				[1]	phy_rxulpsesc_1	0x0	Lane module 1 has entered the Ultra Low Power mode.
				[0]	phy_rxulpsesc_0	0x0	Lane module 0 has entered the Ultra Low Power mode.
	4CH	PHY_STOPSTATE	RO	[31:17]	Reserved		
				16	phy_stopstateclk	0x0	D-PHY Clock lane in Stop state.
				[15:4]	Reserved		
				[3]	phy_stopstatedata_3	0x0	Data lane 3 in Stop state.
				[2]	phy_stopstatedata_2	0x0	Data lane 2 in Stop state.
				[1]	phy_stopstatedata_1	0x0	Data lane 1 in Stop state.
				[0]	phy_stopstatedata_0	0x0	Data lane 0 in Stop state.
	50H	PHY_TEST_CTRL0	RW	[31:2]	Reserved		
				[1]	phy_testclk	0x0	Clock to capture testdin bus contents into the macro, with testen signal controlling the operation selection.
				[0]	phy_testclr	0x1	When active, performs vendor specific interface initialization. Active High. **Note:** This line needs an initial high pulse after power up for analog programmability default values to be preset.
	54H	PHY_TEST_CTRL1	RW	[31:17]	Reserved		
			RW	[16]	phy_testen	0x0	When asserted high, it configures an address write operation on the falling edge of testclk. When asserted low, it configures a data write operation on the rising edge of testclk.
			RO	[15:8]	phy_testdout	0x0	Vendor-specific 8-bit data output for reading data and other probing functionalities.
			RW	[7:0]	phy_testdin	0x0	Test interface 8-bit data input for programming internal registers and accessing test functionalities.
	80H	IPI_MODE	RW	[31:25]	Reserved		

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BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[24]	ipi_enable	0x0	This register enables the interface.
			[23:17]	Reserved		
			[16]	ipi_cut_through	0x0	This field indicates cut-through mode state: 0: Cut-through mode inactive. 1: Cut-through mode active.
			[15:9]	Reserved		
			[8]	ipi_color_com	0x0	This field indicates if color mode components are delivered as follows: 0: 48 bits interface. 1: 16 bits interface.
			[7:1]	Reserved		
			[0]	ipi_mode	0x0	This field indicates the video mode transmission type as follows: 0: Camera timing. 1: Controller timing.
84H	IPI_VCID	RW	[31:2]	Reserved		
			[1:0]	ipi_vcid	0x0	Virtual channel of data to be processed by pixel interface.
88H	IPI_DATA_TYPE	RW	[31:9]	Reserved		
			[8]	embedded_data	0x0	This bit enables embedded data processing on IPI interface.
			[7:6]	Reserved		
			[5:0]	ipi_data_type	0x0	Data type of data to be processed by pixel interface.
8CH	IPI_MEM_FLUSH	RW	[31:9]	Reserved		
			[8]	ipi_auto_flush	0x0	Memory is automatically flushed at each vsync.
			[7:1]	Reserved		
			[0]	ipi_flush	0x0	Flush IPI memory. This bit is auto clear.
90H	IPI_HSA_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hsa_time	0x0	This field configures the Horizontal Synchronism Active period in pixclk cycles.
94H	IPI_HBP_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hbp_time	0x0	This field configures the Horizontal Back Porch period in pixclk cycles.
98H	IPI_HSD_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hsd_time	0x0	This field configures the Horizontal Sync Porch delay period in pixclk cycles.
9CH	IPI_HLINE_TIME	RW	[31:12]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11:0]	ipi_hline_time	0x0	This field configures the size of the line time counted in pixclk cycles.
	A0H	IPI_SOFTRSTN	RW	[31:13]	Reserved		
				[12]	ipi4_softrstn	0x1	This field resets IPI four. Active Low.
				[11:9]	Reserved		
				[8]	ipi3_softrstn	0x1	This field resets IPI four. Active Low.
				[7:5]	Reserved		
				[4]	ipi2_softrstn	0x1	This field resets IPI four. Active Low.
				[3:1]	Reserved		
				[0]	ipi_softrstn	0x1	This field resets IPI four. Active Low.
	ACH	IPI_ADV_FEATURES	RW	[31:25]	Reserved		
				[24]	pi_sync_event_mode	0x0	For Camera Mode: 0: Frame Start dont trigger any sync event. 1: Legacy mode. Frame start will trigger a sync event.
				[23:22]	Reserved		
				[21]	en_embedded	0x0	This register allows to use embedded packets for IPI synchronization events.
				[20]	en_blanking	0x0	This register allows to use blanking packets for IPI synchronization events.
				[19]	en_null	0x0	This register allows to use null packets for IPI synchronization events.
				[18]	en_line_start	0x0	This register allows to use line start packets for IPI synchronization events.
				[17]	en_video	0x0	This register allows to use video packets for IPI synchronization events.
				[16]	line_event_selection	0x0	For Camera Mode, this register allows to manualy select the Packet for line delimiter as follows: 0: Controller select it automatically. 1: Select packets from list programmed in [17:21].
				[15:14]	Reserved		
				[13:8]	ipi_dt	0x0	Datatype to overwrite.
				[7:1]	Reserved		
				[0]	ipi_dt_overwrite	0x0	Ignore datatype of the header using the programed datatype for decoding.
	B0H	IPI_VSA_LINES	RW	[31:10]	Reserved		

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[9:0]	ipi_vsa_lines	0x0	This field configures the Vertical Synchronism Active period measured in number of horizontal lines.
B4H	IPI_VBP_LINES	RW	[31:10]	Reserved		
			[9:0]	ipi_vbp_lines	0x0	This field configures the Vertical Back Porch period measured in number of horizontal lines.
B8H	IPI_VFP_LINES	RW	[31:10]	Reserved		
			[9:0]	ipi_vfp_lines	0x0	This field configures the Vertical Front Porch period measured in number of horizontal lines.
BCH	IPI_VACTIVE_LINES	RW	[31:10]	Reserved		
			[9:0]	ipi_vactive_lines	0x0	This field configures the Vertical Active period measured in number of horizontal lines.
CCH	PHY_CAL	RO	[31:1]	Reserved		
			[0]	rxskewcalhs	0x0	A low-to-high transition on rxskewcalhs signal means that the PHY has initiated the de-skew calibration.
E0H	INT_ST_PHY_FATAL	RO	[31:4]	Reserved		
			[3]	phy_errsotsynchs_3	0x0	Start of transmission error on data lane 3 (no synchronization achieved).
			[2]	phy_errsotsynchs_2	0x0	Start of transmission error on data lane 2 (no synchronization achieved).
			[1]	phy_errsotsynchs_1	0x0	Start of transmission error on data lane 1 (no synchronization achieved).
			[0]	phy_errsotsynchs_0	0x0	Start of transmission error on data lane 0 (no synchronization achieved).
E4H	INT_MSK_PHY_FATAL	RW	[31:4]	Reserved		
			[3]	mask_phy_errsotsynchs_3	0x0	Mask for phy_errsotsynchs_3.
			[2]	mask_phy_errsotsynchs_2	0x0	Mask for phy_errsotsynchs_2.
			[1]	mask_phy_errsotsynchs_1	0x0	Mask for phy_errsotsynchs_1.
			[0]	mask_phy_errsotsynchs_0	0x0	Mask for phy_errsotsynchs_0.
E8H	INT_FORCE_PHY_FATAL	RW	[31:4]	Reserved		
			[3]	Force_phy_errsotsynchs_3	0x0	Force phy_errsotsynchs_3.
			[2]	Force_phy_errsotsynchs_2	0x0	Force phy_errsotsynchs_2.
			[1]	Force_phy_errsotsynchs_1	0x0	Force phy_errsotsynchs_1.
			[0]	Force_phy_errsotsynchs_0	0x0	Force phy_errsotsynchs_0.
F0H	INT_ST_PKT_FATAL	RO	[31:17]	Reserved		
			[16]	err_ecc_double	0x0	D-PHY mode : Header ECC contains at least 2 errors, unrecoverable.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[31:4]	Reserved		
				[3]	vc3_err_crc	0x0	Payload Checksum error detected on virtual channel 3.
				[2]	vc2_err_crc	0x0	Payload Checksum error detected on virtual channel 2.
				[1]	vc1_err_crc	0x0	Payload Checksum error detected on virtual channel 1.
				[0]	vc0_err_crc	0x0	Payload Checksum error detected on virtual channel 0.
	F4H	INT_MASK_PKT_FATAL	RW	[31:17]	Reserved		
				[16]	mask_err_ecc_double	0x0	Mask for err_ecc_double.
				[31:4]	Reserved		
				[3]	mask_vc3_err_crc	0x0	Mask for vc3_err_crc.
				[2]	mask_vc2_err_crc	0x0	Mask for vc2_err_crc.
				[1]	mask_vc1_err_crc	0x0	Mask for vc1_err_crc.
				[0]	mask_vc0_err_crc	0x0	Mask for vc0_err_crc.
	F8H	INT_FORCE_PKT_FATAL	RW	[31:17]	Reserved		
				[16]	Force_err_ecc_double	0x0	Force err_ecc_double.
				[31:4]	Reserved		
				[3]	Force_vc3_err_crc	0x0	Force vc3_err_crc.
				[2]	Force_vc2_err_crc	0x0	Force vc2_err_crc.
				[1]	Force_vc1_err_crc	0x0	Force vc1_err_crc.
				[0]	Force_vc0_err_crc	0x0	Force vc0_err_crc.
	100H	INT_ST_FRAME_FATAL	RO	[31:20]	Reserved		
				[19]	err_frame_data_vc3	0x0	Last received Frame in virtual channel 3, had at least one CRC error.
				[18]	err_frame_data_vc2	0x0	Last received Frame in virtual channel 2, had at least one CRC error.
				[17]	err_frame_data_vc1	0x0	Last received Frame in virtual channel 1, had at least one CRC error.
				[16]	err_frame_data_vc0	0x0	Last received Frame in virtual channel 0, had at least one CRC error.
				[15:12]	Reserved		
				[11]	err_f_seq_vc3	0x0	Incorrect Frame sequence detected in Virtual Channel 3.
				[10]	err_f_seq_vc2	0x0	Incorrect Frame sequence detected in Virtual Channel 2.
				[9]	err_f_seq_vc1	0x0	Incorrect Frame sequence detected in Virtual Channel 1.
				[8]	err_f_seq_vc0	0x0	Incorrect Frame sequence detected in Virtual Channel 0.
				[7:4]	Reserved		
				[3]	err_f_bndry_match_vc3	0x0	Error matching Frame Start with Frame End for virtual channel 3.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	err_f_bndry_match_vc2	0x0	Error matching Frame Start with Frame End for virtual channel 2.
				[1]	err_f_bndry_match_vc1	0x0	Error matching Frame Start with Frame End for virtual channel 1.
				[0]	err_f_bndry_match_vc0	0x0	Error matching Frame Start with Frame End for virtual channel 0.
	104H	INT_MSK_FRAME_FATAL	RW	[31:20]	Reserved		
				[19]	mask_err_frame_data_vc3	0x0	Mask for err_frame_data_vc3.
				[18]	mask_err_frame_data_vc2	0x0	Mask for err_frame_data_vc2.
				[17]	mask_err_frame_data_vc1	0x0	Mask for err_frame_data_vc1.
				[16]	mask_err_frame_data_vc0	0x0	Mask for err_frame_data_vc0.
				[15:12]	Reserved		
				[11]	mask_err_f_seq_vc3	0x0	Mask for err_f_seq_vc3
				[10]	mask_err_f_seq_vc2	0x0	Mask for err_f_seq_vc2
				[9]	mask_err_f_seq_vc1	0x0	Mask for err_f_seq_vc1
				[8]	mask_err_f_seq_vc0	0x0	Mask for err_f_seq_vc0
				[7:4]	Reserved		
				[3]	mask_err_f_bndry_match_vc3	0x0	Mask for err_f_bndry_match_vc3
				[2]	mask_err_f_bndry_match_vc2	0x0	Mask for err_f_bndry_match_vc2
				[1]	mask_err_f_bndry_match_vc1	0x0	Mask for err_f_bndry_match_vc1
				[0]	mask_err_f_bndry_match_vc0	0x0	Mask for err_f_bndry_match_vc0
	108H	INT_FORCE_FRAME_FATA	RW	[31:20]	Reserved		
				[19]	Force_err_frame_data_vc3	0x0	Force err_frame_data_vc3.
				[18]	Force_err_frame_data_vc2	0x0	Force err_frame_data_vc2.
				[17]	Force_err_frame_data_vc1	0x0	Force err_frame_data_vc1.
				[16]	Force_err_frame_data_vc0	0x0	Force err_frame_data_vc0.
				[15:12]	Reserved		
				[11]	Force_err_f_seq_vc3	0x0	Force err_f_seq_vc3.
				[10]	Force_err_f_seq_vc2	0x0	Force err_f_seq_vc2.
				[9]	Force_err_f_seq_vc1	0x0	Force err_f_seq_vc1.
				[8]	Force_err_f_seq_vc0	0x0	Force err_f_seq_vc0.

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:4]	Reserved		
				[3]	Force_err_f_bndry_match_vc3	0x0	Force err_f_bndry_match_vc3.
				[2]	Force_err_f_bndry_match_vc2	0x0	Force err_f_bndry_match_vc2.
				[1]	Force_err_f_bndry_match_vc1	0x0	Force err_f_bndry_match_vc1.
				[0]	Force_err_f_bndry_match_vc0	0x0	Force err_f_bndry_match_vc0.
	110H	INT_ST_PHY	RO	[31:20]	Reserved		
				[19]	phy_erresc_3	0x0	Escope mode Error on data lane 3.
				[18]	phy_erresc_2	0x0	Escope mode Error on data lane 2.
				[17]	phy_erresc_1	0x0	Escope mode Error on data lane 1.
				[16]	phy_erresc_0	0x0	Escope mode Error on data lane 0.
				[15:4]	Reserved		
				[3]	phy_errsoths_3	0x0	Start of transmission error on data lane 3 (synchronization can still be achieved).
				[2]	phy_errsoths_2	0x0	Start of transmission error on data lane 2 (synchronization can still be achieved).
				[1]	phy_errsoths_1	0x0	Start of transmission error on data lane 1 (synchronization can still be achieved).
				[0]	phy_errsoths_0	0x0	Start of transmission error on data lane 0 (synchronization can still be achieved).
	114H	INT_MSK_PHY	RW	[31:20]	Reserved		
				[19]	mask_phy_erresc_3	0x0	Mask for phy_erresc_3.
				[18]	mask_phy_erresc_2	0x0	Mask for phy_erresc_2.
				[17]	mask_phy_erresc_1	0x0	Mask for phy_erresc_1.
				[16]	mask_phy_erresc_0	0x0	Mask for phy_erresc_0.
				[15:4]	Reserved		
				[3]	mask_phy_errsoths_3	0x0	Mask for phy_errsoths_3.
				[2]	mask_phy_errsoths_2	0x0	Mask for phy_errsoths_2.
				[1]	mask_phy_errsoths_1	0x0	Mask for phy_errsoths_1.

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MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	mask_phy_errsoths_0	0x0	Mask for phy_errsoths_0.
	118H	INT_FORCE_PHY	RW	[31:20]	Reserved		
				[19]	Force_phy_erresc_3	0x0	Force phy_erresc_3.
				[18]	Force_phy_erresc_2	0x0	Force phy_erresc_2.
				[17]	Force_phy_erresc_1	0x0	Force phy_erresc_1.
				[16]	Force_phy_erresc_0	0x0	Force phy_erresc_0.
				[15:4]	Reserved		
				[3]	Force_phy_errsoths_3	0x0	Force phy_errsoths_3.
				[2]	Force_phy_errsoths_2	0x0	Force phy_errsoths_2.
				[1]	Force_phy_errsoths_1	0x0	Force phy_errsoths_1.
				[0]	Force_phy_errsoths_0	0x0	Force phy_errsoths_0.
	120H	INT_ST_PKT	RO	[31:20]	Reserved		
				[19]	vc3_err_ecc_corrected	0x0	D-PHY mode : Header error detected and corrected on virtual channel 3.
				[18]	vc2_err_ecc_corrected	0x0	D-PHY mode : Header error detected and corrected on virtual channel 2.
				[17]	vc1_err_ecc_corrected	0x0	D-PHY mode : Header error detected and corrected on virtual channel 1.
				[16]	vc0_err_ecc_corrected	0x0	D-PHY mode : Header error detected and corrected on virtual channel 0.
				[15:4]	Reserved		
				[3]	err_id_vc3	0x0	Unrecognized or unimplemented data type detected in virtual channel 3.
				[2]	err_id_vc2	0x0	Unrecognized or unimplemented data type detected in virtual channel 2.
				[1]	err_id_vc1	0x0	Unrecognized or unimplemented data type detected in virtual channel 1.
				[0]	err_id_vc0	0x0	Unrecognized or unimplemented data type detected in virtual channel 0.
	124H	INT_MSK_PKT	RW	[31:20]	Reserved		
				[19]	mask_vc3_err_ecc_corrected	0x0	Mask for vc3_err_ecc_corrected.
				[18]	mask_vc2_err_ecc_corrected	0x0	Mask for vc2_err_ecc_corrected.
				[17]	mask_vc1_err_ecc_corrected	0x0	Mask for vc1_err_ecc_corrected.
				[16]	mask_vc0_err_ecc_corrected	0x0	Mask for vc0_err_ecc_corrected.
				[15:4]	Reserved		
				[3]	mask_err_id_vc3	0x0	Mask for err_id_vc3.
				[2]	mask_err_id_vc2	0x0	Mask for err_id_vc2.
				[1]	mask_err_id_vc1	0x0	Mask for err_id_vc1.
				[0]	mask_err_id_vc0	0x0	Mask for err_id_vc0.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
128H	INT_FORCE_PKT	RW	[31:20]	Reserved		
			[19]	Force_vc3_err_ecc_corrected	0x0	Force vc3_err_ecc_corrected.
			[18]	Force_vc2_err_ecc_corrected	0x0	Force vc2_err_ecc_corrected.
			[17]	Force_vc1_err_ecc_corrected	0x0	Force vc1_err_ecc_corrected.
			[16]	Force_vc0_err_ecc_corrected	0x0	Force vc0_err_ecc_corrected.
			[15:4]	Reserved		
			[3]	Force_err_id_vc3	0x0	Force err_id_vc3.
			[2]	Force_err_id_vc2	0x0	Force err_id_vc2.
			[1]	Force_err_id_vc1	0x0	Force err_id_vc1.
			[0]	Force_err_id_vc0	0x0	Force err_id_vc0.
140H	INT_ST_IPI	RO	[31:6]	Reserved		
			[5]	int_event_fifo_overflow	0x0	Reporting internal fifo overflow.
			[4]	pixel_if_hline_err	0x0	Horizontal line time error (only available in controller mode).
			[3]	pixel_if_fifo_nempty_fs	0x0	The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked.
			[2]	pixel_if_frame_sync_err	0x0	New frame is received but previous has not been completed.
			[1]	pixel_if_fifo_overflow	0x0	The FIFO of pixel interface has lost information because some more data arrived when it was full.
			[0]	pixel_if_fifo_underflow	0x0	The FIFO has become empty before the expected number of pixels (calculated from the packet's header) could be extracted to the pixel interface.
144H	INT_MSK_IPI	RW	[31:6]	Reserved		
			[5]	mask_int_event_fifo_overflow	0x0	Mask int_event_fifo_overflow.
			[4]	mask_pixel_if_hline_err	0x0	Mask pixel_if_hline_err.
			[3]	mask_pixel_if_fifo_nempty_fs	0x0	Mask pixel_if_fifo_nempty_fs.
			[2]	mask_pixel_if_frame_sync_err	0x0	Mask pixel_if_frame_sync_err.

MIPI CSI-2 Host

BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[1]	mask_pixel_if_fifo_overflow	0x0	Mask pixel_if_fifo_overflow.
			[0]	mask_pixel_if_fifo_underflow	0x0	Mask pixel_if_fifo_underflow.
148H	INT_FORCE_IPI	RW	[31:6]	Reserved		
			[5]	Force_int_event_fifo_overflow	0x0	Force int_event_fifo_overflow.
			[4]	Force_pixel_if_hline_err	0x0	Force pixel_if_hline_err.
			[3]	Force_pixel_if_fifo_nempty_fs	0x0	Force pixel_if_fifo_nempty_fs.
			[2]	Force_pixel_if_frame_sync_err	0x0	Force pixel_if_frame_sync_err.
			[1]	Force_pixel_if_fifo_overflow	0x0	Force pixel_if_fifo_overflow.
			[0]	Force_pixel_if_fifo_underflow	0x0	Force pixel_if_fifo_underflow.
150H	INT_ST_IPI2	RO	[31:6]	Reserved		
			[5]	int_event_fifo_overflow	0x0	Reporting internal fifo overflow.
			[4]	pixel_if_hline_err	0x0	Horizontal line time error (only available in controller mode).
			[3]	pixel_if_fifo_nempty_fs	0x0	The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked.
			[2]	pixel_if_frame_sync_err	0x0	New frame is received but previous has not been completed.
			[1]	pixel_if_fifo_overflow	0x0	The FIFO of pixel interface has lost information because some more data arrived when it was full.
			[0]	pixel_if_fifo_underflow	0x0	The FIFO has become empty before the expected number of pixels (calculated from the packet's header) could be extracted to the pixel interface.
154H	INT_MSK_IPI2	RW	[31:6]	Reserved		
			[5]	mask_int_event_fifo_overflow	0x0	Mask int_event_fifo_overflow.
			[4]	mask_pixel_if_hline_err	0x0	Mask pixel_if_hline_err.
			[3]	mask_pixel_if_fifo_nempty_fs	0x0	Mask pixel_if_fifo_nempty_fs.
			[2]	mask_pixel_if_frame_sync_err	0x0	Mask pixel_if_frame_sync_err.
			[1]	mask_pixel_if_fifo_overflow	0x0	Mask pixel_if_fifo_overflow.
			[0]	mask_pixel_if_fifo_underflow	0x0	Mask pixel_if_fifo_underflow.

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	158H	INT_FORCE_IPI2	RW	[31:6]	Reserved		
				[5]	Force_int_event_fifo_overflow	0x0	Force int_event_fifo_overflow.
				[4]	Force_pixel_if_hline_err	0x0	Force pixel_if_hline_err.
				[3]	Force_pixel_if_fifo_nempty_fs	0x0	Force pixel_if_fifo_nempty_fs.
				[2]	Force_pixel_if_frame_sync_err	0x0	Force pixel_if_frame_sync_err.
				[1]	Force_pixel_if_fifo_overflow	0x0	Force pixel_if_fifo_overflow.
				[0]	Force_pixel_if_fifo_underflow	0x0	Force pixel_if_fifo_underflow.
	160H	INT_ST_IPI3	RO	[31:6]	Reserved		
				[5]	int_event_fifo_overflow	0x0	Reporting internal fifo overflow.
				[4]	pixel_if_hline_err	0x0	Horizontal line time error (only available in controller mode).
				[3]	pixel_if_fifo_nempty_fs	0x0	The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked.
				[2]	pixel_if_frame_sync_err	0x0	New frame is received but previous has not been completed.
				[1]	pixel_if_fifo_overflow	0x0	The FIFO of pixel interface has lost information because some more data arrived when it was full.
				[0]	pixel_if_fifo_underflow	0x0	The FIFO has become empty before the expected number of pixels (calculated from the packet's header) could be extracted to the pixel interface.
	164H	INT_MSK_IPI3	RW	[31:6]	Reserved		
				[5]	mask_int_event_fifo_overflow	0x0	Mask int_event_fifo_overflow.
				[4]	mask_pixel_if_hline_err	0x0	Mask pixel_if_hline_err.
				[3]	mask_pixel_if_fifo_nempty_fs	0x0	Mask pixel_if_fifo_nempty_fs.
				[2]	mask_pixel_if_frame_sync_err	0x0	Mask pixel_if_frame_sync_err.
				[1]	mask_pixel_if_fifo_overflow	0x0	Mask pixel_if_fifo_overflow.
				[0]	mask_pixel_if_fifo_underflow	0x0	Mask pixel_if_fifo_underflow.
	168H	INT_FORCE_IPI3	RW	[31:6]	Reserved		

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5]	Force_int_event_fifo_overflow	0x0	Force int_event_fifo_overflow.
				[4]	Force_pixel_if_hline_err	0x0	Force pixel_if_hline_err.
				[3]	Force_pixel_if_fifo_nempty_fs	0x0	Force pixel_if_fifo_nempty_fs.
				[2]	Force_pixel_if_frame_sync_err	0x0	Force pixel_if_frame_sync_err.
				[1]	Force_pixel_if_fifo_overflow	0x0	Force pixel_if_fifo_overflow.
				[0]	Force_pixel_if_fifo_underflow	0x0	Force pixel_if_fifo_underflow.
	200H	IPI2_MODE	RW	[31:25]	Reserved		
				[24]	ipi_enable	0x0	This register enables the interface.
				[23:17]	Reserved		
				[16]	ipi_cut_through	0x0	This field indicates cut-through mode state: 0: Cut-through mode inactive. 1: Cut-through mode active.
				[15:9]	Reserved		
				[8]	ipi_color_com	0x0	This field indicates if color mode components are delivered as follows: 0: 48 bits interface. 1: 16 bits interface.
				[7:1]	Reserved		
				[0]	ipi_mode	0x0	This field indicates the video mode transmission type as follows: 0: Camera timing(Pixel Interface 2 only supported in Camera Mode). 1: Controller timing.
	170H	INT_ST_IPI4	RO	[31:6]	Reserved		
				[5]	int_event_fifo_overflow	0x0	Reporting internal fifo overflow.
				[4]	pixel_if_hline_err	0x0	Horizontal line time error (only available in controller mode).
				[3]	pixel_if_fifo_nempty_fs	0x0	The FIFO of pixel interface is not empty at the start of a new frame. If this is expected this interrupt should be masked.
				[2]	pixel_if_frame_sync_err	0x0	New frame is received but previous has not been completed.
				[1]	pixel_if_fifo_overflow	0x0	The FIFO of pixel interface has lost information because some more data arrived when it was full.

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	pixel_if_fifo_underflow	0x0	The FIFO has become empty before the expected number of pixels (calculated from the packet's header) could be extracted to the pixel interface.
	174H	INT_MSK_IPI4	RW	[31:6]	Reserved		
				[5]	mask_int_event_fifo_overflow	0x0	Mask int_event_fifo_overflow.
				[4]	mask_pixel_if_hline_err	0x0	Mask pixel_if_hline_err.
				[3]	mask_pixel_if_fifo_nempty_fs	0x0	Mask pixel_if_fifo_nempty_fs.
				[2]	mask_pixel_if_frame_sync_err	0x0	Mask pixel_if_frame_sync_err.
				[1]	mask_pixel_if_fifo_overflow	0x0	Mask pixel_if_fifo_overflow.
				[0]	mask_pixel_if_fifo_underflow	0x0	Mask pixel_if_fifo_underflow.
	178H	INT_FORCE_IPI4	RW	[31:6]	Reserved		
				[5]	Force_int_event_fifo_overflow	0x0	Force int_event_fifo_overflow.
				[4]	Force_pixel_if_hline_err	0x0	Force pixel_if_hline_err.
				[3]	Force_pixel_if_fifo_nempty_fs	0x0	Force pixel_if_fifo_nempty_fs.
				[2]	Force_pixel_if_frame_sync_err	0x0	Force pixel_if_frame_sync_err.
				[1]	Force_pixel_if_fifo_overflow	0x0	Force pixel_if_fifo_overflow.
				[0]	Force_pixel_if_fifo_underflow	0x0	Force pixel_if_fifo_underflow.
	200H	IPI2_MODE	RW	[31:25]	Reserved		
				[24]	ipi_enable	0x0	This register enables the interface.
				[23:17]	Reserved		
				[16]	ipi_cut_through	0x0	This field indicates cut-through mode state: 0: Cut-through mode inactive. 1: Cut-through mode active.
				[15:9]	Reserved		
				[8]	ipi_color_com	0x0	This field indicates if color mode components are delivered as follows: 0: 48 bits interface. 1: 16 bits interface.

MIPI CSI-2 Host

BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[7:1]	Reserved		
			[0]	ipi_mode	0x0	This field indicates the video mode transmission type as follows: 0: Camera timing(Pixel Interface 2 only supported in Camera Mode). 1: Controller timing.
204H	IPI2_VCID	RW	[31:2]	Reserved		
			[1:0]	ipi_vcid	0x0	Virtual channel of data to be processed by pixel interface 2.
208H	IPI2_DATA_TYPE	RW	[31:9]	Reserved		
			[8]	embedded_data	0x0	This bit enables embedded data processing on IPI interface 2.
			[7:6]	Reserved		
			[5:0]	ipi_data_type	0x0	Data type of data to be processed by pixel interface 2.
20CH	IPI2_MEM_FLUSH	RW	[31:9]	Reserved		
			[8]	ipi_auto_flush	0x0	Memory is automatically flushed at each vsync.
			[7:1]	Reserved		
			[0]	ipi_flush	0x0	Flush IPI2 memory. This bit is auto clear.
210H	IPI2_HSA_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hsa_time	0x0	This field configures the Horizontal Synchronism Active period in pixclk cycles.
214H	IPI2_HBP_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hbp_time	0x0	This field configures the Horizontal Back Porch period in pixclk cycles.
218H	IPI2_HSD_TIME	RW	[31:12]	Reserved		
			[11:0]	ipi_hsd_time	0x0	This field configures the Horizontal Sync Porch delay period in pixclk cycles.
21CH	IPI2_ADV_FEATURES	RW	[31:25]	Reserved		
			[24]	pi_sync_event_mode	0x0	For Camera Mode: 0: Frame Start does not trigger any sync event. 1: Legacy mode. Frame start will trigger a sync event.
			[23:22]	Reserved		
			[21]	en_embedded	0x0	This register allows to use embedded packets for IPI synchronization events.
			[20]	en_blanking	0x0	This register allows to use blanking packets for IPI synchronization events.
			[19]	en_null	0x0	This register allows to use null packets for IPI synchronization events.
			[18]	en_line_start	0x0	This register allows to use line start packets for IPI synchronization events.

MIPI CSI-2 Host

BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[17]	en_video	0x0	This register allows to use video packets for IPI synchronization events.
			[16]	line_event_selection	0x0	For Camera Mode, this register allows to manualy select the Packet for line delimiter as follows: 0: Controller select it automatically. 1: Select packets from list programmed in bits[17:21].
			[15:14]	Reserved		
			[13:8]	ipi_dt	0x0	Datatype to overwrite.
			[7:1]	Reserved		
			[0]	ipi_dt_overwrite	0x0	Ignore datatype of the header using the programed datatype for decoding.
220H	IPI3_MODE	RW	[31:25]	Reserved		
			[24]	ipi_enable	0x0	This register enables the interface.
			[23:17]	Reserved		
			[16]	ipi_cut_through	0x0	This field indicates cut-through mode state: 0: Cut-through mode inactive. 1: Cut-through mode active.
			[15:9]	Reserved		
			[8]	ipi_color_com	0x0	This field indicates if color mode components are delivered as follows: 0: 48 bits interface. 1: 16 bits interface.
			[7:1]	Reserved		
			[0]	ipi_mode	0x0	This field indicates the video mode transmission type as follows: 0: Camera timing(Pixel Interface 2 only supported in Camera Mode). 1: Controller timing.
224H	IPI3_VCID	RW	[31:2]	Reserved		
			[1:0]	ipi_vcid	0x0	Virtual channel of data to be processed by pixel interface 2.
228H	IPI3_DATA_TYPE	RW	[31:9]	Reserved		
			[8]	embedded_data	0x0	This bit enables embedded data processing on IPI interface 2.
			[7:6]	Reserved		
			[5:0]	ipi_data_type	0x0	Data type of data to be processed by pixel interface 2.
22CH	IPI3_MEM_FLUSH	RW	[31:9]	Reserved		
			[8]	ipi_auto_flush	0x0	Memory is automatically flushed at each vsync.

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MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:1]	Reserved		
				[0]	ipi_flush	0x0	Flush IPI3 memory. This bit is auto clear.
	220H	IPI3_HSA_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hsa_time	0x0	This field configures the Horizontal Synchronism Active period in pixclk cycles.
	224H	IPI3_HBP_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hbp_time	0x0	This field configures the Horizontal Back Porch period in pixclk cycles.
	228H	IPI3_HSD_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hsd_time	0x0	This field configures the Horizontal Sync Porch delay period in pixclk cycles.
	22CH	IPI3_ADV_FEATURES	RW	[31:25]	Reserved		
				[24]	pi_sync_event_mode	0x0	For Camera Mode: 0: Frame Start does not trigger any sync event. 1: Legacy mode. Frame start will trigger a sync event.
				[23:22]	Reserved		
				[21]	en_embedded	0x0	This register allows to use embedded packets for IPI synchronization events.
				[20]	en_blanking	0x0	This register allows to use blanking packets for IPI synchronization events.
				[19]	en_null	0x0	This register allows to use null packets for IPI synchronization events.
				[18]	en_line_start	0x0	This register allows to use line start packets for IPI synchronization events.
				[17]	en_video	0x0	This register allows to use video packets for IPI synchronization events.
				[16]	line_event_selection	0x0	For Camera Mode, this register allows to manualy select the Packet for line delimiter as follows: 0: Controller select it automatically. 1: Select packets from list programmed in bits[17:21].
				[15:14]	Reserved		
				[13:8]	ipi_dt	0x0	Datatype to overwrite.
				[7:1]	Reserved		
				[0]	ipi_dt_overwrite	0x0	Ignore datatype of the header using the programed datatype for decoding.
	240H	IPI4_MODE	RW	[31:25]	Reserved		
				[24]	ipi_enable	0x0	This register enables the interface.

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23:17]	Reserved		
				[16]	ipi_cut_through	0x0	This field indicates cut-through mode state: 0: Cut-through mode inactive. 1: Cut-through mode active.
				[15:9]	Reserved		
				[8]	ipi_color_com	0x0	This field indicates if color mode components are delivered as follows: 0: 48 bits interface. 1: 16 bits interface.
				[7:1]	Reserved		
				[0]	ipi_mode	0x0	This field indicates the video mode transmission type as follows: 0: Camera timing(Pixel Interface 2 only supported in Camera Mode). 1: Controller timing.
	244H	IPI4_VCID	RW	[31:2]	Reserved		
				[1:0]	ipi_vcid	0x0	Virtual channel of data to be processed by pixel interface 2.
	248H	IPI4_DATA_TYPE	RW	[31:9]	Reserved		
				[8]	embedded_data	0x0	This bit enables embedded data processing on IPI interface 2.
				[7:6]	Reserved		
				[5:0]	ipi_data_type	0x0	Data type of data to be processed by pixel interface 2.
	24CH	IPI4_MEM_FLUSH	RW	[31:9]	Reserved		
				[8]	ipi_auto_flush	0x0	Memory is automatically flushed at each vsync.
				[7:1]	Reserved		
				[0]	ipi_flush	0x0	Flush IPI4 memory. This bit is auto clear.
	250H	IPI4_HSA_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hsa_time	0x0	This field configures the Horizontal Synchronism Active period in pixclk cycles.
	254H	IPI4_HBP_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hbp_time	0x0	This field configures the Horizontal Back Porch period in pixclk cycles.
	258H	IPI4_HSD_TIME	RW	[31:12]	Reserved		
				[11:0]	ipi_hsd_time	0x0	This field configures the Horizontal Sync Porch delay period in pixclk cycles.
	25CH	IPI4_ADV_FEATURES	RW	[31:25]	Reserved		

MIPI CSI-2 Host	BASE_ADDR: 0xA4350000, 0xA4350800, 0xA4351000, 0xA4351800						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[24]	pi_sync_event_mode	0x0	For Camera Mode: 0: Frame Start does not trigger any sync event. 1: Legacy mode. Frame start will trigger a sync event.
				[23:22]	Reserved		
				[21]	en_embedded	0x0	This register allows to use embedded packets for IPI synchronization events.
				[20]	en_blanking	0x0	This register allows to use blanking packets for IPI synchronization events.
				[19]	en_null	0x0	This register allows to use null packets for IPI synchronization events.
				[18]	en_line_start	0x0	This register allows to use line start packets for IPI synchronization events.
				[17]	en_video	0x0	This register allows to use video packets for IPI synchronization events.
				[16]	line_event_selection	0x0	For Camera Mode, this register allows to manualy select the Packet for line delimiter as follows: 0: Controller select it automatically. 1: Select packets from list programmed in bits[17:21].
				[15:14]	Reserved		
				[13:8]	ipi_dt	0x0	Datatype to overwrite.
				[7:1]	Reserved		
				[0]	ipi_dt_overwrite	0x0	Ignore datatype of the header using the programed datatype for decoding.
	300H	SCRAMBLING	RW	[31:1]	Reserved		
				[0]	scramble_enable	0x0	Enables data de-scrambling on the controller side.
	304H	SCRAMBLING_SEED1	RW	[31:16]	Reserved		
				[15:0]	scramble_seed_lane1	0x1008	Seed used by De-scrambler block for lane 1.
	308H	SCRAMBLING_SEED2	RW	[31:16]	Reserved		
				[15:0]	scramble_seed_lane2	0x1188	Seed used by De-scrambler block for lane 2.
	30CH	SCRAMBLING_SEED3	RW	[31:16]	Reserved		
				[15:0]	scramble_seed_lane3	0x1248	Seed used by De-scrambler block for lane 3.
	310H	SCRAMBLING_SEED4	RW	[31:16]	Reserved		
				[15:0]	scramble_seed_lane4	0x13c8	Seed used by De-scrambler block for lane 4.

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	VERSION	RO	[31:0]	version	0x3133312a	This field indicates the version of the mipi_csi2_device.
04H	CSI2_RESETN	RW	[31:1]	Reserved		
			[0]	csi2_resetn_rw	0x0	The mipi_csi2_device reset output. Active Low.Can reset all the logic module except APB.
20H	INT_ST_MAIN	RC	[31:4]	Reserved		
			[3]	int_st_phy	0x0	Status of INT_ST_PHY interrupt source group: 0: Interrupt source group is inactive. 1: Interrupt source group is active.
			[2]	int_st_ipi	0x0	Status of INT_ST_IPI interrupt source group: 0: Interrupt source group is inactive. 1: Interrupt source group is active.
			[1]	Reserved		
			[0]	int_st_vpg	0x0	Status of INT_ST_VPG interrupt source group: 0: Interrupt source group is inactive. 1: Interrupt source group is active.
24H	INT_ST_VPG	RC	[31:1]	Reserved		
			[0]	vpg_pkt_lost	0x0	Packet lost of video pattern generator.
2CH	INT_ST_IPI	RC	[31:28]	Reserved		
			[27]	ipi4_fifo_underflow	0x0	The IPI4 Payload FIFO has lost information because read data when it was already empty. This is used for Cut through Mode.
			[26]	ipi4_errline	0x0	Indicator for inconsistent between IPI4 line configuration and the number of input lines.
			[25]	ipi4_fifo_overflow	0x0	The IPI4 Header FIFO or Payload FIFO has lost information because data arrived when it was already full.
			[24]	ipi4_errpixel	0x0	Indicator for inconsistent between IPI4 Pixel configuration and the number of input pixels.
			[23:20]	Reserved		
			[19]	ipi3_fifo_underflow	0x0	The IPI3 Payload FIFO has lost information because read data when it was already empty. This is used for Cut through Mode.
			[18]	ipi3_errline	0x0	Indicator for inconsistent between IPI3 line configuration and the number of input lines.
			[17]	ipi3_fifo_overflow	0x0	The IPI3 Header FIFO or Payload FIFO has lost information because data arrived when it was already full.
			[16]	ipi3_errpixel	0x0	Indicator for inconsistent between IPI3 Pixel configuration and the number of input pixels.

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[15:12]	Reserved		
			[11]	ipi2_fifo_underflow	0x0	The IPI2 Payload FIFO has lost information because read data when it was already empty. This is used for Cut through Mode.
			[10]	ipi2_errline	0x0	Indicator for inconsistent between IPI2 line configuration and the number of input lines.
			[9]	ipi2_fifo_overflow	0x0	The IPI2 Header FIFO or Payload FIFO has lost information because data arrived when it was already full.
			[8]	ipi2_errpixel	0x0	Indicator for inconsistent between IPI2 Pixel configuration and the number of input
			[7:5]	Reserved		
			[4]	ipi_trans_conflict	0x0	This bit indicates that IPI packet transmission is in conflict with IDI interface.
			[3]	ipi_fifo_underflow	0x0	The IPI Payload FIFO has lost information because read data when it was already empty. This is used for Cut through Mode.
			[2]	ipi_errline	0x0	Indicator for inconsistent between IPI line configuration and the number of input lines.
			[1]	ipi_fifo_overflow	0x0	The IPI Header FIFO or Payload FIFO has lost information because data arrived when it was already full.
			[0]	ipi_errpixel	0x0	Indicator for inconsistent between IPI Pixel configuration and the number of input pixels.
30H	INT_ST_PHY	RC	[31:3]	Reserved	0x0	
			[2]	errcontentionlp1	0x0	This bit indicates LP1 contention error ErrContentionLP1 from Lane 0.
			[1]	errcontentionlp0	0x0	This bit indicates LP0 contention error ErrContentionLP0 from Lane 0.
			[0]	to_hs_tx	0x0	This bit indicates that the high-speed transmission timeout counter reached the end and contention has been detected.
40H	INT_MASK_N_VPG	RW	[31:1]	Reserved		
			[0]	mask_vpg_pkt_lost	0x0	Mask for vpg_pkt_lost.
44H	INT_FORCE_VPG	WC	[31:1]	Reserved		
			[0]	force_vpg_pkt_lost	0x0	Force for vpg_pkt_lost.
50H	INT_MASK_N_IPI	RW	[31:28]	Reserved		
			[27]	mask_ipi4_fifo_underflo	0x0	Mask for ipi4_fifo_underflow.
			[26]	mask_ipi4_errline	0x0	Mask for ipi4_errline.
			[25]	mask_ipi4_fifo_overflow	0x0	Mask for ipi4_fifo_overflow.
			[24]	mask_ipi4_errpixel	0x0	Mask for ipi4_errpixel.
			[23:20]	Reserved		
			[19]	mask_ipi3_fifo_underflo	0x0	Mask for ipi3_fifo_underflow.
			[18]	mask_ipi3_errline	0x0	Mask for ipi3_errline.
			[17]	mask_ipi3_fifo_overflow	0x0	Mask for ipi3_fifo_overflow.

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[16]	mask_ipi3_errpixel	0x0	Mask for ipi3_errpixel.
			[15:12]	Reserved		
			[11]	mask_ipi2_fifo_underflo	0x0	Mask for ipi2_fifo_underflow.
			[10]	mask_ipi2_errline	0x0	Mask for ipi2_errline.
			[9]	mask_ipi2_fifo_overflow	0x0	Mask for ipi2_fifo_overflow.
			[8]	mask_ipi2_errpixel	0x0	Mask for ipi2_errpixel.
			[7:5]	Reserved		
			[4]	mask_ipi_trans_conflict		Mask for ipi_trans_conflict
			[3]	mask_ipi_fifo_underflow	0x0	Mask for ipi_fifo_underflow.
			[2]	mask_ipi_errline	0x0	Mask for ipi_errline.
			[1]	mask_ipi_fifo_overflow	0x0	Mask for ipi_fifo_overflow.
			[0]	mask_ipi_errpixel	0x0	Mask for ipi_errpixel.
54H	INT_FORCE_IPI	WC	[31:28]	Reserved		
			[27]	force_ipi4_fifo_underflo	0x0	Force for ipi4_fifo_underflow.
			[26]	force_ipi4_errline	0x0	Force for ipi4_errline.
			[25]	force_ipi4_fifo_overflow	0x0	Force for ipi4_fifo_overflow.
			[24]	force_ipi4_errpixel	0x0	Force for ipi4_errpixel.
			[23:20]	Reserved		
			[19]	force_ipi3_fifo_underflo	0x0	Force for ipi3_fifo_underflow.
			[18]	force_ipi3_errline	0x0	Force for ipi3_errline.
			[17]	force_ipi3_fifo_overflow	0x0	Force for ipi3_fifo_overflow.
			[16]	force_ipi3_errpixel	0x0	Force for ipi3_errpixel.
			[15:12]	Reserved		
			[11]	force_ipi2_fifo_underflo	0x0	Force for ipi2_fifo_underflow.
			[10]	force_ipi2_errline	0x0	Force for ipi2_errline.
			[9]	force_ipi2_fifo_overflow	0x0	Force for ipi2_fifo_overflow.
			[8]	force_ipi2_errpixel	0x0	Force for ipi2_errpixel.
			[7:5]	Reserved		
			[3]	force_ipi_fifo_underflow	0x0	Force for ipi_fifo_underflow.
			[2]	force_ipi_errline	0x0	Force for ipi_errline.
			[1]	force_ipi_fifo_overflow	0x0	Force for ipi_fifo_overflow.
			[0]	force_ipi_errpixel	0x0	Force for ipi_errpixel.
58H	INT_MASK_N_PHY	RW	[31:3]	Reserved	0x0	

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[2]	mask_errcontentionlp1	0x0	Mask for errcontentionlp1.
			[1]	mask_errcontentionlp0	0x0	Mask for errcontentionlp0.
			[0]	mask_to_hs_tx	0x0	Mask for to_hs_tx.
5CH	INT_FORCE_PHY	WC	[31:3]	Reserved	0x0	
			[2]	force_errcontentionlp1	0x0	Force for errcontentionlp1.
			[1]	force_errcontentionlp0	0x0	Force for errcontentionlp0.
			[0]	force_to_hs_tx	0x0	Force for to_hs_tx.
80H	VPG_CTRL	RW	[31:1]	Reserved	0x0	
			[0]	vpg_en	0x0	Video pattern generator enable signal. Active High.
84H	VPG_STATUS	RO	[31:1]	Reserved	0x0	
			[0]	vpg_active	0x0	Video pattern status: 0: One video pattern transmission finished and the next transmission can be started. 1: Video pattern generation is running and vpg_en should not be set to 1 again.
88H	VPG_MODE_CFG	RW	[31:17]	Reserved	0x0	
			[16]	vpg_orientation	0x0	This field indicates the color bar orientation: 0: Vertical Mode. 1: Horizontal Mode.
			[15:1]	Reserved	0x0	
			[0]	vpg_mode	0x0	Pattern Type: 0: Color bar(verrtical or horizontal). 1: BER pattern(vertical only).
8CH	VPG_PKT_CFG	RW	[31:12]	Reserved		
			[11]	vpg_frame_num_mode	0x0	This field indicates the frame number mode: 0: Frame Number Zero mode. 1: Frame Number Increments One mode.
			[10:9]	vpg_line_num_mode	0x0	This field indicates line number mode: 00: Line Number Zero mode. 01: Line Number Increments One mode. 10: Line Number Increments Arbitrary Value mode. 11: Reserved.
			[8]	vpg_hsync_pkt_en	0x0	This field indicates the line synchronization packets mode: 0: Don't transmit line synchronization packets. 1: Transmit line synchronization packets.
			[7:6]	vpg_vc	0x0	The Virtual Channel of video pattern packet.

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MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[5:0]	vpg_dt	0x0	The Data Type of video pattern packet.
90H	VPG_PKT_SIZE	RW	[31:14]	Reserved	0x0	
			[13:0]	vpg_pkt_size	0x0	The number of pixels in a single video pattern packet.
94H	VPG_HSA_TIME	RW	[31:12]	Reserved	0x0	
			[11:0]	vpg_hsa_time	0x0	The configuration of horizontal synchronism active period in lane byte clock domain. The smallest value is 1.
98H	VPG_HBP_TIME	RW	[31:12]	Reserved	0x0	
			[11:0]	vpg_hbp_time	0x0	The configuration of horizontal back porch period in lane byte clock domain. The smallest value is 1.
9CH	VPG_HLINE_TIME	RW	[31:15]	Reserved	0x0	
			[14:0]	vpg_hline_time	0x0	The size of total line time(HAS + HBP + HACT + HFP) counted in lane byte clock domain.
A0H	VPG_VSA_LINES	RW	[31:10]	Reserved	0x0	
			[9:0]	vpg_vsa_lines	0x0	The vertical synchronism active period measured in number of horizontal lines. The smallest value is 1.
A4H	VPG_VBP_LINES	RW	[31:10]	Reserved	0x0	
			[9:0]	vpg_vbp_lines	0x0	The vertical back porch period measured in number of horizontal lines. The smallest value is 1.
A8H	VPG_VFP_LINES	RW	[31:10]	Reserved	0x0	
			[9:0]	vpg_vfp_lines	0x0	The vertical front porch period measured in number of horizontal lines. The smallest value is 1.
ACH	VPG_ACT_LINES	RW	[31:14]	Reserved	0x0	
			[13:0]	vpg_act_lines	0x0	The vertical active period measured in number of horizontal lines. The smallest value is
B0H	VPG_MAX_FRAME_NUM	RW	[31:16]	Reserved	0x0	
			[15:0]	vpg_max_frame_num	0x0	Define the max frame number under Frame Number Increments one mode.
B4H	VPG_START_LINE_NUM	RW	[31:16]	Reserved	0x0	
			[15:0]	vpg_start_line_num	0x0	Define the start line number under Line Number Increments Arbitrary Value mode. The value must be a non-zero value.
B8H	VPG_STEP_LINE_NUM	RW	[31:16]	Reserved	0x0	
			[15:0]	vpg_step_line_num	0x0	Define the step value for line number under Line Number Increments Arbitrary Value mode. The value must be greater than one.

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
E0H	PHY_RSTZ	RW	[31:4]	Reserved	0x0	
			[3]	phy_forcepll	0x0	When the D-PHY is in ULPS, this bit enables the D-PHY PLL.
			[2]	phy_enableclk	0x0	When set to 1, this bit enables the D-PHY Clock Lane Module.
			[1]	phy_rstz	0x0	When set to 0, this bit places the digital section of the D-PHY in the reset state.
			[0]	phy_shutdownz	0x0	When set to 0, this bit places the complete D-PHY macro in power-down state.
E4H	PHY_IF_CFG	RW	[31:16]	Reserved	0x0	
			[15:8]	phy_stop_wait_time	0x0	This field configures the minimum wait period to request a highspeed transmission after data lanes return to Stop State.
			[7:3]	Reserved		
			[2:0]	lane_en_num	3	This field configures the number of active data lanes: 000: 1 data lane (lane 0). 001: 2 data lanes (lanes 0 - 1). 010: 3 data lanes (lanes 0 - 2). 011: 4 data lanes (lanes 0 - 3). 100: Reserved 101: Reserved 110: Reserved 111: Reserved Can only be updated when phy_shutdownz and phy_rstz are both low.
E8H	LPCLK_CTRL	RW	[31:1]	Reserved	0x0	
			[0]	phy_txreqclkhs_con	0x0	This bit controls the D-PHY PPI txrequestclkhs signal: 0: Non-continuous clock mode. 1: Continuous clock mode.
ECH	PHY_ULPS_CTRL	RW	[31:4]	Reserved	0x0	
			[3]	phy_txexitulpslan	0x0	ULPS mode Exit on all active data lanes. (when asserted, duration need exceed 1 tx_esc_clk cycle; it can't be asserted with tx_triggers_en at the same time.)
			[2]	phy_txrequlpslan	0x0	ULPS mode Request on all active data lanes. (when asserted, duration need exceed 1 tx_esc_clk cycle; it can't be asserted with tx_triggers_en at the same time.)
			[1]	phy_txexitulpsclk	0x0	ULPS mode Exit on clock lane. (when asserted, duration need exceed 1 tx_esc_clk cycle; it can't be asserted with tx_triggers_en at the same time.)
			[0]	phy_txrequlpsclk	0x0	ULPS mode Request on clock lane. (when asserted, the duration need exceed 1 tx_esc_clk cycle; it can't be asserted with tx_triggers_en at the same time.)
F0H	CLKMGR_CFG	RW	[31:16]	Reserved	0x0	

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MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:8]	to_clk_division	0x0	This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
			[7:0]	tx_esc_clk_division	0x0	This field indicates the division factor for the TX Escape clock source (lanebyteclk). The values 0 and 1 stop the TX_ESC clock generation.
F4H	PHY_TX_TRIGGERS	RW	[31:8]	Reserved	0x0	
			[7]	tx_triggers_en	0x0	This bit is the trigger enable signal, (when asserted, duration must exceed 1 tx_esc_clk cycle), can't be set to 1 when PHY_ULPS_CTRL register is active: 0: No trigger transmission. 1: Trigger active.
			[6:2]	Reserved		
			[1:0]	tx_triggers	0x0	This field activates the trigger transmissions when tx_trigger_en is asserted (when asserted, the duration need exceed 1 tx_esc_clk cycle): 00: Trigger 0 active. 01: Trigger 1 active. 10: Trigger 2 active. 11: Trigger 3 active.
F8H	PHY_CAL	RW	[31:1]	Reserved	0x0	
			[0]	phy_cal	0x0	This bit controls calibration pin of D-PHY: 0: No calibration. 1: High-speed transmit skew calibration is activated.
FCH	TO_CNT_CFG	RW	[31:16]	Reserved	0x0	
			[15:0]	hstx_to_cnt	0x0	This field configures the timeout counter that triggers a high speed transmission timeout contention detection (measured in tx_esc_clk cycles). For CSI2 device, the CSI link returns the LP state once per packet, then you should configure the TO_CLK_DIVISION and hstx_to_cnt to be in accordance with: hstx_to_cnt * lanebyteclkperiod * TO_CLK_DIVISION >= the time of one data packet transmission in PPI * (1 + 10%)
110H	PHY_STATUS	RO	[31:14]	Reserved	0x0	
			[13]	TxUlpsActiveNot_L3	0x1	This bit indicates the status of TxUlpsActiveNot_L3 D-PHY signal.
			[12]	TxStopState_L3	0x0	This bit indicates the status of TxStopState_L3 D-PHY signal.
			[11]	TxUlpsActiveNot_L2	0x1	This bit indicates the status of TxUlpsActiveNot_L2 D-PHY signal.
			[10]	TxStopState_L2	0x0	This bit indicates the status of TxStopState_L2 D-PHY signal.
			[9]	TxUlpsActiveNot_L1	0x1	This bit indicates the status of TxUlpsActiveNot_L1 D-PHY signal.
			[8]	TxStopState_L1	0x0	This bit indicates the status of TxStopState_L1 D-PHY signal.

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MIPI CSI-2 Device	BASE_ADDR: 0xA4354000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	TxUlpsActiveNot_L0	0x1	This bit indicates the status of TxUlpsActiveNot_L0 D-PHY signal.
				[6]	TxStopState_L0	0x0	This bit indicates the status of TxStopState_L0 D-PHY signal.
				[5]	TxUlpsActiveNot_Clk	0x0	This bit indicates the status of xUlpsActiveNot_Clk D-PHY signal: 0: ULPS state of clock lane. 1: Not ulps state of clock lane.
				[4]	TxStopState_Clk	0x0	This bit indicates the status of TxStopState_Clk D-PHY signal: 0: Not stop state of clock lane. 1: Stop state of clock lane.
				[3]	PLL_Lock	0x0	This bit indicates the status of phylock D-PHY signal: 0: PLL unlocked. 1: PLL locked.
				[2:0]	lane_max_num	0x0	This 3-bit indicates the maximum number of D-PHY lanes.
	114H	PHY0_TST_CTRL0	RW	[31:2]	Reserved		
				[1]	phy0_testclk	0x0	This bit is used to clock the TESTDIN bus into the D-PHY0.
				[0]	phy0_testclr	0x1	PHY0 test interface clear. Active High.
	118H	PHY0_TST_CTRL1	RW	[31:17]	Reserved		
				[16]	phy0_testen	0x0	PHY0 test interface operation selector: 0: the data write operation is set on the rising edge of the testclk signal. 1: the address write operation is set on the falling edge of the testclk signal.
			RO	[15:8]	phy0_testdout	0x0	PHY0 output 8-bit data bus for read-back and internal probing functionalities.
				[7:0]	phy0_testdin	0x0	PHY0 test interface input 8-bit data bus for internal register programming and test functionalities access.
	140H	IPI_PKT_CFG	RW	[31:17]	Reserved		
				[16]	ipi_mode	0x0	This field is to select the IPI mode: 0: Store and Forward Mode Stores the full pixel packet before forwarding. 1: Cut through Mode Initiates the HS transmission to the PHY after the configured number of ipi_clk cycles. Makes use of very shallow memory.
				[15:12]	Reserved		
				[11]	ipi_frame_num_mode	0x0	This field indicates the IPI frame number mode: 0: Frame Number Zero mode. 1: Frame Number Increments One mode.

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MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[10:9]	ipi_line_num_mode	0x0	This field indicates IPI line number mode: 00: Line Number Zero mode. 01: Line Number Increments One mode. 10: Line Number Increments Arbitrary Value mode. 11: Reserved.
			[8]	ipi_hsync_pkt_en	0x1	This field indicates the line synchronization packets mode: 0: Don't transmit line synchronization packets. 1: Transmit line synchronization packets.
			[7:6]	ipi_vc	0x0	The Virtual Channel of IPI packet.
			[5:0]	ipi_dt	0x0	The Data Type of IPI packet.
144H	IPI_PIXELS	RW	[31:17]	Reserved		
			[16:0]	ipi_pixels	0x0	This field configures horizontal resolution for IPI. For YUV, RGB and RAW, this field configures pixel number of data packet for IPI. For User Defined Byte-based Data, this field configures byte number of data packet for IPI.
148H	IPI_MAX_FRAME_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi_max_frame_num	0x0	If Frame Number Increments One mode is selected, this field is to define the max frame number of IPI frame ynchronization packet.
14CH	IPI_START_LINE_NUM	RW	[31:16]	Reserved		
			[15:0]	pi_start_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the start line number of line synchronization packet. The start value must be a non-zero.
150H	IPI_STEP_LINE_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi_step_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the step value for Line number increments. The step value must be greater than 1.
154H	IPI_LINES	RW	[31:17]	Reserved		
			[16:0]	ipi_line	0x0	This field configures line number of a frame for IPI The step value must be greater than 1.
158H	IPI_DATA_SEND_START	RW	[31:17]	Reserved		
			[16:0]	ipi_data_send_start	0x0	This field configures the number of ipi_clk cycles for start to send data packet after the ipi_data_en is asserted in Cut through Mode.
15CH	IPI_FIFO_STATUS	RO	[31:4]	Reserved		
			[3]	ipi_pl_fifo_full	0x0	This field indicates the payload FIFO full status of IPI interface, active HIGH.

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MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[2]	ipi_hd_fifo_full	0x0	This field indicates the header FIFO full status of IPI interface, active HIGH.
			[1]	ipi_pl_fifo_emptyz	0x0	This field indicates the payload FIFO empty status of IPI interface, active LOW.
			[0]	ipi_hd_fifo_emptyz	0x0	This field indicates the header FIFO empty status of IPI interface, active LOW.
200H	IPI2_PKT_CFG	RW	[31:17]	Reserved		
			[16]	ipi2_mode	0x0	This field is to select the ipi2 mode: 0: Store and Forward Mode Stores the full pixel packet before forwarding. 1: Cut through Mode Initiates the HS transmission to the PHY after the configured number of ipi2_clk cycles. Makes use of very shallow memory.
			[15:12]	Reserved		
			[11]	ipi2_frame_num_mode	0x0	This field indicates the ipi2 frame number mode: 0: Frame Number Zero mode. 1: Frame Number Increments One mode.
			[10:9]	ipi2_line_num_mode	0x0	This field indicates ipi2 line number mode: 00: Line Number Zero mode. 01: Line Number Increments One mode. 10: Line Number Increments Arbitrary Value mode. 11: Reserved.
			[8]	ipi2_hsync_pkt_en	0x1	This field indicates the line synchronization packets mode: 0: Don't transmit line synchronization packets. 1: Transmit line synchronization packets.
			[7:6]	ipi2_vc	0x0	The Virtual Channel of ipi2 packet.
			[5:0]	ipi2_dt	0x0	The Data Type of ipi2 packet.
204H	IPI2_PIXELS	RW	[31:17]	Reserved		
			[16:0]	ipi2_pixels	0x0	This field configures horizontal resolution for ipi2. For YUV, RGB and RAW, this field configures pixel number of data packet for ipi2. For User Defined Byte-based Data, this field configures byte number of data packet for ipi2.
208H	IPI2_MAX_FRAME_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi2_max_frame_num	0x0	If Frame Number Increments One mode is selected, this field is to define the max frame number of ipi2 frame ynchronization packet.
20CH	IPI2_START_LINE_NU	RW	[31:16]	Reserved		
			[15:0]	pi_start_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the start line number of line synchronization packet. The start value must be a non-zero.
210H	IPI2_STEP_LINE_NUM	RW	[31:16]	Reserved		

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	ipi2_step_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the step value for Line number increments. The step value must be greater than 1.
214H	IPI2_LINES	RW	[31:17]	Reserved		
			[16:0]	ipi2_line	0x0	This field configures line number of a frame for ipi2 The step value must be greater than 1.
218H	IPI2_DATA_SEND_START	RW	[31:17]	Reserved		
			[16:0]	ipi2_data_send_start	0x0	This field configures the number of ipi2_clk cycles for start to send data packet after the ipi2_data_en is asserted in Cut through Mode.
21CH	IPI2_FIFO_STATUS	RO	[31:4]	Reserved		
			[3]	ipi2_pl_fifo_full	0x0	This field indicates the payload FIFO full status of ipi2 interface, active HIGH.
			[2]	ipi2_hd_fifo_full	0x0	This field indicates the header FIFO full status of ipi2 interface, active HIGH.
			[1]	ipi2_pl_fifo_emptyz	0x0	This field indicates the payload FIFO empty status of ipi2 interface, active LOW.
			[0]	ipi2_hd_fifo_emptyz	0x0	This field indicates the header FIFO empty status of ipi2 interface, active LOW.
240H	IPI3_PKT_CFG	RW	[31:17]	Reserved		
			[16]	ipi3_mode	0x0	This field is to select the ipi3 mode: 0: Store and Forward Mode Stores the full pixel packet before forwarding. 1: Cut through Mode Initiates the HS transmission to the PHY after the configured number of ipi3_clk cycles. Makes use of very shallow memory.
			[15:12]	Reserved		
			[11]	ipi3_frame_num_mode	0x0	This field indicates the ipi3 frame number mode: 0: Frame Number Zero mode. 1: Frame Number Increments One mode.
			[10:9]	ipi3_line_num_mode	0x0	This field indicates ipi3 line number mode: 00: Line Number Zero mode. 01: Line Number Increments One mode. 10: Line Number Increments Arbitrary Value mode. 11: Reserved.
			[8]	ipi3_hsync_pkt_en	0x1	This field indicates the line synchronization packets mode: 0: Don't transmit line synchronization packets. 1: Transmit line synchronization packets.
			[7:6]	ipi3_vc	0x0	The Virtual Channel of ipi3 packet.
			[5:0]	ipi3_dt	0x0	The Data Type of ipi3 packet.
244H	IPI3_PIXELS	RW	[31:17]	Reserved		

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MIPI CSI-2 Device

BASE_ADDR: 0xA4354000						
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[16:0]	ipi3_pixels	0x0	This field configures horizontal resolution for ipi3. For YUV, RGB and RAW, this field configures pixel number of data packet for ipi3. For User Defined Byte-based Data, this field configures byte number of data packet for ipi3.
248H	IPI3_MAX_FRAME_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi3_max_frame_num	0x0	If Frame Number Increments One mode is selected, this field is to define the max frame number of ipi3 frame ynchronization packet.
24CH	IPI3_START_LINE_NU	RW	[31:16]	Reserved		
			[15:0]	pi_start_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the start line number of line synchronization packet. The start value must be a non-zero.
250H	IPI3_STEP_LINE_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi3_step_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the step value for Line number increments. The step value must be greater than 1.
254H	IPI3_LINES	RW	[31:17]	Reserved		
			[16:0]	ipi3_line	0x0	This field configures line number of a frame for ipi3 The step value must be greater than 1.
258H	IPI3_DATA_SEND_START	RW	[31:17]	Reserved		
			[16:0]	ipi3_data_send_start	0x0	This field configures the number of ipi3_clk cycles for start to send data packet after the ipi3_data_en is asserted in Cut through Mode.
25CH	IPI3_FIFO_STATUS	RO	[31:4]	Reserved		
			[3]	ipi3_pl_fifo_full	0x0	This field indicates the payload FIFO full status of ipi3 interface, active HIGH.
			[2]	ipi3_hd_fifo_full	0x0	This field indicates the header FIFO full status of ipi3 interface, active HIGH.
			[1]	ipi3_pl_fifo_emptyz	0x0	This field indicates the payload FIFO empty status of ipi3 interface, active LOW.
			[0]	ipi3_hd_fifo_emptyz	0x0	This field indicates the header FIFO empty status of ipi3 interface, active LOW.
280H	IPI4_PKT_CFG	RW	[31:17]	Reserved		
			[16]	ipi4_mode	0x0	This field is to select the ipi4 mode: 0: Store and Forward Mode Stores the full pixel packet before forwarding. 1: Cut through Mode Initiates the HS transmission to the PHY after the configured number of ipi4_clk cycles. Makes use of very shallow memory.
			[15:12]	Reserved		

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[11]	ipi4_frame_num_mode	0x0	This field indicates the ipi4 frame number mode: 0: Frame Number Zero mode. 1: Frame Number Increments One mode.
			[10:9]	ipi4_line_num_mode	0x0	This field indicates ipi4 line number mode: 00: Line Number Zero mode. 01: Line Number Increments One mode. 10: Line Number Increments Arbitrary Value mode. 11: Reserved.
			[8]	ipi4_hsync_pkt_en	0x1	This field indicates the line synchronization packets mode: 0: Don't transmit line synchronization packets. 1: Transmit line synchronization packets.
			[7:6]	ipi4_vc	0x0	The Virtual Channel of ipi4 packet.
			[5:0]	ipi4_dt	0x0	The Data Type of ipi4 packet.
284H	IPI4_PIXELS	RW	[31:17]	Reserved		
			[16:0]	ipi4_pixels	0x0	This field configures horizontal resolution for ipi4. For YUV, RGB and RAW, this field configures pixel number of data packet for ipi4. For User Defined Byte-based Data, this field configures byte number of data packet for ipi4.
288H	IPI4_MAX_FRAME_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi4_max_frame_num	0x0	If Frame Number Increments One mode is selected, this field is to define the max frame number of ipi4 frame ynchronization packet.
28CH	IPI4_START_LINE_NU	RW	[31:16]	Reserved		
			[15:0]	pi_start_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the start line number of line synchronization packet. The start value must be a non-zero.
290H	IPI4_STEP_LINE_NUM	RW	[31:16]	Reserved		
			[15:0]	ipi4_step_line_num	0x0	If Line Number Increments Arbitrary Value mode is selected, this field is to define the step value for Line number increments. The step value must be greater than 1.
294H	IPI4_LINES	RW	[31:17]	Reserved		
			[16:0]	ipi4_line	0x0	This field configures line number of a frame for ipi4 The step value must be greater than 1.
298H	IPI4_DATA_SEND_START	RW	[31:17]	Reserved		

MIPI CSI-2 Device

BASE_ADDR: 0xA4354000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[16:0]	ipi4_data_send_start	0x0	This field configures the number of ipi4_clk cycles for start to send data packet after the ipi4_data_en is asserted in Cut through Mode.
29CH	IPI4_FIFO_STATUS	RO	[31:4]	Reserved		
			[3]	ipi4_pl_fifo_full	0x0	This field indicates the payload FIFO full status of ipi4 interface, active HIGH.
			[2]	ipi4_hd_fifo_full	0x0	This field indicates the header FIFO full status of ipi4 interface, active HIGH.
			[1]	ipi4_pl_fifo_emptyz	0x0	This field indicates the payload FIFO empty status of ipi4 interface, active LOW.
			[0]	ipi4_hd_fifo_emptyz	0x0	This field indicates the header FIFO empty status of ipi4 interface, active LOW.

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MIPI DSI Host

BASE_ADDR: 0xA4355000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00H	VERSION	RO	[31:0]	version	0x3134302a	This field indicates the version of the mipi_dsi_host.
04H	PWR_UP	RW	[31:1]	Reserved		
			[0]	shutdownz	0x0	Active High. This field controls the power up of the core.
08H	CLKMGR_CFG	RW	[31:1]	Reserved		
			[15:8]	to_clk_division	0x0	This field indicates the division factor for the time out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
			[7:0]	to_esc_clk_division	0x0	This field indicates the division factor for the TX escape clock source. The value 0 and 1 stop the TX_ESC clock generation.
2CH	PCKHDL_CFG	RW	[31:6]	Reserved		
			[5]	eotp_tx_lp_en	0x0	When set to 1, this bit enables the EoTp transmission in Low Power.
			[4]	crc_rx_en	0x0	When set to 1, this bit enables the CRC reception and error reporting.
			[3]	ecc_rx_en	0x0	When set to 1, this bit enables the ECC reception error correction, and reporting.
			[2]	bta_en	0x0	When set to 1, this bit enables the Bus turnaround.
			[1]	eotp_rx_en	0x0	When set to 1, this bit enables the EoTp reception.
			[0]	eotp_tx_en	0x0	When set to 1, this bit enables the EoTp transmission in High-Speed.
34H	MODE_CFG	RW	[31:1]	Reserved		
			[0]	cmd_video_mode	0x1	This field configures the mode of operation between Video or Command mode. 0: Video mode. 1: Command mode.
38H	VID_MODE_CFG	RW	[31:25]	Reserved		
			[24]	vpg_orientation	0x0	This field indicates the color bar orientation: 0: Vertical Mode. 1: Horizontal Mode.
			[23:21]	Reserved		
			[20]	vpg_mode	0x0	Pattern Type: 0: Color bar(vertical or horizontal). 1: BER pattern(vertical only).
			[19:17]	Reserved		
			[16]	vpg_en	0x0	Enables the video mode pattern generator.
			[15]	lp_cmd_en	0x0	Enables the command transmission only in low-power mode.
			[14]	frame_bta_ack_en	0x0	Enables the request for an acknowledge response at the end of a frame.
			[13]	lp_hfp_en	0x0	Enables the return to low-power inside the HFP period when timing allows.
			[12]	lp_hbp_en	0x0	Enables the return to low-power inside the HBP period when timing allows.

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			[11]	lp_vact_en	0x0	Enables the return to low-power inside the VACT period when timing allows.
			[10]	lp_vfp_en	0x0	Enables the return to low-power inside the VFP period when timing allows.
			[9]	lp_vbp_en	0x0	Enables the return to low-power inside the VBP period when timing allows.
			[8]	lp_vsa_en	0x0	Enables the return to low-power inside the VSA period when timing allows.
			[7:2]	Reserved		
			[1:0]	vid_mode_type	0x0	This field indicates the video mode transmission type as follows: 00: Non-burst with sync pulses. 01: Non-burst with sync events. 10: Burst mode. 11: Burst mode.
3CH	VID_PKT_SIZE	RW	[31:14]	Reserved		
			[13:0]	vid_pkt_size	0x0	This field configures the number of pixels in a single video packet.
40H	VID_NUM_CHUNKS	RW	[31:13]	Reserved		
			[12:0]	vid_num_chunks	0x0	This field configures the number of chunks to be transmitted during a line period.
44H	VID_NULL_SIZE	RW	[31:13]	Reserved		
			[12:0]	vid_null_size	0x0	This field configures the number of bytes inside a null packet, set 0 disables null
48H	VID_HSA_TIME	RW	[31:12]	Reserved		
			[11:0]	vid_hsa_time	0x0	This field configures horizontal sync active period in lane byte clock cycles.
4CH	VID_HBP_TIME	RW	[31:12]	Reserved		
			[11:0]	vid_hbp_time	0x0	This field configures horizontal back porch period in lane byte clock cycles.
50H	VID_HLINE_TIME	RW	[31:15]	Reserved		
			[14:0]	vid_hline_time	0x0	This field configures the size of the total line time counted in lane byte clock cycles.
54H	VID_VSA_LINES	RW	[31:10]	Reserved		
			[9:0]	vsa_lines	0x0	This field configures the vertical sync active period measured in number of horizontal lines.
58H	VID_VBP_LINES	RW	[31:10]	Reserved		
			[9:0]	vbp_lines	0x0	This field configures the vertical back porch period measured in number of horizontal lines.
5CH	VID_VFP_LINES	RW	[31:10]	Reserved		
			[9:0]	vfp_lines	0x0	This field configures the vertical front porch period measured in number of horizontal lines.
60H	VID_VACTIVE_LINES	RW	[31:14]	Reserved		
			[13:0]	v_active_lines	0x0	This field configures the vertical active period measured in number of horizontal lines.
68H	VID_MODE_CFG	RW	[31:25]	Reserved		

[24]	max_rd_pkt_size	0x0	This bit configures the maximum read packet size command transmission type: 0: High Speed. 1: Low Power.
[23:20]	Reserved		
[19]	dcs_lw_tx	0x0	This bit configures the DCS long write packet command transmission type: 0: High Speed. 1: Low Power.
[18]	dcs_sr_0p_tx	0x0	This bit configures the DCS short read packet with zero parameter command transmission type: 0: High Speed. 1: Low Power.
[17]	dcs_sw_1p_tx	0x0	This bit configures the DCS short write packet with one parameter command transmission type: 0: High Speed. 1: Low Power.
[16]	dcs_sw_0p_tx	0x0	This bit configures the DCS short write packet with zero parameter command transmission type: 0: High Speed. 1: Low Power.
[15]	Reserved		
[14]	gen_lw_tx	0x0	This bit configures the generic long write packet command transmission type: 0: High Speed. 1: Low Power.
[13]	gen_sr_2p_tx	0x0	This bit configures the generic short read packet with two parameter command transmission type: 0: High Speed. 1: Low Power.
[12]	gen_sr_1p_tx	0x0	This bit configures the generic short read packet with one parameter command transmission type: 0: High Speed. 1: Low Power.
[11]	gen_sr_0p_tx	0x0	This bit configures the generic short read packet with zero parameter command transmission type: 0: High speed. 1: Low power.

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			[10]	gen_sw_2p_tx	0x0	This bit configures the generic short write packet with two parameter command transmission type: 0: High Speed. 1: Low Power.
			[9]	gen_sw_1p_tx	0x0	This bit configures the generic short write packet with one parameter command transmission type: 0: High Speed. 1: Low Power.
			[8]	gen_sw_0p_tx	0x0	This bit configures the generic short write packet with zero parameter command transmission type: 0: High Speed. 1: Low Power.
			[7:2]	Reserved		
			[1]	ack_rqst_en	0x0	This bit enables the acknowledge request after each packet transmission.
			[0]	tear_fx_en	0x0	This bit enables the tearing effect acknowledge request.
6CH	GEN_HDR	RW	[31:24]	Reserved		
			[23:16]	gen_wc_msbyte	0x0	This field configures the MSB of the header of the short packet's word count for data 1.
			[15:8]	gen_wc_lsbyte	0x0	This field configures the LSB of the header of the short packet's word count for data 1.
			[7:6]	gen_vc	0x0	This field configures the virtual channel ID of the header packet.
			[5:0]	gen_dt	0x0	This field configures the packet data type of the header packet.
6CH	GEN_PLD_DATA	RW	[31:24]	gen_pld_b4	0x0	The field indicates byte 4 of the packet payload.
			[23:16]	gen_pld_b3	0x0	The field indicates byte 3 of the packet payload.
			[15:8]	gen_pld_b2	0x0	The field indicates byte 2 of the packet payload.
			[7:0]	gen_pld_b1	0x0	The field indicates byte 1 of the packet payload.
74H	CMD_PKT_STATUS	RO	[31:20]	Reserved		
			[19]	gen_buff_pld_full		The full status of the generic payload internal buffer.
			[18]	gen_buff_pld_empty		The empty status of the generic payload internal buffer.
			[17]	gen_buff_cmd_full		The full status of the generic command internal buffer.
			[16]	gen_buff_cmd_empty		The empty status of the generic command internal buffer.
			[15:7]	Reserved		
			[6]	gen_rd_cmd_busy		This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO.
			[5]	gen_pld_r_full		The full status of the generic read payload FIFO.
			[4]	gen_pld_r_empty		The empty status of the generic read payload FIFO.
			[3]	gen_pld_w_full		The full status of the generic write payload FIFO.
			[2]	gen_pld_w_empty		The empty status of the generic write payload FIFO.
			[1]	gen_cmd_full		The full status of the generic command FIFO.

			[0]	gen_cmd_empty		The empty status of the generic command FIFO.
8CH	BTA_TO_CNT	RW	[31:16]	Reserved		
			[15:0]	bta_to_cnt	0x0	This field sets a period for which the link still after completing a BTA.
94H	LPCLK_CTRL	RW	[31:1]	Reserved		
			[1]	auto_clklane_ctrl	0x0	This bit enables the auto mechanism to stop providing the clock in clock lane when time allows.
			[0]	phy_txreqclkhs_con	0x0	This bit controls the D-PHY PPI txrequestclkhs signal: 0: Non-continuous clock mode. 1: Continuous clock mode.
98H	PHY_TMR_LPCLK_CFG	RW	[31:26]	Reserved		
			[25:16]	phy_clkhs2lp_time	0x0	The field configures the max time that clock lane take to go from HS to LP transmission measured in byte clock cycles.
			[15:10]	Reserved		
			[9:0]	phy_clklp2hs_time	0x0	The field configures the max time that clock lane take to go from LP to HS transmission measured in byte clock cycles.
9CH	PHY_TMR_CFG	RW	[31:26]	Reserved		
			[25:16]	phy_hs2lp_time	0x0	The field configures the max time that data lane take to go from HS to LP transmission measured in byte clock cycles.
			[15:10]	Reserved		
			[9:0]	phy_lp2hs_time	0x0	The field configures the max time that data lane take to go from LP to HS transmission measured in byte clock cycles.
A0H	PHY_RSTZ	RW	[31:4]	Reserved		
			[3]	phy_forcepll	0x0	When the D-PHY is in ULPS, this bit enables the D-PHY PLL.
			[2]	phy_enableclk	0x0	When set to 1, this bit enables the D-PHY Clock Lane Module.
			[1]	phy_rstz	0x0	When set to 0, this bit places the digital section of the D-PHY in the reset state.
			[0]	phy_shutdownz	0x0	When set to 0, this bit places the complete D-PHY macro in power-down state.
A4H	PHY_IF_CFG	RW	[31:16]	Reserved		
			[15:8]	phy_stop_wait_time	0x0	This field configures the minimum wait period to request a high-speed transmission after data lanes return to Stop State.
			[7:2]	Reserved		
			[1:0]	lane_en_num	0x3	This field configures the number of active data lanes: 00: 1 data lane (lane 0). 01: 2 data lanes (lanes 0 - 1). 10: 3 data lanes (lanes 0 - 2). 11: 4 data lanes (lanes 0 - 3). Can only be updated when phy_shutdownz and phy_rstz are both low.
B0H	PHY_STATUS	RO	[31:13]	Reserved	0x0	

			[12]	TxUlpsActiveNot_L3	0x1	This bit indicates the status of TxUlpsActiveNot_L3 D-PHY signal.
			[11]	TxStopState_L3	0x0	This bit indicates the status of TxStopState_L3 D-PHY signal.
			[10]	TxUlpsActiveNot_L2	0x1	This bit indicates the status of TxUlpsActiveNot_L2 D-PHY signal.
			[9]	TxStopState_L2	0x0	This bit indicates the status of TxStopState_L2 D-PHY signal.
			[8]	TxUlpsActiveNot_L1	0x1	This bit indicates the status of TxUlpsActiveNot_L1 D-PHY signal.
			[7]	TxStopState_L1	0x0	This bit indicates the status of TxStopState_L1 D-PHY signal.
			[6]	RxUlpsesc_L0		This bit indicates the status of RxUlpsesc_L0 D-PHY signal.
			[5]	TxUlpsActiveNot_L0	0x1	This bit indicates the status of TxUlpsActiveNot_L0 D-PHY signal.
			[4]	TxStopState_L0	0x0	This bit indicates the status of TxStopState_L0 D-PHY signal.
			[3]	TxUlpsActiveNot_Clk	0x0	This bit indicates the status of xUlpsActiveNot_Clk D-PHY signal: 0: ULPS state of clock lane. 1: Not ulps state of clock lane.
			[2]	TxStopState_Clk	0x0	This bit indicates the status of TxStopState_Clk D-PHY signal: 0: Not stop state of clock lane. 1: Stop state of clock lane.
			[1]	Phy_direction		This bit indicates the status of phy direction
			[0]	PLL_Lock	0x0	This bit indicates the status of phylock D-PHY signal: 0: PLL unlocked. 1: PLL locked.
B4H	PHY_TST_CTRL0	RW	[31:2]	Reserved		
			[1]	phy_testclk	0x0	This bit is used to clock the TESTDIN bus into the D-PHY0.
			[0]	phy_testclr	0x1	PHY0 test interface clear. Active High.
B8H	PHY_TST_CTRL1	RW	[31:17]	Reserved		
			[16]	phy0_testen	0x0	PHY0 test interface operation selector: 0: The data write operation is set on the rising edge of the testclk signal. 1: The address write operation is set on the falling edge of the testclk signal.
		RO	[15:8]	phy0_testdout	0x0	PHY0 outputs 8-bit data bus for read-back and internal probing functionalities.
			[7:0]	phy0_testdin	0x0	PHY0 test interface inputs 8-bit data bus for internal register programming and test functionalities access.
BCH	INT_ST0	RO	[31:21]	Reserved		
			[20]	dphy_errors_4		This bit indicates LP1 contention error from Lane 0.
			[19]	dphy_errors_3		This bit indicates LP0 contention error from Lane 0.
			[18]	dphy_errors_2		This bit indicates control error from Lane 0.
			[17]	dphy_errors_1		This bit indicates LP data transmission sync error from Lane 0.
			[16]	dphy_errors_0		This bit indicates ESC entry error from Lane 0.
			[15]	ack_with_err_15		This bit retrieves the DSI protocol from the Acknowledge error report.

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			[14]	ack_with_err_14		This bit retrieves the reserved from the Acknowledge error report.
			[13]	ack_with_err_13		This bit retrieves the invalid transmission length from the Acknowledge error report.
			[12]	ack_with_err_12		This bit retrieves the DSI VC ID from the Acknowledge error report.
			[11]	ack_with_err_11		This bit retrieves the not recognized DSI data type from the Acknowledge error report.
			[10]	ack_with_err_10		This bit retrieves the CRC error from the Acknowledge error report.
			[9]	ack_with_err_9		This bit retrieves the EoT error from the Acknowledge error report.
			[8]	ack_with_err_8		This bit retrieves the EoT error from the Acknowledge error report.
			[7]	ack_with_err_7		This bit retrieves the SoT sync error from the Acknowledge error report.
			[6]	ack_with_err_6		This bit retrieves the SoT error from the Acknowledge error report.
			[5]	ack_with_err_5		This bit retrieves the LP transmit sync error from the Acknowledge error report.
			[4]	ack_with_err_4		This bit retrieves the ESC mode entry command error from the Acknowledge error report.
			[3]	ack_with_err_3		This bit retrieves the EoT error from the Acknowledge error report.
			[2]	ack_with_err_2		This bit retrieves the EoT error from the Acknowledge error report.
			[1]	ack_with_err_1		This bit retrieves the SoT sync error from the Acknowledge error report.
			[0]	ack_with_err_0		This bit retrieves the SoT error from the Acknowledge error report.
C0H	INT_ST1	RO	[31:20]	Reserved		
			[19]	dpi_buff_pld_under		This bit indicates underflow has occurred when reading payload to build DSI packet for video mode.
			[18:13]	Reserved		
			[12]	gen_pld_recev_err		This bit indicates that during generic interface packet read back, payload FIFO full and data corrupted.
			[11]	gen_pld_rd_err		This bit indicates that during DSC read data, payload FIFO empty and data corrupted.
			[10]	gen_pld_send_err		This bit indicates generic packet build, payload FIFO empty and data corrupted.
			[9]	gen_pld_wr_err		This bit indicates generic packet build, payload FIFO full and data corrupted.
			[8]	gen_cmd_wr_err		This bit indicates that system write command through generic FIFO is full and data lost.
			[7]	dpi_pld_wr_err		This bit indicates DPI pixel line storage, the payload FIFO is full, and data corrupted.
			[6]	eopt_err		This bit indicates that EoTp packet has not been received.
			[5]	pkt_size_err		This bit indicates that packet size error.
			[4]	crc_err		This bit indicates that CRC error in payload data.
			[3]	ecc_multi_err		This bit indicates that header ECC has multiple error.
			[2]	ecc_single_err		This bit indicates that header ECC has single error.
			[1]	to_lp_rx		This bit indicates that LP reception timeout counter reached the end.
			[0]	to_hs_tx		This bit indicates that HS transmission timeout counter reached the end.
C4H	INT_MSK0	RW	[31:21]	Reserved		
			[20]	msk_dphy_errors_4	0x0	Mask for dphy_errors_4.

			[19]	msk_dphy_errors_3	0x0	Mask for dphy_errors_3.
			[18]	msk_dphy_errors_2	0x0	Mask for dphy_errors_2.
			[17]	msk_dphy_errors_1	0x0	Mask for dphy_errors_1.
			[16]	msk_dphy_errors_0	0x0	Mask for dphy_errors_0.
			[15]	msk_ack_with_err_15	0x0	Mask for ack_with_err_15.
			[14]	msk_ack_with_err_14	0x0	Mask for ack_with_err_14.
			[13]	msk_ack_with_err_13	0x0	Mask for ack_with_err_13.
			[12]	msk_ack_with_err_12	0x0	Mask for ack_with_err_12.
			[11]	msk_ack_with_err_11	0x0	Mask for ack_with_err_11.
			[10]	msk_ack_with_err_10	0x0	Mask for ack_with_err_10.
			[9]	msk_ack_with_err_9	0x0	Mask for ack_with_err_9.
			[8]	msk_ack_with_err_8	0x0	Mask for ack_with_err_8.
			[7]	msk_ack_with_err_7	0x0	Mask for ack_with_err_7.
			[6]	msk_ack_with_err_6	0x0	Mask for ack_with_err_6.
			[5]	msk_ack_with_err_5	0x0	Mask for ack_with_err_5.
			[4]	msk_ack_with_err_4	0x0	Mask for ack_with_err_4.
			[3]	msk_ack_with_err_3	0x0	Mask for ack_with_err_3.
			[2]	msk_ack_with_err_2	0x0	Mask for ack_with_err_2.
			[1]	msk_ack_with_err_1	0x0	Mask for ack_with_err_1.
			[0]	msk_ack_with_err_0	0x0	Mask for ack_with_err_0.
C8H	INT_MSK1	RW	[31:20]	Reserved		
			[19]	msk_dpi_buff_pld_under	0x0	Mask for dpi_buff_pld_under.
			[18:13]	Reserved		
			[12]	msk_gen_pld_recev_err	0x0	Mask for gen_pld_recev_err.
			[11]	msk_gen_pld_rd_err	0x0	Mask for gen_pld_rd_err.
			[10]	msk_gen_pld_send_err	0x0	Mask for gen_pld_send_err.
			[9]	msk_gen_pld_wr_err	0x0	Mask for gen_pld_wr_err.
			[8]	msk_gen_cmd_wr_err	0x0	Mask for gen_cmd_wr_err.
			[7]	msk_dpi_pld_wr_err	0x0	Mask for dpi_pld_wr_err.
			[6]	msk_eopt_err	0x0	Mask for eopt_err.
			[5]	msk_pkt_size_err	0x0	Mask for pkt_size_err.
			[4]	msk_crc_err	0x0	Mask for crc_err.
			[3]	msk_ecc_multi_err	0x0	Mask for ecc_multi_err.
			[2]	msk_ecc_single_err	0x0	Mask for ecc_single_err.
			[1]	msk_to_lp_rx	0x0	Mask for to_lp_rx.
			[0]	msk_to_hs_tx	0x0	Mask for to_hs_tx.

CCH	PHY_CAL	RW	[31:1]	Reserved		
			[0]	phy_cal	0x0	This bit controls calibration pin of D-PHY: 0: No calibration. 1: High-speed transmit skew calibration is activated.
D8H	INT_Force0	RW	[31:21]	Reserved		
			[20]	force_dphy_errors_4	0x0	Forces dphy_errors_4.
			[19]	force_dphy_errors_3	0x0	Forces dphy_errors_3.
			[18]	force_dphy_errors_2	0x0	Forces dphy_errors_2.
			[17]	force_dphy_errors_1	0x0	Forces dphy_errors_1.
			[16]	force_dphy_errors_0	0x0	Forces dphy_errors_0.
			[15]	force_ack_with_err_15	0x0	Forces ack_with_err_15.
			[14]	force_ack_with_err_14	0x0	Forces ack_with_err_14.
			[13]	force_ack_with_err_13	0x0	Forces ack_with_err_13.
			[12]	force_ack_with_err_12	0x0	Forces ack_with_err_12.
			[11]	force_ack_with_err_11	0x0	Forces ack_with_err_11.
			[10]	force_ack_with_err_10	0x0	Forces ack_with_err_10.
			[9]	force_ack_with_err_9	0x0	Forces ack_with_err_9.
			[8]	force_ack_with_err_8	0x0	Forces ack_with_err_8.
			[7]	force_ack_with_err_7	0x0	Forces ack_with_err_7.
			[6]	force_ack_with_err_6	0x0	Forces ack_with_err_6.
			[5]	force_ack_with_err_5	0x0	Forces ack_with_err_5.
			[4]	force_ack_with_err_4	0x0	Forces ack_with_err_4.
			[3]	force_ack_with_err_3	0x0	Forces ack_with_err_3.
			[2]	force_ack_with_err_2	0x0	Forces ack_with_err_2.
			[1]	force_ack_with_err_1	0x0	Forces ack_with_err_1.
			[0]	force_ack_with_err_0	0x0	Forces ack_with_err_0.
DCH	INT_FORCE1	RW	[31:20]	Reserved		
			[19]	force_dpi_buff_pld_under	0x0	Forces dpi_buff_pld_under.
			[18:13]	Reserved		
			[12]	force_gen_pld_recev_err	0x0	Forces gen_pld_recev_err.
			[11]	force_gen_pld_rd_err	0x0	Forces gen_pld_rd_err.
			[10]	force_gen_pld_send_err	0x0	Forces gen_pld_send_err.
			[9]	force_gen_pld_wr_err	0x0	Forces gen_pld_wr_err.
			[8]	force_gen_cmd_wr_err	0x0	Forces gen_cmd_wr_err.
			[7]	force_dpi_pld_wr_err	0x0	Forces dpi_pld_wr_err.
			[6]	force_eopt_err	0x0	Forces eopt_err.

			[5]	force_pkt_size_err	0x0	Forces pkt_size_err.
			[4]	force_crc_err	0x0	Forces crc_err.
			[3]	force_ecc_multi_err	0x0	Forces ecc_multi_err.
			[2]	force_ecc_single_err	0x0	Forces ecc_single_err.
			[1]	force_to_lp_rx	0x0	Forces to_lp_rx.
			[0]	force_to_hs_tx	0x0	Forces to_hs_tx.

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