X3M Register Reference Manual
BIFSD

Revision History

Revision	Date	Description
1.0	September-19-2020	Initial Release

BIFSD

BASE_ADDR: 0xA1007000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0000H	SD_eMMC_Program	RO	[31:20]	MMC_rtl_revision_no	12'h101	Revision number of the RTL release.
		RW	[19]	Generate_switch_err_for_ext_csd	1'h0	If the IP will not generate a switch error, and cmd6 writes ext_csd address < 192, all the bits of the register being written are reserved. Firmware is responsible for generating the switch error for these bytes.
		RW	[18]	Packed2alternate	1'h0	Alternate packed cmd handling flow: If this bit is set to 1, IP will handle packed cmd as per alternate packed cmd handling flow. For new customers it is recommended that user use this new flow, by setting this bit to 1. From the JEDEC spec, it seems that the intention of packed cmd is simply a software protocol on top of existing (4.41) eMMC HW. For the cmd handling and data transfer, the packed cmd state transitions are identical to the regular multi block write/read sequences. The HW only need to add some packed failure status register bits that the FW can access. The new FW flow will require the FW to first detect the packed bit in CMD23 by reading the bit[30] of the Set/Erase Block Count register (74H), and then treat the following cmd as packed cmd. Hardware(HW) does not need to distinguish between packed and non-packed cmd. None of the packed cmd specific interrupts will be generated since hardware will now treat packed command as regular cmd25 or cmd18. Firmware(FW) will parse the header (as it already does), and sets up additional transfers to the proper LBAs as necessary (or report any packed failures). For error handling Firmware need to set ext_csd registers PACKED_COMMAND_STATUS[36] and PACKED_FAILURE_INDEX[35], apart from following cmd25 or cmd18 flows. Firmware need to buffer packed commands. Firware has to ensure that in case of error, incorrect data is not written to final Physical memory.
		RW	[17]	Generate_switch_err_for_BKOPS	1'h0	1: IP will not generate a switch error for writing BKOPS_ena[7:6]. Firmware can generate this switch error. IP will not generate a switch error for writing BKOPS_ena[7:2] if sd_emmc_prog_reg_17 =1. Code is (!sd_emmc_prog_reg_17 && (|bkops_en_t_7_2[5:0])).
		RW	[16]	Firmware_fix	1'h0	1: IP will never go to inactive state for any OCR mismatch by cmd1. This bit will override any other OCR values mismatch related settings of other registers. Namely Power Up[1] and Power Up[3]. This bit is used as firmware fix, if any issue is found later in OCR mismatch error handling, or some host interprets the specs differently. It is recommended to set this bit to 1'b0.
		RW	[15]	Generate_switch_err_or_not	1'h0	1: IP will not generate switch error, Firmware has to generate a switch error. May be used for isolating issues. Always set this bit to 1'b0.
		RO	[14]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[13]	RCA_for_cmd7	1'h0	1: RCA = 0, it will be considered as valid RCA value for cmd7(select/deselect).
			RW	[12:11]	CRC_status_send_or_not	2'h0	2'b00 : For packed cmd data part errors, CRC status will be sent as 110. For other errors in data part of commands, CRC status will not be sent. Host will time out and send cmd12 and will know the type of error. 2'b01 : If an error in packed header is found by RTL ,then instead of sending CRC status 110, now CRC status will not be sent. 2'b10 : If an error in packed header is found by RTL ,then instead of sending CRC status 110, now CRC status 010 (OK CRC) will be sent. 2'b11 : For packed cmd errors with 110, instead of 110 CRC status, now no CRC status will be sent. (If bit [11] is set bit [12] is ignored). It is recommended to set it to 2'b11. If you use 2'b10, the firmware flow may be a bit different.
			RW	[10]	Cmd25_wp	1'h0	This bit is used to make IP give CRC status for Write protect violations for all commands including cmd25, cmd54, cmd47. So now the host will not timeout. 0: Firmware does not need to check for write protect violations, IP will not give the CRC status and will set "write protect violations" for the next cmd. 1: Firmware needs to to check for write protect violations.
			RW	[9]	Cmd24_wp	1'h0	Setting this bit makes IP give the CRC status of cmd 24 Write protect violations.
			RW	[8]	Send_CRC_status_Settin	1'h0	Setting this bit makes IP give the CRC status of the cmd27 and cmd26.
			RO	[7]	Reserved		
			RO	[6]	Single sector enable	1'h0	0: Configures the card to drive busy when two FIFOs are full. 1: Configures the card to drive busy when one of the FIFO is full.
			RO	[5]	Protocol partition enable	1'h0	0: Configures the device to set an illegal command when CMD53/CMD54 are received when the card is not in the USER AREA. 1: The device will not set an illegal command when the command is received in the non-user area location.
			RW	[4]	CMD7_Program	1'h0	0: Configures the selected card to ignore the CMD7 when it receives with its own RCA. 1: Configures the selected card to consider illegal command when it receives CMD7 with its own RCA.
			RW	[3]	Prog_busy_cntrl	1'h0	0: Configures the core to extend the program busy signal until the completion of DMA operation. 1: Configures the core to extend the program busy signal until the flash completes the programming of last block of write data. Always set this bit to 1'b1.
			RO	[2]	Reserved		
			RW	[1]	eMMC_program	1'h0	When set to 1, it informs the core to act as a eMMC5.0 device.
			RW	[0]	SD_program	1'h0	When set to 1, it informs the core to act as a SD device.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0004H	OCR	WO	[31:0]	OCR	32'h40FF8080	Used to store the OCR content. These bits should be programmed with the value of 32'h00FF8080 for Standard capacity eMMC cards and 32'h40FF8080 for High capacity eMMC cards.
0008H	CSD_0	WO	[31:8]	CSD_content_0	24'h0	Used to store CSD content for a SD controller.
		RW	[7:0]	Programmable	8'h0	The programmable bits that stores the contents of the CSD register contents of a SD controller. **Note:** During reading of this field, only the updated CSD value is read (only these 8 bits are updated during the program CSD interrupt).
000CH	CSD_1	WO	[31:0]	CSD_content_1	32'h0	Used to store the CSD content for a SD controller.
0010H	CSD_2	WO	[31:0]	CSD_content_2	32'h0	Used to store the CSD content of a SD controller.
0014H	CSD_3	WO	[31:24]	Reserved		
			[23:0]	CSD_content_3	24'h0	Used to store the CSD content of a SD controller.
0018H	CID_0	RW	[31:0]	CID_content_0	32'h0	Used to store the CID content of a SD controller. **Note:** During reading of this field, the updated CID value is read.
001CH	CID_1	RW	[31:0]	CID_content_1	32'h0	Used to store the CID content of a SD controller. **Note:** During reading of this field, the updated CID value is read.
0020H	CID_2	RW	[31:0]	CID_content_2	32'h0	Used to store the CID content of a SD controller. **Note:** During reading of this field, the updated CID value is read.
0024H	CID_3	RW	[31:24]	CID_update_ena	8'h0	0X00: CID update is enabled. 0X01: CID update is disabled.
			[23:0]	CID_content_3	24'h0	Used to store the CID content of a SD controller. **Note:** During reading of this field, the updated CID value is read.
0028H	SD eMMC Card State	RO	[31:15]	Reserved		
			[14]	High speed	1'h0	Indicates the card is in High speed mode.
			[13]	Default speed	1'h0	Indicates the card is in Default speed mode.
			[12]	SDR12 mode	1'h0	Indicates the card is in SDR12 mode.
			[11]	DDR50 mode	1'h0	Indicates the card is in DDR50 mode.
			[10]	SDR104 mode	1'h0	Indicates the card is in SDR104 mode.
			[9]	SDR50 mode	1'h0	Indicates the card is in SDR50 mode.
			[8]	High_speed_mode	1'h0	Indicates the card is in high speed mode.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[7]	WR_FIFO_full2	1'h0	Indicates the FIFO full condition of FIFO2.
			[6]	WR_FIFO_full1	1'h0	Indicates the FIFO full condition of FIFO1.
			[5]	WR_FIFO_empty2	1'h1	Indicates the FIFO empty condition of FIFO2.
			[4]	WR_FIFO_empty1	1'h1	Indicates the FIFO empty condition of FIFO1.
			[3:0]	SD / MMC state	4'h0	Indicates the present state of SD / MMC card.
002CH	SCR_0	RW	[31:0]	SCR_content_0	32'h0	SD0 card configuration content.
0030H	SCR_1	RW	[31:0]	SCR_content_1	32'h0	SD1 card configuration content.
0034H	Out_of_Range Address	WO	[31:0]	Out_of_range_address		Shows the address boundary to signal out of range error if the accessing address exceeds this value.
0038H	Interrupt Enable 1	RW	[31]	Multi block write/read commands	1'h0	Enables the multi block write/read commands interrupt. **Note:** This bit should be enabled only when the read command interrupt bit or write command interrupt bit is enabled.
			[30]	MMC block count clear	1'h0	Enables the MMC block count clear interrupt.
			[29]	General read/write	1'h0	Enables the general read/write interrupt.
			[28]	Write_protect group status	1'h0	Enables the get write protected group status.
			[27]	Clear to write protect	1'h0	Enables the clear write protected group interrupt.
			[26]	Set write protect	1'h0	Enables the set write protected group interrupt.
			[25]	Unlock card	1'h0	Enables the unlock card interrupt.
			[24]	Lock card	1'h0	Enables the lock card interrupt.
			[23]	Clear password	1'h0	Enables the clear password interrupt.
			[22]	Set password	1'h0	Enables the set new password interrupt.
			[21]	Force erase	1'h0	Enables the set force erase interrupt.
			[20]	Erase	1'h0	Enables the set erase interrupt.
			[19]	Set end address for erase	1'h0	Enables the set the erase ending address interrupt.
			[18]	Set start address for erase	1'h0	Enables the set erase start address interrupt.
			[17]	Number of well written blocks (SD)	1'h0	Enables the number of well written blocks (SD) interrupt.
			[16]	Reserved		
			[15]	Speed class control	1'h0	Enables the speed class control interrupt.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[14]	Voltage switch or cmd8	1'h0	Enables the voltage switch or cmd8 interrupt.
			[13]	Read block count reached	1'h0	Enables the read block count reached interrupt.
			[12]	Write block count reached	1'h0	Enables the write block count reached interrupt.
			[11]	Write	1'h0	Enables the write command interrupt.
			[10]	Read	1'h0	Enables the read command interrupt.
			[9]	Cmd40	1'h0	Enables the cmd40 interrupt.
			[8]	CMD61 interrupt	1'h0	Enables the vendor command CMD61 interrupt.
			[7]	Cmd6_always	1'h0	Enables the cmd6_always_interrupt.
			[6]	Block length	1'h0	Enables the set block length Interrupt.
			[5]	Inactive	1'h0	Enables the go_inactive [CMD15] interrupt.
			[4]	Idle	1'h0	Enables the go_idle [CMD0] interrupt.
			[3]	Stop	1'h0	Enables the stop command interrupt.
			[2]	Set block count or erase block count	1'h0	Enables the set block count command interrupt [applicable to eMMC cards]. Enables the set erase block count command interrupt [applicable to SD cards].
			[1]	CID	1'h0	Enables the program CID command interrupt [applicable to eMMC cards only].
			[0]	CSD	1'h0	Enables the program CSD command interrupt.
003CH	Interrupt Status 1	W1C	[31]	Multi block write/read commands bit	1'h0	This interrupt bit is set when Multi block write/read commands [CMD18 or CMD25] is received. **Note:** This bit will be set only along with the first Read interrupt or with the first Write interrupt of the Multiple block commands. If this multi_blk interrupt comes, but no write_int(intr_reg[11]) or read_int(intr_reg[10]) is present, it means some cmd12 masked write_int(intr_reg[11]) or read_int(intr_reg[10]). To overcome this condition, firmware should find out what was the last cmd by reading IP pins sig_rx_arg[37:32]. If last cmd was mult_block_read(cmd18), then firmware should also execute interrupt service routine for read_interrupt(intr_reg[10]). If last cmd was multi_block_write(cmd25), then firmware should also execute interrupt service routine for write_interrupt(intr_reg[11]).
			[30]	MMC block count clear	1'h0	This interrupt bit is set when CMD23 reception is not followed by the reception of CMD18 or CMD25. This interrupt informs the firmware to clear the set block count.
			[29]	General read/write	1'h0	This interrupt bit is set when the general read/write command [CMD56] is received.
			[28]	Write_protect group status	1'h0	This interrupt bit is set when the send_write_prot command to get write protection group status [CMD30] is received.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27]	Clear to write protect	1'h0	This interrupt bit is set when the clear write protect command [CMD29] is received.
				[26]	Set write protect	1'h0	This interrupt bit is set when the set write protect command [CMD28] is received.
				[25]	Unlock card	1'h0	This interrupt bit is set when the unlock the card bit is set in the received CMD42.
				[24]	Lock card	1'h0	This interrupt bit is set when the lock the card bit is set in the received CMD42.
				[23]	Clear password	1'h0	This interrupt bit is set when the clear the password contents bit is set in the received CMD42.
				[22]	Set password	1'h0	This interrupt bit is set when the new password reception bit is set in the received CMD42.
				[21]	Force erase	1'h0	This interrupt bit is set when the erase the entire card contents bit is set in the received CMD42.
				[20]	Erase	1'h0	This interrupt bit is set when the erase command [CMD38] is received.
				[19]	Set end address for erase	1'h0	This interrupt bit is set when the ending address of the data to be erased CMD33 [SD] or CMD36 [MMC] is received.
				[18]	Set start address for erase	1'h0	This interrupt bit is set when the starting address of the data to be erased CMD32 [SD] or CMD35 [MMC] is received.
				[17]	Number of well written blocks (SD)	1'h0	For eMMC_device: During wait_IRQ_state if device gets "0 on cmd line", IP will move back to STBY state from IRQ state, and generate this interrupt. The firmware flow for eMMC_device: Firmware clears this Interrupt Status 1[9] interrupt. For sd_device: This interrupt bit is set when the number of well written blocks (SD) command [ACMD22] is received.
				[16]	CMD55	1'h0	This interrupt bit is set when the application specific command cmd55 is received. On getting this interrupt, firmware can also read the argument register value, to know cmd55 arguments. Sample test to run is testcases/ver_4.4/chk_cases/ bus_test_cmd55 For our eMMC IP, there are 3 application commands that are used by our IP. So all other cmds that come after cmd55 will not be treated as application specific cmd, but will work as normal cmds. Refer to eMMC5.1 specs, section 6.6.23 Application-specific commands: - 1.1 app_cmd61. - 1.2.1 app_cmd6. - 1.2.2 app_cmd41.
				[15]	Speed class control	1'h0	This interrupt bit is set when the speed class control command [CMD20] is received.
				[14]	Voltage switch or cmd8	1'h0	This interrupt bit is set when cmd8 in case of mmc mode or the voltage switch interrupt [CMD11] is received in SD mode for SD3.0 compatible devices. Indicates the voltage need to switch from 3.3v to 1.8v.
				[13]	Read block count reached	1'h0	This interrupt bit is set to inform the successful completion of a read block transfer.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	Write block count reached	1'h0	This interrupt bit is set to inform the successful completion of a write block transfer.
				[11]	Write	1'h0	This interrupt bit is set when the write command [CMD24/25] is received. **Note:** If the stop and write interrupts are set simultaneously, then the processor should understand that the old write command should be terminated and a new write command is to be serviced. The previous write operation is completed and the stop interrupt should be serviced first before servicing the write interrupt.
				[10]	Read	1'h0	This interrupt bit is set when the read command [CMD17/18] is received. **Note:** If the stop and read interrupts are set simultaneously, then the processor should understand that the old read command should be terminated and a new read command is to be serviced. The previous read operation is completed and the stop interrupt should be serviced first before servicing the read interrupt.
				[9]	Cmd40	1'h0	This interrupt will come only if "Device cmd class of class 9 = 1, is set in CCC field of CSD, i.e. cmd40 is supported". For this setting of CLASS 9 =1, when cmd40 is received, IP will go to wait_IRQ state, and generate an Interrupt Status 1[9] interrupt. If during wait_IRQ_state, firmware writes 1 to Mem_Mgmt[19], IP will move to STBY state and send R5 Response. "On getting 0 on cmd line", IP will move back to STBY state from wait_IRQ state. So firmware flow will be: On getting this interrupt firmware waits for some time and then may optionally {reads "SD / eMMC card state register (28H)" bits[3:0] to check if the new state of IP is wait_IRQ state}. Firmware writes 1 to Mem_Mgmt[19], IP will move to STBY state and send R5 Response. Firmware clears this interrupt. If before firmware writes 1 to Mem_Mgmt[19], an Interrupt Status 1[17] interrupt comes, then IP is already out of wait_IRQ state so firmware will not write 1 to Mem_Mgmt[19]. Firmware will clear this Interrupt Status 1[9] interrupt. There are 2 ways IP can come out of wait_IRQ state. - If host sends 0 on cmd line (i.e., due to start bit some other cmd). For this IP generates an Interrupt Status 1[17] interrupt, and comes to STBY state. - Firmware writes 1 to Mem_Mgmt[19]. IP comes to STBY state and send R5 Response.
				[8]	CMD61	1'h0	This interrupt bit is set when the vendor command CMD61 is received.
				[7]	Cmd6_always	1'h0	Whenever host writes less than 192 ext_csd registers, the cmd6_always_interrupt is received. IP will generate busy until the mem_management_register is not written by firmware. Firmware can read the argument register to know the details of the cmd6 received.
				[6]	Block length	1'h0	This interrupt bit is set when the Set block length cmd16 is received.
				[5]	Inactive	1'h0	This interrupt bit is set when the Go_inactive [CMD15] is received.
				[4]	Idle	1'h0	This interrupt bit is set when the Go_idle [CMD0] is received.
				[3]	Stop	1'h0	This interrupt bit is set when the Stop command [cmd12] is received.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	Set block count or erase block count	1'h0	For MMC cards, this interrupt bit is set when the set_block_count cmd23 is received. For SD cards, this interrupt bit is set when the set_wr_blk_erase_count ACMD23 is received. **Note:** The set block count interrupt will not be generated if Host sends CMD23 during the packed read command data transfer.
				[1]	CID	1'h0	This interrupt bit is set when program_ cid command, cmd26 is received.
				[0]	CSD	1'h0	This interrupt bit is set when program_csd command, cmd27 is received.
	0040H	Mem_Mgmt	RW	[31:20]	Reserved		
				[19]	Wait_IRQ_2_STBY	1'h0	If IP is in wait_IRQ_state. Writing 1 to this bit moves IP from wait_IRQ_state to STBY state, and send R5 response.
				[18]	Recover_from_any_potential_boundary_err	1'h0	In some combinations of password error conditions, it may be possible that the IP takes incorrect password length value. This bit is provided to recover from any potential boundary error conditions. Writing 1 to this bit will set the password length as set by firmware in "Password length register". This bit is set in intr_reg2[26] interrupt service routine.
				[17]	WP_Violation2_signal	1'h0	WP_Violation2 signal for write protect violation
				[16]	Product_auto_preload_done	1'h0	Production Auto Preload Done
				[15]	Lock_unlock_failed_err	1'h0	Lock unlock failed error
				[14]	Ext_security_err	1'h0	Extended security error
				[13]	Exception_event_status	1'h0	Exception event status(except security error). Writing 1 to this bit will set the EXCEPTION_EVENT bit in device status. The EXCEPTION_EVENT bit in device status will be set continuously, until firmware does not write 0 to this bit.
				[12]	Firmware_switch_err	1'h0	Firmware Switch Error
				[11]	AKE_err	1'h0	AKE Error
				[10]	Card_ECC_failed	1'h0	Card ECC failed
				[9]	WR_protect_erase_skip	1'h0	Write protect erase skip
				[8]	Erase_parameter_err	1'h0	Erase parameter error
				[7]	Write_protect_violation	1'h0	Write protect violation
				[6]	Boot_data_completed	1'h0	Boot data completed
				[5]	Tran_completed	1'h0	Transfer complete (set after password, CSD, CID are updated, erased and forced to erase).
				[4]	Addr_misalign_err	1'h0	Address misalignment error in block read/write command argument.
				[3]	Out_of_range_err	1'h0	Out of range error during block transfer completion.
				[2]	General_err	1'h0	General Error. It indicates the operation has been completed with unrecoverable errors.
				[1]	Program_err	1'h0	Program error. It indicates the operation has been completed with errors.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[0]	No_err	1'h1	No error
0044H	Argument	RO	[31:0]	Argument	32'h0	Address where the memory read or write operations will be performed for a read or write interrupt.
0048H	DMA Address	RW	[31:0]	DMA address	32'h0	Address where DMA read or DMA write operations will be performed. ATA status register contents if the interrupt is fast IO interrupt.
004CH	SD_MMC Block Count	RW	[31:16]	Reserved		
			[15:0]	SD_MMC_BLK_CNT	16'h0	Total number of block transfers for which the ARM is ready.
0050H	Password_0	RW	[31:0]	Password_0	32'h0	After power up, password 0 (if any) is updated in this register. Similarly, password is updated by the core when a set password interrupt is raised. **Note:** During reading of this field, the updated password is read.
0054H	Password_1	RW	[31:0]	Password_1	32'h0	After power up, password 1 (if any) is updated in this register. Similarly, password is updated by the core when a set password interrupt is raised. **Note:** During reading of this field, the updated password is read.
0058H	Password_2	RW	[31:0]	Password_2	32'h0	After power up, password 2 (if any) is updated in this register. Similarly, password is updated by the core when a set password interrupt is raised. **Note:** During reading of this field, the updated password is read.
005CH	Password_3	RW	[31:0]	Password_3	32'h0	After power up, password 3 (if any) is updated in this register. Similarly, password is updated by the core when a set password interrupt is raised. **Note:** During reading of this field, the updated password is read.
0060H	SD Status 0	RW	[31:8]	SD_status_0	24'h0	Used to store the data of the SD0 status register.
			[7:0]	Reserved		
0064H	SD Status 1	RW	[31:0]	SD_status_1	32'h0	Used to store the data of the SD1 status register.
0068H	SD Status 2	RW	[31:0]	SD_status_2	32'h0	Used to store the data of the SD2 status register.
006CH	SD Status 3	RW	[31:0]	SD_status_3	32'h0	Used to store the data of the SD3 status register.
0070H	Block Length	RO	[31:0]	Block length	32'h0	The size of the block to be transferred.
0074H	Set/Erase Block Count	RO	[31]	Reliable write request	1'h0	Defines the reliable write parameter for block write command: 0: Deactivates reliable write operation. 1: Activates reliable write operation.
			[30]	Packed command	1'h0	Defines the next command to be packed write / packed read command: 0: Non packed command. 1: Next command is packed command.

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	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
				[29]	TAG request	1'h0	Defines the Tag request for block write command: 0: Deactivates Data TAG mechanism in write operation. 1: Activates Data TAG mechanism in write operation.
				[28:25]	Context ID	4'h0	Defines the context IDS for block write / block read command: 0: Deactivates Context ID. 1: Activates Context ID.
				[24]	Forced programming	1'h0	Defines the forced programming operation for block write command: 0: Deactivates the forced programming. 1: Forcefully programmed to non-volatile storage.
				[23:0]	Number of blocks	24'h0	The Number of blocks to be transferred in MMC mode (bits [15:0], bits[23:16] are set to 0). The Number of blocks to be erased before writing in SD mode (bits[22:0]).
	0078H	Erase Start Address	RO	[31:0]	Erase start address	32'h0	Address of the first block to be erased.
	007CH	Erase End Address	RO	[31:0]	Erase end address	32'h0	Address of the last block to be erased.
	0080H	Set Write Protect	RO	[31:0]	Data address	32'h0	Address of the group to be write protected.
	0084H	Clear Write Protect	RO	[31:0]	Data address	32'h0	Address of the group to be cleared from write protection.
	008CH	Hardware Reset Count	RW	[31:7]	Reserved		
				[6:0]	Hardware reset count	7'h0	The count value indicates the number of AHB clock cycles equivalent to 1 microsecond. This count value is used to check the validity of the assertion of hardware reset signal.
	0090H	DMA Count	RO	[31:16]	Reserved		
				[15:0]	DMA count value	16'h0	The DMA count value indicates how many blocks have been transferred by DMA.
	0094H	Updated EXT CSD	RO	[31:8]	Reserved		
				[7:0]	Updated EXT CSD register field value	8'h0	These bits indicate the updated field value of the EXT CSD register.
	0098H	Boot Block Count	RW	[31:16]	Reserved		
				[15:0]	Read and write block count for boot	16'h0	Number of blocks for read and write operation in boot mode (Block size 512).
	009CH	Interrupt Enable 2	RW	[31]	FIFO_not_empty_cmd45	1'h0	Enables the FIFO_not_empty_cmd45_interrupt.
				[30]	Cmd46_interrupt	1'h0	Enables the cmd46_interrupt.
				[29]	Cmd47_interrupt	1'h0	Enables the cmd47_interrupt.
				[28]	Cmd48_interrupt	1'h0	Enables the cmd48_interrupt.
				[27]	CMD1_interrupt	1'h0	Enables the CMD1_interrupt.
				[26]	PWD_CMD_FAIL	1'h0	Enables the password command fail interrupt.
				[25]	Security protocol write	1'h0	Enables the CMD54 interrupt.
				[24]	Security protocol read	1'h0	Enables the CMD53 interrupt.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[23]	Card status change	1'h0	Enables the SD eMMC card status change interrupt.
				[22]	Packed Failure status	1'h0	Enables the packed failure status interrupt.
				[21]	Packed completion	1'h0	Enables the packed command completion interrupt.
				[20]	GO_PRE_IDLE	1'h0	Enables the GO_PRE_IDLE interrupt.
				[19]	Hardware reset completed	1'h0	Enables the Hardware reset completed interrupt.
				[18]	Update EXT_CSD	1'h0	Enables the interrupt for Update EXT_CSD register (MMC) / switch command (SD).
				[17]	Partition setting completed	1'h0	Enables the partition setting completed interrupt.
				[16]	Get write protect type	1'h0	Enables the get write protect type interrupt.
				[15]	Real time clock	1'h0	Enables the real time clock interrupt.
				[14]	Packed command start	1'h0	Enables the packed command start interrupt.
				[13]	Tcase support	1'h0	Enables the tcase support interrupt.
				[12]	Flush cache	1'h0	Enables the flush cache interrupt.
				[11]	Sanitize start	1'h0	Enables the sanitize start interrupt.
				[10]	Card deselect	1'h0	Enables the card deselect interrupt.
				[9]	Card select	1'h0	Enables the card select interrupt.
				[8]	CMD12	1'h0	Enables the CMD12 interrupt.
				[7]	CMD CRC error	1'h0	Enables the command CRC error interrupt.
				[6]	Data CRC error	1'h0	Enables the data CRC error interrupt.
				[5]	High priority	1'h0	Enables the high priority interrupt.
				[4]	BKOPS_start	1'h0	Enables the BKOPS start interrupt.
				[3]	Awake Command	1'h0	Enables the Awake command interrupt.
				[2]	Sleep Command	1'h0	Enables the Sleep command interrupt.
				[1]	Boot Stop	1'h0	Enables the Boot Stop interrupt.
				[0]	Boot Start	1'h0	Enables the Boot Start interrupt.
	00A0H	Interrupt Status 2	W1C	[31]	FIFO_not_empty_cmd45	1'h0	This interrupt is generated when the cmd queue FIFO is not empty, i.e., valid cmd44 & cmd45 are written in the FIFO. **Note:** The interrupt is cleared when firmware reads all contents of the FIFO, so that the cmd queue FIFO is empty. int_reg2[31] is directly coming from the FIFO not empty signal.
				[30]	Cmd46_interrupt	1'h0	This interrupt bit is set when the cmd46_interrupt is active.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[29]	Cmd47_interrupt	1'h0	This interrupt bit is set when the cmd47_interrupt is active.
			[28]	Cmd48_interrupt	1'h0	This interrupt bit is set when the cmd48_interrupt is active.
			[27]	CMD1_interrupt	1'h0	This interrupt bit is set when the CMD1 is received in valid state.
			[26]	PWD_CMD_FAIL	1'h0	The interrupt bit is set when the host controller defines the cmd16 block length less then lock_unlock card data structure and when CRC error is detected in the cmd42 data. **Note:** If this interrupt is asserted firmware should program the existing password again into the PASSWORD register and set transfer complete bit in the memory management register.
			[25]	Security protocol write	1'h0	This interrupt bit is set when the CMD54 is received.
			[24]	Security protocol read	1'h0	This interrupt bit is set when the CMD53 is received.
			[23]	Card status change	1'h0	This interrupt bit is set when there is any change in the SD eMMC card state register.
			[22]	Packed Failure status	1'h0	This interrupt bit is set when the card detects error in the packet header.
			[21]	Packed completion	1'h0	This interrupt bit is set when the card completes the packed data transfer.
			[20]	GO_PRE_IDLE	1'h0	This interrupt bit is set when the CMD0 is received with argument[0xF0F0F0F0].
			[19]	Hardware reset completed	1'h0	This interrupt bit is set when the reset lasts for one microsecond.
			[18]	Update EXT_CSD	1'h0	This bit is set when the interrupt for Update EXT_CSD register (MMC) / switch command (SD) is set in the CMD6. For MMC, this interrupt bit is generated only for the addresses [updatable fields] under 'modes segment' of the Ext_CSD register except for BUS_WIDTH and CMD_SET.
			[17]	Partition setting completed	1'h0	This interrupt bit is set when the partition setting completed [CMD6] is received.
			[16]	Get write protect type	1'h0	This interrupt bit is set when the get write protect type [CMD31] is received.
			[15]	Real time clock	1'h0	This interrupt bit is set when the card receives the CMD49 command.
			[14]	Packed command start	1'h0	This interrupt bit is set when the packed command bit is set the received CMD23.
			[13]	Tcase support	1'h0	This interrupt bit is set when the tcase support interrupt bit is set in the received CMD6.
			[12]	Flush cache	1'h0	This interrupt bit is set when the flush cache bit is set in the received CMD6.
			[11]	Sanitize start	1'h0	This interrupt bit is set when the sanitize start bit is set in the received CMD6.
			[10]	Card deselect	1'h0	This interrupt bit is set when the CMD7 is received with different RCA other than card RCA to move the card to standby state.
			[9]	Card select	1'h0	This interrupt bit is set when the CMD7 is received with card RCA to move the card to transfer state.
			[8]	CMD12	1'h0	This interrupt bit is set when the CMD12 is received from Host.
			[7]	CMD CRC error	1'h0	This interrupt bit is set to indicate the CRC error has occurred in the received command.

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Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[6]	Data CRC error	1'h0	This interrupt bit is set to indicate the CRC error has occurred in the received data block.
			[5]	High priority	1'h0	This interrupt bit is set to stop the data transfer when the card is in programming state.
			[4]	BKOPS_start	1'h0	This interrupt bit is set when the host allows the card to perform background operation.
			[3]	Awake Command	1'h0	This interrupt bit is set when the sleep/awake bit is cleared by the received command [CMD5].
			[2]	Sleep Command	1'h0	This interrupt bit is set when the sleep/awake bit is set in the received command [CMD5].
			[1]	Boot Stop	1'h0	This interrupt bit is set when the host signals the boot stop operation by making the command line high.
			[0]	Boot Start	1'h0	This interrupt bit is set : - If command line is low for 74 clocks then the Boot Start interrupt is set. - If CMD0 with argument FFFFFFFA is received then the Boot Start interrupt is set.
0240H	Password Length	RW	[31:5]	Reserved		
			[4:0]	Password length	5'h0	These bits contain the length of the password.
0244H	Power Up	RW	[31:4]	Reserved		
			[3]	Voltage_value_check	1'h0	Checks voltage values of OCR: 0: By default, mismatch in Voltage values of OCR register will be ignored. Even if there is mismatch between voltage values supported by device and sent by host, device will not go to inactive state. 1: If voltage value sent by host does not match device value, IP will go to inactive state.
			[2]	SD/MMC init	1'h0	To configure SD/MMC device IP to respond CMD1/ ACMD41 before programming in SD_MMC program register: 0: Response to ACMD41. 1: Response to CMD1.
			[1]	Card_capa_chk_disable	1'h0	Disables the Host Capacity Support bit comparison in OCR: 0: The card goes to inactive state when its OCR[30] = 0 (byte mode), but the host sends OCR[30] = 1 (sector mode). 1: The card does not go to inactive state when its OCR[30] = 0 (byte mode), but the host sends OCR[30] = 1 (sector mode). **Note:** This bit is used to support a high capacity MMC host when the card is configured as a standard capacity MMC card.
			[0]	CMD8 enable	1'h0	Enables the CMD8 response: 0: Card does not send response to CMD8. 1: Card sends response to CMD8. **Note:** This bit is invalid after sd_emmc program_register is configured. This bit must not be set to 1'b1 for MMC mode.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0248H	SD Security Interrupt Enable	RW	[31:12]	Reserved		
			[11]	Exit secure mode	1'h0	Enables the exit secure mode interrupt.
			[10]	Change Secure Area-Command	1'h0	Enables the Change Secure Area command interrupt.
			[9]	GET_CER_RES1 Command	1'h0	Enables the GET_CER_RES1 command interrupt.
			[8]	SET_CER_RES2 Command	1'h0	Enables the SET_CER_RES2 command interrupt.
			[7]	GET_CER_RN 2 Command	1'h0	Enables the GET_CER_RN2 command interrupt.
			[6]	SET_CER_RN 1 Command	1'h0	Enables the SET_CER_RN1 command interrupt.
			[5]	Get Media ID	1'h0	Enables the Get Media ID command interrupt.
			[4]	Get MKB	1'h0	Enables the Get MKB command interrupt.
			[3]	Secure Erase	1'h0	Enables the Secure Erase command interrupt.
			[2]	Secure Write MKB	1'h0	Enables the Secure Write MKB command interrupt.
			[1]	Secure Write multi block	1'h0	Enables the Secure Write multi block command interrupt.
			[0]	Secure Read multi block	1'h0	Enables the Secure Read multi block command interrupt.
024CH	SD Security Interrupt Status	W1C	[31:12]	Reserved		
			[11]	Exit secure mode	1'h0	This interrupt bit is set when the exit secure mode interrupt occurs.
			[10]	Change Secure Area Command	1'h0	This interrupt bit is set when Change Secure Area command ACMD49 is received.
			[9]	GET_CER_RES1 Command	1'h0	This interrupt bit is set when GET_CER_RES1 command ACMD48 is received.
			[8]	SET_CER_RES2 Command	1'h0	This interrupt bit is set when SET_CER_RES2 command ACMD47 is received.
			[7]	GET_CER_RN 2 Command	1'h0	This interrupt bit is set when GET_CER_RN2 command ACMD46 is received.
			[6]	SET_CER_RN 1 Command	1'h0	This interrupt bit is set when SET_CER_RN1 command ACMD45 is received.
			[5]	Get Media ID	1'h0	This interrupt bit is set when Get Media ID command ACMD44 is received.
			[4]	Get MKB	1'h0	This interrupt bit is set when Get MKB command ACMD43 is received.
			[3]	Secure Erase	1'h0	This interrupt bit is set when Secure Erase command ACMD38 is received.
			[2]	Secure Write MKB	1'h0	This interrupt bit is set when Secure Write MKB command ACMD26 is received.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[1]	Secure Write multi block	1'h0	This interrupt bit is set when Secure Write multi block command ACMD25 is received.
			[0]	Secure Read multi block	1'h0	This interrupt bit is set when Secure Read multi block command [ACMD18] is received.
0250H	Set Block Count (security)	RW	[31]	Card ECC disabled	1'h0	0: Internal Card ECC check is enabled. 1: Internal Card ECC check is disabled.
			[30:16]	Reserved		
			[15:0]	Block Count value	16'h0	Block count value for security commands in AKE process.
0254H	Packed Count	RW	[31:0]	Packed_count	32'h0	Packed Count Value
0258H	eMMC Timing	RW	[31:19]	Reserved		
			[18:16]	NCRC_value	3'h2	Host cmd to device RES timings. (Min = 2, Max = 8). New register bits: ncrc_programmable_count_reg [2:0]. ncrc_programmable_count_reg = 2, NCRC = 2 (best performance, recommended and reset value). ncrc_programmable_count_reg = 3, NCRC = 3 (safe value, good performance). ncrc_programmable_count_reg = 4, NCRC = 4. ncrc_programmable_count_reg = 7, NCRC = 7.
			[15:14]	Reserved		
			[13:8]	NCR_value	6'h0	Host cmd to device RES timinngs. (Min = 2, Max = 64). ncr_programmable_count_reg = 2, NCR = 2 (best performance). ncr_programmable_count_reg = 3, NCR = 3 (safe value, good performance). ncr_programmable_count_reg = 4, NCR = 4. ncr_programmable_count_reg = 55, NCR = 55. above 55 values not recomended, due to potential boundary conditions.
			[7:4]	NAC_HS200_400	4'h4	For HS200 and HS400, Min = 8, so one option is to set NAC to 4, 5, 6, 7, 8, 9, 10, 11. (bit_cnt[3:0] == nac_programmable_count_hs200_400[3:0]) nac_programmable_count_hs200_400 = 1, NAC = 5 (specs violation). nac_programmable_count_hs200_400 = 2, NAC = 6 (specs violation). nac_programmable_count_hs200_400 = 3, NAC = 7 (specs violation). nac_programmable_count_hs200_400 = 4, NAC = 8 (best performance, recomended value). nac_programmable_count_hs200_400 = 5, NAC = 9 (safe value, good performance). nac_programmable_count_hs200_400 = 6, NAC = 10. nac_programmable_count_hs200_400 = 7, NAC = 11.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3:0]	NAC_non_HS200_400	4'h2	For non HS200 and HS400 modes, NAC (Min) = 2. (bit_cnt[3:0] == nac_programmable_count_non_hs200_400[3:0]) nac_programmable_count_non_hs200_400 = 1, NAC= 1 (specs violation). nac_programmable_count_non_hs200_400 = 2, NAC= 2 (best performance, recomended value). nac_programmable_count_non_hs200_400 = 3, NAC= 3 (safe value, good performance). nac_programmable_count_non_hs200_400 = 4, NAC= 4. nac_programmable_count_non_hs200_400 = 15, NAC= 15. No synchronizers save gates on nac_programmable_count_hs200_400[3:0] and nac_programmable_count_non_hs200_400[3:0]. So these nac count programmable value registers should not be updated during read commands.
	0268H	Queue Status	RO	[31:0]	Queue Status	32'h0	Queue Status
	026CH	FIFO Read	RO	[31:0]	FIFO DATA	32'h0	FIFO DATA

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00A4H	Reserved	RW	120	Reserved	120'h0	Reserved
00B3H	cmd_queue_mode_ena	RW	8	cmd_queue_mode_ena	8'h0	Command Queue Mode Enable
00B4H	sec_removal_type	RW	8	sec_removal_type	8'h0	Secure Removal Type
00B5H	product_state_aware_ena	RW	8	product_state_aware_ena	8'h0	Production State Awareness Enable
00B6H	max_auto_preload_data_size_ena_0	RW	16	max_auto_preload_data_size_ena_0	16'h0	Max Auto-Preloading Data Size Enable
00B8H	max_auto_preload_data_size_ena_1	RW	16	max_auto_preload_data_size_ena_1	16'h0	Max Auto-Preloading Data Size Enable
00BAH	auto_preload_data_size_ena_0	RW	16	auto_preload_data_size_ena_0	16'h0	Auto-Preloading Data Size Enable
00BCH	auto_preload_data_size_ena_1	RW	16	auto_preload_data_size_ena_1	16'h0	Auto-Preloading Data Size Enable
00BEH	FFU_STATUS	RW	8	FFU_STATUS	8'h0	FFU STATUS
00BFH	Reserved	RW	16	Reserved	16'h0	Reserved
00C1H	mode_oper_code	RW	8	mode_oper_code	8'h0	Mode Operation Code
00C2H	mode_cfg	RW	8	mode_cfg	8'h0	Mode Configuration
00C3H	ctrl_barrier	RW	8	ctrl_barrier	8'h0	Used to turn on/off the Barrier.
00C4H	FLUSH_CACHE	RW	8	FLUSH_CACHE	8'h0	Used to store the FLUSH_CACHE.
00C5H	ctrl_cache	RW	8	ctrl_cache	8'h0	Used to turn on/off the cache.
00C6H	pwr_off_notification	RW	8	pwr_off_notification	8'h0	Used to store power off notifications.
00C7H	pack_cmd_idx_err	RW	8	pack_cmd_idx_err	8'h0	Used to store the packet command index error.
00C8H	pack_cmd_status	RW	8	pack_cmd_status	8'h0	Used to store the packet command status.
00C9H	CONTEXT_CONF_0	RW	24	CONTEXT_CONF_0	24'h0	Used to store CONTEXT_CONF 0.
00CCH	CONTEXT_CONF_1	RW	32	CONTEXT_CONF_1	32'h0	Used to store CONTEXT_CONF 1.
00D0H	CONTEXT_CONF_2	RW	32	CONTEXT_CONF_2	32'h0	Used to store CONTEXT_CONF 2.
00D4H	CONTEXT_CONF_3	RW	32	CONTEXT_CONF_3	32'h0	Used to store CONTEXT_CONF 3.
00D8H	EXT_PARTITIONS_ATTRIBUTE	RW	16	EXT_PARTITIONS_ATTRIBUTE	16'h0	Used to store EXT_PARTITIONS_ATTRIBUTE.
00DAH	EXCEPTION_EVENTS_STATUS	RW	16	EXCEPTION_EVENTS_STATUS	16'h0	Used to store EXCEPTION_EVENTS_STATUS.
00DCH	EXCEPTION_EVENTS_CTRL	RW	16	EXCEPTION_EVENTS_CTRL	16'h0	Used to store EXCEPTION_EVENTS_CTRL.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
00DEH	DYNCAP_NEEDED	RW	8	DYNCAP_NEEDED	8'h0	Used to store DYNCAP_NEEDED.
00DFH	CLASS6_CTRL	RW	8	CLASS6_CTRL	8'h0	Used to store CLASS6_CTRL.
00E0H	INI_TIMEOUT_EMU	RW	8	INI_TIMEOUT_EMU	8'h0	Used to store the INI_TIMEOUT_EMU value.
00E1H	data_sector_size	RW	8	data_sector_size	8'h0	Used to store the data sector size.
00E2H	use_native_sector	RW	8	use_native_sector	8'h0	Used to store the use native sector.
00E3H	native_sector_size	RW	8	native_sector_size	8'h0	Used to store the native sector size.
00E4H	vendor_specific_fields_0	RW	32	vendor_specific_fields_0	32'h0	Vendor Specific Fields 0
00E8H	vendor_specific_fields_1	RW	32	vendor_specific_fields_1	32'h0	Vendor Specific Fields 1
00ECH	vendor_specific_fields_2	RW	32	vendor_specific_fields_2	32'h0	Vendor Specific Fields 2
00F0H	vendor_specific_fields_3	RW	32	vendor_specific_fields_3	32'h0	Vendor Specific Fields 3
00F4H	Reserved	RW	16	Reserved	16'h0	Reserved
00F6H	program_csd_cid_ddr_support	RW	8	program_csd_cid_ddr_support	8'h0	Used to store program_csd_cid_ddr_support.
00F7H	periodic_wakeup	RW	8	periodic_wakeup	8'h0	Used to store periodic_wakeup.
00F8H	TCASE_SUPPORT	RW	8	TCASE_SUPPORT	8'h0	Used to store TCASE_SUPPORT.
00F9H	product_state_aware	RW	8	product_state_aware	8'h0	Production State Awareness
00FAH	sec_bad_blk_mgmnt	RW	8	sec_bad_blk_mgmnt	8'h0	Used to store the sec_bad_blk_mgmnt value.
00FBH	Reserved	RW	8	Reserved	8'h0	Reserved
00FCH	enhanced_start_addr	RW	32	enhanced_start_addr	32'h0	Used to store the enhanced start address.
0100H	enhance_size_mult	RW	24	enhance_size_mult	24'h0	Enhanced Size Multiply
0103H	gp_size_mult_0	RW	8	gp_size_mult_0	8'h0	Gp_size Multiply 0
0104H	gp_size_mult_1	RW	32	gp_size_mult_1	32'h0	Gp_size Multiply 1
0108H	gp_size_mult_2	RW	32	gp_size_mult_2	32'h0	Gp_size Multiply 2
010CH	gp_size_mult_3	RW	24	gp_size_mult_3	24'h0	Gp_size Multiply 3
010FH	part_set_complete	RW	8	part_set_complete	8'h0	Used to store partition setting complete.
0110H	part_attr	RW	8	part_attr	8'h0	Used to store the partition attribute.
0111H	max_enh_size_mult	RW	24	max_enh_size_mult	24'h0	Used to store maximum enhanced size multiply.
0114H	part_support	RW	8	part_support	8'h0	Used to store partition support.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0115H	HPI_manage	RW	8	HPI_manage	8'h0	Used to store HPI management.
0116H	rst_n_func	RW	8	rst_n_func	8'h0	Used to store rst_n function.
0117H	BKOPS_ena	RW	8	BKOPS_ena	8'h0	Used to store BKOPS enable.
0118H	BKOPS_start	RW	8	BKOPS_start	8'h0	Used to store BKOPS start.
0119H	Sanitize_start	RW	8	Sanitize_start	8'h0	Used to store Sanitize start.
011AH	WR_REL_PARAM	RW	8	WR_REL_PARAM	8'h0	Used to store WR_REL_PARAM.
011BH	WR_REL_EN	RW	8	WR_REL_EN	8'h0	Used to store WR_REL_EN.
011CH	RPMB_size_mult	RW	8	RPMB_size_mult	8'h0	Used to store RPMB size multiply.
011DH	FW_CONFIG	RW	8	FW_CONFIG	8'h0	Used to store FW_CONFIG.
011EH	Reserved	RW	8	Reserved	8'h0	Reserved
011FH	USER_WP	RW	8	USER_WP	8'h0	Used to store USER_WP.
0120H	Reserved	RW	8	Reserved	8'h0	Reserved
0121H	BOOT_WP	RW	8	BOOT_WP	8'h0	Used to store BOOT_WP.
0122H	boot_wr_protect_status	RW	8	boot_wr_protect_status	8'h0	Used to store the boot write protection status register.
0123H	high_capacity_erase_unit_size_and_timeout	RW	8	high_capacity_erase_unit_size_and_timeout	8'h0	Used to store the high capacity erase unit size and timeout value.
0124H	Reserved	RW	8	Reserved	8'h0	Reserved
0125H	bus_width_for_boot	RW	8	bus_width_for_boot	8'h0	Used to store the Bus width for boot operation.
0126H	BOOT_CONFIG_PROT	RW	8	BOOT_CONFIG_PROT	8'h0	Used to store BOOT_CONFIG_PROT.
0127H	cfg_for_part	RW	8	cfg_for_part	8'h0	Used to store the configuration for partition.
0128H	Reserved	RW	8	Reserved	8'h0	Reserved
0129H	erase_mem_content	RW	8	erase_mem_content	8'h0	Erased Memory Content
012AH	Reserved	RW	8	Reserved	8'h0	Reserved
012BH	bus_width_mode	RW	8	bus_width_mode	8'h0	Used to store the bus width mode.
012CH	strobe_support	RW	8	strobe_support	8'h0	Strobe Support
012DH	high_speed_interface_timing	RW	8	high_speed_interface_timing	8'h0	Used to store the high speed interface timing.
012EH	Reserved	RW	8	Reserved	8'h0	Reserved
012FH	power_class	RW	8	power_class	8'h0	Used to store the power class.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0130H	Reserved	RW	8	Reserved	8'h0	Reserved
0131H	cmd_set_revision	RW	8	cmd_set_revision	8'h0	Used to store command set revision.
0132H	Reserved	RW	8	Reserved	8'h0	Reserved
0133H	cmd_set	RW	8	cmd_set	8'h0	Used to store command set.
0134H	ext_csd_revision	RW	8	ext_csd_revision	8'h0	Used to store extended CSD revision.
0135H	Reserved	RW	8	Reserved	8'h0	Reserved
0136H	csd_structure_ver	RW	8	csd_structure_ver	8'h0	Used to store the CSD structure version.
0137H	Reserved	RW	8	Reserved	8'h0	Reserved
0138H	card_type	RW	8	card_type	8'h0	Used to store the card type.
0139H	IO_driver_strength	RW	8	IO_driver_strength	8'h0	Used to store the I/O driver strength.
013AH	out_of_int_busy_timing	RW	8	out_of_int_busy_timing	8'h0	Used to store the interrupt busy timing exceeded.
013BH	part_switch_timing	RW	8	part_switch_timing	8'h0	Used to store the partition switch timing.
013CH	power_class_52_195	RW	8	power_class_52_195	8'h0	Used to store the power class for 52 MHz (1.95v).
013DH	power_class_26_195	RW	8	power_class_26_195	8'h0	Used to store the power class for 26 MHz (1.95v).
013EH	power_class_52_36	RW	8	power_class_52_36	8'h0	Used to store the power class for 52 MHz (3.6v).
013FH	power_class_26_36	RW	8	power_class_26_36	8'h0	Used to store the power class for 26 MHz (3.6v).
0140H	Reserved	RW	8	Reserved	8'h0	Reserved
0141H	rd_4bit_26M	RW	8	rd_4bit_26M	8'h0	Used to store the minimum read performance for 4 bit at 26MHz.
0142H	wr_4bit_26M	RW	8	wr_4bit_26M	8'h0	Used to store the minimum write performance for 4 bit at 26MHz.
0143H	rd_8bit_26M	RW	8	rd_8bit_26M	8'h0	Used to store the minimum read performance for 8 bit at 26MHz/4 bit at 52MHz.
0144H	wr_8bit_26M	RW	8	wr_8bit_26M	8'h0	Used to store the minimum write performance for 8 bit at 26MHz/4 bit at 52MHz.
0145H	rd_8bit_52M	RW	8	rd_8bit_52M	8'h0	Used to store the minimum read performance for 8 bit at 52MHz.
0146H	wr_8bit_52M	RW	8	wr_8bit_52M	8'h0	Used to store the minimum write performance for 8 bit at 52MHz.
0147H	secure_WP_INFO	RW	8	secure_WP_INFO	8'h0	Secure WP Information
0148H	sector_cnt	RW	32	sector_cnt	32'h0	Sector Count
014CH	sleep_notification_time	RW	8	sleep_notification_time	8'h0	Sleep Notification Time
014DH	max_timeout_for_stby_slp	RW	8	max_timeout_for_stby_slp	8'h0	Used to store the maximum time out value for state transitions from Standby state (stby) to Sleep state (slp) and from Sleep state (slp) to Standby state (stby).

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
014EH	product_state_aware_timeout	RW	8	product_state_aware_timeout	8'h0	Production State Awareness Timeout
014FH	S_C_VCCQ	RW	8	S_C_VCCQ	8'h0	Used to store the maximum VCC current (S_C_VCCQ) consumption during the Sleep state.
0150H	S_C_VCC	RW	8	S_C_VCC	8'h0	Used to store the maximum VCC current (S_C_VCC) consumption during the Sleep state.
0151H	wr_protect_group_size	RW	8	wr_protect_group_size	8'h0	Used to store the write protect group size for high-capacity memory.
0152H	sector_cnt	RW	8	sector_cnt	8'h0	Used to store the sector count for reliable write operation.
0153H	calcu_erase_time_out	RW	8	calcu_erase_time_out	8'h0	Used to calculate the Erase time out for High capacity Erase operations.
0154H	calcu_erase_unit_size	RW	8	calcu_erase_unit_size	8'h0	Used to calculate the Erase unit size for High capacity memory card.
0155H	calcu_sup_page_size	RW	8	calcu_sup_page_size	8'h0	Used to calculate the super page size for boot area access.
0156H	calcu_boot_part_size	RW	8	calcu_boot_part_size	8'h0	Used to calculate the boot partition size.
0157H	Reserved	RW	8	Reserved	8'h0	Reserved
0158H	boot_info	RW	8	boot_info	8'h0	Used to store boot information.
0159H	SEC_TRIM_MULT	RW	8	SEC_TRIM_MULT	8'h0	Used to store SEC TRIM MULTIPLY.
015AH	SEC_ERASE_MULT	RW	8	SEC_ERASE_MULT	8'h0	Used to store SEC ERASE MULTIPLY.
015BH	SEC_FEATURE_SUPPORT	RW	8	SEC_FEATURE_SUPPORT	8'h0	Used to store SEC FEATURE SUPPORT.
015CH	TRIM_MULT	RW	8	TRIM_MULT	8'h0	Used to store TRIM MULTIPLY.
015DH	Reserved	RW	8	Reserved	8'h0	Reserved
015EH	MIN_PERF_DDR_R_8_52	RW	8	MIN_PERF_DDR_R_8_52	8'h0	Used to store MIN_PERF_DDR_R_8_52.
015FH	MIN_PERF_DDR_w_8_52	RW	8	MIN_PERF_DDR_w_8_52	8'h0	Used to store MIN_PERF_DDR_w_8_52.
0160H	PWR_CL 200_130	RW	8	PWR_CL 200_130	8'h0	Used to store PWR_CL 200_130.
0161H	PWR_CL 200_195	RW	8	PWR_CL 200_195	8'h0	Used to store PWR_CL 200_195.
0162H	PWR_CL DDR_52_195	RW	8	PWR_CL DDR_52_195	8'h0	Used to store PWR_CL DDR_52_195.
0163H	PWR_CL DDR_52_360	RW	8	PWR_CL DDR_52_360	8'h0	Used to store PWR_CL DDR_52_360.
0164H	cache_flushing_policy	RW	8	cache_flushing_policy	8'h0	Cache Flushing Policy
0165H	ini_timeout_ap	RW	8	ini_timeout_ap	8'h0	Used to store ini_timeout_ap.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0166H	correctly_program_sectors_num_0	RW	16	correctly_program_sectors_num_0	16'h0	Used to store the number of FW sectors correctly programmed.
0168H	correctly_program_sectors_num_1	RW	16	correctly_program_sectors_num_1	16'h0	Used to store the number of FW sectors correctly programmed.
016AH	background_operation_status	RW	8	background_operation_status	8'h0	Used to store the background operation status.
016BH	POWER_OFF_LONG_TIME	RW	8	POWER_OFF_LONG_TIME	8'h0	Used to store POWER_OFF_LONG_TIME.
016CH	GENERIC_CMD6_TIME	RW	8	GENERIC_CMD6_TIME	8'h0	Used to store GENERIC_CMD6_TIME.
016DH	CACHE_SIZE_0	RW	24	CACHE_SIZE_0	24'h0	Used to store CACHE_SIZE.
0170H	CACHE_SIZE_1	RW	8	CACHE_SIZE_1	8'h0	Used to store CACHE_SIZE.
0171H	PWR_CL_DDR_200_360	RW	8	PWR_CL_DDR_200_360	8'h0	PWR_CL_DDR_200_360
0172H	firmware_ver_0	RW	16	firmware_ver_0	16'h0	Firmware Version 0
0174H	firmware_ver_1	RW	32	firmware_ver_1	32'h0	Firmware Version 1
0178H	firmware_ver_2	RW	16	firmware_ver_2	16'h0	Firmware Version 2
017AH	device_ver	RW	16	device_ver	16'h0	Device Version
017CH	optimal_trim_unit_size	RW	8	optimal_trim_unit_size	8'h0	Optimal Trim Unit Size
017DH	optimal_write_size	RW	8	optimal_write_size	8'h0	Optimal Write Size
017EH	optimal_read_size	RW	8	optimal_read_size	8'h0	Optimal Read Size
017FH	PRE_EOL_INFO	RW	8	PRE_EOL_INFO	8'h0	PRE_EOL_INFO
0180H	DEVICE_LIFE_TIME_EST_TYP_A	RW	8	DEVICE_LIFE_TIME_EST_TYP_A	8'h0	DEVICE_LIFE_TIME_EST_TYP_A
0181H	DEVICE_LIFE_TIME_EST_TYP_B	RW	8	DEVICE_LIFE_TIME_EST_TYP_B	8'h0	DEVICE_LIFE_TIME_EST_TYP_B
0182H	vendor_proprietary_health_report_0	RW	16	vendor_proprietary_health_report_0	16'h0	Vendor Proprietary Health Report
0184H	vendor_proprietary_health_report_1	RW	32	vendor_proprietary_health_report_1	32'h0	Vendor Proprietary Health Report
0188H	vendor_proprietary_health_report_2	RW	32	vendor_proprietary_health_report_2	32'h0	Vendor Proprietary Health Report
018CH	vendor_proprietary_health_report_3	RW	32	vendor_proprietary_health_report_3	32'h0	Vendor Proprietary Health Report
0190H	vendor_proprietary_health_report_4	RW	32	vendor_proprietary_health_report_4	32'h0	Vendor Proprietary Health Report

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0194H	vendor_proprietary_health_report_5	RW	32	vendor_proprietary_health_report_5	32'h0	Vendor Proprietary Health Report
0198H	vendor_proprietary_health_report_6	RW	32	vendor_proprietary_health_report_6	32'h0	Vendor Proprietary Health Report
019CH	vendor_proprietary_health_report_7	RW	32	vendor_proprietary_health_report_7	32'h0	Vendor Proprietary Health Report
01A0H	vendor_proprietary_health_report_8	RW	16	vendor_proprietary_health_report_8	16'h0	Vendor Proprietary Health Report
01A2H	FW_sector_correct_program_num_0	RW	16	FW_sector_correct_program_num_0	16'h0	Number of FW Sector Correctly Programmed
01A4H	FW_sector_correct_program_num_1	RW	16	FW_sector_correct_program_num_1	16'h0	Number of FW Sector Correctly Programmed
01A6H	Reserved	RW	8	Reserved	8'h0	Reserved
01A7H	cmd_queue_depth	RW	8	cmd_queue_depth	8'h0	CMD Queuing Depth
01A8H	cmd_queue_support	RW	8	cmd_queue_support	8'h0	CMD Queuing Support
01A9H	Reserved	RW	464	Reserved	464'h0	Reserved
01E3H	Reserved	RW	472	Reserved	472'h0	Reserved
021EH	barrier_support	RW	8	barrier_support	8'h0	Barrier Support
021FH	FFU_ARG_0	RW	8	FFU_ARG_0	8'h0	FFU_ARG
0220H	FFU_ARG_1	RW	24	FFU_ARG_1	24'h0	FFU_ARG
0223H	oper_code_time	RW	8	oper_code_time	8'h0	Operation Code Time
0224H	FFU_features	RW	8	FFU_features	8'h0	FFU Features
0225H	supported_mode	RW	8	supported_mode	8'h0	Supported Mode
0226H	EXT_SUPPORT	RW	8	EXT_SUPPORT	8'h0	Used to store EXT_SUPPORT.
0227H	LARGE_UNIT_SIZE_M1	RW	8	LARGE_UNIT_SIZE_M1	8'h0	Used to store LARGE_UNIT_SIZE_M1.
0228H	CONTEXT_CAPABILITIES	RW	8	CONTEXT_CAPABILITIES	8'h0	Used to store CONTEXT_CAPABILITIES.
0229H	TAG_RES_SIZE	RW	8	TAG_RES_SIZE	8'h0	Used to store TAG_RES_SIZE.
022AH	TAG_UNIT_SIZE	RW	8	TAG_UNIT_SIZE	8'h0	Used to store TAG_UNIT_SIZE.
022BH	DATA_TAG_SUPPORT	RW	8	DATA_TAG_SUPPORT	8'h0	Used to store DATA_TAG_SUPPORT.
022CH	MAX_PACKED_WRITE	RW	8	MAX_PACKED_WRITE	8'h0	Used to store MAX_PACKED_WRITE.
022DH	MAX_PACKED_READS	RW	8	MAX_PACKED_READS	8'h0	Used to store MAX_PACKED_READS.

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Offset	Register Name	Access	Bits	Field Name	Default Value	Description
022EH	background_operation	RW	8	background_operation	8'h0	Used to store background operation support.
022FH	high_proirity_int_supp	RW	8	high_proirity_int_supp	8'h0	Used to store high proirity interrupt feature.
0230H	supp_cd_sets_0	RW	8	supp_cd_sets_0	8'h0	Used to store supported command sets 0 - standard eMMC.
0231H	ext_security_cmd_err	RW	8	ext_security_cmd_err	8'h0	Extended Security Command Error
0232H	Reserved	RW	48	Reserved	48'h0	Reserved