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Horizon Robotics

Power Delivery Network Analysis

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
0.1	2021/05/20	Initial draft
1.0	2021/07/12	First Revision

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1 Overview

Power integrity (PI) is a broad term used in the electronics industry that refers to the analysis of how effectively power is delivered from the source to the load within a system. The power delivery network (PDN) consists of all the interconnects in the power supply path from the voltage regulator modules (VRMs) to the circuits on the die. Generally, these include passive components and interconnects from the source to the load including packaging up to the semiconductor.

PDN performances were not considered as major criteria in the early of the PCB designs. In today's platform with lower voltage, higher current, smaller voltage noise margin, PDN performances should be estimated early in the PCB design and optimized to meet the device specification.

The objective of a PDN is to supply a clean and stable voltage to the device. However the PDN is not ideal due to the parasitic added by the elements constituting the power network. Figure 1 presents a break-down model of a complete PDN network from Voltage Resource Manager (VRM) to the Application Processor (AP).

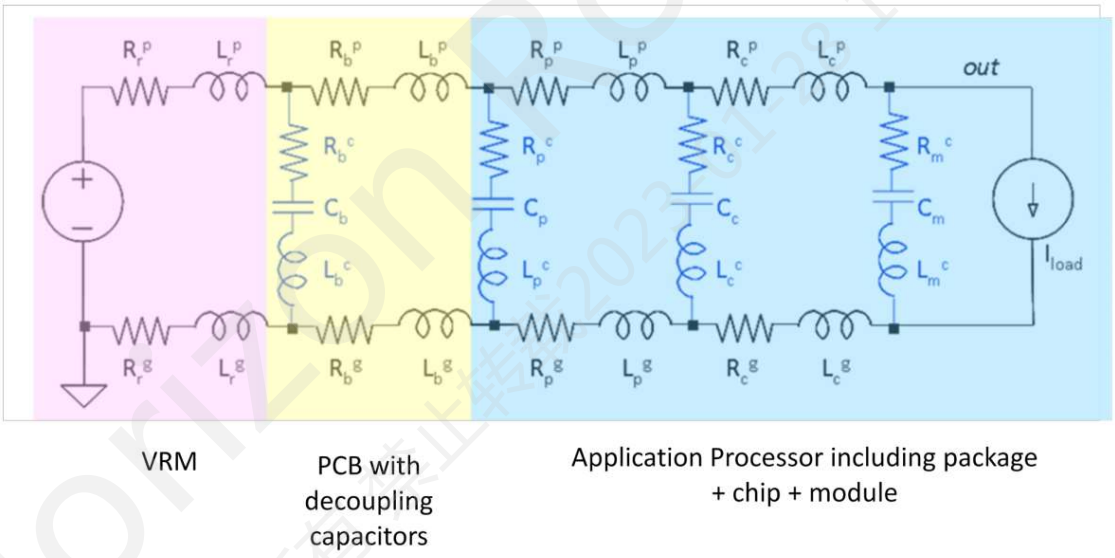

Figure 1: Power Delivery Network model

The purpose of the PDN is to:

- Distribute low-noise DC voltage and power to the active devices doing all the work.
- Provide a low-noise return path for all the signals.
- Mitigate electromagnetic interference (EMI) problems without contributing to radiated emissions.

Here we focus on the first role of the PDN: to distribute a DC voltage and power to all the active devices requiring power and to keep the noise below an acceptable level. Unsuccessful noise control on the PDN will contribute to contraction of the eye of any signal. The amplitude of the eye in the vertical direction collapses from voltage noise. The time of the

signal crossing a reference spreads out in the horizontal direction creating jitter and reduction of the eye opening. Internal core circuits might suffer setup and hold-time errors, leading to functional failures.

This APN focuses on the analysis of the PCB and the decoupling capacitors strategy used.

2 Necessities

To extract the PDN performances of the PCB layout, you will need some design related inputs as listed in Table 1.

Table 1: The necessities for PDN extraction

Item	Necessities	Description
1	Schematic	*.DSN, *.pdf, etc.
2	PCB Layout	*.brd, ODB++, etc.
3	PCB Stack-up with dielectric properties (Dk and Df)	See Table 2
4	Bill of material	Including Part Number, Value and reference
5	S-parameters capacitors models from manufacturer	SnP models from manufacturer
6	Power Integrity (PI) tool	3D-EM (at least 2.5D) solver

Layer stack up should include all metal and dielectric physical and electrical characteristics, including material, thickness, Dk and Df. Table 2 is a reference PCB Stackup 8 Layers for PDN Extraction.

Table 2: Reference PCB Stackup 8 Layers

Subclass Name	Type	Thickness (Mil)	Cu (Oz)	Dielectric Constant(Dk)	Loss Tangent(Df)
	Solder Mask	0.5		4	0.026
Top	Signal	1.9	1/3+Plating		
	IT-180A_1067(PP)	2.76		3.79	0.0161
L2	Plane	1.2	1		
	IT-180A_1080X2(CORE)	4.33		4.15	0.0154
L3	Signal	1.2	1		
	IT-180A_7628(PP)	7.06		4.53	0.0148
L4	Plane	1.2	1		
	IT-180A_7628X3(CORE)	20.07		4.62	0.0147
L5	Plane	1.2	1		
	IT-180A_7628(PP)	7.06		4.53	0.0148
L6	Signal	1.2	1		
	IT-180A_1080X2(CORE)	4.33		4.15	0.0154
L7	Plane	1.2	1		
	IT-180A_1067(PP)	2.76		3.79	0.0161
Bottom	Signal	1.9	1/3+Plating		
	Solder Mask	0.5		4	0.026

3 DC resistance

DC resistance is determined by the geometry of the net, its material conductivity, refer to Figure 2.

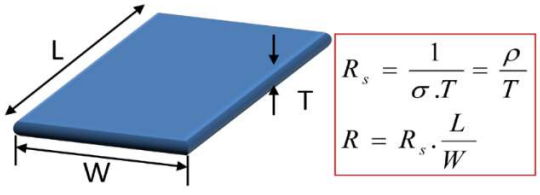

Figure 2 DC resistance

The resistance Rs of a plane conductor for a unit length and unit width is called the surface resistivity (ohms per square).

Once DC resistance is determined, IR drop can be calculated with Ohm's law.

$$DC\ IR\ drop = R_{dc} \cdot I$$

An IR drop of 0.5%-2.5% of the nominal voltage is tolerated depending on the total system-level margin allowed for proper device functionality and sense line position.

TI specifies in the Data Manual (DM) a board DC resistance budget, from VRM to OMAP balls for critical power nets.

Due to the shape geometry complexity, vias and multilayer's used during the net routing, it is difficult to calculate manually the DC resistance. Numerous Signal Integrity (SI) or Layout EDA tools extract the DC resistance.

Figure 3 describe the flow used by most of the tool to extract DC resistance. In HR PDN analysis, the lumped methodology is preferred; each power and GND pins of VRM and AP are grouped.

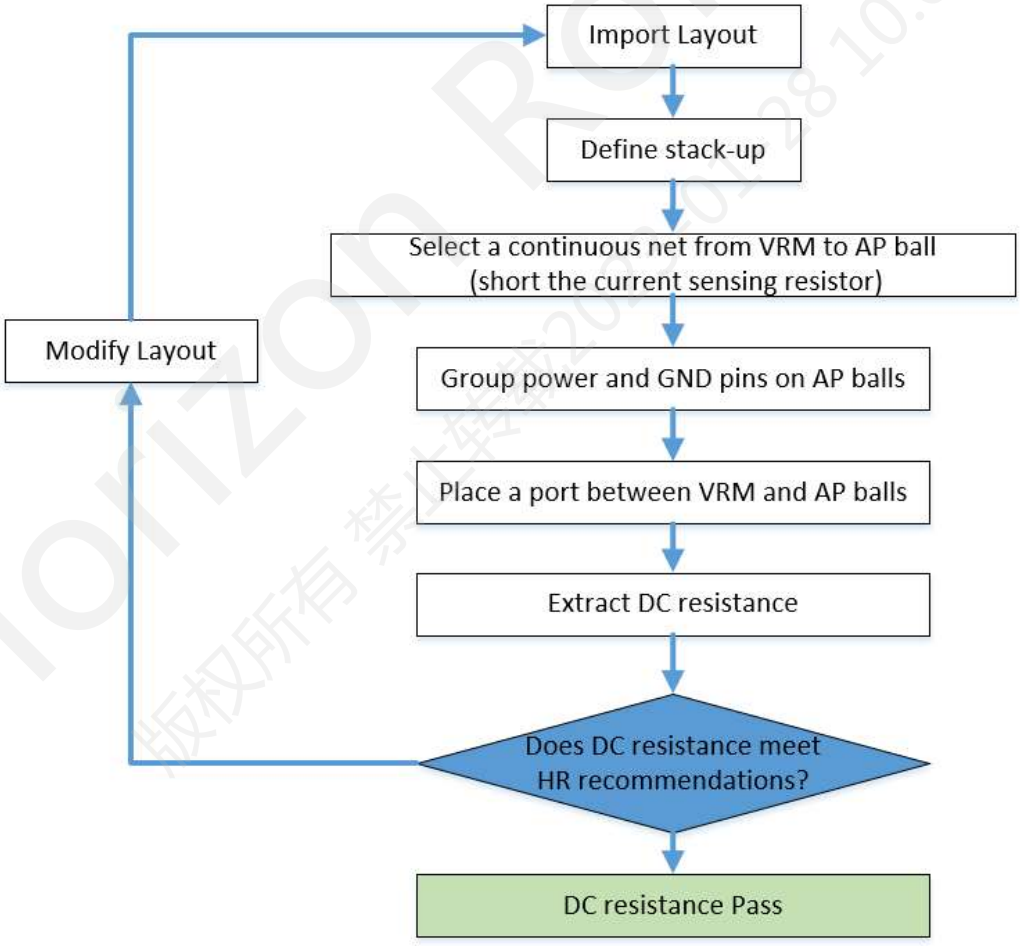

Figure 3 DC resistance extraction flow

Table 3 presents the DC resistivity analysis of VDD_CNN0, VDD_CNN1, VDD_CPU and

VDD_CORE_PD on J3 reference PCB. DC resistance, which should be as low as possible, are below the recommendations in J3 hardware design guide.

Table 3: DC resistance of J3 reference design

	Extracted resistance(mOhm)	HR recommendations(mOhm)
VDD_CNN0	6	<10
VDD_CNN1	6	<10
VDD_CPU	14	<15
VDD_CORE_PD	5	<9

General recommendations for minimizing DC resistivity:

- Shorten the length of the power nets trace by optimizing VRM and AP placement but also their balls positioning.
- Widen the power nets trace.
- Avoid discontinuity in power nets trace by inserting other signal nets or matrix of vias with their associated anti-pads (Swiss cheese effect) within the power nets.
- Avoid via starvation by determining maximum current carrying capacity and numbers of transitional via.

4 Capacitor Loop inductance

The loop inductance is a parameter quantifying the effectiveness of a decoupling capacitor. Figure 4 represents the different loop inductances added to the capacitor ESL.

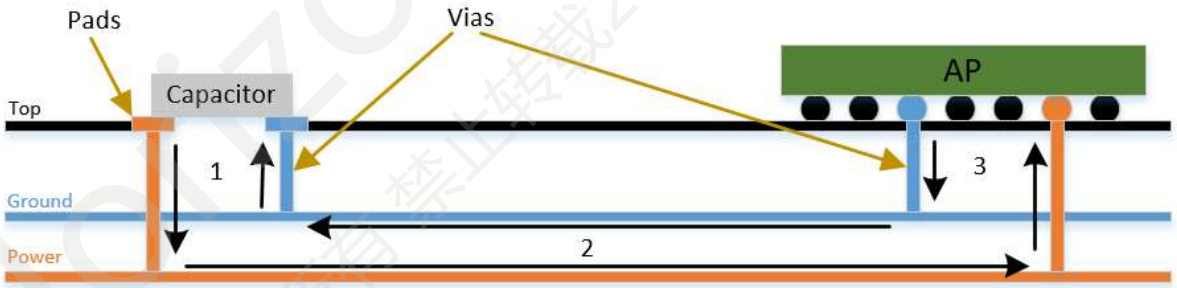

Figure 4: Loop inductance principle

Figure 5 shows a typical flow for capacitors Z-parameters extraction. Once Z-parameters is extracted, the loop inductance of a capacitor is determined by

$$L_{eff} = \frac{Imaginary\ Z_{power,gnd\ pads\ of\ caps}}{2\pi * Freq}$$

Where Leff is the effective loop inductance, Zpower , gnd pads of caps represents the Z-

response of the port defined across the power and ground pads of the corresponding capacitors.

Typically, capacitors loop inductance is determined at a frequency of 100 MHz.

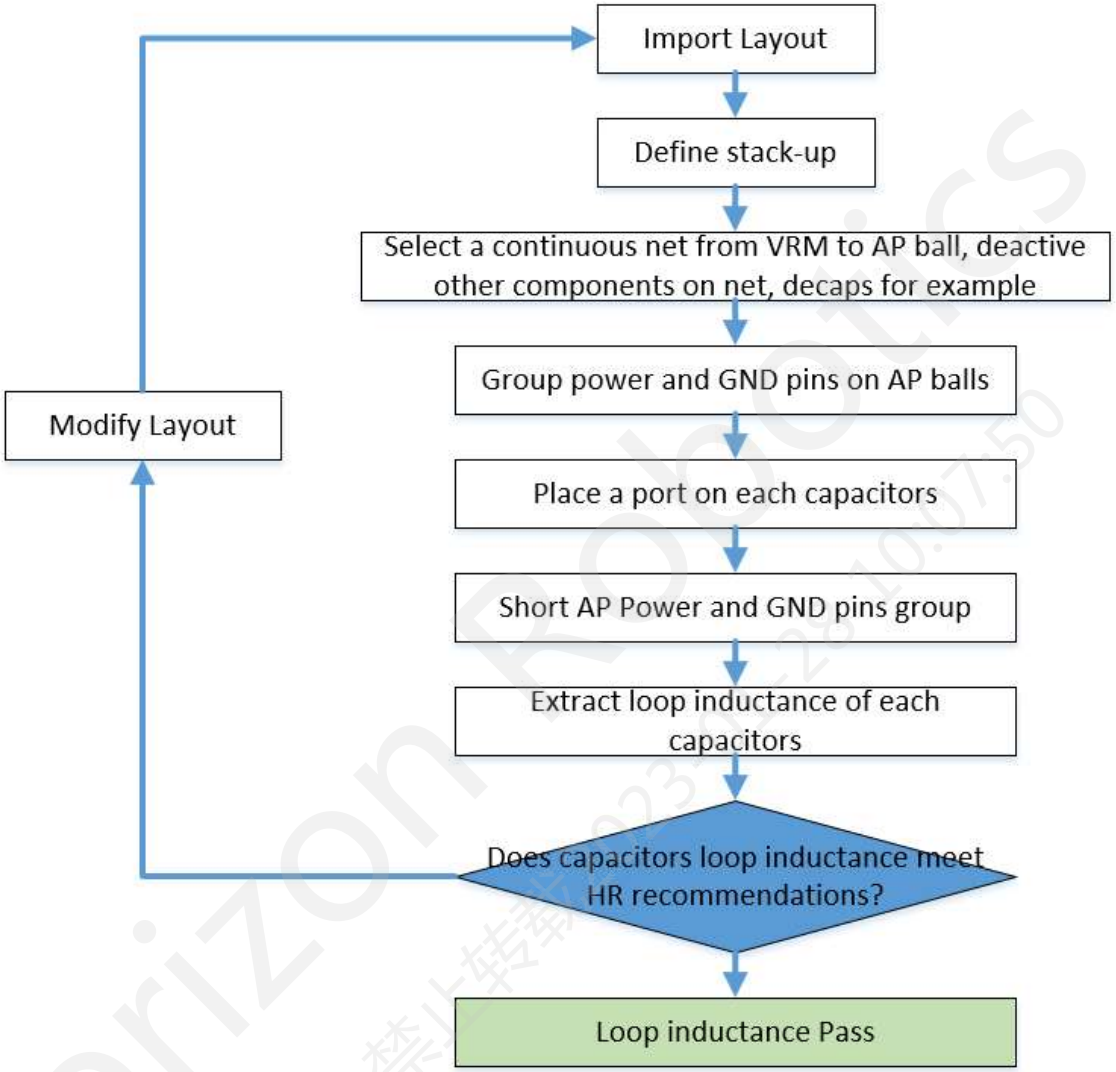

Figure 5 Capacitors Loop inductance extraction flow

Table 4 presents the loop inductance results of VDDQ decoupling capacitors at the back of J3 chip on reference PCB at 100 MHz. The key capacitors loop inductances, which should be as low as possible, are below 0.7nH which recommended in J3 hardware design guide.

Table 4: Capacitors Loop inductance on J3 VDDQ

Capacitor instances	Loop inductance at 100MHz	HR Recommendation
CF038	0.1673nH	<0.7nH
CF046	0.1986nH	
CF054	0.2084nH	
CF061	0.283nH	
CF062	0.2669nH	

CF114	0.1848nH	
CF112	0.6383nH	
CF115	0.4297nH	
CF116	0.5527nH	
CF117	0.4832nH	

General recommendations for minimizing capacitors loop inductance:

- Place vias as close to AP balls.
- Add more vias for AP balls.
- Use via-in-pads for capacitors.
- Place decoupling capacitors closed to AP.
- Select capacitors with small footprint to minimize ESL.

5 PDN Extraction

5.1 PDN Extraction Guidelines

The board level extraction guidelines are intended to work in any EDA extraction tool and are not tool-specific.

- Check the board stack-up for accurate layer thickness and material properties. (Djordjevic-Sarkar models is recommended)
- Extract power plane in a 3D-EM (at least 2.5D) solver.
- If the board layout is cut prior to extraction (to reduce simulation time), please define a cut boundary that is at least 0.25 inch away from the power nets.
- Check the via pad stack definitions. Ensure that the non-functional internal layer pads on signal vias are modeled the same way they would be fabricated.
- Use wide-band Spice/S-parameter models (typically available from the vendor) for modeling all passives (especially the capacitors) in the system.
- Use a normalized impedance of 1 Ohm.
- Span from DC point up to ftop=5GHz. Table 5 is the advised s-parameter number of points/sweep by frequency range.

Table 5: Sweep Frequency and Point Setting

Frequency [Hz]	Sweep	# points
0	Lin	1
[1k, ftop]	Dec	300/Dec

It is important to ensure that the frequency sweep begins at 0Hz, which is required by the nature of causality.

The frequency step/spacing/ftop of the S-parameter data also affect the causality of the data, the closer the frequency spacing and a higher maximum frequency, the better the S-parameter model.

- Proposed PDN Flow are based on loop resistance/inductance between power supply from PMIC output to AP package balls.
- The perspective of the PDN analysis is viewed from the side of the AP balls.
- The PDN impedance does not include the PMIC、AP package and silicon die.
- Recommend that PDN impedance be as low as possible.

Figure 6 presents a typical flow for a PDN impedance extraction.

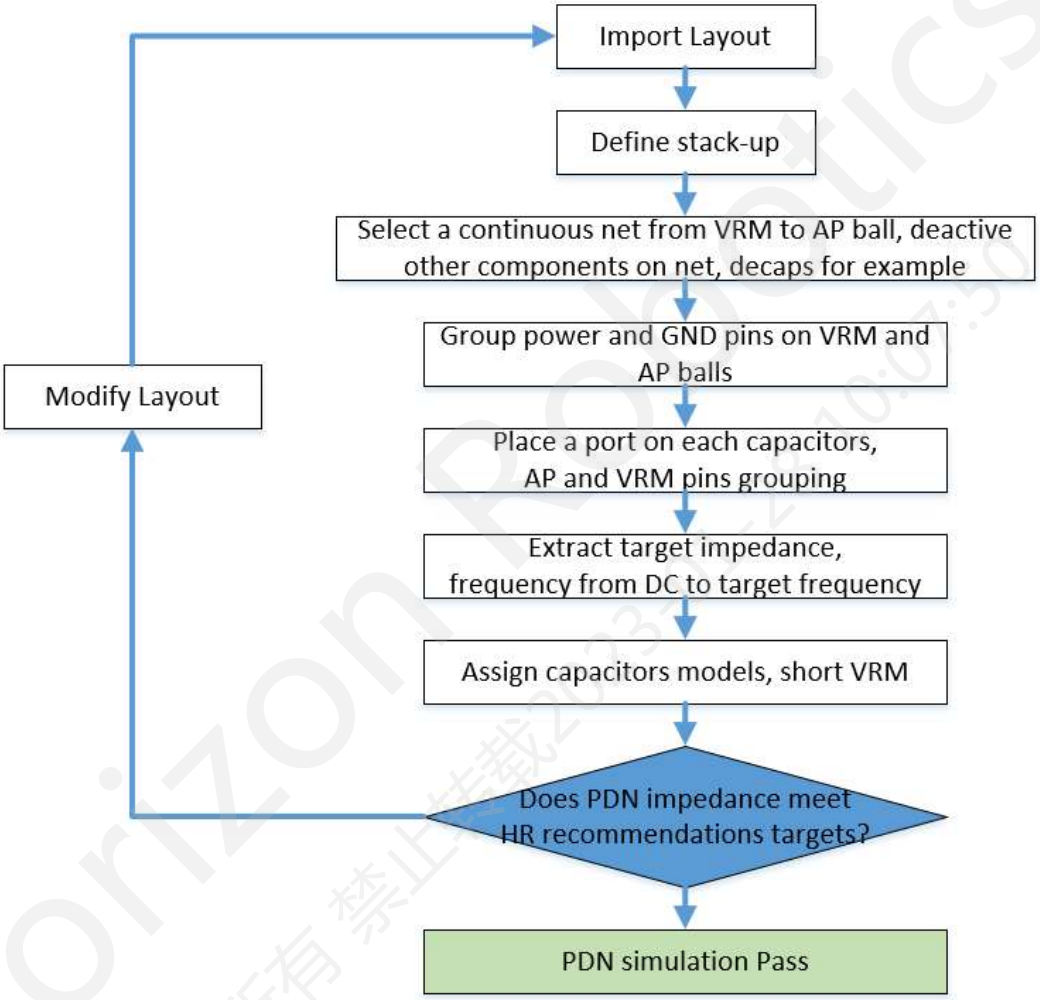

Figure 6: PDN Extraction Flow

6 PDN Target

Horizon specifies an impedance target (ZTARGET) and a frequency range (FMAX) in hardware design guide document. **PDN simulation results must meet these ZTARGETs at the respective specified frequency FMAX before PCB Gerber out.**

As an example, Table 6 refers to J3 PDN requirements for VDDQ in LPDDR4 mode.

Table 6: PDN Target for J3 VDDQ in LPDDR4 Mode

PARAMETERS	PDN IMPEDANCE CHARACTERISTCS		PCB DC RESISTANCE 0~200KHz (mOhm)	MAXIMUM LOOP INDUCTANCE PER CAPACITOR(WO ESL)(nH)
	IMPEDANCE TARGET(mOhm)	FREQUENCY OF INTEREST(MHz)		
VDDQ_DDR	37.4	30	6	0.5
	105	160		
VDD_DDR	44	30	12	0.5
	76	70		

During the PDN analysis it is important to capture the decoupling frequency achieved for the required target impedance but also the target impedance achieved at the required decoupling frequency.

Recommendations for improving target impedance response are similar to the recommendations to reduce the capacitors loop inductances. It is clear that reducing or removing capacitors with high loop inductance could help improving the ZTARGET response.

If resonant peak appears before the required decoupling frequency then the decoupling strategy should be modified, add or replace a capacitor by the appropriate value to remove or decrease the resonant peak.

7 PDN Optimization

PCB-PDN design faces challenge of reducing noise margins. One aspect of PDN design is to find the number of decoupling capacitors required for each power rail. As more capacitors are added, the mid frequency equivalent inductance in the impedance of the PCB-PDN converges to a minimum value for each placement pattern. This convergence is studied for different placement patterns to find the least number of capacitors required to satisfy a certain convergence criteria.

For each power supply, there are several options to optimize the PDN results:

- Optimal set of capacitors
- Inductance of capacitor
- BGA via pair loop inductance
- Power/Ground plane inductance

To achieve optimal performance, the composite impedance must meet the target impedance up until the PCB cutoff frequency. If the design impedance exceeds the target impedance, there will be PSIJ problems, which will affect the signal integrity.

7.1 Cascaded Capacitors Optimization

Different decoupling capacitors have different self-resonant frequency which allow the noise that lies near the self-resonant frequency to pass, it is critical to choose the right capacitor for decoupling based on PDN extraction result.

The solution is to cascade the same and different capacitors to reduce the ESR, widen the impedance bandwidth, and lower the physical inductance.

Figure 7 represents various target impendence responses with different decoupling strategy, bare PCB (no capacitors), only 100nF capacitors, HR recommendation (the combination of 1.5nf+3.3nf+10nf+100nf).

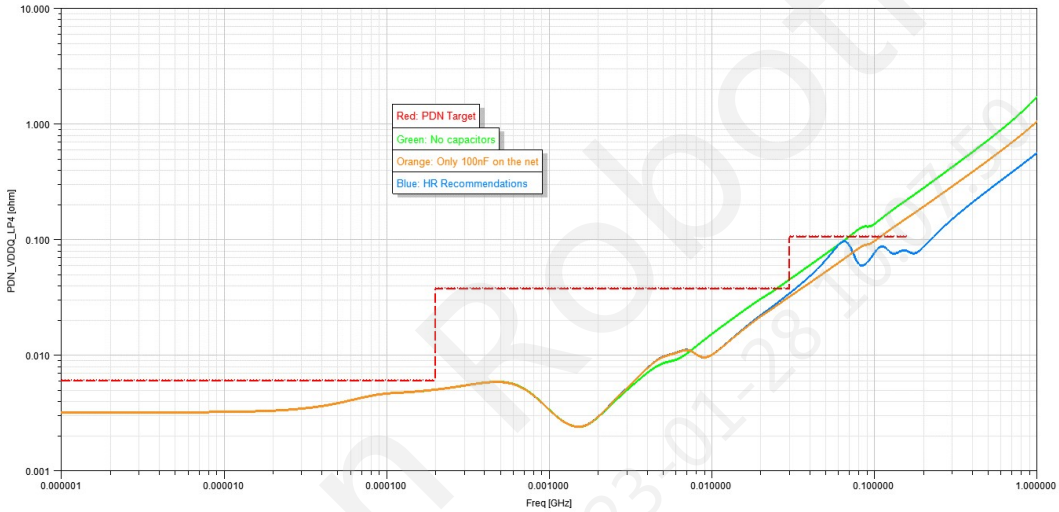

Figure 7: J3 VDDQ PDN response

7.2 Fanout Optimization

To increase the effectiveness of capacitors, the parasitic inductance of BGA and capacitor fan-out trace must be minimized. Parasitic inductance is mostly in the pad and via structure and inductance is minimized by minimizing the area of the current loop.

In order to avoid the long, inductive plated through hole vias (PTH), there are three methods:

- Reduce the thickness of PCB stackup to get a short PTH
- Add the number of BGA vias
- Use via-in-pad design for BGA and capacitor fanout

Merge multiple BGA balls to a BGA via will add bare PCB inductance and reduce the effectiveness of peripheral capacitors. To minimize the inductance of BGA via pair loop inductance, we strongly recommend each BGA ball has one or two BGA via and the ratio of BGA via to VGA ball should equal or larger than 1:1. Figure 8 represents an example of BGA fanout method from Horizon reference board.

Figure 8: Recommended BGA Fanout Example

Also different capacitor PCB footprints have different loop area and the resulting mounting inductance. Via-in-pad method has smallest inductance and become more popular in nowadays application. We strongly recommend via-in-pad design as Figure 9 for DDR application.

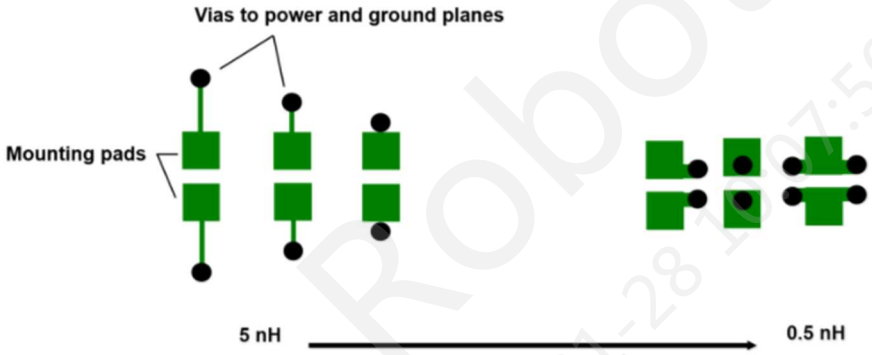

Figure 9: Various Capacitor Footprints

Furthermore, place decoupling caps on the top layer and use higher layer in the PCB stackup for power planes to which connect the decoupling cap's power vias. This further reduce inductance again by minimizing loop area of the power network.