X3M Register Reference Manual
eMMC Host

Revision History

Revision	Date	Description
1.0	August-27-2020	Initial Release

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	00H	CTRL	R/W	[31:26]	Reserved		
				[25]	use_internal_dmac	1'h0	Present only for the Internal DMAC configuration; else, it is reserved. 0: The host performs data transfers through the slave interface. 1: Internal DMAC used for data transfer.
				[24]		1'h1	External open-drain pull up: 0: Disable. 1: Enable. Inverted value of this bit is output to ccmd_od_pullup_en_n port. When bit is set, command output always driven in open-drive mode; that is, mobile_storage drives either 0 or high impedance, and does not drive hard 1.
				[23:20]	Card_voltage_b	4'h0	Read/Write bits, but not used. No loading.
				[19:16]	Card_voltage_a	4'h0	Read/Write bits, but not used. No loading.
				[15:12]	Reserved		
				[11]	ceata_device_interrupt_status	1'h0	0: Interrupts not enabled in CE-ATA device (nIEN = 1 in ATA control register). 1: Interrupts are enabled in CE-ATA device (nIEN = 0 in ATA control register). Software should appropriately write to this bit after power-on reset or any other reset to CE-ATA device. After reset, usually CE-ATA device interrupt is disabled (nIEN = 1). If the host enables CE-ATA device interrupt, then software should set this bit.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10]	send_auto_stop_ccsd	1'h0	0: Clears bit if mobile_storage does not reset the bit. 1: Sends internally generated STOP after sending CCSD to CE-ATA device. **Note:** Always set send_auto_stop_ccsd and send_ccsd bits together; send_auto_stop_ccsd should not be set independent of send_ccsd. When set, mobile_storage automatically sends internally generated STOP command (CMD12) to CE-ATA device. After sending internally-generated STOP command, Auto Command Done (ACD) bit in RINTSTS is set and generates interrupt to host if Auto Command Done interrupt is not masked. After sending the CCSD, Mobile_storage automatically clears send_auto_stop_ccsd bit.
				[9]	send_ccsd	1'h0	0: Clears bit if mobile_storage does not reset the bit. 1: Sends Command Completion Signal Disable (CCSD) to CE-ATA device. When set, mobile_storage sends CCSD to CE-ATA device. Software sets this bit only if current command is expecting CCS (that is, RW_BLK) and interrupts are enabled in CE-ATA device. Once the CCSD pattern is sent to device, mobile_storage automatically clears send_ccsd bit. It also sets Command Done (CD) bit in RINTSTS register and generates interrupt to host if Command Done interrupt is not masked. **Note:** Once send_ccsd bit is set, it takes two card clock cycles to drive the CCSD on the CMD line. Due to this, during the boundary conditions it may happen that CCS.
				[8]	abort_read_data	1'h0	0: No change 1: After suspend command is issued during read-transfer, software polls card to find when suspend happened. Once suspend occurs, software sets bit to reset data state-machine, which is waiting for next block of data. Bit automatically clears once data state machine resets to idle. Used in SDIO card suspend sequence.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	send_irq_response	1'h0	0: No change. 1: Sends auto IRQ response. Bit automatically clears once response is sent. To wait for MMC card interrupts, host issues CMD40, and mobile_storage waits for interrupt response from MMC card(s). In meantime, if host wants mobile_storage to exit waiting for interrupt state, it can set this bit, at which time mobile_storage command state-machine sends CMD40 response on bus and returns to idle state.
				[6]	read_wait	1'h0	0: Clears read wait. 1: Asserts read wait. For sending read-wait to SDIO cards.
				[5]	Reserved		
				[4]	int_enable	1'h0	Global interrupt enable/disable bit: 0: Disable interrupts. 1: Enable interrupts. The int port is 1 only when this bit is 1 and one or more unmasked interrupts are set.
				[3]	Reserved		
				[2]	dma_reset	1'h0	0: No change. 1: Reset internal DMA interface control logic. To reset DMA interface, firmware should set bit to 1. This bit is auto-cleared after two AHB clocks.
				[1]	fifo_reset	1'h0	0: No change. 1: Reset to data FIFO To reset FIFO pointers. To reset FIFO, firmware should set bit to 1. This bit is auto-cleared after completion of reset operation. **Note:** FIFO pointers will be out of reset after 2 cycles of system clocks in addition to synchronization delay (2 cycles of card clock), after the fifo_reset is cleared.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	controller_reset	1'h0	0: No change. 1: Reset mobile_storage controller. To reset controller, firmware should set bit to 1. This bit is auto-cleared after two AHB and two cclk_in clock cycles. This resets: - BIU/CIU interface. - CIU and state machines. - Abort_read_data, send_irq_response, and read_wait bits of Control register. - Start_cmd bit of Command register. Does not affect any registers or DMA interface, or FIFO or host interrupts.
	04H	PWREN	RW	[31:30]	Reserved		
				[0]	power_enable	1'h0	Read/Write bit, but not used. No loading.
	08H	CLKDIV	RW	[31:24]	clk_divider3	8'h0	Read/Write bits, but not used. No loading.
				[23:16]	clk_divider2	8'h0	Read/Write bits, but not used. No loading.
				[15:8]	clk_divider1	8'h0	Read/Write bits, but not used. No loading.
				[7:0]		8'h0	Clock divider-0 value. Clock division is 2*n. For example, value of 0 means divide by 2*0 = 0 (no division, bypass), value of 1 means divide by 2*1 = 2, value of ff means divide by 2*255 = 510, and so on.
	10H	CLKENA	RW	[31:17]	Reserved		
				[16]	cclk_low_power	1'h0	Low-power control for one SD card clock or one MMC card clock supported. 0: Non-low-power mode. 1: Low-power mode; stop clock when card in IDLE (should be normally set to only MMC and SD memory cards; for SDIO cards, if interrupts must be detected, clock should not be stopped).
				[15:1]	Reserved		
				[0]	cclk_enable	1'h0	Clock-enable control for one SD card clock or one MMC card clock supported. 0: Clock disabled. 1: Clock enabled.

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	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
	14H	TMOUT	RW	[31:8]	data_timeout	24'hffffff	Value for card Data Read Timeout; same value also used for Data Starvation by Host timeout. The timeout counter is started only after the card clock is stopped. Value is in number of card output clocks – cclk_out of selected card. **Note:** The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt needs to be disabled.
				[7:0]	response_timeout	8'h40	Response timeout value. Value is in number of card output clocks – cclk_out.
	18H	CTYPE	RW	[31:17]	Reserved		
				[16]	card_type	1'h0	Indicates if card is 8-bit: 0: Non 8-bit mode. 1: 8-bit mode.
				[15:1]	Reserved		
				[0]	card_width	1'h0	Indicates if card is 1-bit or 4-bit: 0: 1-bit mode. 1: 4-bit mode.
	1CH	BLKSIZ	RW	[31:16]	Reserved		
				[15:0]	block_size	16'h200	Block size.
	20H	BYTCNT	RW	[31:0]	byte_count	32'h200	Number of bytes to be transferred; should be integer multiple of Block Size for block transfers. For undefined number of byte transfers, byte count should be set to 0. When byte count is set to 0, it is responsibility of host to explicitly send stop/abort command to terminate data transfer.
	24H	INTMASK	RW	[31:17]	Reserved		
				[16]	sdio_int_mask	1'h0	Mask SDIO interrupts. When masked, SDIO interrupt detection for that card is disabled. A 0 masks an interrupt, and 2 enables an interrupt.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:0]	int_mask	16'h0	Bits used to mask unwanted interrupts. 0: Masks interrupt. 1: Enables interrupt. Bit[15] – End-bit error (read)/Write no CRC (EBE). Bit[14] – Auto command done (ACD). Bit[13] – Start Bit Error(SBE)/Busy Clear Interrupt (BCI). Bit[12] – Hardware locked write error (HLE). Bit[11] – FIFO underrun/overrun error (FRUN). Bit[10] – Data starvation-by-host timeout (HTO) /Volt_switch_int. Bit[9] – Data read timeout (DRTO). Bit[8] – Response timeout (RTO). Bit[7] – Data CRC error (DCRC). Bit[6] – Response CRC error (RCRC). Bit[5] – Receive FIFO data request (RXDR). Bit[4] – Transmit FIFO data request (TXDR). Bit[3] – Data transfer over (DTO). Bit[2] – Command done (CD). Bit[1] – Response error (RE). Bit[0] – Card detect (CD).
	28H	CMDARG	RW	[31:0]		1'h0	Value indicates command argument to be passed to card.
	2CH	CMD	RW	[31]	start_cmd	1'h0	Start command. Once command is taken by CIU, bit is cleared. When bit is set, host should not attempt to write to any command registers. If write is attempted, hardware lock error is set in raw interrupt register. Once command is sent and response is received from SD_MMC_CEATA cards, Command Done bit is set in raw interrupt register.
				[30]	Reserved		
				[29]	use_hold_reg	1'h1	Use Hold Register. 0: CMD and DATA sent to card bypassing HOLD Register. 1: CMD and DATA sent to card through the HOLD Register.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[28]	volt_switch	1'h0	Voltage switch bit. 0: No voltage switching. 1: Voltage switching enabled; must be set for CMD11 only.
				[27]	boot_mode	1'h0	Boot Mode. 0: Mandatory Boot operation. 1: Alternate Boot operation.
				[26]	disable_boot	1'h0	Disable Boot. When software sets this bit along with start_cmd, CIU terminates the boot operation. Do NOT set disable_boot and enable_boot together.
				[25]	expect_boot_ack	1'h0	Expect Boot Acknowledge. When Software sets this bit along with enable_boot, CIU expects a boot acknowledge start pattern of 0-1-0 from the selected card.
				[24]	enable_boot	1'h0	Enable Boot. This bit should be set only for mandatory boot mode. When Software sets this bit along with start_cmd, CIU starts the boot sequence for the corresponding card by asserting the CMD line low. Do NOT set disable_boot and enable_boot together.
				[23]	ccs_expected	1'h0	0: Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from device. 1: Interrupts are enabled in CE-ATA device (nIEN = 0), and RW_BLK command expects command completion signal from CE-ATA device. If the command expects Command Completion Signal (CCS) from the CE-ATA device, the software should set this control bit. The mobile_storage sets Data Transfer Over (DTO) bit in RINTSTS register and generates interrupt to host if Data Transfer Over interrupt is not masked.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[22]	read_ceata_device	1'h0	0: Host is not performing read access (RW_REG or RW_BLK) towards CE-ATA device. 1: Host is performing read access (RW_REG or RW_BLK) towards CE-ATA device. Software should set this bit to indicate that CE-ATA device is being accessed for read transfer. This bit is used to disable read data timeout indication while performing CE-ATA read transfers. Maximum value of I/O transmission delay can be no less than 10 seconds. The mobile_storage should not indicate read data timeout while waiting for data from CE-ATA device.
				[21]	update_clock_registers_only	1'h0	0: Normal command sequence. 1: Do not send commands, just update clock register value into card clock domain. Following register values transferred into card clock domain: CLKDIV, CLRSRC, CLKENA. Changes card clocks (change frequency, truncate off or on, and set low-frequency mode); provided in order to change clock frequency or stop clock without having to send command to cards. During normal command sequence, when update_clock_registers_only = 0, following control registers are transferred from BIU to CIU: CMD, CMDARG, TMOUT, CTYPE, BLKSIZ, BYTCNT. CIU uses new register values for new command sequence to card(s). When bit is set, there are no Command Done interrupts because no command is sent to SD_MMC_CEATA cards.
				[20:16]	card_number	1'h0	Card number in use. Represents physical slot number of card being accessed. **Note:** Do not change the default value.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15]	send_initialization	1'h0	0: Do not send initialization sequence (80 clocks of 1) before sending this command. 1: Send initialization sequence before sending this command. After power on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending first command to card so that controller will initialize clocks before sending command to card. This bit should not be set for either of the boot modes (alternate or mandatory).
				[14]	stop_abort_cmd	1'h0	0: Neither stop nor abort command to stop current data transfer in progress. If abort is sent to function-number currently selected or not in data-transfer mode, then bit should be set to 0. 1: Stop or abort command intended to stop current data transfer in progress. When open-ended or predefined data transfer is in progress, and host issues stop or abort command to stop data transfer, bit should be set so that command/data state-machines of CIU can return correctly to idle state. This is also applicable for Boot mode transfers. To Abort boot mode, this bit should be set along with CMD[26] = disable_boot.
				[13]	wait_prvdata_complete	1'h0	0: Send command at once, even if previous data transfer has not completed. 1: Wait for previous data transfer completion before sending command. The wait_prvdata_complete = 0 option typically used to query status of card during data transfer or to stop current data transfer; card_number should be same as in previous command.

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	send_auto_stop	1'h0	0: No stop command sent at end of data transfer. 1: Send stop command at end of data transfer. When set, mobile_storage sends stop command to SD_MMC_CEATA cards at end of data transfer. Determine: - When send_auto_stop bit should be set, since some data transfers do not need explicit stop commands. - Open-ended transfers that software should explicitly send to stop command. Additionally, when “resume” is sent to resume – suspended memory access of SD-Combo card – bit should be set correctly if suspended data transfer needs send_auto_stop. Don't care if no data expected from card.
				[11]	transfer_mode	1'h0	0: Block data transfer command. 1: Stream data transfer command. Don’t care if no data expected.
				[10]	read/write	1'h0	0: Read from card. 1: Write to card. Don’t care if no data expected from card.
				[9]	data_expected	1'h0	0: No data transfer expected (read/write). 1: Data transfer expected (read/write).
				[8]	check_response_crc	1'h0	0: Do not check response CRC. 1: Check response CRC. Some of command responses do not return valid CRC bits. Software should disable CRC checks for those commands in order to disable CRC checking by controller.
				[7]	response_ length	1'h0	0: Short response expected from card. 1: Long response expected from card.
				[6]	response_expect	1'h0	0: No response expected from card. 1: Response expected from card.
				[5:0]	cmd_index	6'h0	Command index.

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BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
30H	RESP0	RO	[31:0]	response 0	32'h0	Bit[31:0] of response.
34H	RESP1	RO	[31:0]	response 1	32'h0	Register represents bit[63:32] of long response. When CIU sends auto-stop command, then response is saved in register. Response for previous command sent by host is still preserved in Response 0 register. Additional auto-stop issued only for data transfer commands, and response type is always “short” for them.
38H	RESP2	RO	[31:0]	response 2	32'h0	Bit[95:64] of long response.
3CH	RESP3	RO	[31:0]	response 3	32'h0	Bit[127:96] of long response.
40H	MINTSTS	RO	[31:17]	Reserved		
			[16]	sdio_interrupt	1'h0	Interrupt from SDIO card. This bit is for Card[0]. SDIO interrupt for card enabled only if corresponding sdio_int_mask bit is set in Interrupt mask register (mask bit 1 enables interrupt; 0 masks interrupt). 0: No SDIO interrupt from card. 1: SDIO interrupt from card.
			[15:0]	int_status	16'h0	Interrupt enabled only if corresponding bit in interrupt mask register is set. Bit[15] – End-bit error (read)/Write no CRC (EBE). Bit[14] – Auto command done (ACD). Bit[13] – Start Bit Error(SBE)/Busy Clear Interrupt (BCI). Bit[12] – Hardware locked write error (HLE). Bit[11] – FIFO underrun/overrun error (FRUN). Bit[10] – Data starvation-by-host timeout (HTO) /Volt_switch_int. Bit[9] – Data read timeout (DRTO). Bit[8] – Response timeout (RTO). Bit[7] – Data CRC error (DCRC). Bit[6] – Response CRC error (RCRC). Bit[5] – Receive FIFO data request (RXDR). Bit[4] – Transmit FIFO data request (TXDR). Bit[3] – Data transfer over (DTO). Bit[2] – Command done (CD). Bit[1] – Response error (RE). Bit[0] – Card detect (CD).

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BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
44H	RINTSTS	RW	[31:17]	Reserved		
			[16]		1'h0	Interrupt from SDIO card. This bit is for Card[0]. Writes to this bit clear it. Value of 1 clears bit and 0 leaves bit intact. 0: No SDIO interrupt from card. 1: SDIO interrupt from card. This bit is logged regardless of interrupt mask status.
			[15:0]		16'h0	Writes to bits clear status bit. Value of 1 clears status bit, and value of 0 leaves bit intact. Bits are logged regardless of interrupt mask status. Bit[15] – End-bit error (read)/Write no CRC (EBE). Bit[14] – Auto command done (ACD). Bit[13] – Start Bit Error(SBE)/Busy Clear Interrupt (BCI). Bit[12] – Hardware locked write error (HLE). Bit[11] – FIFO underrun/overrun error (FRUN). Bit[10] – Data starvation-by-host timeout (HTO) /Volt_switch_int. Bit[9] – Data read timeout (DRTO). Bit[8] – Response timeout (RTO). Bit[7] – Data CRC error (DCRC). Bit[6] – Response CRC error (RCRC). Bit[5] – Receive FIFO data request (RXDR). Bit[4] – Transmit FIFO data request (TXDR). Bit[3] – Data transfer over (DTO). Bit[2] – Command done (CD). Bit[1] – Response error (RE). Bit[0] – Card detect (CD).
48H	STATUS	RO	[31]	dma_req	1'h0	DMA request signal state; either h_dma_req or ge_dma_req, depending on H-DMA or Generic-DMA selection.
			[30]	dma_ack	1'h0	DMA acknowledge signal state; either h_dma_ack or ge_dma_ack, depending on H-DMA or Generic-DMA selection.
			[29:17]	fifo_count	13'h0	FIFO count – Number of filled locations in FIFO.
			[16:11]	response_index	6'h0	Index of previous response, including any auto-stop sent by core.
			[10]	data_state_mc_busy	1'h1	Data transmit or receive state-machine is busy.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[9]	data_busy	1'h1 or 1'h0; depends on cdata_in.	Inverted version of raw selected card_data[0] 0: Card data not busy. 1: Card data busy.
				[8]	data_3_status	1'h1 or 1'h0; depends on cdata_in.	Raw selected card_data[3]; checks whether card is present. 0: Card not present. 1: Card present.
				[7:4]	command_fsm_states	4'h0	Command FSM states: Bit[0] – Idle Bit[1] – Send init sequence Bit[2] – Tx cmd start bit Bit[3] – Tx cmd tx bit Bit[4] – Tx cmd index + arg Bit[5] – Tx cmd crc7 Bit[6] – Tx cmd end bit Bit[7] – Rx resp start bit Bit[8] – Rx resp IRQ response Bit[9] – Rx resp tx bit Bit[10] – Rx resp cmd idx Bit[11] – Rx resp data Bit[12] – Rx resp crc7 Bit[13] – Rx resp end bit Bit[14] – Cmd path wait NCC Bit[15] – Wait; CMD-to-response turnaround **Note:** The command FSM state is represented using 19 bits. The STATUS Register(7:4) has 4 bits to represent the command FSM states. Using these 4 bits, only 16 states can be represented. Thus three states cannot be represented in the STATUS(7:4) register. The three states that are not represented in the STATUS Register(7:4) are: - Bit[16] – Wait for CCS. - Bit[17] – Send CCSD. - Bit[18] – Boot Mode. Due to this, while command FSM is in Wait for CCS state or Send CCSD or Boot Mode, the Status register indicates status as 0 for the bit field [7:4].
				[3]	fifo_full	1'h0	FIFO is full status.
				[2]	fifo_empty	1'h1	FIFO is empty status.
				[1]	fifo_tx_watermark	1'h1	FIFO reached Transmit watermark level; not qualified with data transfer.
				[0]	fifo_rx_watermark	1'h0	FIFO reached Receive watermark level; not qualified with data transfer.
	4CH	FIFOTH	RW	[31]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[30:28]	DW_DMA_Mutiple_ Transaction_Size	3'h000	Burst size of multiple transaction; should be programmed same as H-DMA controller multiple-transaction-size SRC/DEST_MSIZE: 000: 1 transfers; 001: 4; 010: 8; 011: 16; 100: 32; 101: 64; 110: 128; 111: 256 The units for transfers is the H_DATA_WIDTH parameter. A single transfer (h_dma_single assertion in case of Non H DMA interface) would be signaled based on this value. Value should be sub-multiple of (RX_WMark+1)*(F_DATA_WIDTH/H_DATA_WIDTH) and (FIFO_DEPTH - TX_WMark)* (F_DATA_WIDTH/H_DATA_WIDTH) For example, if FIFO_DEPTH = 16, FDATA_WIDTH == H_DATA_WIDTH Allowed combinations for MSize and TX_WMark are: - MSize = 1, TX_WMARK = 1-15 - MSize = 4, TX_WMark = 8 - MSize = 4, TX_WMark = 4 - MSize = 4, TX_WMark = 12 - MSize = 8, TX_WMark = 8 - MSize = 8, TX_WMark = 4 Allowed combinations for MSize and RX_WMark are: - MSize = 1, RX_WMARK = 0-14 - MSize = 4, RX_WMark = 3 - MSize = 4, RX_WMark = 7 - MSize = 4, RX_WMark = 11 - MSize = 8, RX_WMark = 7 Recommended: MSize = 8, TX_WMark = 8, RX_WMark = 7

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27:16]	RX_Wmark	12'hFF	FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits – 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: RX_WMark <= FIFO_DEPTH-2 Recommended: (FIFO_DEPTH/2) - 1; (means greater than (FIFO_DEPTH/2) - 1) **Note:** In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS timeout.
				[15:12]	Reserved		

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11:0]	TX_Wmark	1'h0	FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits – 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: TX_WMark >= 1 Recommended: FIFO_DEPTH/2; (means less than or equal to FIFO_DEPTH/2)
	50H	CDETECT	RO	[31:1]	Reserved		
				[0]	card_detect_n		Value on SD0_DET_N; read-only bit. This bit is applicable only for SD0. 0 represents presence of card.
	54H	WRTPRT	RO	[31:1]			
				[0]	write_protect		Value on SD0_WPROT. This bit is applicable only for SD0. 1 represents write protection.
	58H	GPIO	RW	[31:24]	Reserved		
				[23:8]	gpo	16'h0	Read/Write bits, but not used. No loading.
				[7:0]	Reserved		

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BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
5CH	TCBCNT	RO	[31:0]	trans_card_byte_count	32'h0	Number of bytes transferred by CIU unit to card. In 32-bit AMBA data-bus-width mode, register should be accessed in full to avoid read-coherency problems. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied. Both TCBCNT and TBBCNT share same coherency register. When AREA_OPTIMIZED parameter is 1, register should be read only after data transfer completes; during data transfer, register returns 0.
60H	TBBCNT	RO	[31:0]	trans_fifo_byte_count	32'h0	Number of bytes transferred between Host/DMA memory and BIU FIFO. In 32-bit AMBA data-bus-width mode, register should be accessed in full to avoid read-coherency problems. In 16-bit AMBA data-bus-width mode, internal 16-bit coherency register is implemented. User should first read lower 16 bits and then higher 16 bits. When reading lower 16 bits, higher 16 bits of counter are stored in temporary register. When higher 16 bits are read, data from temporary register is supplied. Both TCBCNT and TBBCNT share same coherency register.
64H	DEBNCE	RW	[31:24]	Reserved		
			[23:0]	debounce_count	24'hff_ffff	Number of host clocks (clk) used by debounce filter logic; typical debounce time is 5-25 ms.
68H	USRID	RW	[31:0]	USRID	32'h7967797	User identification register; value set by user. Default reset value can be picked by user while configuring core before synthesis. Can also be used as scratch pad register by user.
6CH	VERID	RO	[31:0]	VERID	32'h5342_290a	Version identification register; register value is hard-wired. Can be read by firmware to support different versions of core.

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	70H	HCON	RO	[31:0]	Configuration Dependent	32'hc44c81	Hardware configurations selected by user before synthesizing core. Register values can be used to develop configuration-independent software drivers. Bit[0] – CARD_TYPE 1: SD_MMC Bits[5:1] = 0 Bit[6] – H_BUS_TYPE 0: APB Bits[9:7] – H_DATA_WIDTH 001: 32 bits Bits[15:10] – H_ADDR_WIDTH Bits[17:16] – DMA_INTERFACE 00: None 19: 20 bits Bits[20:18] – GE_DMA_DATA_WIDTH 001: 32 bits Bit[21]: FIFO_RAM_INSIDE 0: Outside Bit[22] – IMPLEMENT_HOLD_REG 1: Hold register Bit[23] – SET_CLK_FALSE_PATH 1: False path set Bits[25:24] = 0 Bit[26] – AREA_OPTIMIZED 0: No area optimization For 64-bit Address Configuration only Bit[27] – ADDR_CONFIG 0: 32-bit addressing supported For 32-bit Address Configuration only: Bits[31:27] – Reserved (0) For FIFO_DEPTH parameter, power-on value of RX_WMark value of FIFO Threshold Watermark Register represents FIFO_DEPTH - 1.
	74H	UHS_REG	RW	[31:17]	Reserved		

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[16]	DDR_REG	1'h0	DDR mode. These bits indicate DDR mode of operation to the core for the data transfer. 0: Non-DDR mode 1: DDR mode Only set to 0 for card number 0.
				[15:1]	Reserved		
				[0]	VOLT_REG	1'h0	High Voltage mode. Determines the voltage fed to the buffers by an external voltage regulator. 0: Buffers supplied with 3.3V Vdd 1: Buffers supplied with 1.8V Vdd These bits function as the output of the host controller and are fed to an external voltage regulator. The voltage regulator must switch the voltage of the buffers of a particular card to either 3.3V or 1.8V, depending on the value programmed in the register. VOLT_REG[0] should be set to 1’b1 for card number 0 in order to make it operate for 1.8V.
	78H	RST_n	RW	[31:1]	Reserved		
				[0]	CARD_RESET	1'h1	Hardware reset. 1: Active mode 0: Reset These bits cause the cards to enter pre-idle state, which requires them to be re-initialized. This bit should be set to 1’b0 to reset card number 0.
	100H	CardThrCtl	RW	[31:28]	Reserved		
				[27:16]	CardThreshold	12'h0	Card Threshold size; N depends on the FIFO size: N = 26, FIFO Size = 256 Note: This register is applicable when CardWrThrEn is set to 1 or CardRdThrEn is set to 1.
				[15:3]	Reserved		

eMMC Host	BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	CardWrThrEn	1'h0	Card Write Threshold Enable. This bit is not applicable because HS400 mode is not supported.
				[1]	BsyClrIntEn	1'h0	Busy Clear Interrupt generation: 1'b0: Busy Clear Interrupt disabled 1'b1: Busy Clear Interrupt enabled **Note:** The application can disable this feature if it does not want to wait for a Busy Clear Interrupt. For example, in a multi-card scenario, the application can switch to the other card without waiting for a busy to be completed. In such cases, the application can use the polling method to determine the status of busy. By default this feature is disabled and backward-compatible to the legacy drivers where polling is used.
				[0]	CardRd ThrEn	1'h0	Card Read Threshold Enable. 1'b0: Card Read Threshold disabled. 1'b1: Card Read Threshold enabled. Host Controller initiates Read. Transfer only if Card Threshold amount of space is available in receive FIFO.
	104H	Back_end_power	RW	[31:1]			
				[0]	Back End Power	1'h0	Back end power. 1'b0: Off; Reset. 1'b1: Back-end Power supplied to card application; one pin per card.
	108H	UHS_REG_EXT	RW	[31:30]	EXT_CLK_MUX_CTRL	2'h0	Read/Write bits, but not used. No loading.
				[29:23]	CLK_DRV_PHASE_CTRL	7'h0	Read/Write bits, but not used. No loading.
				[22:16]	CLK_SMPL_PHASE_CTRL	7'h0	Read/Write bits, but not used. No loading.
				[15:1]	Reserved		

eMMC Host

BASE_ADDR: 0xA501_0xxx, 0xA501_1xxx, 0xA501_2xxx

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[0]	MMC_VOLT_REG	1'h0	1.2V is not supported. MMC_VOLT_REG bits; must be read in combination with UHS_VOLT_REG to decode output selected voltage. The biu_volt_reg_1_2[NUM_CARD_BUS-1:0] signal decodes the voltage combination selected for the I/O voltage logic. Host controllers that support only SD standard or standard versions before eMMC4.41 do not program MMC_VOLT_REG. Only host controllers that support Two versions—3.3,1.8 V—can program MMC_VOLT_REG and connect biu_volt_reg_1_2. For output voltages corresponding to I/O voltage logic, refer to the table below. I/O Voltage Logic for UHS_REG_EXT Register: VOLT_REG MMC_VOLT_REG biu_volt_reg biu_volt_reg_1_2 Output Decoded 0 0 0 0 3.3V 0 1 0 1 3.3V 1 0 1 0 1.8V
10CH	EMMC_DDR_REG	RW	[31]	hs400_mode	1'h0	HS400 Mode enable. 1: Enable 0: Disable HS400 mode is not supported. This bit should be set 0.
			[30:16]	Reserved		
			[15:0]		16'h0	Control for start bit detection mechanism inside mobile_storage based on duration of start bit; each bit refers to one slot. Read/Write bits, but not used.
110H	ENABLE_SHIFT	RW	[31:2]	Reserved		
			[1:0]	Enable_shift	2'h0	Control for the amount of phase shift provided on the default enables in the design. The bits control card0/slot0 and indicate the following. 00: Default phase shift. 01: Enables shifted to next immediate positive edge. 10: Enables shifted to next immediate negative edge. 11: Reserved