X3M Register Reference Manual
GPIO/PIN Group

Revision History

Revision	Date	Description
1.0	July-03-2020	Initial Release
1.1	November-11-2020	• Corrected the register name from QSPI_MOSI_IO1 to QSPI_MISO_IO1. • Corrected the bit field name from QSPI_MOSI_IO1_XX to QSPI_MISO_IO1_XX. • Corrected the register name from QSPI_MOSI_IO2 to QSPI_WP_IO2. • Corrected the bit field name from QSPI_MOSI_IO2_XX to QSPI_WP_IO2_XX. • Corrected the register name from QSPI_MOSI_IO3 to QSPI_HOLD_IO3. • Corrected the bit field name from QSPI_MOSI_IO3_XX to QSPI_HOLD_IO3_XX.

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	008H	GPIO0_OUTPUT_CTRL	RW	[31:16]	GPIO0_DIR	16'h0	GPIO0 pin direction. 0: Input. 1: Output.
				[15:0]	GPIO0_OUTPUT_VALUE	16'h0	GPIO0 output register. 0: Output 0. 1: Output 1.
	00CH	GPIO0_INPUT_VALUE	RO	[31:16]	Reserved		
				[15:0]	GPIO0_INPUT_VALUE	16'h0	GPIO0 pin value. 0: Input 0. 1: Input 1.
	018H	GPIO1_OUTPUT_CTRL	RW	[31:16]	GPIO1_DIR	16'h0	GPIO1 pin direction. 0: Input. 1: Output.
				[15:0]	GPIO1_OUTPUT_VALUE	16'h0	GPIO1 output register. 0: Output 0. 1: Output 1.
	01CH	GPIO1_INPUT_VALUE	RO	[31:16]	Reserved		
				[15:0]	GPIO1_INPUT_VALUE	16'h0	GPIO1 pin value. 0: Input 0. 1: Input 1.
	028H	GPIO2_OUTPUT_CTRL	RW	[31:16]	GPIO2_DIR	16'h0	GPIO2 pin direction. 0: Input. 1: Output.
				[15:0]	GPIO2_OUTPUT_VALUE	16'h0	GPIO2 output register. 0: Output 0. 1: Output 1.
	02CH	GPIO2_INPUT_VALU	RO	[31:16]	Reserved		

GPIO

BASE_ADDR:0xA600_3000						
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	E		[15:0]	GPIO2_INPUT_VALUE	16'h0	GPIO2 pin value. 0: Input 0. 1: Input 1.
038H	GPIO3_OUTPUT_CTRL	RW	[31:16]	GPIO3_DIR	16'h0	GPIO3 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO3_OUTPUT_VALUE	16'h0	GPIO3 output register. 0: Output 0. 1: Output 1.
03CH	GPIO3_INPUT_VALUE	RO	[31:16]	Reserved		
			[15:0]	GPIO3_INPUT_VALUE	16'h0	GPIO3 pin value. 0: Input 0. 1: Input 1.
048H	GPIO4_OUTPUT_CTRL	RW	[31:16]	GPIO4_DIR	16'h0	GPIO4 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO4_OUTPUT_VALUE	16'h0	GPIO4 output register. 0: Output 0. 1: Output 1.
04CH	GPIO4_INPUT_VALUE	RO	[31:16]	Reserved		
			[15:0]	GPIO4_INPUT_VALUE	16'h0	GPIO4 pin value. 0: Input 0. 1: Input 1.
058H	GPIO5_OUTPUT_CTRL	RW	[31:16]	GPIO5_DIR	16'h0	GPIO5 pin direction. 0: Input. 1: Output.
			[15:0]	GPIO5_OUTPUT_VALUE	16'h0	GPIO5 output register. 0: Output 0. 1: Output 1.
05CH	GPIO5_INPUT_VALU	RO	[31:16]	Reserved		

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
		E		[15:0]	GPIO5_INPUT_VALUE	16'h0	GPIO5 pin value. 0: Input 0. 1: Input 1.
	068H	GPIO6_OUTPUT_CTRL	RW	[31:16]	GPIO6_DIR	16'h0	GPIO6 pin direction. 0: Input. 1: Output.
				[15:0]	GPIO6_OUTPUT_VALUE	16'h0	GPIO6 output register. 0: Output 0. 1: Output 1.
	06CH	GPIO6_INPUT_VALUE	RO	[31:16]	Reserved		
				[15:0]	GPIO6_INPUT_VALUE	16'h0	GPIO6 pin value. 0: Input 0. 1: Input 1.
	078H	GPIO7_OUTPUT_CTRL	RW	[31:25]	Reserved		
				[24:16]	GPIO7_DIR	9'h0	GPIO7 pin direction. 0: Input. 1: Output.
				[8:0]	GPIO7_OUTPUT_VALUE	9'h0	GPIO7 output register. 0: Output 0. 1: Output 1.
	07CH	GPIO7_INPUT_VALUE	RO	[31:9]	Reserved		
				[8:0]	GPIO7_INPUT_VALUE	9'h0	GPIO7 pin value. 0: Input 0. 1: Input 1.
	100H	GPIO_INT_MUX_SEL	RW	[31]	Reserved		

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[30:24]	GPIO_INT3_MUX_SEL	7'h0	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 3. 7'd00: GPIO0. 7'd01: GPIO1. ... 7'd120: GPIO120. 7'd121~7'd127: 1'b0.
				[23]	Reserved		
				[22:16]	GPIO_INT2_MUX_SEL	7'h0	GPIO interrupt 2 mux selection. The specific GPIO that will generate interrupt 2. 7'd00: GPIO0. 7'd01: GPIO1. ... 7'd120: GPIO120. 7'd121~7'd127: 1'b0.
				[15]	Reserved		
				[14:8]	GPIO_INT1_MUX_SEL	7'h0	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 1. 7'd00: GPIO0. 7'd01: GPIO1. ... 7'd120: GPIO120. 7'd121~7'd127: 1'b0.
				[7]	Reserved		
				[6:0]	GPIO_INT0_MUX_SEL	7'h0	GPIO interrupt 3 mux selection. The specific GPIO that will generate interrupt 0. 7'd00: GPIO0. 7'd01: GPIO1. ... 7'd120: GPIO120. 7'd121~7'd127: 1'b0.
	104H	GPIO_INTE	RW	[31:4]	Reserved		

GPIO

BASE_ADDR:0xA600_3000						
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[3:0]	GPIO_INTE	4'h0	GPIO interrupt enable. The specific bit that enables interrupt generation for corresponding input GPIO. Interrupt can be enabled only when GPIO_DIR is configured to input.
108H	GPIO_INT_POS	RW	[31:4]	Reserved		
			[3:0]	GPIO_INT_POS	4'hf	GPIO positive edge interrupt flag. The specific bit indicates the corresponding bit has positive/negtive edge interrupt. 0: Disabled. 1: Enabled.
10CH	GPIO_INT_NEG	RW	[31:4]	Reserved		
			[3:0]	GPIO_INT_NEG	4'hf	GPIO negtive edge interrupt flag. The specific bit indicates the corresponding bit has positive/negtive edge interrupt. 0: Disabled. 1: Enabled.
110H	GPIO_INT_WIDTH	RW	[31:0]	GPIO_INT_WIDTH	32'h1	Valid input holding width for GPIO interrupt generation, the holding time is calculated as 2 * (GPIO_INT_WIDTH + 1) * padc_mclk Period.
120H	GPIO_INTMASK	RO	[31:4]	Reserved		
			[3:0]	GPIO_INTMASK	4'h0	0: Unmasked. 1: Masked.
124H	GPIO_SETMASK	WO	[31:4]	Reserved		
			[3:0]	GPIO_SETMASK	4'h0	Writing setmask[i] = 1 means mask bit i. 0: Unmasked. 1: Masked.
128H	GPIO_UNMASK	WO	[31:4]	Reserved		
			[3:0]	GPIO_UNMASK	4'h0	Writing unmask[i] = 1 means unmask bit i. 0: Unmasked. 1: Unmasked.
12CH	GPIO_SRCPND	W1C	[31:4]	Reserved		

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3:0]	GPIO_SRCPND	4'h0	For read: 0: Interrupt source inactive. 1: Interrupt source active. For write: 0: No effect. 1: Clears corresponding source.
	130H	IRQOUT_CTRL	RW	[31:21]	Reserved		
				[20]	IRQOUT_TRIG	1'b0	X2A_IRQOUT_N edge type interrupt trigger. SW should configure IRQOUT_POL before IRQOUT_TRIG. 1'b0: No effect. 1'b1: Triggers interrupt.
				[19:17]	Reserved		
				[16]	IRQOUT_POL	1'b0	X2A_IRQOUT_N edge type interrupt polority: 1'b0: Low active. 1'b1: High active.
				[15:0]	IRQOUT_PERIOD	16'h20	X2A_IRQOUT_N edge type interrupt pulse width. The width is IRQ_PERIOD 24MHz cycles.
	140H	STRAP_PIN	RO	[31:17]	Reserved		
				[16]	SW_STRAP[16]	1'b0	Reserved.
				[15]	SW_STRAP[15]	1'b0	Reserved.
				[14]	SW_STRAP[14]	1'b0	Reserved.
				[13]	SW_STRAP[13]	1'b0	0: SPI NAND has 1 plane, you do not need to set plane selection for 03H command. 1: SPI NAND has 2 planes, you need to set plane selection for 03H command.
				[12]	SW_STRAP[12]	1'b0	Whether dummy byte is inserted when SPI NAND reading ID: 0: Inserts dummy byte when SPI NAND flash reading device ID (9FH command). 1: No dummy byte inserted when SPI NAND flash reading device ID (9FH command).

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	SW_STRAP[11]	1'b0	Watchdog disable: 0: Enables WatchDog to protect clock switch. Triggers system reset if system hangs in the process of clock switch. 1: Disables WatchDog. Enable watchdog before clock switch to PLL, and disable watchdog after the success of clock switch.
				[10]	SW_STRAP[10]	1'b0	SPI flash reset is only valid if 2NDBOOT=SPI FLASH. 0: No operation. 1: Triggers a flash reset command before reading NAND/NOR FLASH.
				[9]	SW_STRAP[9]	1'b0	When Warm boot: 0: Load SPL from SRAM. 1: Load SPL from flash/emmc/uart/bifspi/usb.
				[8]	SW_STRAP[8]	1'b0	Reserved.
				[7]	SW_STRAP[7]	1'b0	UART baud rate: 0: 921600 bps. 1: 115200 bps.
				[6:5]	SW_STRAP[6:5]	2'b0	Fast boot selection, CPU/BUS frequency selection: 00: cpu_clk=1.2G, ace_aclk=sys_noc_aclk=600M, sys_ap_aclk=400M, sys_pclk=cx_dbgclk=300M. 01: cpu_clk=600M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M, sys_pclk=cx_dbgclk=150M. 10: cpu_clk=300M, ace_aclk=sys_noc_aclk=300M, sys_ap_aclk=300M, sys_pclk=cx_dbgclk=150M. 11: No clock switch to high freq, cpu_clk=24M, ace_aclk=sys_noc_aclk=12M, sys_pclk=4.8M, sys_ap_aclk=cx_dbgclk=8M.

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	SW_STRAP[4]	1'b0	Device mode. When 2NDBOOT=EMMC: 0: DRV CLK phase shift 180°, falling edge launch and rising edge capture. 1: DRV CLK no phase shift, rising edge launch and rising edge capture. When 2NDBOOT_SEL=SPI NAND FLASH: 0: 2KB Page Size. 1: 4KB Page Size. When 2NDBOOT_SEL=SPI NOR FLASH: 0: 32-bit addr mode. 1: 24-bit addr mode.
				[3:1]	SW_STRAP[3:1]	3'b0	000: 2NDBOOT from EMMC 001: 2NDBOOT from SPI FLASH(SPI NAND FLASH) 010: 2NDBOOT from AP BIFSPI 011: 2NDBOOT from UART XMODEM 100: 2NDBOOT from USB, Normal boot 101: 2NDBOOT from SPI FLASH(SPI NOR FLASH) 110: 2NDBOOT from USB with program 111: RESERVED (2NDBOOT from UART) **Note:** 100 or 110 (USB boot or USB program) will detect USB ID pin (GPIO[65], SD0_WPROT) 0: The chip is playing as a USB host, perform USB host operation 1: The chip is playing as a USB device, perform UART boot
				[0]	SW_STRAP[0]	1'b0	Reserved.
	170H	SD_MODE_CTRL	RW	[31:4]	Reserved		
				[3]	SD2_MODE_SEL	1'b0	SD2 mode selector 0: 3.0V mode 1: 1.8V mode
				[2]	SD1_MODE_SEL	1'b0	SD1 mode selector 0: 3.0V mode 1: 1.8V mode

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	SD0_MODE_SEL_DOMAIN1	1'b0	SD0 mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[0]	SD0_MODE_SEL_DOMAIN0	1'b0	SD0 mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
	174H	IO_MODE_CTRL	RW	[31:12]	Reserved		
				[11]	RGMII_MODE_SEL_DOMAIN1	1'b0	RGMII I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[10]	RGMII_MODE_SEL_DOMAIN0	1'b0	RGMII I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
				[9]	I2C2_MODE_SEL	1'b0	I2C2/I2C3 I/O mode selector 0: 3.0V mode 1: 1.8V mode
				[8]	I2C0_MODE_SEL	1'b0	I2C0/Sensor2_MCLK/Sensor3_MCLK I/O mode selector 0: 3.0V mode 1: 1.8V mode
				[7]	Reserved		
				[6]	BT1120_MODE_SEL_DOMAIN2	1'b0	BT1120 I/O mode selector in SD domain 2 0: 3.0V mode 1: 1.8V mode
				[5]	BT1120_MODE_SEL_DOMAIN1	1'b0	BT1120 I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[4]	BT1120_MODE_SEL_DOMAIN0	1'b0	BT1120 I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode

GPIO	BASE_ADDR:0xA600_3000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	BIFSD_MODE_SEL_DOMAIN1	1'b0	BIFSD I/O mode selector in SD domain 1 0: 3.0V mode 1: 1.8V mode
				[2]	BIFSD_MODE_SEL_DOMAIN0	1'b0	BIFSD I/O mode selector in SD domain 0 0: 3.0V mode 1: 1.8V mode
				[1]	BIFSPI_MODE_SEL	1'b0	BIFSPI I/O mode selector 0: 3.0V mode 1: 1.8V mode
				[0]	JTG_MODE_SEL	1'b0	JTAG I/O mode selector 0: 3.0V mode 1: 1.8V mode
	180H	GPIO_TS_SEL	RW	[31:7]	Reserved		
				[6:0]	GPIO_TS_SEL	7'h0	GPIO mux selection for timestamp trigger source The specific which GPIO will be sent to vio subsys 7'd00: GPIO0 7'd01: GPIO1 ... 7'd120: GPIO120 7'd121~7'd127: 1'b0
	200H	DUMMY0	RW	[31:0]	DUMMY0	32'h0	Dummy register 0.
	204H	DUMMY1	RW	[31:0]	DUMMY1	32'hFFFFFFFF	Dummy register 1.

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SYSTEM	0000H	EN_VDD_CORE	RW				PIN configuration register	GPIO0[0]
				[31:9]	Reserved			
				[8]	EN_VDD_CORE_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	EN_VDD_CORE_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	EN_VDD_CORE_PE	1'h0	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	EN_VDD_CORE_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EN_VDD_CORE_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0004H	EN_VDD_CNN0	RW				PIN configuration register	GPIO0[1]
				[31:9]	Reserved			
				[8]	EN_VDD_CNN0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	EN_VDD_CNN0_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	EN_VDD_CNN0_PE	1'h0	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	EN_VDD_CNN0_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EN_VDD_CNN0_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0008H	EN_VDD_CNN1	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:9]	Reserved			GPIO0[2]
				[8]	EN_VDD_CNN1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	EN_VDD_CNN1_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	EN_VDD_CNN1_PE	1'h0	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	EN_VDD_CNN1_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EN_VDD_CNN1_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	000CH	JTG_TCK	RW				PIN configuration register	GPIO0[3]
				[31:10]	Reserved			
				[9]	JTG_TCK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TCK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TCK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	JTG_TCK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TCK_FS	2'h0	PIN function selection 00: Normal function 01: SPI1_SCLK 10: N/A 11: GPIO	
	0010H	JTG_TRSTN	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
JTAG				[31:10]	Reserved			GPIO0[4]
				[9]	JTG_TRSTN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TRSTN_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TRSTN_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	JTG_TRSTN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TRSTN_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: PWM0 11: GPIO	
	0014H	JTG_TMS	RW				PIN configuration register	
				[31:10]	Reserved			GPIO0[5]
				[9]	JTG_TMS_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TMS_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TMS_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	JTG_TMS_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TMS_FS	2'h0	PIN function selection 00: Normal function 01: SPI1_CSN 10: N/A 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
	0018H	JTG_TDI	RW				PIN configuration register	GPIO0[6]
				[31:10]	Reserved			
				[9]	JTG_TDI_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TDI_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TDI_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	JTG_TDI_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	JTG_TDI_FS	2'h0	PIN function selection 00: Normal function 01: SPI1_MOSI 10: N/A 11: GPIO	
	001CH	JTG_TDO	RW				PIN configuration register	GPIO0[7]
				[31:10]	Reserved			
				[9]	JTG_TDO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	JTG_TDO_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	JTG_TDO_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	JTG_TDO_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[1:0]	JTG_TDO_FS	2'h0	PIN function selection 00: Normal function 01: SPI1_MISO 10: N/A 11: GPIO	
I2C0	0020H	I2C0_SCL	RW				PIN configuration register	GPIO0[8]
				[31:10]	Reserved			
				[9]	I2C0_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C0_SCL_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C0_SCL_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	I2C0_SCL_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C0_SCL_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0024H	I2C0_SDA	RW				PIN configuration register	GPIO0[9]
				[31:10]	Reserved			
				[9]	I2C0_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C0_SDA_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C0_SDA_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	I2C0_SDA_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C0_SDA_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
I2C1	0028H	I2C1_SCL	RW				PIN configuration register	GPIO0[10]
				[31:9]	Reserved			
				[8]	I2C1_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2C1_SCL_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2C1_SCL_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2C1_SCL_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C1_SCL_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	002CH	I2C1_SDA	RW				PIN configuration register	GPIO0[11]
				[31:9]	Reserved			
				[8]	I2C1_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2C1_SDA_PU	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2C1_SDA_PD	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	I2C1_SDA_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C1_SDA_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
I2C2	0030H	I2C2_SCL	RW				PIN configuration register	GPIO0[12]
				[31:10]	Reserved			
				[9]	I2C2_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C2_SCL_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C2_SCL_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	I2C2_SCL_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C2_SCL_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_MOSI 10: PWM7 11: GPIO	
	0034H	I2C2_SDA	RW				PIN configuration register	GPIO0[13]
				[31:10]	Reserved			
				[9]	I2C2_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C2_SDA_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C2_SDA_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			

PIN Group	*PIN_REG BASE_ADDR: 0xA600_4000*							
	Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**	**GPIO**
				[5:2]	I2C2_SDA_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C2_SDA_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_MISO 10: PWM8 11: GPIO	
I2C3	0038H	I2C3_SCL	RW				PIN configuration register	**GPIO0[14]**
				[31:10]	Reserved			
				[9]	I2C3_SCL_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C3_SCL_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C3_SCL_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	I2C3_SCL_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C3_SCL_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_SCLK 10: N/A 11: GPIO	
	003CH	I2C3_SDA	RW				PIN configuration register	**GPIO0[15]**
				[31:10]	Reserved			
				[9]	I2C3_SDA_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	I2C3_SDA_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	I2C3_SDA_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	I2C3_SDA_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2C3_SDA_FS	2'h3	PIN function selection 00: Normal function 01: SPI2_CSN 10: N/A 11: GPIO	
	0040H	SPI0_CSN	RW				PIN configuration register	GPIO1[0]
				[31:9]	Reserved			
				[8]	SPI0_CSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SPI0_CSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SPI0_CSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	SPI0_CSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_CSN_FS	2'h3	PIN function selection 00: Normal function 01: I2C4_SDA 10: N/A 11: GPIO	
	0044H	SPI0_SCLK	RW				PIN configuration register	GPIO1[1]
				[31:9]	Reserved			
				[8]	SPI0_SCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SPI0_SCLK_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SPI0_SCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SPI0				[5:2]	SPI0_SCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_SCLK_FS	2'h3	PIN function selection 00: Normal function 01: I2C4_SCL 10: N/A 11: GPIO	
	0048H	SPI0_MOSI	RW				PIN configuration register	GPIO1[2]
				[31:9]	Reserved			
				[8]	SPI0_MOSI_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SPI0_MOSI_PS	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[6]	SPI0_MOSI_PE	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[5:2]	SPI0_MOSI_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_MOSI_FS	2'h3	PIN function selection 00: Normal function 01: I2C5_SDA 10: PWM5 11: GPIO	
	004CH	SPI0_MISO	RW				PIN configuration register	GPIO1[3]
				[31:9]	Reserved			
				[8]	SPI0_MISO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SPI0_MISO_PS	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[6]	SPI0_MISO_PE	1'h1	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	SPI0_MISO_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SPI0_MISO_FS	2'h3	PIN function selection 00: Normal function 01: I2C5_SCL 10: PWM6 11: GPIO	
	0050H	BIFSD_CLK	RW				PIN configuration register	GPIO1[4]
				[31:10]	Reserved			
				[9]	BIFSD_CLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_CLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_CLK_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: RGB_VSYNC 11: GPIO	
	0054H	BIFSD_CMD	RW				PIN configuration register	GPIO1[5]
				[31:10]	Reserved			
				[9]	BIFSD_CMD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	BIFSD_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_CMD_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: RGB_HSYNC 11: GPIO	
	0058H	BIFSD_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	**GPIO1[6]**
				[6]	Reserved			
				[5:2]	BIFSD_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA0_FS	2'h0	PIN function selection 00: Normal function 01: PWM1 10: RGB_DAT16 11: GPIO	
	005CH	BIFSD_DATA1	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA1_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
BIFSD				[7]	BIFSD_DATA1_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1[7]
				[6]	Reserved			
				[5:2]	BIFSD_DATA1_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA1_FS	2'h0	PIN function selection 00: Normal function 01: PWM2 10: RGB_DAT17 11: GPIO	
	0060H	BIFSD_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA2_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA2_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1[8]
				[6]	Reserved			
				[5:2]	BIFSD_DATA2_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA2_FS	2'h0	PIN function selection 00: Normal function 01: PWM3 10: RGB_DAT18 11: GPIO	
	0064H	BIFSD_DATA3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_DATA3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	BIFSD_DATA3_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	GPIO1[9]
				[7]	BIFSD_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA3_FS	2'h0	PIN function selection 00: Normal function 01: PWM4 10: RGB_DAT19 11: GPIO	
	0068H	BIFSD_RSTN	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSD_RSTN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_RSTN_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_RSTN_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO1[10]
				[6]	Reserved			
				[5:2]	BIFSD_RSTN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_RSTN_FS	2'h0	PIN function selection 00: Normal function 01: PPS_TRIG_IN 10: RGB_DE 11: GPIO	
	006CH	BIFSPI_CSN	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	BIFSPI_CSN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO1[11]
				[8]	BIFSPI_CSN_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_CSN_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSPI_CSN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_CSN_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0070H	BIFSPI_SCLK	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BIFSPI_SCLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_SCLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_SCLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO1[12]
				[6]	Reserved			
				[5:2]	BIFSPI_SCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_SCLK_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0074H	BIFSPI_MOSI	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
BIFSPI				[31:10]	Reserved			GPIO1[13]
				[9]	BIFSPI_MOSI_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_MOSI_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_MOSI_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSPI_MOSI_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_MOSI_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0078H	BIFSPI_MISO	RW				PIN configuration register	
				[31:10]	Reserved			GPIO1[14]
				[9]	BIFSPI_MISO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_MISO_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_MISO_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSPI_MISO_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_MISO_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
	007CH	BIFSPI_RSTN	RW				PIN configuration register	GPIO1[15]
				[31:10]	Reserved			
				[9]	BIFSPI_RSTN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSPI_RSTN_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSPI_RSTN_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSPI_RSTN_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSPI_RSTN_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0080H	QSPI_CSN	RW				PIN configuration register	GPIO2[0]
				[31:9]	Reserved			
				[8]	QSPI_CSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_CSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_CSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_CSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_CSN_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
QSPI	0084H	QSPI_SCLK	RW				PIN configuration register	GPIO2[1]
				[31:9]	Reserved			
				[8]	QSPI_SCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_SCLK_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_SCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_SCLK_DS	4'h2	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_SCLK_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0088H	QSPI_MOSI_IO0	RW				PIN configuration register	GPIO2[2]
				[31:9]	Reserved			
				[8]	QSPI_MOSI_IO0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_MOSI_IO0_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_MOSI_IO0_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_MOSI_IO0_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_MOSI_IO0_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	008CH	QSPI_MISO_IO1	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:9]	Reserved			GPIO2[3]
				[8]	QSPI_MISO_IO1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_MISO_IO1_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_MISO_IO1_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_MISO_IO1_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_MISO_IO1_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0090H	QSPI_WP_IO2	RW				PIN configuration register	GPIO2[4]
				[31:9]	Reserved			
				[8]	QSPI_WP_IO2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_WP_IO2_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_WP_IO2_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_WP_IO2_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_WP_IO2_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0094H	QSPI_HOLD_IO3	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	QSPI_HOLD_IO3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO2[5]
				[7]	QSPI_HOLD_IO3_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_HOLD_IO3_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_HOLD_IO3_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_HOLD_IO3_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0098H	EPHY_CLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	EPHY_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	EPHY_CLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	EPHY_CLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO2[6]
				[5:2]	EPHY_CLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	EPHY_CLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	009CH	MDCK	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	MDCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO2[7]
				[7]	MDCK_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	MDCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	MDCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	MDCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00A0H	MDIO	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	MDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	MDIO_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	MDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO2[8]
				[5:2]	MDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	MDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00A4H	RGMII_RX_CLK	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	RGMII_RX_CLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO2[9]
				[8]	RGMII_RX_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RX_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RX_CLK_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RX_CLK_FS	2'h3	PIN function selection 00: Normal function (RGMII_RX_CLK or RMII_REF_CLK_IN) 01: N/A 10: N/A 11: GPIO	
	00A8H	RGMII_RXD0	RW				PIN configuration register	GPIO2[10]
				[31:10]	Reserved			
				[9]	RGMII_RXD0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RXD0_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RXD0_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RXD0_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD0_FS	2'h3	PIN function selection 00: Normal function (RGMII_RXD0 or RMII_RXD0) 01: N/A 10: N/A 11: GPIO	
	00ACH	RGMII_RXD1	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO2[11]
				[9]	RGMII_RXD1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RXD1_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RXD1_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RXD1_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD1_FS	2'h3	PIN function selection 00: Normal function (RGMII_RXD1 or RMII_RXD1) 01: N/A 10: N/A 11: GPIO	
	00B0H	RGMII_RXD2	RW				PIN configuration register	
				[31:10]	Reserved			GPIO2[12]
				[9]	RGMII_RXD2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RXD2_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RXD2_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RXD2_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
Ethernet MAC	00B4H	RGMII_RXD3	RW				PIN configuration register	GPIO2[13]
				[31:10]	Reserved			
				[9]	RGMII_RXD3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RXD3_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RXD3_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RXD3_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_RXD3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00B8H	RGMII_RX_DV	RW				PIN configuration register	GPIO2[14]
				[31:10]	Reserved			
				[9]	RGMII_RX_DV_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_RX_DV_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_RX_DV_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_RX_DV_DS	4'h0	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[1:0]	RGMII_RX_DV_FS	2'h3	PIN function selection 00: Normal function (RGMII_RX_DV or RMII_CRS_DV) 01: N/A 10: N/A 11: GPIO	
	00BCH	RGMII_TX_CLK	RW				PIN configuration register	GPIO2[15]
				[31:10]	Reserved			
				[9]	RGMII_TX_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TX_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_TX_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_TX_CLK_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TX_CLK_FS	2'h3	PIN function selection 00: Normal function (RGMII_TX_CLK or RMII_REF_CLK_OUT) 01: N/A 10: N/A 11: GPIO	
	00C0H	RGMII_TXD0	RW				PIN configuration register	GPIO3[0]
				[31:10]	Reserved			
				[9]	RGMII_TXD0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TXD0_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_TXD0_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	RGMII_TXD0_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TXD0_FS	2'h3	PIN function selection 00: Normal function (RGMII_TXD0 or RMII_TXD0) 01: N/A 10: N/A 11: GPIO	
	00C4H	RGMII_TXD1	RW				PIN configuration register	GPIO3[1]
				[31:10]	Reserved			
				[9]	RGMII_TXD1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TXD1_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_TXD1_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	RGMII_TXD1_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TXD1_FS	2'h3	PIN function selection 00: Normal function (RGMII_TXD1 or RMII_TXD1) 01: N/A 10: N/A 11: GPIO	
	00C8H	RGMII_TXD2	RW				PIN configuration register	GPIO3[2]
				[31:10]	Reserved			
				[9]	RGMII_TXD2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TXD2_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_TXD2_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	RGMII_TXD2_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TXD2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00CCH	RGMII_TXD3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	RGMII_TXD3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TXD3_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	RGMII_TXD3_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	**GPIO3[3]**
				[6]	Reserved			
				[5:2]	RGMII_TXD3_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TXD3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00D0H	RGMII_TX_EN	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	RGMII_TX_EN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	RGMII_TX_EN_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[7]	RGMII_TX_EN_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[4]
				[6]	Reserved			
				[5:2]	RGMII_TX_EN_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	RGMII_TX_EN_FS	2'h3	PIN function selection 00: Normal function (RGMII_TX_EN or RMII_TX_EN) 01: N/A 10: N/A 11: GPIO	
	00D4H	SD0_CLK	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[5]
				[6]	Reserved			
				[5:2]	SD0_CLK_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_CLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00D8H	SD0_CMD	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_CMD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	SD0_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	GPIO3[6]
				[7]	SD0_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_CMD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00DCH	SD0_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_DATA0_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[7]
				[6]	Reserved			
				[5:2]	SD0_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA0_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E0H	SD0_DATA1	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	SD0_DATA1_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO3[8]
				[8]	SD0_DATA1_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA1_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA1_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA1_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E4H	SD0_DATA2	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD0_DATA2_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA2_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA2_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO3[9]
				[6]	Reserved			
				[5:2]	SD0_DATA2_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00E8H	SD0_DATA3	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SD0				[9]	SD0_DATA3_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO3[10]
				[8]	SD0_DATA3_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00ECH	SD0_DATA4	RW				PIN configuration register	GPIO3[11]
				[31:10]	Reserved			
				[9]	SD0_DATA4_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA4_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA4_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA4_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA4_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00F0H	SD0_DATA5	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO3[12]
				[9]	SD0_DATA5_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA5_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA5_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA5_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA5_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00F4H	SD0_DATA6	RW				PIN configuration register	
				[31:10]	Reserved			GPIO3[13]
				[9]	SD0_DATA6_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA6_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA6_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA6_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA6_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
	00F8H	SD0_DATA7	RW				PIN configuration register	GPIO3[14]
				[31:10]	Reserved			
				[9]	SD0_DATA7_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA7_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA7_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA7_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DATA7_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	00FCH	SD0_DATA_STRB	RW				PIN configuration register	GPIO3[15]
				[31:10]	Reserved			
				[9]	SD0_DATA_STRB_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD0_DATA_STRB_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD0_DATA_STRB_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD0_DATA_STRB_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[1:0]	SD0_DATA_STRB_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0100H	SD0_DET_EN	RW				PIN configuration register	GPIO4[0]
				[31:9]	Reserved			
				[8]	SD0_DET_EN_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SD0_DET_EN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SD0_DET_EN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	SD0_DET_EN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD0_DET_EN_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0104H	SD0_WPROT	RW				PIN configuration register	GPIO4[1]
				[31:9]	Reserved			
				[8]	SD0_WPROT_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SD0_WPROT_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SD0_WPROT_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	SD0_WPROT_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[1:0]	SD0_WPROT_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0108H	SD1_CLK	RW				PIN configuration register	GPIO4[2]
				[31:10]	Reserved			
				[9]	SD1_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD1_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD1_CLK_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_CLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	010CH	SD1_CMD	RW				PIN configuration register	GPIO4[3]
				[31:10]	Reserved			
				[9]	SD1_CMD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD1_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SD1				[5:2]	SD1_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_CMD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0110H	SD1_DATA0	RW				PIN configuration register	GPIO4[4]
				[31:10]	Reserved			
				[9]	SD1_DATA0_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD1_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD1_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA0_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0114H	SD1_DATA1	RW				PIN configuration register	GPIO4[5]
				[31:10]	Reserved			
				[9]	SD1_DATA1_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_DATA1_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD1_DATA1_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	SD1_DATA1_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA1_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0118H	SD1_DATA2	RW				PIN configuration register	GPIO4[6]
				[31:10]	Reserved			
				[9]	SD1_DATA2_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_DATA2_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD1_DATA2_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD1_DATA2_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	011CH	SD1_DATA3	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD1_DATA3_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD1_DATA3_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[7]	SD1_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO4[7]
				[6]	Reserved			
				[5:2]	SD1_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD1_DATA3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0120H	SD2_CLK	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD2_CLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD2_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO4[8]
				[6]	Reserved			
				[5:2]	SD2_CLK_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_CLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0124H	SD2_CMD	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD2_CMD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SD2				[8]	SD2_CMD_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	GPIO4[9]
				[7]	SD2_CMD_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_CMD_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_CMD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0128H	SD2_DATA0	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	SD2_DATA0_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD2_DATA0_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_DATA0_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	GPIO4[10]
				[6]	Reserved			
				[5:2]	SD2_DATA0_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA0_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	012CH	SD2_DATA1	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	SD2_DATA1_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO4[11]
				[8]	SD2_DATA1_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_DATA1_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_DATA1_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA1_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0130H	SD2_DATA2	RW				PIN configuration register	GPIO4[12]
				[31:10]	Reserved			
				[9]	SD2_DATA2_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD2_DATA2_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_DATA2_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_DATA2_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA2_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0134H	SD2_DATA3	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO4[13]
				[9]	SD2_DATA3_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SD2_DATA3_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SD2_DATA3_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SD2_DATA3_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SD2_DATA3_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0138H	BT1120_OUT_CLK	RW				PIN configuration register	
				[31:10]	Reserved			GPIO4[14]
				[9]	BT1120_OUT_CLK_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_CLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_CLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_CLK_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_CLK_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_CLK or BT656_OUT_CLK) 01: DVP_IN_PCLK 10: RGB_CLK 11: GPIO	
	013CH	BT1120_OUT_DAT0	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO4[15]
				[9]	BT1120_OUT_DAT0_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT0_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT0_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT0_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT0_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT0 or BT656_DAT0) 01: DVP_IN_VSYNC 10: RGB_DAT0 11: GPIO	
	0140H	BT1120_OUT_DAT1	RW				PIN configuration register	GPIO5[0]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT1_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT1_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT1_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT1_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT1 or BT656_DAT1) 01: DVP_IN_HSYNC 10: RGB_DAT1 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
	0144H	BT1120_OUT_DAT2	RW				PIN configuration register	GPIO5[1]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT2_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT2_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT2_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT2_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT2_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT2 or BT656_DAT2) 01: DVP_IN_DATA0 10: RGB_DAT2 11: GPIO	
	0148H	BT1120_OUT_DAT3	RW				PIN configuration register	GPIO5[2]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT3_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT3_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT3_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT3_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[1:0]	BT1120_OUT_DAT3_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT3 or BT656_DAT3) 01: DVP_IN_DATA1 10: RGB_DAT3 11: GPIO	
	014CH	BT1120_OUT_DAT4	RW				PIN configuration register	**GPIO5[3]**
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT4_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT4_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT4_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT4_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT4_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT4 or BT656_DAT4) 01: DVP_IN_DATA2 10: RGB_DAT4 11: GPIO	
	0150H	BT1120_OUT_DAT5	RW				PIN configuration register	**GPIO5[4]**
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT5_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT5_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT5_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[5:2]	BT1120_OUT_DAT5_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT5_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT5 or BT656_DAT5) 01: DVP_IN_DATA3 10: RGB_DAT5 11: GPIO	
	0154H	BT1120_OUT_DAT6	RW				PIN configuration register	GPIO5[5]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT6_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT6_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT6_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT6_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT6_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT6 or BT656_DAT6) 01: DVP_IN_DATA4 10: RGB_DAT6 11: GPIO	
BT1120_OUT	0158H	BT1120_OUT_DAT7	RW				PIN configuration register	GPIO5[6]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT7_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT7_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT7_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT7_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT7_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT7 or BT656_DAT7) 01: DVP_IN_DATA5 10: RGB_DAT7 11: GPIO	
	015CH	BT1120_OUT_DAT8	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT8_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT8_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT8_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	**GPIO5[7]**
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT8_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT8_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT8 or BT656_DAT0) 01: DVP_IN_DATA6 10: RGB_DAT8 11: GPIO	
	0160H	BT1120_OUT_DAT9	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT9_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT9_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[7]	BT1120_OUT_DAT9_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[8]
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT9_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT9_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT9 or BT656_DAT1) 01: DVP_IN_DATA7 10: RGB_DAT9 11: GPIO	
	0164H	BT1120_OUT_DAT10	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT10_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT10_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT10_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[9]
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT10_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT10_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT10 or BT656_DAT2) 01: DVP_IN_DATA8 10: RGB_DAT10 11: GPIO	
	0168H	BT1120_OUT_DAT11	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT11_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	BT1120_OUT_DAT11_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	GPIO5[10]
				[7]	BT1120_OUT_DAT11_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT11_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT11_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT11 or BT656_DAT3) 01: DVP_IN_DATA9 10: RGB_DAT11 11: GPIO	
	016CH	BT1120_OUT_DAT12	RW				PIN configuration register	
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT12_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT12_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT12_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	GPIO5[11]
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT12_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT12_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT12 or BT656_DAT4) 01: DVP_IN_DATA10 10: RGB_DAT12 11: GPIO	
	0170H	BT1120_OUT_DAT13	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	BT1120_OUT_DAT13_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO5[12]
				[8]	BT1120_OUT_DAT13_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT13_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT13_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT13_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT13 or BT656_DAT5) 01: DVP_IN_DATA11 10: RGB_DAT13 11: GPIO	
	0174H	BT1120_OUT_DAT14	RW				PIN configuration register	GPIO5[13]
				[31:10]	Reserved			
				[9]	BT1120_OUT_DAT14_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT14_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT14_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT14_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT14_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT14 or BT656_DAT6) 01: N/A 10: RGB_DAT14 11: GPIO	
	0178H	BT1120_OUT_DAT15	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO5[14]
				[9]	BT1120_OUT_DAT15_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BT1120_OUT_DAT15_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BT1120_OUT_DAT15_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BT1120_OUT_DAT15_DS	4'h3	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BT1120_OUT_DAT15_FS	2'h3	PIN function selection 00: Normal function (BT1120_OUT_DAT15 or BT656_DAT7) 01: N/A 10: RGB_DAT15 11: GPIO	
	017CH	UART0_TXD	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	UART0_TXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART0_TXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART0_TXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO5[15]
				[5:2]	UART0_TXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART0_TXD_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
UART0	0180H	UART0_RXD	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:9]	Reserved			GPIO6[0]
				[8]	UART0_RXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART0_RXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART0_RXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	UART0_RXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART0_RXD_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0184H	UART1_TXD	RW				PIN configuration register	GPIO6[1]
				[31:9]	Reserved			
				[8]	UART1_TXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_TXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_TXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	UART1_TXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_TXD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0188H	UART1_RXD	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
UART1				[8]	UART1_RXD_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[2]
				[7]	UART1_RXD_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_RXD_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	UART1_RXD_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_RXD_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	018CH	UART1_RTSN	RW				PIN configuration register	GPIO6[3]
				[31:9]	Reserved			
				[8]	UART1_RTSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	UART1_RTSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_RTSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	UART1_RTSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_RTSN_FS	2'h3	PIN function selection 00: Normal function 01: UART2_TXD 10: N/A 11: GPIO	
	0190H	UART1_CTSN	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	UART1_CTSN_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[4]
				[7]	UART1_CTSN_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	UART1_CTSN_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	UART1_CTSN_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	UART1_CTSN_FS	2'h3	PIN function selection 00: Normal function 01: UART2_RXD 10: N/A 11: GPIO	
	0194H	I2S0_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S0_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S0_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S0_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[5]
				[5:2]	I2S0_MCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	0198H	I2S0_BCLK	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
I2S0				[8]	I2S0_BCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[6]
				[7]	I2S0_BCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S0_BCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2S0_BCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_BCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	019CH	I2S0_LRCK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S0_LRCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S0_LRCK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S0_LRCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[7]
				[5:2]	I2S0_LRCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_LRCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A0H	I2S0_SDIO	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	I2S0_SDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[8]
				[7]	I2S0_SDIO_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S0_SDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2S0_SDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S0_SDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A4H	I2S1_MCLK	RW				PIN configuration register	GPIO6[9]
				[31:9]	Reserved			
				[8]	I2S1_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2S1_MCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01A8H	I2S1_BCLK	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
I2S1				[8]	I2S1_BCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[10]
				[7]	I2S1_BCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_BCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2S1_BCLK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_BCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01ACH	I2S1_LRCK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	I2S1_LRCK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	I2S1_LRCK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_LRCK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[11]
				[5:2]	I2S1_LRCK_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_LRCK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B0H	I2S1_SDIO	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[8]	I2S1_SDIO_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[12]
				[7]	I2S1_SDIO_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	I2S1_SDIO_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	I2S1_SDIO_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	I2S1_SDIO_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B4H	SENSOR0_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	SENSOR0_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	SENSOR0_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SENSOR0_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO6[13]
				[5:2]	SENSOR0_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR0_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01B8H	SENSOR1_MCLK	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
SENSOR				[8]	SENSOR1_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO6[14]
				[7]	SENSOR1_MCLK_PS	1'h0	PIN pull selector 0: Pull down 1: Pull up	
				[6]	SENSOR1_MCLK_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	SENSOR1_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR1_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01BCH	SENSOR2_MCLK	RW				PIN configuration register	GPIO6[15]
				[31:10]	Reserved			
				[9]	SENSOR2_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	SENSOR2_MCLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SENSOR2_MCLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SENSOR2_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR2_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: UART3_TXD 10: N/A 11: GPIO	
	01C0H	SENSOR3_MCLK	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[9]	SENSOR3_MCLK_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO7[0]
				[8]	SENSOR3_MCLK_PU	1'h0	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	SENSOR3_MCLK_PD	1'h1	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	SENSOR3_MCLK_DS	4'h1	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	SENSOR3_MCLK_FS	2'h3	PIN function selection 00: Normal function 01: UART3_RXD 10: N/A 11: GPIO	
	01C4H	WDT_RSTOUT_N	RW				PIN configuration register	GPIO7[1]
				[31:9]	Reserved			
				[8]	WDT_RSTOUT_N_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	WDT_RSTOUT_N_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	WDT_RSTOUT_N_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	WDT_RSTOUT_N_DS	4'h1	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	WDT_RSTOUT_N_FS	2'h0	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01C8H	X2A_WKUPIN_N	RW				PIN configuration register	
				[31:9]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
MISC				[8]	X2A_WKUPIN_N_ST	1'h1	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO7[2]
				[7]	X2A_WKUPIN_N_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	X2A_WKUPIN_N_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	X2A_WKUPIN_N_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	X2A_WKUPIN_N_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01CCH	X2A_IRQOUT_N	RW				PIN configuration register	
				[31:9]	Reserved			
				[8]	X2A_IRQOUT_N_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	X2A_IRQOUT_N_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	X2A_IRQOUT_N_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	GPIO7[3]
				[5:2]	X2A_IRQOUT_N_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	X2A_IRQOUT_N_FS	2'h3	PIN function selection 00: Normal function 01: N/A 10: N/A 11: GPIO	
	01D0H	BIFSD_DATA4	RW				PIN configuration register	
				[31:10]	Reserved			

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
BIFSD				[9]	BIFSD_DATA4_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	GPIO7[4]
				[8]	BIFSD_DATA4_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA4_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA4_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA4_FS	2'h0	PIN function selection 00: Normal function 01: LPWM0 10: RGB_DAT20 11: GPIO	
	01D4H	BIFSD_DATA5	RW				PIN configuration register	GPIO7[5]
				[31:10]	Reserved			
				[9]	BIFSD_DATA5_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA5_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA5_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA5_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA5_FS	2'h0	PIN function selection 00: Normal function 01: LPWM1 10: RGB_DAT21 11: GPIO	
	01D8H	BIFSD_DATA6	RW				PIN configuration register	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
				[31:10]	Reserved			GPIO7[6]
				[9]	BIFSD_DATA6_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA6_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA6_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA6_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA6_FS	2'h0	PIN function selection 00: Normal function 01: LPWM2 10: RGB_DAT22 11: GPIO	
	01DCH	BIFSD_DATA7	RW				PIN configuration register	
				[31:10]	Reserved			GPIO7[7]
				[9]	BIFSD_DATA7_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[8]	BIFSD_DATA7_PU	1'h1	PIN pull up enable 0: Disabled 1: Enabled	
				[7]	BIFSD_DATA7_PD	1'h0	Pin pull down enable 0: Disabled 1: Enabled	
				[6]	Reserved			
				[5:2]	BIFSD_DATA7_DS	4'h6	PIN Driving selector (typical value) 0000: 6mA 0001: 9mA 0010: 12mA 0011: 15mA 0100: 18mA 0101: 21mA 0110: 24mA 0111:27mA 1000: 30mA 1001: 33mA 1010: 36mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	BIFSD_DATA7_FS	2'h0	PIN function selection 00: Normal function 01: LPWM3 10: RGB_DAT23 11: GPIO	

PIN Group	PIN_REG BASE_ADDR: 0xA600_4000							
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description	GPIO
QSPI	01E0H	QSPI_CSN1	RW				PIN configuration register	GPIO7[8]
				[31:9]	Reserved			
				[8]	QSPI_CSN1_ST	1'h0	PIN Schmitt trigger enable 0: Disabled 1: Enabled	
				[7]	QSPI_CSN1_PS	1'h1	PIN pull selector 0: Pull down 1: Pull up	
				[6]	QSPI_CSN1_PE	1'h1	Pin pull enable 0: Pull function is disabled 1: Pull function is enabled	
				[5:2]	QSPI_CSN1_DS	4'h0	PIN Driving selector (typical value) 0000: 3mA 0001: 6mA 0010: 9mA 0011: 12mA 0100: 17mA 0101: 20mA 0110: 22mA 0111:25mA 1000: 33mA 1001: 35mA 1010: 37mA 1011: 39mA 1100: 41mA 1101: 42.5mA 1110: 44mA 1111:45mA	
				[1:0]	QSPI_CSN1_FS	2'h3	PIN function selection 00: Normal function 01: SPI0_CSN1 10: N/A 11: GPIO	