地 平 线
Horizon Robotics

Sunrise 3

DDR4/LPDDR4/4X Board Design Checklist

Rev. 1.1

Jul 14 2021

Important Notice and Disclaimer

Information in this document is provided solely to enable system and software implementers to use Horizon products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

The information in this document is subject to change without notice. Every effort has been made in the preparation of this document to ensure accuracy of the contents, but all statements, information, and recommendations in this document do not constitute a warranty of any kind, express or implied.

All statements, information and recommendations in this document are provided "AS IS". Horizon makes no warranty, representation or guarantee of any kind, express or implied, regarding the merchantability, fitness or suitability of its products for any particular purpose, and non-infringement of any third party intellectual property rights, nor does Horizon assume any liability arising out of the application or use of any product, and specifically disclaims any and all liability, including without limitation consequential or incidental damages.

"Typical" parameters that may be provided in Horizon datasheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Buyers and others who are developing systems that incorporate Horizon products (collectively, "Users") understand and agree that Users shall remain responsible for using independent analysis, evaluation and judgment in designing their applications and that Users have full and exclusive responsibility to assure the safety of Users' applications and compliance of their applications (and of all Horizon products used in or for Users' applications) with all applicable regulations, laws and other applicable requirements.

User agrees to fully indemnify Horizon and its representatives against any claims, damages, costs, losses and/or liabilities arising out of User's unauthorized application of Horizon products and non-compliance with any terms of this notice.

Horizon Robotics, Inc.

https://www.horizon.ai

Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
1.0	2021/02/04	Initial release
1.1	2021/07/14	Update PDN checklist and SI checklist

Contents

Figures

未找到图形项目表。

Tables

1 Scope

The document is intended to provide necessary points which needs to be checked during the Sunrise3 DDR4/LPDDR4/4X schematic design, PCB layout design and PCB manufacturing.

Any compromise should be carefully evaluated, otherwise the customer design may have high risk to degrade the DDR4/LPDDR4/4X data rate.

2 Schematic Checklist

Table 2-1 Schematic Checklist

Item	Description	Y/N
1	X3's VDDQ & VDDQLP power plane should be combined together and supplied by one DCDC power supply for DDR4/LPDDR4 design.	
2	Current output capability of power supply to X3 VDDQ&VDDQLP and LPDDR4 VDDQ&VDD2 should be > 3A	
3	BP_ZN of X3 should be pulled down to VSS with a 120Ω ± 1% resistor	
4	The value of De-coupling capacitors for X3 VDDQ&VDDQLP should follow X3 reference design, and the capacitors should be placed as close as possible to X3 VDDQ&VDDQLP pins. Being Placed on the back side of the X3's power ball is highly preferred for smaller value (<1uH) capacitors.	
5	The value of De-coupling capacitors for X3 VDD_DDR should follow X3 reference design, and the capacitors should be placed as close as possible to the X3 VDD_DDR pins. Being placed on the back side of the X3's power ball is highly preferred for smaller value (<1uH) capacitors.	

3 PCB Layout Checklist

Table 3-1 PCB Layout Checklist

Item	Description	Y/N
1	The PCB stack up should follow reference design, 8-layer. Refer to X3's HW Design Guide, Section 2.2. Any change to the stack-up should be carefully evaluated, especially SIPI simulation should be re-conducted to ensure that the trace impedance and PDN impedance meet target.	
2	The DDR signal trace length should be controlled to meet the requirements mentioned in X3 HW Design Guide Section 2.4.4 & 2.4.5.	
3	The PCB trace impedance should be strictly controlled. Refer to X3 HW	

	Design Guide Section 2.4.4 & 2.4.5 for the requirement.	
4	The decoupling capacitors of X3 VDDQ & VDDQLP should be placed on the back side of X3's power ball. PI simulation should be conducted to ensure the VDDQ PDN's AC impedance meet target mentioned in X3 HW Design Guide, Section 3.4.	
5	The decoupling capacitors of X3's VDD_DDR should be placed on the back side of X3's Power ball. PI simulation should be conducted to ensure the VDD_DDR PDN's AC impedance meet target mentioned in X3 HW Design Guide, Section 3.4.	

4 PDN Checklist

In order to meet PDN target efficiently and reduce the repetitive iterations between design and simulation, X3's reference design should be followed carefully during PCB layout and Table 4-1 should be done before PDN simulation.

Table 4-1 PDN Review Checklist

Item	Description	Y/N
1	The PCB's total thickness should be equal to or less than reference design, 1.5mm of 8-layer PCB. Refer to X3's HW Design Guide, Section 2.2.	
2	The utilization of each layer should follow reference design, 8-layer. Refer to X3's HW Design Guide, Section 2.2.	
3	The part number of decoupling capacitors of X3 VDDQ & VDDQLP & VDD DDR should follow reference design. Refer to X3's HW Design Guide, Section 2.3.2 and Section 2.3.3.	
4	The number of decoupling capacitors of X3 VDDQ & VDDQLP & VDD DDR should follow reference design. Refer to X3's HW Design Guide, Section 2.3.2 and Section 2.3.3.	
5	The decoupling capacitors of X3 VDDQ & VDDQLP & VDD DDR should be placed on the back side of X3's power ball to reduce the capacitor's loop inductance. Refer to X3's HW Design Guide, Section 2.3.1 and Section 2.3.3.	
6	Each BGA ball has one or two BGA via and the ratio of BGA via to VGA ball should equal or larger than 1:1 to minimize the inductance of BGA via pair loop inductance. Refer to "Power Delivery Network Analysis.pdf", Section 7.2.	
7	The capacitor's fanout has been optimized and Via-in-pad method has beed used to reduce capacitor's loop inductance. Refer to "Power	

	Delivery Network Analysis.pdf", Section 7.2.	

During PDN simulation, the PDN extraction flow and PDN results for each power supply must meet respective requirements defined by Horizon. Table 4-2 should be done before PCB's Gerber out.

Table 4-2 PDN Simulation Checklist

Item	Description	Y/N
1	The PDN impedances of VDDQ & VDDQLP & VDD DDR meet PDN targets at the specified frequency given in X3 HW Design Guide Section 3.4.	
2	The PCB DC resistance of VDDQ & VDDQLP & VDD DDR meet DC resistance targets given in X3 HW Design Guide Section 3.4.	
3	The loop inductance per capacitor of VDDQ & VDDQLP & VDD DDR meet loop inductance targets given in X3 HW Design Guide Section 3.4.	
4	The extraction flow of PDN impedances meets PDN extraction guidelines given in "Power Delivery Network Analysis.pdf", Section 5.	
5	The extraction flow of PCB DC resistance meets DC resistance extraction flow given in "Power Delivery Network Analysis.pdf", Section 3.	
6	The extraction flow of capacitor's loop inductance meets DC resistance extraction flow given in "Power Delivery Network Analysis.pdf", Section 4.	
7	If PDN impedances of VDDQ & VDDQLP & VDD DDR above PDN targets defined in X3 HW Design Guide Section 3.4, PDN optimization has been done based on these methods mentioned in "Power Delivery Network Analysis.pdf", Section 7.	

5 SI Checklist

The X3's reference design should be followed carefully during PCB layout and Table 5-1 should be done before SI simulation.

Table 5-1 SI Review Checklist

Item	Description	Y/N
1	The PCB's total thickness should be equal to or less than reference design, 1.5mm of 8-layer PCB. Refer to X3's HW Design Guide, Section 2.2.	
2	The utilization of each layer should follow reference design, 8-layer. Refer to X3's HW Design Guide, Section 2.2.	

3	The main reference plane for signal routing should be an uninterrupted GND plane, and the height to the reference plane should be kept as low as possible.	
4	Vias can be a significant source of crosstalk. Do not merge Gnd vias in BGA fanout region and keep GND ball's fanout as short as possible.	
5	Place a ground stitching via as near as possible to the signal via when switching reference planes to avoid signal via's crosstalk.	
6	The minimum spacing between DDR signals should meet the line spacing rule. Refer to X3's HW Design Guide, Section 2.4.1.	

During SI simulation, the simulation topology and eye results for DDR SI simulation must meet respective requirements defined by Horizon in Section 3.5 of X3's HW Design Guide. Table 5-2 should be done before PCB's Gerber out.

Table 5-2 SI Simulation Checklist

Item	Description	Y/N
1	The SI simulation for DDR should include SI-Write, SI-Read, SI-Addr and CLK-Jitter. Refer to X3's HW Design Guide, Section 3.5.	
2	The topology for SI simulation should follow X3's HW Design Guide, Section 3.5.1, Section 3.5.2, Section 3.5.3.	
3	The correct package models have been used for X3 and DDR SDRAM. S-Parameter and Spice model , rather than RLC model, are recommended for package modeling in DDR SI simulation. Refer to X3's HW Design Guide, Section 3.5.1, Section 3.5.2, Section 3.5.3.	
4	The eye results of SI simulation must meet Eye mask defined in X3's HW Design Guide, Section 3.6.1.	
5	If Eye results do not meet Eye mask requirements, Layout review in Table 3-1 and SI review in Table 4-1 have been double checked.	

6 Manufacturing Checklist

Generally, PCB factory probably would request to change the PCB stack up and dielectric material according to factory's material availability.

Caution: Any change to the PCB stack up and dielectric material should be carefully evaluated. The following points should be checked one by one.

Table 6-1 Manufacturing Checklist

Item	Description	Y/N
1	Requirements on Impedance of DQ, DM and DQS should meet target	

2	Requirements on Impedance of CA should meet target	
3	Requirements on Impedance of CA should meet target	
4	Requirements on Impedance of CLK_T/C should meet target	
5	PI simulation should be conducted based on new stack up and dielectric material to ensure the PDNs' AC impedance meet target. Especially VDDQ & VDD_DDR for DD4/LPDDR4 mode, VDDQ, VDDQ_LP & VDD_DDR for LPDDR4X mode	
6	DK & DF factor for new dielectric should be better than dielectric used in reference design (IT180-A).	
Note: Refer to X3s' HW Design Guide Section 2.4.4 & 2.4.5 for the trace impedance requirements and Section 3.4 for PDN's AC impedance target.		