X3M Register Reference Manual
Ethernet MAC

Revision History

Revision	Date	Description
1.0	September-10-2020	Initial Release

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	00H	MAC_Configuration	RW	[31]	ARPEN	1'h0	ARP Offload Enable When this bit is set, the MAC can recognize an incoming ARP request packet and schedules the ARP packet for transmission. It forwards the ARP packet to the application and also indicate the events in the RxStatus. 0: ARP Offload is disabled 1: ARP Offload is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
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				[30:28]	SARC	3'h0	Source Address Insertion or Replacement Control Bit[30] specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits[29:28]: **2'b0x:** The mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation. **2'b10:** If Bit[30] is set to 0, the MAC inserts the content of the MAC Address 0 registers in the SA field of all transmitted packets. If Bit[30] is set to 1 the MAC Address Register 1 is enabled while configuring the core, the MAC inserts the content of the MAC Address 1 registers in the SA field of all transmitted packets. **2'b11:** If Bit[30] is set to 0, the MAC replaces the content of the MAC Address 0 registers in the SA field of all transmitted packets. If Bit[30] is set to 1 and the MAC Address Register 1 is enabled, the MAC replaces the content of the MAC Address 1 registers in the SA field of all transmitted packets. **Note:** Changes to this field take effect only on the start of a packet. If you write to this register field when a packet is being transmitted, only the subsequent packet can use the updated value, that is, the current packet does not use the updated

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							value. 0: mti_sa_ctrl_i and ati_sa_ctrl_i input signals control the SA field generation 2: Contents of MAC Addr-0 inserted in SA field 3: Contents of MAC Addr-0 replaces SA field 6: Contents of MAC Addr-1 inserted in SA field 7: Contents of MAC Addr-1 replaces SA field
				[27]	IPC	1'h0	Checksum Offload 0: IP header/payload checksum checking is disabled 1: IP header/payload checksum checking is enabled
				[26:24]	IPG	3'h0	Inter-Packet Gap The above function (IPG less than 96 bit times) is valid only when EIPGEN bit in MAC_Ext_Configuration register is reset. When EIPGEN is set, then the minimum IPG (greater than 96 bit times) is controlled as per the description given in EIPG field in MAC_Ext_Configuration register. 0 (IPG96): 96 bit times IPG 1 (IPG88): 88 bit times IPG 2 (IPG80): 80 bit times IPG 3 (IPG72): 72 bit times IPG 4 (IPG64): 64 bit times IPG 5 (IPG56): 56 bit times IPG 6 (IPG48): 48 bit times IPG 7 (IPG40): 40 bit times IPG
				[23]	GPSLCE	1'h0	Giant Packet Size Limit Control Enable The programmed giant packet limit should be less than the watchdog limit to get the giant packet status. 0: Giant Packet Size Limit Control is disabled 1: Giant Packet Size Limit Control is enabled

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				[22]	S2KP	1'h0	IEEE 802.3as Support for 2K Packets **Note:** When the JE bit is set, setting this bit has no effect on the giant packet status. 0: Support up to 2K packet is disabled 1: Support up to 2K packet is Enabled
				[21]	CST	1'h0	CRC stripping for Type packets When this bit is set, the last four bytes (FCS) of all packets of Ether type (type field greater than 1,536) are stripped and dropped before forwarding the packet to the application. 0: CRC stripping for Type packets is disabled 1: CRC stripping for Type packets is enabled
				[20]	ACS	1'b0	Automatic Pad or CRC Stripping When this bit is set, the MAC strips the Pad or FCS field on the incoming packets only if the value of the length field is less than 1,536 bytes. All received packets with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field. 0: Automatic Pad or CRC Stripping is disabled 1: Automatic Pad or CRC Stripping is enabled
				[19]	WD	1'h0	Watchdog Disable When this bit is set, the MAC disables the watchdog timer on the receiver. The MAC can receive packets of up to 16,383 bytes. 0: Watchdog is enabled 1: Watchdog is disabled

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				[18]	BE	1'h0	Packet Burst Enable When this bit is set, the MAC allows packet bursting during transmission in the GMII half-duplex mode. 0: Packet Burst is disabled 1: Packet Burst is enabled
				[17]	JD	1'b0	Jabber Disable When this bit is set, the MAC disables the jabber timer on the transmitter. The MAC can transfer packets of up to 16,383 bytes. 0: Jabber is enabled 1: Jabber is disabled
				[16]	JE	1'h0	Jumbo Packet Enable When this bit is set, the MAC allows jumbo packets of 9,018 bytes (9,022 bytes for VLAN tagged packets) without reporting a giant packet error in the Rx packet status. 0: Jumbo packet is disabled 1: Jumbo packet is enabled
				[15]	PS	1'h0	Port Select This bit selects the Ethernet line speed. 0: For 1000 or 2500 Mbps operations 1: For 10 or 100 Mbps operations
				[14]	FES	1'h0	Speed This bit selects the speed mode. 0 (10_1000M): 10 Mbps when PS bit is 1 and 1 Gbps when PS bit is 0 1 (100_2500M): 100 Mbps when PS bit is 1 and 2.5 Gbps when PS bit is 0

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				[13]	DM	1'h0	Duplex Mode When this bit is set, the MAC operates in the full-duplex mode in which it can transmit and receive simultaneously. 0: Half-duplex mode 1: Full-duplex mode
				[12]	LM	1'h0	Loopback Mode When this bit is set, the MAC operates in the loopback mode at GMII. 0: Loopback is disabled 1: Loopback is enabled
				[11]	ECRSFD	1'h0	Enable Carrier Sense Before Transmission in Full-Duplex Mode When this bit is set, the MAC transmitter checks the Carrier Sense (CRS) signal before packet transmission in the full-duplex mode. The MAC starts the transmission only when the CRS signal is low. 0: ECRSFD is disabled 1: ECRSFD is enabled
				[10]	DO	1'h0	Disable Receive Own When this bit is set, the MAC disables the reception of packets in the half-duplex mode. This bit is not applicable in the full-duplex mode. 0: Receive Own is enabled 1: Receive Own is disabled

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				[9]	DCRS	1'h0	Disable Carrier Sense During Transmission When this bit is set, the MAC transmitter ignores the (G)MII CRS signal during packet transmission in the half-duplex mode. As a result, no errors are generated because of Loss of Carrier or No Carrier during transmission. 0: Carrier Sense During Transmission is enabled 1: Carrier Sense During Transmission is disabled
				[8]	DR	1'h0	Disable Retry When this bit is set, the MAC attempts only one transmission. When a collision occurs on the GMII interface, the MAC ignores the current packet transmission and reports a Packet Abort with excessive collision error in the Tx packet status. This bit is applicable only in the half-duplex mode. 0: Retry is enabled 1: Retry is disabled
				[7]	Reserved		
				[6:5]	BL	2'h0	Back-Off Limit The back-off limit determines the random integer number (r) of slot time delays (4,096 bit times for 1000/2500 Mbps; 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision. n = retransmission attempt. The random integer r takes the value in the range 0 <= r < 2^k This bit is applicable only in the half-duplex mode. 0 (MIN_N_10): k = min(n,10) 1 (MIN_N_8): k = min(n,8) 2 (MIN_N_4): k = min(n,4) 3 (MIN_N_1): k = min(n,1)

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				[4]	DC	1'h0	Deferral Check When this bit is set, the deferral check function is enabled in the MAC. The MAC issues a Packet Abort status, along with the excessive deferral error bit set in the Tx packet status, when the Tx state machine is deferred for more than 24,288 bit times in 10 or 100 Mbps mode. If the MAC is configured for 1000/2500 Mbps operation, the threshold for deferral is 155,680 bits times. This bit is applicable only in the half-duplex mode. 0: Deferral check function is disabled 1: Deferral check function is enabled
				[3:2]	PRELEN	2'h0	Preamble Length for Transmit packets These bits control the number of preamble bytes that are added to the beginning of every Tx packet. The preamble reduction occurs only when the MAC is operating in the full-duplex mode. 0: 7 bytes of preamble 1: 5 bytes of preamble 2: 3 bytes of preamble 3: Reserved
				[1]	TE	1'h0	Transmitter Enable When this bit is set, the Tx state machine of the MAC is enabled for transmission on the GMII interface. 0: Transmitter is disabled 1: Transmitter is enabled

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				[0]	RE	1'h0	Receiver Enable When this bit is set, the Rx state machine of the MAC is enabled for receiving packets from the GMII interface. 0: Receiver is disabled 1: Receiver is enabled
	04H	MAC_Ext_Configuration	RW	[31:30]	Reserved		
				[29:25]	EIPG	5'h0	Extended Inter-Packet Gap The value in this field is applicable when the EIPGEN bit is set. 8'h00: 104 bit times 8'h01: 112 bit times 8'h02: 120 bit times ---------- 8'hFF: 2144 bit times
				[24]	EIPGEN	1'h0	Extended Inter-Packet Gap Enable When this bit is set, the MAC interprets EIPG field and IPG field in MAC_Configuration register together as minimum IPG greater than 96 bit times in steps of 8 bit times. **Note:** The extended Inter-Packet Gap feature must be enabled when operating in Full-Duplex mode only. There may be undesirable effects on back-pressure function and frame transmission if it is enabled in Half-Duplex mode. 0: Extended Inter-Packet Gap is disabled 1: Extended Inter-Packet Gap is enabled
				[23]	Reserved		

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				[22:20]	HDSMS	3'h0	Maximum Size for Splitting the Header Data These bits indicate the maximum header size allowed for splitting the header data in the received packet. 0: Maximum Size for Splitting the Header Data is 64 bytes 1: Maximum Size for Splitting the Header Data is 128 bytes 2: Maximum Size for Splitting the Header Data is 256 bytes 3: Maximum Size for Splitting the Header Data is 512 bytes 4: Maximum Size for Splitting the Header Data is 1024 bytes 5: Reserved
				[19]	Reserved		
				[18]	USP	1'h0	Unicast Slow Protocol Packet Detect When this bit is set, the MAC detects the Slow Protocol packets with unicast address of the station specified in the MAC_Address0_High and MAC_Address0_Low registers. The MAC also detects the Slow Protocol packets with the Slow Protocols multicast address (01-80-C2-00-00-02). 0: Unicast Slow Protocol Packet Detection is disabled 1: Unicast Slow Protocol Packet Detection is enabled
				[17]	SPEN	1'h0	Slow Protocol Detection Enable When this bit is set, MAC processes the Slow Protocol packets (Ether Type 0x8809) and provides the Rx status. The MAC discards the Slow Protocol packets with invalid sub-types. 0: Slow Protocol Detection is disabled 1: Slow Protocol Detection is enabled
				[16]	DCRCC	1'h0	Disable CRC Checking for Received Packets When this bit is set, the MAC receiver does not check the CRC field in the received packets 0: CRC Checking is enabled 1: CRC Checking is disabled

Ethernet MAC

BASE_ADDR: 0xA501_4000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:14]	Reserved		
			[13:0]	GPSL	14'h0	Giant Packet Size Limit If the received packet size is greater than the value programmed in this field in units of bytes, the MAC declares the received packet as Giant packet. The value programmed in this field must be greater than or equal to 1,518 bytes. Any other programmed value is considered as 1,518 bytes. For VLAN tagged packets, the MAC adds 4 bytes to the programmed value.
08H	MAC_Packet_Filter	RW	[31]	RA	1'h0	Receive All When this bit is set, the MAC Receiver module passes all received packets to the application, irrespective of whether they pass the address filter or not. 0: Receive All is disabled 1: Receive All is enabled
			[30:22]	Reserved		
			[21]	DNTU	1'h0	Drop Non-TCP/UDP over IP Packets When this bit is set, the MAC drops the non-TCP or UDP over IP packets. The MAC forward only those packets that are processed by the Layer 4 filter. 0: Forward Non-TCP/UDP over IP Packets 1: Drop Non-TCP/UDP over IP Packets
			[20]	IPFE	1'h0	Layer 3 and Layer 4 Filter Enable When this bit is set, the MAC drops packets that do not match the enabled Layer 3 and Layer 4 filters. If Layer 3 or Layer 4 filters are not enabled for matching, this bit does not have any effect. 0: Layer 3 and Layer 4 Filters are disabled 1: Layer 3 and Layer 4 Filters are enabled

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[19:17]	Reserved		
				[16]	VTFE	1'h0	VLAN Tag Filter Enable When this bit is set, the MAC drops the VLAN tagged packets that do not match the VLAN Tag. 0: VLAN Tag Filter is disabled 1: VLAN Tag Filter is enabled
				[15:11]	Reserved		
				[10]	HPF	1'h0	Hash or Perfect Filter When this bit is set, the address filter passes a packet if it matches either the perfect filtering or hash filtering as set by the HMC or HUC bit. 0: Hash or Perfect Filter is disabled 1: Hash or Perfect Filter is enabled
				[9]	SAF	1'h0	Source Address Filter Enable 0: SA Filtering is disabled 1: SA Filtering is enabled
				[8]	SAIF	1'h0	SA Inverse Filtering 0: SA Inverse Filtering is disabled 1: SA Inverse Filtering is enabled

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				[7:6]	PCF	2'h0	Pass Control Packets These bits control the forwarding of all control packets (including unicast and multicast Pause packets). 0: MAC filters all control packets from reaching the application 1: MAC forwards all control packets except Pause packets to the application even if they fail the Address filter 2: MAC forwards all control packets to the application even if they fail the Address filter 3: MAC forwards the control packets that pass the Address filter
				[5]	DBF	1'h0	Disable Broadcast Packets When this bit is set, the AFM module blocks all incoming broadcast packets. In addition, it overrides all other filter settings. 0: Enable Broadcast Packets 1: Disable Broadcast Packets
				[4]	PM	1'h0	Pass All Multicast When this bit is set, it indicates that all received packets with a multicast destination address (first bit in the destination address field is '1') are passed. 0: Pass All Multicast is disabled 1: Pass All Multicast is enabled
				[3]	DAIF	1'h0	DA Inverse Filtering When this bit is set, the Address Check block operates in inverse filtering mode for the DA address comparison for both unicast and multicast packets. 0: DA Inverse Filtering is disabled 1: DA Inverse Filtering is enabled

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	HMC	1'h0	Hash Multicast When this bit is set, the MAC performs the destination address filtering of received multicast packets according to the hash table. 0: Hash Multicast is disabled 1: Hash Multicast is enabled
				[1]	HUC	1'h0	Hash Unicast When this bit is set, the MAC performs the destination address filtering of unicast packets according to the hash table. 0: Hash Unicast is disabled 1: Hash Unicast is enabled
				[0]	PR	1'h0	Promiscuous Mode When this bit is set, the Address Filtering module passes all incoming packets irrespective of the destination or source address. The SA or DA Filter Fails status bits of the Rx Status Word are always cleared when PR is set. 0: Promiscuous Mode is disabled 1: Promiscuous Mode is enabled
	0CH	MAC_Watchdog_Timeout	RW	[31:9]	Reserved		
				[8]	PWE	1'h0	Programmable Watchdog Enable When this bit is set and the WD bit of the MAC_Configuration register is reset, the WTO field is used as watchdog timeout for a received packet. 0: Programmable Watchdog is disabled 1: Programmable Watchdog is enabled
				[7:4]	Reserved		

Ethernet MAC

BASE_ADDR: 0xA501_4000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[3:0]	WTO	4'h0	Watchdog Timeout When the PWE bit is set and the WD bit of the MAC_Configuration register is reset, this field is used as watchdog timeout for a received packet. **Note:** When the PWE bit is set, the value in this field should be more than 1,522 (0x05F2). Otherwise, the IEEE 802.3-specified valid tagged packets are declared as error packets and then dropped. 0: 2 KB; 1: 3 KB; 2: 4 KB; 3: 5 KB; 4: 6 KB; 5: 7 KB; 6: 8 KB; 7: 9 KB; 8: 10 KB; 9: 11 KB; a: 12 KB; b: 13 KB; c: 14 KB; d: 15 KB; e: 16383 Bytes; f: Reserved
10H	MAC_Hash_Table_Reg0	RW	[31:0]	HT31T0	32'h0	MAC Hash Table First 32 Bits This field contains the first 32 Bits [31:0] of the Hash table.
14H	MAC_Hash_Table_Reg1	RW	[31:0]	HT63T32	32'h0	MAC Hash Table Second 32 Bits This field contains the second 32 Bits [63:32] of the Hash table.
70H	MAC_Q0_Tx_Flow_Ctrl	RW	[31:16]	PT	16'h0	Pause Time This field holds the value to be used in the Pause Time field in the Tx control packet. If the Pause Time bits are configured to be double-synchronized to the (G)MII clock domain, consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain.
			[15:8]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	DZPQ	1'h0	Disable Zero-Quanta Pause When this bit is set, it disables the automatic generation of the zero-quanta Pause packets on de-assertion of the flow-control signal from the FIFO layer. 0: Zero-Quanta Pause packet generation is enabled 1: Zero-Quanta Pause packet generation is disabled
				[6:4]	PLT	3'h0	Pause Low Threshold The threshold values should be always less than the Pause Time configured in Bits[31:16]. The following list provides the threshold values for different values. The slot time is defined as the time taken to transmit 512 bits (64 bytes) on the GMII interface. This (approximate) computation is based on the packet size (64, 1518, 2000, 9018, 16384, or 32768) + 2 Pause Packet Size + IPG in Slot Times. 0: Pause Time minus 4 Slot Times (PT -4 slot times) 1: Pause Time minus 28 Slot Times (PT -28 slot times) 2: Pause Time minus 36 Slot Times (PT -36 slot times) 3: Pause Time minus 144 Slot Times (PT -144 slot times) 4: Pause Time minus 256 Slot Times (PT -256 slot times) 5: Pause Time minus 512 Slot Times (PT -512 slot times) 6: Reserved
				[3:2]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	TFE	1'h0	Transmit Flow Control Enable In the full-duplex mode, when this bit is set, the MAC enables the flow control operation to Tx Pause packets. In the half-duplex mode, when this bit is set, the MAC enables the backpressure operation. 0: Transmit Flow Control is disabled 1: Transmit Flow Control is enabled
				[0]	FCB_BPA	1'h0	Flow Control Busy or Backpressure Activate This bit initiates a Pause packet in the full-duplex mode and activates the backpressure function in the half-duplex mode if the TFE bit is set. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Flow Control Busy or Backpressure Activate is disabled 1: Flow Control Busy or Backpressure Activate is enabled
	90H	MAC_Rx_Flow_Ctrl	RW	[31:2]	Reserved		
				[1]	UP	1'h0	Unicast Pause Packet Detect A pause packet is processed when it has the unique multicast address specified in the IEEE 802.3. When this bit is set, the MAC can also detect Pause packets with unicast address of the station. 0: Unicast Pause Packet Detect disabled 1: Unicast Pause Packet Detect enabled

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	RFE	1'h0	Receive Flow Control Enable When this bit is set and the MAC is operating in full-duplex mode, the MAC decodes the received Pause packet and disables its transmitter for a specified (Pause) time. When PFC is enabled, flow control is enabled for PFC packets. The MAC decodes the received PFC packet and disables the Transmit queue, with matching priorities, for a duration of received Pause time. 0: Receive Flow Control is disabled 1: Receive Flow Control is enabled
	94H	MAC_RxQ_Ctrl4	RW	[31:19]	Reserved		
				[18:17]	VFFQ	2'h0	VLAN Tag Filter Fail Packets Queue This field holds the Rx queue number to which the tagged packets failing the Destination or Source Address filter (and UFFQE/MFFQE not enabled) or failing the VLAN tag filter must be routed to. This field is valid only when the VFFQE bit is set.
				[16]	VFFQE	1'h0	VLAN Tag Filter Fail Packets Queuing Enable When this bit is set, the tagged packets which fail the Destination or Source address filter or fail the VLAN tag filter, are routed to the Rx Queue Number programmed in the VFFQ. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0: VLAN tag Filter Fail Packets Queuing is disabled 1: VLAN tag Filter Fail Packets Queuing is enabled
				[15:11]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10:9]	MFFQ	2'h0	Multicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Multicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the MFFQE bit is set.
				[8]	MFFQE	1'h0	Multicast Address Filter Fail Packets Queuing Enable. When this bit is set, the Multicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the MFFQ. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0: Multicast Address Filter Fail Packets Queuing is disabled 1: Multicast Address Filter Fail Packets Queuing is enabled
				[7:3]	Reserved		
				[2:1]	UFFQ	2'h0	Unicast Address Filter Fail Packets Queue. This field holds the Rx queue number to which the Unicast packets failing the Destination or Source Address filter are routed to. This field is valid only when the UFFQE bit is set.
				[0]	UFFQE	1'h0	Unicast Address Filter Fail Packets Queuing Enable. When this bit is set, the Unicast packets which fail the Destination or Source address filter is routed to the Rx Queue Number programmed in the UFFQ. This bit is valid only when the RA bit of the MAC_Packet_Filter register is set. 0: Unicast Address Filter Fail Packets Queuing is disabled 1: Unicast Address Filter Fail Packets Queuing is enabled
	A0H	MAC_RxQ_Ctrl0	RW	[31:8]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:6]	RXQ3EN	2'h0	Receive Queue 3 Enable This field is similar to the RXQ0EN field. 0: Queue not enabled 1: Reserved 2: Queue enabled for Generic 3: Reserved
				[5:4]	RXQ2EN	2'h0	Receive Queue 2 Enable This field is similar to the RXQ0EN field. 0: Queue not enabled 1: Reserved 2: Queue enabled for Generic 3: Reserved
				[3:2]	RXQ1EN	2'h0	Receive Queue 1 Enable This field is similar to the RXQ0EN field. 0: Queue not enabled 1: Reserved 2: Queue enabled for Generic 3: Reserved
				[1:0]	RXQ0EN	2'h0	Receive Queue 0 Enable This field indicates whether Rx Queue 0 is enabled. 0: Queue not enabled 1: Reserved 2: Queue enabled for Generic 3: Reserved
	A4H	MAC_RxQ_Ctrl1	RW	[31:27]	Reserved		

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				[26:24]	FPRQ	3'h0	Frame Preemption Residue Queue This field holds the Rx queue number to which the residual preemption frames must be forwarded. The Queue-0 is used as a default queue for express frames, so this field cannot be programmed to a value 0.
				[23:22]	TPQC	2'h0	Tagged PTP over Ethernet Packets Queuing Control. This field controls the routing of the VLAN Tagged PTPoE packets. 0: VLAN Tagged PTPoE packets are routed as generic VLAN Tagged packet (based on PSRQ for Generic enabled Rx Queues). 1: VLAN Tagged PTPoE packets are routed to Rx Queues specified by PTPQ field.
				[21]	TACPQE	1'h0	Tagged AV Control Packets Queuing Enable. When set, the MAC routes the received Tagged AV Control packets to the Rx queue specified by AVCPQ field. 0: Tagged AV Control Packets Queuing is disabled 1: Tagged AV Control Packets Queuing is enabled
				[20]	MCBCQEN	1'h0	Multicast and Broadcast Queue Enable This bit specifies that Multicast or Broadcast packets routing to the Rx Queue is enabled and the Multicast or Broadcast packets must be routed to Rx Queue specified in MCBCQ field. 0: Multicast and Broadcast Queue is disabled 1: Multicast and Broadcast Queue is enabled
				[19]	Reserved		

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				[18:16]	MCBCQ	3'h0	Multicast and Broadcast Queue This field specifies the Rx Queue onto which Multicast or Broadcast Packets are routed. 0: Receive Queue 0 1: Receive Queue 1 2: Receive Queue 2 3: Receive Queue 3 4: Receive Queue 4 5: Receive Queue 5 6: Receive Queue 6 7: Receive Queue 7
				[15]	Reserved		
				[14:12]	UPQ	3'h0	Untagged Packet Queue This field indicates the Rx Queue to which Untagged Packets are to be routed. 0: Receive Queue 0 1: Receive Queue 1 2: Receive Queue 2 3: Receive Queue 3 4: Receive Queue 4 5: Receive Queue 5 6: Receive Queue 6 7: Receive Queue 7
				[11:7]	Reserved		

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6:4]	PTPQ	3'h0	PTP Packets Queue This field specifies the Rx queue on which the PTP packets sent over the Ethernet payload (not over IPv4 or IPv6) are routed. 0: Receive Queue 0 1: Receive Queue 1 2: Receive Queue 2 3: Receive Queue 3 4: Receive Queue 4 5: Receive Queue 5 6: Receive Queue 6 7: Receive Queue 7
				[3]	Reserved		
				[2:0]	AVCPQ	3'h0	AV Untagged Control Packets Queue This field specifies the Receive queue on which the received AV tagged and untagged control packets are routed. The AV tagged (when TACPQE bit is set) and untagged control packets are routed to Receive queue specified by this field. 0: Receive Queue 0 1: Receive Queue 1 2: Receive Queue 2 3: Receive Queue 3 4: Receive Queue 4 5: Receive Queue 5 6: Receive Queue 6 7: Receive Queue 7

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	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	A8H	MAC_RxQ_Ctrl2	RW	[31:24]	PSRQ3	8'h0	Priorities Selected in the Receive Queue 3 This field decides the priorities assigned to Rx Queue 3. All packets with priorities that match the values set in this field are routed to Rx Queue 3. For example, if PSRQ3[6, 3] are set, packets with USP field equal to 3 or 6 are routed to Rx Queue 3. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.
				[23:16]	PSRQ2	8'h0	Priorities Selected in the Receive Queue 2 This field decides the priorities assigned to Rx Queue 2. All packets with priorities that match the values set in this field are routed to Rx Queue 2. For example, if PSRQ2[1, 0] are set, packets with USP field equal to 1 or 0 are routed to Rx Queue 2. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.
				[15:8]	PSRQ1	8'h0	Priorities Selected in the Receive Queue 1 This field decides the priorities assigned to Rx Queue 1. All packets with priorities that match the values set in this field are routed to Rx Queue 1. For example, if PSRQ1[4] is set, packets with USP field equal to 4 are routed to Rx Queue 1. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:0]	PSRQ0	8'h0	Priorities Selected in the Receive Queue 0 This field decides the priorities assigned to Rx Queue 0. All packets with priorities that match the values set in this field are routed to Rx Queue 0. For example, if PSRQ0[5] is set, packets with USP field equal to 5 are routed to Rx Queue 0. The software must ensure that the content of this field is mutually exclusive to the PSRQ fields for other queues, that is, the same priority is not mapped to multiple Rx queues.
	B0H	MAC_Interrupt_Status	RO	[31:21]	Reserved		
				[20]	MFRIS	1'h0	MMC FPE Receive Interrupt Status This bit is set high when an interrupt is generated. This bit is cleared when all bits in this interrupt register are cleared. 0: MMC FPE Receive Interrupt status not active 1: MMC FPE Receive Interrupt status active
				[19]	MFTIS	1'h0	MMC FPE Transmit Interrupt Status This bit is set high when an interrupt is generated in the MMC FPE Transmit Interrupt Register. This bit is cleared when all bits in this interrupt register are cleared. 0: MMC FPE Transmit Interrupt status not active 1: MMC FPE Transmit Interrupt status active
				[18]	MDIOIS	1'h0	MDIO Interrupt Status This bit indicates an interrupt event after the completion of MDIO operation. Access restriction applies. Self-set to 1 on internal event. 0: MDIO Interrupt status not active 1: MDIO Interrupt status active

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17]	FPEIS	1'h0	Frame Preemption Interrupt Status This bit indicates an interrupt event during the operation of Frame Preemption. To reset this bit, the application must clear the event that has caused the Interrupt. 0: Frame Preemption Interrupt status not active 1: Frame Preemption Interrupt status active
				[16:15]	Reserved		
				[14]	RXSTSIS	1'h0	Receive Status Interrupt This bit indicates the status of received packets. This bit is set when the RWT bit is set in the MAC_Rx_Tx_Status register. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1) in the MAC_Rx_Tx_Status register. 0: Receive Interrupt status not active 1: Receive Interrupt status active

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[13]	TXSTSIS	1'h0	Transmit Status Interrupt This bit indicates the status of transmitted packets. This bit is set when any of the following bits is set in the MAC_Rx_Tx_Status register: - Excessive Collision (EXCOL) - Late Collision (LCOL) - Excessive Deferral (EXDEF) - Loss of Carrier (LCARR) - No Carrier (NCARR) - Jabber Timeout (TJT) This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1) in the MAC_Rx_Tx_Status register. 0: Transmit Interrupt status not active 1: Transmit Interrupt status active
				[12]	TSIS	1'h0	Timestamp Interrupt Status This bit is set when any of the following conditions is true: The system time value is equal to or exceeds the value specified in the Target Time High and Low registers. There is an overflow in the Seconds register. The Target Time Error occurred, that is, programmed target time already elapsed. This bit is cleared when the corresponding interrupt source bit is read (or corresponding interrupt source bit is written to 1) . 0: Timestamp Interrupt status not active 1: Timestamp Interrupt status active

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11]	MMCRXIPIS	1'h0	MMC Receive Checksum Offload Interrupt Status This bit is set high when an MMC Receive Checksum Offload Interrupt is generated. This bit is cleared when all bits in the interrupt register are cleared. 0: MMC Receive Checksum Offload Interrupt status not active 1: MMC Receive Checksum Offload Interrupt status active
				[10]	MMCTXIS	1'h0	MMC Transmit Interrupt Status This bit is set high when an MMC Transmit Interrupt is generated. This bit is cleared when all bits in the interrupt register are cleared. 0: MMC Transmit Interrupt status not active 1: MMC Transmit Interrupt status active
				[9]	MMCRXIS	1'h0	MMC Receive Interrupt Status This bit is set high when an MMC Receive Interrupt is generated in the Register. This bit is cleared when all bits in thes interrupt register are cleared. 0: MMC Receive Interrupt status not active 1: MMC Receive Interrupt status active
				[8]	MMCIS	1'h0	MMC Interrupt Status This bit is set high when Bit 11, Bit 10, or Bit 9 is set high. This bit is cleared only when all these bits are low. 0: MMC Interrupt status not active 1: MMC Interrupt status active
				[7:4]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	PHYIS	1'h0	PHY Interrupt This bit is set when rising edge is detected on the phy_intr_i input. This bit is cleared when this register is read (or this bit is written to 1). 0: PHY Interrupt not detected 1: PHY Interrupt detected
				[2:1]	Reserved		
				[0]	RGSMIIIS	1'h0	RGMII Interrupt Status This bit is set because of any change in value of the Link Status of RGMII interface. 0: RGMII Interrupt Status is not active 1: RGMII Interrupt Status is active
	B4H	MAC_Interrupt_Enable	RW	[31:19]	Reserved		
				[18]	MDIOIE	1'h0	MDIO Interrupt Enable When this bit is set, it enables the assertion of the interrupt when MDIOIS field is set in the MAC_Interrupt_Status register. 0: MDIO Interrupt is disabled 1: MDIO Interrupt is enabled
				[17]	FPEIE	1'h0	Frame Preemption Interrupt Enable When this bit is set, it enables the assertion of the interrupt when FPEIS field is set in the MAC_Interrupt_Status register. 0: Frame Preemption Interrupt is disabled 1: Frame Preemption Interrupt is enabled
				[16:15]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[14]	RXSTSIE	1'h0	Receive Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RXSTSIS bit in the MAC_Interrupt_Status register. 0: Receive Status Interrupt is disabled 1: Receive Status Interrupt is enabled
				[13]	TXSTSIE	1'h0	Transmit Status Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TXSTSIS bit in the MAC_Interrupt_Status register. 0: Timestamp Status Interrupt is disabled 1: Timestamp Status Interrupt is enabled
				[12]	TSIE	1'h0	Timestamp Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of TSIS bit in MAC_Interrupt_Status register. 0: Timestamp Interrupt is disabled 1: Timestamp Interrupt is enabled
				[11:4]	Reserved		
				[3]	PHYIE	1'h0	PHY Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of PHYIS bit in MAC_Interrupt_Status register. 0: PHY Interrupt is disabled 1: PHY Interrupt is enabled
				[2:1]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	RGSMIIIE	1'h0	RGMII Interrupt Enable When this bit is set, it enables the assertion of the interrupt signal because of the setting of RGSMIIIS bit in MAC_Interrupt_Status register. 0: RGMII Interrupt is disabled 1: RGMII Interrupt is enabled
	B8H	MAC_Rx_Tx_Status	RO	[31:9]	Reserved		
				[8]	RWT	1'h0	Receive Watchdog Timeout This bit is set when a packet with length greater than 2,048 bytes is received (10, 240 bytes when Jumbo Packet mode is enabled) and the WD bit is reset in the MAC_Configuration register. This bit is set when a packet with length greater than 16,383 bytes is received and the WD bit is set in the MAC_Configuration register. Access restriction applies. Self-set to 1 on internal event. 0: No receive watchdog timeout 1: Receive watchdog timed out
				[7:6]	Reserved		
				[5]	EXCOL	1'h0	Excessive Collisions When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the transmission aborted after 16 successive collisions while attempting to transmit the current packet. If the DR bit is set in the MAC_Configuration register, this bit is set after the first collision and the packet transmission is aborted. Access restriction applies. Self-set to 1 on internal event. 0: No collision 1: Excessive collision is sensed

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	LCOL	1'h0	Late Collision When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the packet transmission aborted because a collision occurred after the collision window. This bit is not valid if the Underflow error occurs. Access restriction applies. Self-set to 1 on internal event. 0: No collision 1: Late collision is sensed
				[3]	EXDEF	1'h0	Excessive Deferral When the DTXSTS bit is set in the MTL_Operation_Mode register and the DC bit is set in the MAC_Configuration register, this bit indicates that the transmission ended because of excessive deferral of over 24,288 bit times (155,680 in 1000/2500 Mbps mode or when Jumbo packet is enabled). Access restriction applies. Self-set to 1 on internal event. 0: No Excessive deferral 1: Excessive deferral
				[2]	LCARR	1'h0	Loss of Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the loss of carrier occurred during packet transmission. This bit is valid only for packets transmitted without collision. Access restriction applies. Self-set to 1 on internal event. 0: Carrier is present 1: Loss of carrier

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	NCARR	1'h0	No Carrier When the DTXSTS bit is set in the MTL_Operation_Mode register, this bit indicates that the carrier signal from the PHY is not present at the end of preamble transmission. Access restriction applies. Self-set to 1 on internal event. 0: Carrier is present 1: No carrier
				[0]	TJT	1'h0	Transmit Jabber Timeout This bit indicates that the Transmit Jabber Timer expired which happens when the packet size exceeds 2,048 bytes (10,240 bytes when the Jumbo packet is enabled) and JD bit is reset in the MAC_Configuration register. This bit is set when the packet size exceeds 16,383 bytes and the JD bit is set in the MAC_Configuration register. Access restriction applies. Self-set to 1 on internal event. 0: No Transmit Jabber Timeout 1: Transmit Jabber Timeout occurred
	F8H	MAC_PHYIF_Control_Status	RO	[31:20]	Reserved		
			RO	[19]	LNKSTS	1'h0	Link Status This bit indicates whether the link is up (1'b1) or down (1'b0). 0: Link down 1: Link up
			RO	[18:17]	LNKSPEED	2'h0	Link Speed This bit indicates the current speed of the link. 0: 2.5 MHz 1: 25 MHz 2: 125 MHz 3: Reserved

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RO	[16]	LNKMOD	1'h0	Link Mode This bit indicates the current mode of operation of the link. 0: Half-duplex mode 1: Full-duplex mode
			RO	[15:2]	Reserved		
			RW	[1]	LUD	1'h0	Link Up or Down This bit indicates whether the link is up or down during transmission of configuration in the RGMII interface. 0: Link down 1: Link up
			RW	[0]	TC	1'h0	Transmit Configuration in RGMII When set, this bit enables the transmission of duplex mode, link speed, and link up or down information to the PHY in the RGMII port. 0: Disable Transmit Configuration in RGMII 1: Enable Transmit Configuration in RGMII
	11CH	MAC_HW_Feature0	RO	[31]	Reserved		
				[30:28]	ACTPHYSEL	3'h0	Active PHY Selected 0: Reserved 1: RGMII 2: Reserved 3: Reserved 4: RMII 5: Reserved 6: Reserved 7: Reserved

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27]	SAVLANINS	1'h1	Source Address or VLAN Insertion Enable 0: Source Address or VLAN Insertion Enable option is not selected 1: Source Address or VLAN Insertion Enable option is selected
				[26:25]	TSSTSSEL	2'h1	Timestamp System Time Source This bit indicates the source of the Timestamp system time. 0: Internal 1: External 2: Both 3: Reserved
				[24]	MACADR64SEL	1'h1	MAC Addresses 64-127 Selected 0: MAC Addresses 64-127 Select option is not selected 1: MAC Addresses 64-127 Select option is selected
				[23]	MACADR32SEL	1'h0	MAC Addresses 32-63 Selected 0: MAC Addresses 32-63 Select option is not selected 1: MAC Addresses 32-63 Select option is selected
				[22:18]	ADDMACADRSEL	5'h8	MAC Addresses 1-31 Selected 0: Additional 1-31 MAC Address Registers Enable option is not selected 1: Additional 1-31 MAC Address Registers Enable option is selected
				[17]	Reserved		
				[16]	RXCOESEL	1'h1	Receive Checksum Offload Enabled 0: Receive Checksum Offload Enable option is not selected 1: Receive Checksum Offload Enable option is selected
				[15]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[14]	TXCOESEL	1'h1	Transmit Checksum Offload Enabled 0: Transmit Checksum Offload Enable option is not selected 1: Transmit Checksum Offload Enable option is selected
				[13]	EEESEL	1'h0	Energy Efficient Ethernet Enabled 0: Energy Efficient Ethernet Enable option is not selected 1: Energy Efficient Ethernet Enable option is selected
				[12]	TSSEL	1'h1	IEEE 1588-2008 Timestamp Enabled 0: IEEE 1588-2008 Timestamp Enable option is not selected 1: IEEE 1588-2008 Timestamp Enable option is selected
				[11:10]	Reserved		
				[9]	ARPOFFSEL	1'h1	ARP Offload Enabled 0: ARP Offload Enable option is not selected 1: ARP Offload Enable option is selected
				[8]	MMCSEL	1'h1	RMON Module Enable 0: RMON Module Enable option is not selected 1: RMON Module Enable option is selected
				[7]	MGKSEL	1'h0	PMT Magic Packet Enable 0: PMT Magic Packet Enable option is not selected 1: PMT Magic Packet Enable option is selected
				[6]	RWKSEL	1'h0	PMT Remote Wake-up Packet Enable 0: PMT Remote Wake-up Packet Enable option is not selected 1: PMT Remote Wake-up Packet Enable option is selected
				[5]	SMASEL	1'h1	SMA (MDIO) Interface 0: SMA (MDIO) Interface not selected 1: SMA (MDIO) Interface selected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	VLHASH	1'h1	VLAN Hash Filter Selected 0: VLAN Hash Filter not selected 1: VLAN Hash Filter selected
				[3]	PCSSEL	1'h0	PCS Registers 0: No PCS Registers 1: PCS Registers
				[2]	HDSEL	1'h1	Half-duplex Support 0: No Half-duplex support 1: Half-duplex support
				[1]	GMIISEL	1'h1	1000 Mbps Support 0: No 1000 Mbps support 1: 1000 Mbps support
				[0]	MIISEL	1'h1	10 or 100 Mbps Support 0: No 10 or 100 Mbps support 1: 10 or 100 Mbps support
	120H	MAC_HW_Feature1	RO	[31]	Reserved		
				[30:27]	L3L4FNUM	4'h1	Total number of L3 or L4 Filters This field indicates the total number of L3 or L4 filters. 0: No L3 or L4 Filter 1: 1 L3 or L4 Filter 2: 2 L3 or L4 Filters 3: 3 L3 or L4 Filters 4: 4 L3 or L4 Filters 5: 5 L3 or L4 Filters 6: 6 L3 or L4 Filters 7: 7 L3 or L4 Filters 8: 8 L3 or L4 Filters
				[26]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[25:24]	HASHTBLSZ	2'h1	Hash Table Size This field indicates the size of the hash table. 0: No hash table 1: 64 2: 128 3: 256
				[23]	POUOST	1'h1	One Step for PTP over UDP/IP Feature Enable 0: One Step for PTP over UDP/IP Feature is not selected 1: One Step for PTP over UDP/IP Feature is selected
				[22]	Reserved		
				[21]	RAVSEL	1'h0	Rx Side Only AV Feature Enable 0: Rx Side Only AV Feature is not selected 1: Rx Side Only AV Feature is selected
				[20]	AVSEL	1'h1	AV Feature Enable 0: AV Feature is not selected 1: AV Feature is selected
				[19]	DBGMEMA	1'h1	DMA Debug Registers Enable 0: DMA Debug Registers option is not selected 1: DMA Debug Registers option is selected
				[18]	TSOEN	1'h1	TCP Segmentation Offload Enable 0: TCP Segmentation Offload Feature is not selected 1: TCP Segmentation Offload Feature is selected
				[17]	SPHEN	1'h1	Split Header Feature Enable 0: Split Header Feature is not selected 1: Split Header Feature is selected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[16]	DCBEN	1'h0	DCB Feature Enable 0: DCB Feature is not selected 1: DCB Feature is selected
				[15:14]	ADDR64	2'h0	Address Width. This field indicates the configured address width. 0: 32 1: 40 2: 48 3: Reserved
				[13]	ADVTHWORD	1'h1	IEEE 1588 High Word Register Enable 0: IEEE 1588 High Word Register option is not selected 1: IEEE 1588 High Word Register option is selected
				[12]	PTOEN	1'h1	PTP Offload Enable 0: PTP Offload feature is not selected 1: PTP Offload feature is selected
				[11]	OSTEN	1'h1	One-Step Timestamping Enable 0: One-Step Timestamping feature is not selected 1: One-Step Timestamping feature is selected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[10:6]	TXFIFOSIZE	5'h7	MTL Transmit FIFO Size This field contains the configured value of MTL Tx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(TXFIFO_SIZE) -7: 0: 128 bytes 1: 256 bytes 2: 512 bytes 3: 1024 bytes 4: 2048 bytes 5: 4096 bytes 6: 8192 bytes 7: 16384 bytes 8: 32 KB 9: 64 KB a: 128 KB b: Reserved
				[5]	SPRAM	1'h0	Single Port RAM Enable 0: Single Port RAM feature is not selected 1: Single Port RAM feature is selected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4:0]	RXFIFOSIZE	5'h7	MTL Receive FIFO Size This field contains the configured value of MTL Rx FIFO in bytes expressed as Log to base 2 minus 7, that is, Log2(RXFIFO_SIZE) -7. 0: 128 bytes 1: 256 bytes 2: 512 bytes 3: 1024 bytes 4: 2048 bytes 5: 4096 bytes 6: 8192 bytes 7: 16384 bytes 8: 32 KB 9: 64 KB a: 128 KB b: 256 KB c: Reserved
	124H	MAC_HW_Feature2	RO	[31]	Reserved		
				[30:28]	AUXSNAPNUM	3'h4	Number of Auxiliary Snapshot Inputs This field indicates the number of auxiliary snapshot inputs. 0: No auxiliary input 1: 1 auxiliary input 2: 2 auxiliary input 3: 3 auxiliary input 4: 4 auxiliary input 5: Reserved
				[27]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[26:24]	PPSOUTNUM	3'h4	Number of PPS Outputs This field indicates the number of PPS outputs. 0: No PPS output 1: 1 PPS output 2: 2 PPS output 3: 3 PPS output 4: 4 PPS output 5: Reserved
				[23:22]	Reserved		
				[21:18]	TXCHCNT	4'h3	Number of DMA Transmit Channels This field indicates the number of DMA Transmit channels. 0: 1 MTL Tx Channel 1: 2 MTL Tx Channels 2: 3 MTL Tx Channels 3: 4 MTL Tx Channels 4: 5 MTL Tx Channels 5: 6 MTL Tx Channels 6: 7 MTL Tx Channels 7: 8 MTL Tx Channels
				[17:16]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15:12]	RXCHCNT	4'h3	Number of DMA Receive Channels This field indicates the number of DMA Receive channels. 0: 1 MTL Rx Channel 1: 2 MTL Rx Channels 2: 3 MTL Rx Channels 3: 4 MTL Rx Channels 4: 5 MTL Rx Channels 5: 6 MTL Rx Channels 6: 7 MTL Rx Channels 7: 8 MTL Rx Channels
				[11:10]	Reserved		
				[9:6]	TXQCNT	4'h3	Number of MTL Transmit Queues This field indicates the number of MTL Transmit queues. 0: 1 MTL Tx Queue 1: 2 MTL Tx Queues 2: 3 MTL Tx Queues 3: 4 MTL Tx Queues 4: 5 MTL Tx Queues 5: 6 MTL Tx Queues 6: 7 MTL Tx Queues 7: 8 MTL Tx Queues
				[5:4]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3:0]	RXQCNT	4'h3	Number of MTL Receive Queues This field indicates the number of MTL Receive queues. 0: 1 MTL Rx Queue 1: 2 MTL Rx Queues 2: 3 MTL Rx Queues 3: 4 MTL Rx Queues 4: 5 MTL Rx Queues 5: 6 MTL Rx Queues 6: 7 MTL Rx Queues 7: 8 MTL Rx Queues
	128H	MAC_HW_Feature3	RO	[31:30]	Reserved		
				[29:28]	ASP	2'h3	Automotive Safety Package 0: No Safety features selected 1: Only "ECC protection for external memory" feature is selected 2 : All the Automotive Safety features are selected without the "Parity Port Enable for external interface" feature 3: All the Automotive Safety features are selected with the "Parity Port Enable for external interface" feature
				[27]	TBSSEL	1'h1	Time Based Scheduling Enable 0: Time Based Scheduling Enable feature is not selected 1: Time Based Scheduling Enable feature is selected
				[26]	FPESEL	1'h1	Frame Preemption Enable 0: Frame Preemption Enable feature is not selected 1: Frame Preemption Enable feature is selected
				[25:22]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[21:20]	ESTWID	2'h3	Width of the Time Interval field in the Gate Control List This field indicates the width of the Configured Time Interval Field. 0 : Width not configured 1: 16 2: 20 3: 24
				[19:17]	ESTDEP	3'h3	Depth of the Gate Control List This field indicates the depth of Gate Control list expressed as Log2(Depth of the Gate Control List)-5. 0: No Depth configured 1: 64 2: 128 3: 256 4: 512 5: 1024 6: Reserved
				[16]	ESTSEL	1'h1	Enhancements to Scheduling Traffic Enable 0: Enable Enhancements to Scheduling Traffic feature is not selected 1: Enable Enhancements to Scheduling Traffic feature is selected
				[15]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[14:13]	FRPES	2'h0	Flexible Receive Parser Table Entries size This field indicates the Max Number of Parser Entries supported by Flexible Receive Parser. 0: 64 Entries 1: 128 Entries 2: 256 Entries 3: Reserved
				[12:11]	FRPBS	2'h0	Flexible Receive Parser Buffer size This field indicates the supported Max Number of bytes of the packet data to be Parsed by Flexible Receive Parser. 0: 64 Bytes 1: 128 Bytes 2: 256 Bytes 3: Reserved
				[10]	FRPSEL	1'h0	Flexible Receive Parser Selected 0: Flexible Receive Parser feature is not selected 1: Flexible Receive Parser feature is selected
				[9]	PDUPSEL	1'h0	Broadcast/Multicast Packet Duplication 0: Broadcast/Multicast Packet Duplication feature is not selected 1: Broadcast/Multicast Packet Duplication feature is selected
				[8:6]	Reserved		
				[5]	DVLAN	1'h1	Double VLAN Tag Processing Selected 0: Double VLAN option is not selected 1: Double VLAN option is selected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[4]	CBTISEL	1'h0	Queue/Channel based VLAN tag insertion on Tx Enable 0: Enable Queue/Channel based VLAN tag insertion on Tx feature is not selected 1: Enable Queue/Channel based VLAN tag insertion on Tx feature is selected
				[3]	Reserved		
				[2:0]	NRVF	3'h1	Number of Extended VLAN Tag Filters Enabled This field indicates the Number of Extended VLAN Tag Filters selected. 0: No Extended Rx VLAN Filters 1: 4 Extended Rx VLAN Filters 2: 8 Extended Rx VLAN Filters 3: 16 Extended Rx VLAN Filters 4: 24 Extended Rx VLAN Filters 5: 32 Extended Rx VLAN Filters 6: Reserved
	200H	MAC_MDIO_Address	RW	[31:28]	Reserved		
				[27]	PSE	1'h0	Preamble Suppression Enable When this bit is set, the SMA suppresses the 32-bit preamble and transmits MDIO frames with only 1 preamble bit. 0: Preamble Suppression disabled 1: Preamble Suppression enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[26]	BTB	1'h0	Back to Back transactions When this bit is set and the NTC has value greater than 0, then the MAC informs the completion of a read or write command at the end of frame transfer (before the trailing clocks are transmitted). The software can thus initiate the next command which is executed immediately irrespective of the number trailing clocks generated for the previous frame. 0: Back to Back transactions disabled 1: Back to Back transactions enabled
				[25:21]	PA	5'h0	Physical Layer Address This field indicates which Clause 22 PHY devices (out of 32 devices) the MAC is accessing.
				[20:16]	RDA	5'h0	Register/Device Address These bits select the PHY register in selected Clause 22 PHY device.
				[15]	Reserved		
				[14:12]	NTC	3'h0	Number of Trailing Clocks This field controls the number of trailing clock cycles generated on gmii_mdc_o (MDC) after the end of transmission of MDIO frame. The valid values can be from 0 to 7. Programming the value to 3'h3 indicates that there are additional three clock cycles on the MDC line after the end of MDIO frame transfer.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[11:8]	CR	4'h0	CSR Clock Range The CSR Clock Range selection determines the frequency of the MDC clock according to the CSR clock frequency used in your design: 0000: CSR clock = 60-100 MHz; MDC clock = CSR clock/42 0001: CSR clock = 100-150 MHz; MDC clock = CSR clock/62 0010: CSR clock = 20-35 MHz; MDC clock = CSR clock/16 0011: CSR clock = 35-60 MHz; MDC clock = CSR clock/26 0100: CSR clock = 150-250 MHz; MDC clock = CSR clock/102 0101: CSR clock = 250-300 MHz; MDC clock = CSR clock/124 0110: CSR clock = 300-500 MHz; MDC clock = CSR clock/204 0111: CSR clock = 500-800 MHz; MDC clock = CSR clock/324 The suggested range of CSR clock frequency applicable for each value (when Bit[11] = 0) ensures that the MDC clock is approximately between 1.0 MHz to 2.5 MHz frequency range. When Bit[11] is set, you can achieve a higher frequency of the MDC clock than the frequency limit of 2.5 MHz (specified in the IEEE 802.3) and program a clock divider of lower value. For example, when CSR clock is of 100 MHz frequency and you program these bits as 1010, the resultant MDC clock is of 12.5 MHz which is above the range specified in IEEE 802.3. Program the following values only if the interfacing chips support faster MDC clocks: 1000: CSR clock/4

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
							1001: CSR clock/6 1010: CSR clock/8 1011: CSR clock/10 1100: CSR clock/12 1101: CSR clock/14 1110: CSR clock/16 1111: CSR clock/18
				[7:5]	Reserved		
				[4]	SKAP	1'h0	Skip Address Packet When this bit is set, the SMA does not send the address packets before read, write, or post-read increment address packets. This bit is valid only when C45E is set. 0: Skip Address Packet is disabled 1: Skip Address Packet is enabled
				[3]	GOC_1	1'h0	GMII Operation Command 1 This bit is higher bit of the operation command to the PHY, GOC_1 and GOC_O is encoded as follows: 00: Reserved 01: Write 10: Post Read Increment Address for Clause 45 PHY 11: Read When Clause 22 PHY is enabled, only Write and Read commands are valid. 0: GMII Operation Command 1 is disabled 1: GMII Operation Command 1 is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	GOC_0	1'h0	GMII Operation Command 0 This is the lower bit of the operation command to the PHY. When in SMA mode (MDIO master) this bit along with GOC_1 determines the operation to be performed to the PHY. 0: GMII Operation Command 0 is disabled 1: GMII Operation Command 0 is enabled
				[1]	C45E	1'h0	Clause 45 PHY Enable When this bit is set, Clause 45 capable PHY is connected to MDIO. When this bit is reset, Clause 22 capable PHY is connected to MDIO. 0: Clause 45 PHY is disabled 1: Clause 45 PHY is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	GB	1'h0	GMII Busy The application sets this bit to instruct the SMA to initiate a Read or Write access to the MDIO slave. The MAC clears this bit after the MDIO frame transfer is completed. Hence the software must not write or change any of the fields in MAC_MDIO_Address and MAC_MDIO_Data registers as long as this bit is set. For write transfers, the application must first write 16-bit data in the GDI field (and also RA field when C45E is set) in MAC_MDIO_Data register before setting this bit. When C45E is set, it should also write into the RA field of MAC_MDIO_Data register before initiating a read transfer. When a read transfer is completed (GB=0), the data read from the PHY register is valid in the GD field of the MAC_MDIO_Data register. **Note:** Even if the addressed PHY is not present, there is no change in the functionality of this bit. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: GMII Busy is disabled 1: GMII Busy is enabled
	204H	MAC_MDIO_Data	RW	[31:16]	RA	16'h0	Register Address This field is valid only when C45E is set. It contains the Register Address in the PHY to which the MDIO frame is intended for.

Ethernet MAC

BASE_ADDR: 0xA501_4000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[15:0]	GD	16'h0	GMII Data This field contains the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.
300H	MAC_Address0_High	RO	[31]	AE	1'h1	Address Enable This bit is always set to 1. 0: Invalid. This bit must be always set to 1 1: This bit is always set to 1
		RW	[30:18]	Reserved		
			[17:16]	DCS	2'h0	DMA Channel Select - If the PDC bit of MAC_Ext_Configuration register is set: This field contains the binary representation of the DMA Channel number to which an Rx packet whose DA matches the MAC Address0 content is routed. - If the PDC bit of MAC_Ext_Configuration register is set: This field contains the one-hot representation of one or more DMA Channel numbers to which an Rx packet whose DA matches the MAC Address0 content is routed.
			[15:0]	ADDRHI	16'hffff	MAC Address0[47:32] This field contains the upper 16 bits [47:32] of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.
304H	MAC_Address0_Low	RW	[31:0]	ADDRLO	32'hffffffff	MAC Address0[31:0] This field contains the lower 32 bits of the first 6-byte MAC address. The MAC uses this field for filtering the received packets and inserting the MAC address in the Transmit Flow Control (Pause) Packets.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	700H	MMC_Control	RW	[31:9]	Reserved		
				[8]	UCDBC	1'h0	Update MMC Counters for Dropped Broadcast Packets **Note:** The CNTRST bit has a higher priority than the CNTPRST bit. Therefore, when the software tries to set both bits in the same write cycle, all counters are cleared and the CNTPRST bit is not set. When set, the MAC updates all related MMC Counters for Broadcast packets that are dropped because of the setting of the DBF bit of MAC_Packet_Filter register. 0: Update MMC Counters for Dropped Broadcast Packets is disabled 1: Update MMC Counters for Dropped Broadcast Packets is enabled
				[7:6]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[5]	CNTPRSTLVL	1'h0	Full-Half Preset When this bit is low and the CNTPRST bit is set, all MMC counters get preset to almost-half value. All octet counters get preset to 0x7FFF_F800 (Half 2KBytes) and all packet-counters gets preset to 0x7FFF_FFF0 (Half 16). When this bit is high and the CNTPRST bit is set, all MMC counters get preset to almost-full value. All octet counters get preset to 0xFFFF_F800 (Full 2KBytes) and all packet-counters gets preset to 0xFFFF_FFF0 (Full 16). For 16-bit counters, the almost-half preset values are 0x7800 and 0x7FF0 for the respective octet and packet counters. Similarly, the almost-full preset values for the 16-bit counters are 0xF800 and 0xFFF0. 0: Full-Half Preset is disabled 1: Full-Half Preset is enabled
				[4]	CNTPRST	1'h0	Counters Preset When this bit is set, all counters are initialized or preset to almost full or almost half according to the CNTPRSTLVL bit. This bit is cleared automatically after 1 clock cycle. This bit, along with the CNTPRSTLVL bit, is useful for debugging and testing the assertion of interrupts because of MMC counter becoming half-full or full. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0: Counters Preset is disabled 1: Counters Preset is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	CNTFREEZ	1'h0	MMC Counter Freeze When this bit is set, it freezes all MMC counters to their current value. 0: MMC Counter Freeze is disabled 1: MMC Counter Freeze is enabled
				[2]	RSTONRD	1'h0	Reset on Read When this bit is set, the MMC counters are reset to zero after Read (self-clearing after reset). The counters are cleared when the least significant byte lane (Bits[7:0]) is read. 0: Reset on Read is disabled 1: Reset on Read is enabled
				[1]	CNTSTOPRO	1'h0	Counter Stop Rollover When this bit is set, the counter does not roll over to zero after reaching the maximum value. 0: Counter Stop Rollover is disabled 1: Counter Stop Rollover is enabled
				[0]	CNTRST	1'h0	Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. Access restriction applies. Self-cleared. Setting 0 clears. Setting 1 sets. 0: Counters are not reset 1: All counters are reset
	8ACH	MMC_Tx_Hold_Req_Cntr	RO	[31:0]	TXHRC	32'h0	Tx Hold Request Counter This field indicates count of number of a hold request is given to MAC.
	C00H	MTL_Operation_Mo	RW	[31:10]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
		de		[9]	CNTCLR	1'h0	Counters Reset When this bit is set, all counters are reset. This bit is cleared automatically after 1 clock cycle. If this bit is set along with CNT_PRESET bit, CNT_PRESET has precedence. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Counters are not reset 1: All counters are reset
				[8]	CNTPRST	1'h0	Counters Preset When this bit is set: - MTL_TxQ[0-7]_Underflow register is initialized/preset to 12'h7F0. - Missed Packet and Overflow Packet counters in MTL_RxQ[0-7]_Missed_Pack。 Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Counters Preset is disabled 1: Counters Preset is enabled
				[7]	Reserved		
				[6:5]	SCHALG	2'h0	Tx Scheduling Algorithm This field indicates the algorithm for Tx scheduling. 0: WRR algorithm 1: Reserved 2: Reserved 3: Strict priority algorithm
				[4:3]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	RAA	1'h0	Receive Arbitration Algorithm This field is used to select the arbitration algorithm for the Rx side. 0: Strict priority (SP) 1: Weighted Strict Priority (WSP)
				[1]	DTXSTS	1'h0	Drop Transmit Status When this bit is set, the Tx packet status received from the MAC is dropped in the MTL. 0: Drop Transmit Status is disabled 1: Drop Transmit Status is enabled
				[0]	Reserved		
	C20H	MTL_Interrupt_Status	RO	[31:19]	Reserved		
				[18]	ESTIS	1'h0	EST (TAS- 802.1Qbv) Interrupt Status This bit indicates an interrupt event during the operation of 802.1Qbv. 0: EST (TAS- 802.1Qbv) Interrupt status not detected 1: EST (TAS- 802.1Qbv) Interrupt status detected
				[17]	DBGIS	1'h0	Debug Interrupt status This bit indicates an interrupt event during the slave access. 0: Debug Interrupt status not detected 1: Debug Interrupt status detected
				[16:4]	Reserved		
				[3]	Q3IS	1'h0	Queue 3 Interrupt status This bit indicates that there is an interrupt from Queue 3. 0: Queue 3 Interrupt status not detected 1: Queue 3 Interrupt status detected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	Q2IS	1'h0	Queue 2 Interrupt status This bit indicates that there is an interrupt from Queue 2. 0: Queue 2 Interrupt status not detected 1: Queue 2 Interrupt status detected
				[1]	Q1IS	1'h0	Queue 1 Interrupt status This bit indicates that there is an interrupt from Queue 1. 0: Queue 1 Interrupt status not detected 1: Queue 1 Interrupt status detected
				[0]	Q0IS	1'h0	Queue 0 Interrupt status This bit indicates that there is an interrupt from Queue 0. 0: Queue 0 Interrupt status not detected 1: Queue 0 Interrupt status detected
	C30H	MTL_RxQ_DMA_Map0	RW	[31:29]	Reserved		
				[28]	Q3DDMACH	1'h0	Queue 3 Enabled for Dynamic (per packet) DMA Channel Selection 0: Queue 3 disabled for DA-based DMA Channel Selection 1: Queue 3 enabled for DA-based DMA Channel Selection
				[27:26]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[25:24]	Q3MDMACH	2'h0	Queue 3 Mapped to DMA Channel This field controls the routing of the received packet in Queue 3 to the DMA channel. 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q3DDMACH field is reset. **Note:** The width of this field depends on the number of RX DMA channels and not all the values may be valid in some configurations. For example, if the number of RX DMA channels selected is 2, only 000 and 001 are valid, the others are reserved.
				[23:21]	Reserved		
				[20]	Q2DDMACH	1'h0	Queue 2 Enabled for DA-based DMA Channel Selection 0: Queue 2 disabled for DA-based DMA Channel Selection 1: Queue 2 enabled for DA-based DMA Channel Selection
				[19:18]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17:16]	Q2MDMACH	2'h0	Queue 2 Mapped to DMA Channel This field controls the routing of the received packet in Queue 2 to the DMA channel. 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q2DDMACH field is reset.
				[15:13]	Reserved		
				[12]	Q1DDMACH	1'h0	Queue 1 Enabled for DA-based DMA Channel Selection 0: Queue 1 disabled for DA-based DMA Channel Selection 1: Queue 1 enabled for DA-based DMA Channel Selection
				[11:10]	Reserved		
				[9:8]	Q1MDMACH	2'h0	Queue 1 Mapped to DMA Channel This field controls the routing of the received packet in Queue 1 to the DMA channel. 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q1DDMACH field is reset.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7:5]	Reserved		
				[4]	Q0DDMACH	1'h0	Queue 0 Enabled for DA-based DMA Channel Selection 0: Queue 0 disabled for DA-based DMA Channel Selection 1: Queue 0 enabled for DA-based DMA Channel Selection
				[3:2]	Reserved		
				[1:0]	Q0MDMACH	2'h0	Queue 0 Mapped to DMA Channel This field controls the routing of the packet received in Queue 0 to the DMA channel: 000: DMA Channel 0 001: DMA Channel 1 010: DMA Channel 2 011: DMA Channel 3 100: DMA Channel 4 101: DMA Channel 5 110: DMA Channel 6 111: DMA Channel 7 This field is valid when the Q0DDMACH field is reset.
	D00H	MTL_TxQ0_Operation_Mode	RW	[31:22]	Reserved		
				[21:16]	TQS	6'h0	Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The TQS field is read-write only if the number of Tx Queues more than one, the reset value is 0x0 and indicates size of 256 bytes. When the number of Tx Queues is one, the field is read-only and the configured TX FIFO size in blocks of 256 bytes is reflected in the reset value.
				[15:7]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6:4]	TTC	3'h0	Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. 0: 32 1: 64 2: 96 3: 128 4: 192 5: 256 6: 384 7: 512
				[3:2]	TXQEN	2'h0	Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Reserved 2'b10: Enabled 2'b11: Reserved **Note:** In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0: Disabled 1: Reserved 2: Enabled 3: Reserved

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	TSF	1'h0	Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0: Transmit Store and Forward is disabled 1: Transmit Store and Forward is enabled
				[0]	FTQ	1'h0	Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. **Note:** The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Flush Transmit Queue is disabled 1: Flush Transmit Queue is enabled
	D18H	MTL_TxQ0_Quantum_Weight	RW	[31:21]	Reserved		
				[20:0]	ISCQW	21'h0	Quantum or Weights This field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero.
	D2CH	MTL_Q0_Interrupt_C	RW	[31:25]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000					
Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	ontrol_Status		[24]	RXOIE	1'h0	Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. 0: Receive Queue Overflow Interrupt is disabled 1: Receive Queue Overflow Interrupt is enabled
			[23:17]	Reserved		
			[16]	RXOVFIS	1'h0	Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Receive Queue Overflow Interrupt Status not detected 1: Receive Queue Overflow Interrupt Status detected
			[15:10]	Reserved		
			[9]	ABPSIE	1'h0	Average Bits Per Slot Interrupt Enable When this bit is set, the Average Bits Per Slot interrupt is enabled. 0: Average Bits Per Slot Interrupt is disabled 1: Average Bits Per Slot Interrupt is enabled
			[8]	TXUIE	1'h0	Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. 0: Transmit Queue Underflow Interrupt Status is disabled 1: Transmit Queue Underflow Interrupt Status is enabled
			[7:2]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	ABPSIS	1'h0	Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Average Bits Per Slot Interrupt Status not detected 1: Average Bits Per Slot Interrupt Status detected
				[0]	TXUNFIS	1'h0	Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Transmit Queue Underflow Interrupt Status not detected 1: Transmit Queue Underflow Interrupt Status detected
	D30H	MTL_RxQ0_Operation_Mode	RW	[31:26]	Reserved		
				[25:20]	RQS	6'h0	Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
				[19]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[18:14]	RFD	5'h0	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB ... 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
				[13]	Reserved		
				[12:8]	RFA	5’h0	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	EHFC	1'h0	Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. 0: Hardware Flow Control is disabled 1: Hardware Flow Control is enabled
				[6]	DIS_TCP_EF	1'h0	Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. 0: Dropping of TCP/IP Checksum Error Packets is enabled 1: Dropping of TCP/IP Checksum Error Packets is disabled
				[5]	RSF	1'h0	Receive Queue Store and Forward When this bit is set, the Ethernet MAC module reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. 0: Receive Queue Store and Forward is disabled 1: Receive Queue Store and Forward is enabled
				[4]	FEP	1'h0	Forward Error Packets When this bit is reset, the Rx queue drops packets with error status (CRC error, GMII_ER, watchdog timeout, or overflow). However, if the start byte (write) pointer of a packet is already transferred to the read controller side (in Threshold mode), the packet is not dropped. 0: Forward Error Packets is disabled 1: Forward Error Packets is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	FUP	1'h0	Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. 0: Forward Undersized Good Packets is disabled 1: Forward Undersized Good Packets is enabled
				[2]	Reserved		
				[1:0]	RTC	2'h0	Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. 0: 64 1: 32 2: 96 3: 128
	D3CH	MTL_RxQ0_Control	RW	[31:4]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	RXQ_FRM_ARBIT	1'h0	Receive Queue Packet Arbitration When this bit is set, the Ethernet OoS module drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue: PBL amount of data (indicated by ari_qN_pbl_i[]) or -Complete data of a packet. The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet MAC module drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0: Receive Queue Packet Arbitration is disabled 1: Receive Queue Packet Arbitration is enabled
				[2:0]	RXQ_WEGT	3'h0	Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle.
	(40H*i)+D00H	MTL_TxQ(i)_Operation_Mode (for i = 1; i <= 3)	RW	[31:22]	Reserved		
				[21:16]	TQS	6'h0	Transmit Queue Size This field indicates the size of the allocated Transmit queues in blocks of 256 bytes. The width of this field depends on the Tx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
				[15:7]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[6:4]	TTC	3'h0	Transmit Threshold Control These bits control the threshold level of the MTL Tx Queue. The transmission starts when the packet size within the MTL Tx Queue is larger than the threshold. In addition, full packets with length less than the threshold are also transmitted. These bits are used only when the TSF bit is reset. 0: 32 1: 64 2: 96 3: 128 4: 192 5: 256 6: 384 7: 512
				[3:2]	TXQEN	2'h0	Transmit Queue Enable This field is used to enable/disable the transmit queue 0. 2'b00: Not enabled 2'b01: Reserved 2'b10: Enabled 2'b11: Reserved **Note:** In multiple Tx queues configuration, all the queues are disabled by default. Enable the Tx queue by programming this field. 0: Not enabled 1: Reserved 2: Enabled 3: Reserved

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	TSF	1'h0	Transmit Store and Forward When this bit is set, the transmission starts when a full packet resides in the MTL Tx queue. When this bit is set, the TTC values specified in Bits[6:4] of this register are ignored. This bit should be changed only when the transmission is stopped. 0: Transmit Store and Forward is disabled 1: Transmit Store and Forward is enabled
				[0]	FTQ	1'h0	Flush Transmit Queue When this bit is set, the Tx queue controller logic is reset to its default values. Therefore, all the data in the Tx queue is lost or flushed. Until this bit is reset, you should not write to the MTL_TxQ1_Operation_Mode register. **Note:** The flush operation is complete only when the Tx queue is empty and the application has accepted the pending Tx Status of all transmitted packets. To complete this flush operation, the PHY Tx clock (clk_tx_i) should be active. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Flush Transmit Queue is disabled 1: Flush Transmit Queue is enabled
	(40H*i)+D1	MTL_TxQ(i)_Quantu	RW	[31:21]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	8H	m_Weight (for i = 1; i <= 3)		[20:0]	ISCQW	21'h0	idleSlopeCredit, Quantum or Weights This field contains the weight for this queue. The maximum value is 0x64. Bits [20:7] must be written to zero. **Note :** This field in respective per queue register must be programmed to some non-zero value when multiple queues are enabled or single queue other than Q0 is enabled. In general, when WRR algorithm is selected a non-zero value must be programmed on both Receive and Transmit. In Receive, the register is MTL_Operation_Mode register. The weights programmed do not correspond to the number of packets but the fraction of bandwidth or time allocated for particular queue w.r.t. total BW or time.
	(40H*i)+D2CH	MTL_Q(i)_Interrupt_Control_Status) (for i = 1; i <= 3)	RW	[31:25]	Reserved		
				[24]	RXOIE	1'h0	Receive Queue Overflow Interrupt Enable When this bit is set, the Receive Queue Overflow interrupt is enabled. 0: Receive Queue Overflow Interrupt is disabled 1: Receive Queue Overflow Interrupt is enabled
				[23:17]	Reserved		
				[16]	RXOVFIS	1'h0	Receive Queue Overflow Interrupt Status This bit indicates that the Receive Queue had an overflow while receiving the packet. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Receive Queue Overflow Interrupt Status not detected 1: Receive Queue Overflow Interrupt Status detected
				[15:10]	Reserved		

Ethernet MAC

BASE_ADDR: 0xA501_4000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			[9]	ABPSIE	1'h0	Average Bits Per Slot Interrupt Enable When this bit is set, the MAC asserts the sbd_intr_o or mci_intr_o interrupt when the average bits per slot status is updated. 0: Average Bits Per Slot Interrupt is disabled 1: Average Bits Per Slot Interrupt is enabled
			[8]	TXUIE	1'h0	Transmit Queue Underflow Interrupt Enable When this bit is set, the Transmit Queue Underflow interrupt is enabled. 0: Transmit Queue Underflow Interrupt Status is disabled 1: Transmit Queue Underflow Interrupt Status is enabled
			[7:2]	Reserved		
			[1]	ABPSIS	1'h0	Average Bits Per Slot Interrupt Status When set, this bit indicates that the MAC has updated the ABS value. This bit is cleared when the application writes 1 to this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Average Bits Per Slot Interrupt Status not detected 1: Average Bits Per Slot Interrupt Status detected
			[0]	TXUNFIS	1'h0	Transmit Queue Underflow Interrupt Status This bit indicates that the Transmit Queue had an underflow while transmitting the packet. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Transmit Queue Underflow Interrupt Status not detected 1: Transmit Queue Underflow Interrupt Status detected
(40H*i)+D3	MTL_RxQ(i)_Operati	RW	[31:26]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	0H	on_Mode (for i = 1; i <= 3)		[25:20]	RQS	6'h0	Receive Queue Size This field indicates the size of the allocated Receive queues in blocks of 256 bytes. The width of this field depends on the Rx memory size selected in your configuration. For example, if the memory size is 2048, the width of this field is 3 bits: LOG2(2048/256) = LOG2(8) = 3 bits
				[19]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[18:14]	RFD	5'h0	Threshold for Deactivating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is de-asserted after activation: 0: Full minus 1 KB, that is, FULL 1 KB 1: Full minus 1.5 KB, that is, FULL 1.5 KB 2: Full minus 2 KB, that is, FULL 2 KB 3: Full minus 2.5 KB, that is, FULL 2.5 KB .. 62: Full minus 32 KB, that is, FULL 32 KB 63: Full minus 32.5 KB, that is, FULL 32.5 KB The de-assertion is effective only after flow control is asserted. The value must be programmed in such a way to make sure that the threshold is a positive number. When the EHFC is set high, these values are applicable only when the Rx queue size determined by the RQS field of this register, is equal to or greater than 4 KB. For a given queue size, the values ranges between 0 and the encoding for FULL minus (QSIZE - 0.5 KB) and all other values are illegal. Here the term FULL and QSIZE refers to the queue size determined by the RQS field of this register. The width of this field depends on RX FIFO size selected during the configuration. Remaining bits are reserved and read only.
				[13]	Reserved		
				[12:8]	RFA	5'h0	Threshold for Activating Flow Control (in half-duplex and full-duplex modes) These bits control the threshold (fill-level of Rx queue) at which the flow control is activated.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	EHFC	1'h0	Enable Hardware Flow Control When this bit is set, the flow control signal operation, based on the fill-level of Rx queue, is enabled. 0: Hardware Flow Control is disabled 1: Hardware Flow Control is enabled
				[6]	DIS_TCP_EF	1'h0	Disable Dropping of TCP/IP Checksum Error Packets When this bit is set, the MAC does not drop the packets which only have the errors detected by the Receive Checksum Offload engine. Such packets have errors only in the encapsulated payload. There are no errors (including FCS error) in the Ethernet packet received by the MAC. 0: Dropping of TCP/IP Checksum Error Packets is enabled 1: Dropping of TCP/IP Checksum Error Packets is disabled
				[5]	RSF	1'h0	Receive Queue Store and Forward When this bit is set, the Ethernet MAC module reads a packet from the Rx queue only after the complete packet has been written to it, ignoring the RTC field of this register. 0: Receive Queue Store and Forward is disabled 1: Receive Queue Store and Forward is enabled
				[4]	FEP	1'h0	Forward Error Packets When this bit is set, all packets except the runt error packets are forwarded to the application or DMA. If the RSF bit is set and the Rx queue overflows when a partial packet is written, the packet is dropped irrespective of the setting of this bit. However, if the RSF bit is reset and the Rx queue overflows when a partial packet is written, a partial packet may be forwarded to the application or DMA. 0: Forward Error Packets is disabled 1: Forward Error Packets is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[3]	FUP	1'h0	Forward Undersized Good Packets When this bit is set, the Rx queue forwards the undersized good packets (packets with no error and length less than 64 bytes), including pad-bytes and CRC. 0: Forward Undersized Good Packets is disabled 1: Forward Undersized Good Packets is enabled
				[2]	Reserved		
				[1:0]	RTC	2'h0	Receive Queue Threshold Control These bits control the threshold level of the MTL Rx queue (in bytes): The received packet is transferred to the application or DMA when the packet size within the MTL Rx queue is larger than the threshold. In addition, full packets with length less than the threshold are automatically transferred. This field is valid only when the RSF bit is zero. 0: 64 1: 32 2: 96 3: 128
	(40H*i)+D3	MTL_RxQ(i)_Control	RW	[31:4]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	CH	(for i = 1; i <= 3)		[3]	RXQ_FRM_ARBIT	1'h0	Receive Queue Packet Arbitration When this bit is set, the Ethernet MAC module drives the packet data to the ARI interface such that the entire packet data of currently-selected queue is transmitted before switching to other queue. The status and the timestamp are not a part of the PBL data. Therefore, the Ethernet MAC module drives the complete status (including timestamp status) during first PBL request for the packet (in store-and-forward mode) or the last PBL request for the packet (in Threshold mode). 0: Receive Queue Packet Arbitration is disabled 1: Receive Queue Packet Arbitration is enabled
				[2:0]	RXQ_WEGT	3'h0	Receive Queue Weight This field indicates the weight assigned to the Rx Queue 0. The weight is used as the number of continuous PBL or packets requests (depending on the RXQ_FRM_ARBIT) allocated to the queue in one arbitration cycle.
	1000H	DMA_Mode	RW	[31:18]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[17:16]	INTM	2'h0	Interrupt Mode This field defines the interrupt mode of Ethernet MAC module. The behavior of the following outputs changes depending on the following settings: -Transmit Per Channel Interrupt -Receive Per Channel Interrupt -Common Interrupt It also changes the behavior of the RI/TI bits in the DMA_CH0_Status. 0: MODE0 1: MODE1 2: MODE2 3: Reserved
				[15:11]	Reserved		
				[10]	SCSW	1'h0	Horizon Robotics Reserved This field is reserved for Horizon Robotics Internal use, and must be set to 0.
				[9]	ARBC	1'h0	Reserved.
				[8]	DSPW	1'h0	Descriptor Posted Write When this bit is set to 0, the descriptor writes are always non-posted. 0: Descriptor Posted Write is disabled 1: Descriptor Posted Write is enabled
				[7:1]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[0]	SWR	1'h0	Software Reset When this bit is set, the MAC and the DMA controller reset the logic and all internal registers of the DMA, MTL, and MAC. This bit is automatically cleared after the reset operation is complete in all Ethernet MAC module clock domains. Before reprogramming any Ethernet MAC module register, a value of zero should be read in this bit. This bit must be read at least 4 CSR clock cycles after it is written to 1. **Note:** It is essential that all PHY inputs clocks (applicable for the selected PHY interface) are present for software reset completion. The time to complete the software reset operation depends on the frequency of the slowest active clock. Access restriction applies. Setting 1 sets. Self-cleared. Setting 0 has no effect. 0: Software Reset is disabled 1: Software Reset is enabled
	1004H	DMA_SysBus_Mode	RW	[31]	EN_LPI	1'h0	Enable Low Power Interface (LPI) When set to 1, this bit enables the LPI mode and accepts the LPI request from the AXI System Clock controller. 0: Low Power Interface (LPI) is disabled 1: Low Power Interface (LPI) is enabled
				[30:28]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[27:24]	WR_OSR_LMT	4'h1	AXI Maximum Write Outstanding Request Limit This value limits the maximum outstanding request on the AXI write interface. Maximum outstanding requests = WR_OSR_LMT + 1 Bit[26] is reserved if Ethernet MAC module_AXI_MAX-_WR_REQ = 4 Bit[27] is reserved if Ethernet MAC module_AXI_MAX-_WR_REQ!= 16
				[23:20]	Reserved		
				[19:16]	RD_OSR_LMT	4'h0	AXI Maximum Read Outstanding Request Limit This value limits the maximum outstanding request on the AXI read interface. Maximum outstanding requests = RD_OSR_LMT + 1 Bit[18] is reserved if parameter Ethernet MAC module_AXI_-MAX_RD_REQ = 4 Bit[19] is reserved if parameter Ethernet MAC module_AXI_-MAX_RD_REQ!= 16
				[15:14]	Reserved		
				[13]	ONEKBBE	1'h0	1 KB Boundary Crossing Enable for the EMAC-AXI Master When set, the burst transfers do not cross 1 KB boundary. When reset, the burst transfers do not cross 4 KB boundary. 0: 1 KB Boundary Crossing for the EMAC-AXI Master Beats is disabled 1: 1 KB Boundary Crossing for the EMAC-AXI Master Beats is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	AAL	1'h0	Address-Aligned Beats When this bit is set to 1, the EMAC-AXI or EMAC-AHB master performs address-aligned burst transfers on Read and Write channels. 0: Address-Aligned Beats is disabled 1: Address-Aligned Beats is enabled
				[11]	Reserved		
				[10]	AALE	1'h0	Automatic AXI LPI enable When set to 1, enables the AXI master to enter into LPI state when there is no activity in the Ethernet MAC module in the AXI LPI Entry Interval. 0: Automatic AXI LPI is disabled 1: Automatic AXI LPI is enabled
				[9:4]	Reserved		
				[3]	BLEN16	1'h0	AXI Burst Length 16 When this bit is set to 1 or the FB bit is set to 0, the EMAC-AXI master can select a burst length of 16 on the AXI interface. 0: No effect 1: AXI Burst Length 16
				[2]	BLEN8	1'h0	AXI Burst Length 8 When this bit is set to 1 or the FB bit is set to 0, the EMAC-AXI master can select a burst length of 8 on the AXI interface. 0: No effect 1: AXI Burst Length 8

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[1]	BLEN4	1'h0	AXI Burst Length 4 When this bit is set to 1 or the FB bit is set to 0, the EMAC-AXI master can select a burst length of 4 on the AXI interface. 0: No effect 1: AXI Burst Length 4
				[0]	FB	1'h0	Fixed Burst Length When this bit is set to 1, the EMAC-AXI master initiates burst transfers of specified lengths as given below. Burst transfers of fixed burst lengths as indicated by the BLEN16, BLEN8, or BLEN4 field 0: Fixed Burst Length is disabled 1: Fixed Burst Length is enabled
	1008H	DMA_Interrupt_Status	RO	[31:18]	Reserved		
				[17]	MACIS	1'h0	MAC Interrupt Status This bit indicates an interrupt event in the MAC. 0: MAC Interrupt Status not detected 1: MAC Interrupt Status detected
				[16]	MTLIS	1'h0	MTL Interrupt Status This bit indicates an interrupt event in the MTL. 0: MTL Interrupt Status not detected 1: MTL Interrupt Status detected
				[15:4]	Reserved		
				[3]	DC3IS	1'h0	DMA Channel 3 Interrupt Status This bit indicates an interrupt event in DMA Channel 3. 0: DMA Channel 3 Interrupt Status not detected 1: DMA Channel 3 Interrupt Status detected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2]	DC2IS	1'h0	DMA Channel 2 Interrupt Status This bit indicates an interrupt event in DMA Channel 2. 0: DMA Channel 2 Interrupt Status not detected 1: DMA Channel 2 Interrupt Status detected
				[1]	DC1IS	1'h0	DMA Channel 1 Interrupt Status This bit indicates an interrupt event in DMA Channel 1. 0: DMA Channel 1 Interrupt Status not detected 1: DMA Channel 1 Interrupt Status detected
				[0]	DC0IS	1'h0	DMA Channel 0 Interrupt Status This bit indicates an interrupt event in DMA Channel 0. 0: DMA Channel 0 Interrupt Status not detected 1: DMA Channel 0 Interrupt Status detected
	(80H*i)+1100H	DMA_CH(i)_Control (for i = 0; i <= 3)	RW	[31:25]	Reserved		
				[24]	SPH	1'h0	Split Headers When this bit is set, the DMA splits the header and payload in the Receive path. The DMA writes the header to the Buffer Address1 of RDES0. The DMA writes the payload to the buffer to which the Buffer Address2 is pointing. The software must ensure that the header fits into the Receive buffers. If the header length exceeds the receive buffer size, the DMA does not split the header and payload. 0: Split Headers feature is disabled 1: Split Headers feature is enabled
				[23:21]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[20:18]	DSL	3'h0	Descriptor Skip Length This bit specifies the Word, Dword, or Lword number (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors. The address skipping starts from the end of the current descriptor to the start of the next descriptor. When the DSL value is equal to zero, the DMA takes the descriptor table as contiguous.
				[17]	Reserved		
				[16]	PBLx8	1'h0	8xPBL mode When this bit is set, the PBL value programmed in Bits[21:16] in DMA_CH0_Tx_Control and Bits[21:16] in DMA_CH0_Rx_Control is multiplied by eight times. 0: 8xPBL mode is disabled 1: 8xPBL mode is enabled
				[15:14]	Reserved		
				[13:0]	MSS	14'h0	Maximum Segment Size This field specifies the maximum segment size that should be used while segmenting the packet. This field is valid only if the TSE bit of DMA_CH0_Tx_Control register is set. The value programmed in this field must be more than the configured Datawidth in bytes. It is recommended to use a MSS value of 64 bytes or more. This bit is valid only for the DMA_CH0_Control register. For the DMA_CH1/2/3_Control register, this bit is reserved.
	(80H*i)+11	DMA_CH(i)_Tx_Cont	RW	[31:29]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	04H	rol (for i = 0; i <= 3)		[28]	EDSE	1'h0	Enhanced Descriptor Enable When this bit is set, the corresponding channel uses Enhanced Descriptors that are 32 Bytes for both Normal and Context Descriptors. When reset, the corresponding channel uses the descriptors that are 16 Bytes. 0: Enhanced Descriptor is disabled 1: Enhanced Descriptor is enabled
				[27:22]	Reserved		
				[21:16]	TxPBL	6'h0	Transmit Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. **Note:** The maximum value of TxPBL must be less than or equal to half the Tx Queue size (TQS field of MTL_TxQ[i]_Operation_Mode register) in terms of beats. This is required so that the Tx Queue has space to store at least another Tx PBL width of data while the MTL Tx Queue Controller is transferring data to MAC.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[15]	IPBL	1'h0	Ignore PBL Requirement When this bit is set, the DMA does not check for PBL number of locations in the MTL before initiating a transfer. If space is not available, the MTL may use handshaking to slow the DMA. **Note:** This bit/mode must not be used when multiple Transmit DMA Channels are enabled as it may block other Transmit and Receive DMA Channels from accessing the Read Data Channel of AXI bus until space is available in Transmit Queue for current transfer. 0: Ignore PBL Requirement is disabled 1: Ignore PBL Requirement is enabled
				[14:13]	TSE_MODE	2'h0	TSE Mode 0: TSO/USO (segmentation functionality is enabled) 1: UFO with Checksum (UDP Fragmentation over IPv4 with Checksum) 2: UFO without Checksum (UDP Fragmentation over IPv4 without Checksum) 3: Reserved
				[12]	TSE	1'h0	TCP Segmentation Enabled When this bit is set, the DMA performs the TCP segmentation or UDP Segmentation/Fragmentation for packets in this channel. The TCP segmentation or UDP packet's segmentation/Fragmentation is done only for those packets for which the TSE bit (TDES0[19]) is set in the Tx Normal descriptor. When this bit is set, the TxPBL value must be greater than 4. 0: TCP Segmentation is disabled 1: TCP Segmentation is enabled

Ethernet MAC

BASE_ADDR: 0xA501_4000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
			[11:5]	Reserved		
			[4]	OSF	1'h0	Operate on Second Packet When this bit is set, it instructs the DMA to process the second packet of the Transmit data even before the status for the first packet is obtained. 0: Operate on Second Packet disabled 1: Operate on Second Packet enabled
			[3:1]	Reserved		
			[0]	ST	1'h0	Start or Stop Transmission Command When this bit is set, transmission is placed in the Running state. When this bit is reset, the transmission process is placed in the Stopped state after completing the transmission of the current packet. The Next Descriptor position in the Transmit list is saved, and it becomes the current position when the transmission is restarted. To change the list address, you need to program DMA_CH0_TxDesc_List_Address register with a new value when this bit is reset. The new value is considered when this bit is set again. The stop transmission command is effective only when the transmission of the current packet is complete or the transmission is in the Suspended state. 0: Stop Transmission Command 1: Start Transmission Command
(80H*i)+1108H	DMA_CH(i)_Rx_Control (for i = 0; i <= 3)	RW	[31]	RPF	1'h0	Rx Packet Flush When this bit is set to 1, then the Ethernet MAC module automatically flushes the packet from the Rx Queues destined to this DMA Rx Channel, when it is stopped. 0: Rx Packet Flush is disabled 1: Rx Packet Flush is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[30:22]	Reserved		
				[21:16]	RxPBL	6'h0	Receive Programmable Burst Length These bits indicate the maximum number of beats to be transferred in one DMA block data transfer. The DMA always attempts max burst as specified in PBL each time it starts a burst transfer on the application bus. You can program PBL with any of the following 1, 2, 4, 8, 16, or 32. Any other value results in undefined behavior. **Note:** The maximum value of RxPBL must be less than or equal to half the Rx Queue size (RQS field of MTL_RxQ[i]_Operation_Mode register) in terms of beats. This is required so that the Rx Queue has space to store at least another Rx PBL width of data while the Rx DMA is transferring a block of data.
				[15]	Reserved		
				[14:3]	RBSZ_13_y	12'h0	Receive Buffer size High RBSZ[13:0] is split into two fields higher RBSZ_13_y and lower RBSZ_x_0. The RBSZ[13:0] field indicates the size of the Rx buffers specified in bytes. The maximum buffer size is limited to 16K bytes. The buffer size is applicable to payload buffers when split headers are enabled. **Note:** The buffer size must be a multiple of 4. This is required even if the value of buffer address pointer is not aligned to data bus width. The RBSZ_13_y indicates the buffer size in terms of locations (with the width same as bus-width).

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[2:1]	RBSZ_x_0	2'h0	Receive Buffer size Low RBSZ[13:0] is split into two fields RBSZ_13_y and RBSZ_x_0. The RBSZ_x_0 is the lower field whose width is based on data bus width of the configuration. This field is read-only (RO) and the value is considered as all-zero.
				[0]	SR	1'h0	Start or Stop Receive When this bit is set, the DMA tries to acquire the descriptor from the Receive list and processes the incoming packets. When this bit is reset, the Rx DMA operation is stopped after the transfer of the current packet. The next descriptor position in the Receive list is saved, and it becomes the current position after the Rx process is restarted. The Stop Receive command is effective only when the Rx process is in the Running (waiting for Rx packet) or Suspended state. 0: Stop Receive 1: Start Receive
	(80H*i)+1114H	DMA_CH(#i)_TxDesc_List_Address (for i = 0; i <= 3)	RW	[31:2]	TDESLA	30'h0	Start of Transmit List This field contains the base address of the first descriptor in the Transmit descriptor list. The DMA ignores the LSB bits [1:0] 32-bit bus width and internally takes these bits as all-zero.
				[1:0]	Reserved_LSB		
	(80H*i)+111CH	DMA_CH(i)_RxDesc_List_Address (for i = 0; i <= 3)	RW	[31:2]	RDESLA	30'h0	Start of Receive List This field contains the base address of the first descriptor in the Rx Descriptor list. The DMA ignores the LSB bits[1:0] for 32-bit bus width and internally takes these bits as all-zero.
				[1:0]	Reserved_LSB		

Ethernet MAC

BASE_ADDR: 0xA501_4000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
(80H*i)+1120H	DMA_CH(i)_TxDesc_Tail_Pointer (for i = 0; i <= 3)	RW	[31:2]	TDTP	30'h0	Transmit Descriptor Tail Pointer This field contains the tail pointer for the Tx descriptor ring. The software writes the tail pointer to add more descriptors to the Tx channel. The hardware tries to transmit all packets referenced by the descriptors between the head and the tail pointer registers.
			[1:0]	Reserved_LSB		
(80H*i)+1128H	DMA_CH(i)_RxDesc_Tail_Pointer (for i = 0; i <= 3)	RW	[31:2]	RDTP	30'h0	Receive Descriptor Tail Pointer This field contains the tail pointer for the Rx descriptor ring. The software writes the tail pointer to add more descriptors to the Rx channel. The hardware tries to write all received packets to the descriptors referenced between the head and the tail pointer registers.
			[1:0]	Reserved_LSB		
(80H*i)+112CH	DMA_CH(i)_TxDesc_Ring_Length (for i = 0; i <= 3)	RW	[31:10]	Reserved		
			[9:0]	TDRL	10'h0	Transmit Descriptor Ring Length This field sets the maximum number of Tx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. A value of 0x9 indicates 10 descriptors.
(80H*i)+1130H	DMA_CH(i)_RxDesc_Ring_Length (for i = 0; i <= 3)	RW	[31:10]	Reserved		
			[9:0]	RDRL	10'h0	Receive Descriptor Ring Length This register sets the maximum number of Rx descriptors in the circular descriptor ring. The maximum number of descriptors is limited to 1K descriptors. A value of 0x9 indicates 10 descriptors.
(80H*i)+11	DMA_CH(i)_Interrup	RW	[31:16]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	34H	t_Enable (for i = 0; i <= 3)		[15]	NIE	1'h0	Normal Interrupt Summary Enable When this bit is set, the normal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit[0]: Transmit Interrupt Bit[2]: Transmit Buffer Unavailable Bit[6]: Receive Interrupt Bit[11]: Early Receive Interrupt 0: Normal Interrupt Summary is disabled 1: Normal Interrupt Summary is enabled
				[14]	AIE	1'h0	Abnormal Interrupt Summary Enable When this bit is set, the abnormal interrupt summary is enabled. This bit enables the following interrupts in the DMA_CH0_Status register: Bit[1]: Transmit Process Stopped Bit[7]: Rx Buffer Unavailable Bit[8]: Receive Process Stopped Bit[9]: Receive Watchdog Timeout Bit[10]: Early Transmit Interrupt Bit[12]: Fatal Bus Error Bit[13]: Context Descriptor Error 0: Abnormal Interrupt Summary is disabled 1: Abnormal Interrupt Summary is enabled
				[13]	CDEE	1'h0	Context Descriptor Error Enable When this bit is set along with the AIE bit, the Descriptor error interrupt is enabled. 0: Context Descriptor Error is disabled 1: Context Descriptor Error is enabled

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[12]	FBEE	1'h0	Fatal Bus Error Enable When this bit is set along with the AIE bit, the Fatal Bus error interrupt is enabled. 0: Fatal Bus Error is disabled 1: Fatal Bus Error is enabled
				[11]	ERIE	1'h0	Early Receive Interrupt Enable When this bit is set along with the NIE bit, the Early Receive interrupt is enabled. When this bit is reset, the Early Receive interrupt is disabled. 0: Early Receive Interrupt is disabled 1: Early Receive Interrupt is enabled
				[10]	ETIE	1'h0	Early Transmit Interrupt Enable When this bit is set along with the AIE bit, the Early Transmit interrupt is enabled. 0: Early Transmit Interrupt is disabled 1: Early Transmit Interrupt is enabled
				[9]	RWTE	1'h0	Receive Watchdog Timeout Enable When this bit is set along with the AIE bit, the Receive Watchdog Timeout interrupt is enabled. 0: Receive Watchdog Timeout is disabled 1: Receive Watchdog Timeout is enabled
				[8]	RSE	1'h0	Receive Stopped Enable When this bit is set along with the AIE bit, the Receive Stopped Interrupt is enabled. 0: Receive Stopped is disabled 1: Receive Stopped is enable

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
				[7]	RBUE	1'h0	Receive Buffer Unavailable Enable When this bit is set along with the AIE bit, the Receive Buffer Unavailable interrupt is enabled. 0: Receive Buffer Unavailable is disabled 1: Receive Buffer Unavailable is enabled
				[6]	RIE	1'h0	Receive Interrupt Enable When this bit is set along with the NIE bit, the Receive Interrupt is enabled. 0: Receive Interrupt is disabled 1: Receive Interrupt is enabled
				[5:3]	Reserved		
				[2]	TBUE	1'h0	Transmit Buffer Unavailable Enable When this bit is set along with the NIE bit, the Transmit Buffer Unavailable interrupt is enabled. 0: Transmit Buffer Unavailable is disabled 1: Transmit Buffer Unavailable is enabled
				[1]	TXSE	1'h0	Transmit Stopped Enable When this bit is set along with the AIE bit, the Transmission Stopped interrupt is enabled. 0: Transmit Stopped is disabled 1: Transmit Stopped is enabled
				[0]	TIE	1'h0	Transmit Interrupt Enable When this bit is set along with the NIE bit, the Transmit Interrupt is enabled. 0: Transmit Interrupt is disabled 1: Transmit Interrupt is enabled
	(80H*i)+11	DMA_CH(i)_Rx_Inter	RW	[31:18]	Reserved		

Ethernet MAC

BASE_ADDR: 0xA501_4000						
Offset	**Register Name**	**Access**	**Bits**	**Field Name**	**Default Value**	**Description**
38H	rupt_Watchdog_Timer (for i = 0; i <= 3)		[17:16]	RWTU	2'h0	Receive Interrupt Watchdog Timer Count Units This fields indicates the number of system clock cycles corresponding to one unit in RWT field. 2'b00: 256 2'b01: 512 2'b10: 1024 2'b11: 2048 For example, when RWT=2 and RWTU=1, the watchdog timer is set for 2*512=1024 system clock cycles.
			[15:8]	Reserved		
			[7:0]	RWT	8'h0	Receive Interrupt Watchdog Timer Count This field indicates the number of system clock cycles, multiplied by factor indicated in RWTU field, for which the watchdog timer is set. The watchdog timer is triggered with the programmed value after the Rx DMA completes the transfer of a packet for which the RI bit is not set in the DMA_CH(#i)_Status register. When the watchdog timer runs out, the RI bit is set and the timer is stopped.
(80H*i)+1144H	DMA_CH(i)_Current_App_TxDesc (for i = 0; i <= 3)	RO	[31:0]	CURTDESAPTR	32'h0	Application Transmit Descriptor Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.
(80H*i)+114CH	DMA_CH(#i)_Current_App_RxDesc (for i = 0; i <= 3)	RO	[31:0]	CURRDESAPTR	32'h0	Application Receive Descriptor Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.
(80H*i)+1154H	DMA_CH(i)_Current_App_TxBuffer (for i = 0; i <= 3)	RO	[31:0]	CURTBUFAPTR	32'h0	Application Transmit Buffer Address Pointer The DMA updates this pointer during Tx operation. This pointer is cleared on reset.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	(80H*i)+115CH	DMA_CH(i)_Current_App_RxBuffer (for i = 0; i <= 3)	RO	[31:0]	CURRBUFAPTR	32'h0	Application Receive Buffer Address Pointer The DMA updates this pointer during Rx operation. This pointer is cleared on reset.
	(80H*i)+1160H	DMA_CH(i)_Status (for i = 0; i <= 3)	RO	[31:22]	Reserved		
			RO	[21:19]	REB	3'h0	Rx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. Bit[21] 0: No Error during data transfer by Rx DMA 1: Error during data transfer by Rx DMA Bit[20] 0: Error during data buffer access 1: Error during descriptor access Bit[19] 0: Error during write transfer 1: Error during read transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RO	[18:16]	TEB	3'h0	Tx DMA Error Bits This field indicates the type of error that caused a Bus Error. For example, error response on the AHB or AXI interface. Bit[18] 0: No Error during data transfer by Tx DMA 1: Error during data transfer by Tx DMA Bit[17] 0: Error during data buffer access 1: Error during descriptor access Bit[16] 0: Error during write transfer 1: Error during read transfer This field is valid only when the FBE bit is set. This field does not generate an interrupt.

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[15]	NIS	1'h0	Normal Interrupt Summary Normal Interrupt Summary bit value is the logical OR of the following bits when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit[0]: Transmit Interrupt - Bit[2]: Transmit Buffer Unavailable - Bit[6]: Receive Interrupt - Bit[11]: Early Receive Interrupt Only unmasked bits (interrupts for which interrupt enable is set in DMA_CH0_Interrupt_Enable register) affect the Normal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit which causes NIS to be set is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Normal Interrupt Summary status not detected 1: Normal Interrupt Summary status detected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[14]	AIS	1'h0	Abnormal Interrupt Summary Abnormal Interrupt Summary bit value is the logical OR of the following when the corresponding interrupt bits are enabled in the DMA_CH0_Interrupt_Enable register: - Bit[1]: Transmit Process Stopped - Bit[7]: Receive Buffer Unavailable - Bit[8]: Receive Process Stopped - Bit[10]: Early Transmit Interrupt - Bit[12]: Fatal Bus Error - Bit[13]: Context Descriptor Error Only unmasked bits affect the Abnormal Interrupt Summary bit. This is a sticky bit. You must clear this bit (by writing 1 to this bit) each time a corresponding bit, which causes AIS to be set, is cleared. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Abnormal Interrupt Summary status not detected 1: Abnormal Interrupt Summary status detected
			RW	[13]	CDE	1'h0	Context Descriptor Error This bit indicates that the DMA Tx/Rx engine received a descriptor error. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Context Descriptor Error status not detected 1: Context Descriptor Error status detected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[12]	FBE	1'h0	Fatal Bus Error This bit indicates that a bus error occurred (as described in the EB field). When this bit is set, the corresponding DMA channel engine disables all bus accesses. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Fatal Bus Error status not detected 1: Fatal Bus Error status detected
			RW	[11]	ERI	1'h0	Early Receive Interrupt This bit when set indicates that the RxDMA has completed the transfer of packet data to the memory. The setting of RI bit automatically clears this bit. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Early Receive Interrupt status not detected 1: Early Receive Interrupt status detected
			RW	[10]	ETI	1'h0	Early Transmit Interrupt This bit when set indicates that the TxDMA has completed the transfer of packet data to the MTL TXFIFO memory. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Early Transmit Interrupt status not detected 1: Early Transmit Interrupt status detected
			RW	[9]	RWT	1'h0	Receive Watchdog Timeout This bit is asserted when a packet with length greater than 2,048 bytes (10,240 bytes when Jumbo Packet mode is enabled) is received. 0: Receive Watchdog Timeout status not detected 1: Receive Watchdog Timeout status detected

Ethernet MAC	BASE_ADDR: 0xA501_4000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[8]	RPS	1'h0	Receive Process Stopped This bit is asserted when the Rx process enters the Stopped state. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Receive Process Stopped status not detected 1: Receive Process Stopped status detected
			RW	[7]	RBU	1'h0	Receive Buffer Unavailable This bit indicates that the application owns the next descriptor in the Receive list, and the DMA cannot acquire it. The Rx process is suspended. To resume processing Rx descriptors, the application should change the ownership of the descriptor and issue a Receive Poll Demand command. In ring mode, the application should advance the Receive Descriptor Tail Pointer register of a channel. This bit is set only when the DMA owns the previous Rx descriptor. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Receive Buffer Unavailable status not detected 1: Receive Buffer Unavailable status detected
			RW	[6]	RI	1'h0	Receive Interrupt This bit indicates that the packet reception is complete. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Receive Interrupt status not detected 1: Receive Interrupt status detected
			RO	[5:3]	Reserved		

Ethernet MAC	BASE_ADDR: 0xA501_4000					
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
			RW	[2]	TBU	1'h0	Transmit Buffer Unavailable This bit indicates that the application owns the next descriptor in the Transmit list, and the DMA cannot acquire it. Transmission is suspended. To resume processing the Transmit descriptors, the application should do the following change the ownership of the descriptor and issue a Receive Poll Demand command. In ring mode, the application should advance the Transmit Descriptor Tail Pointer register of a channel. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Transmit Buffer Unavailable status not detected 1: Transmit Buffer Unavailable status detected
			RW	[1]	TPS	1'h0	Transmit Process Stopped This bit is set when the transmission is stopped. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Transmit Process Stopped status not detected 1: Transmit Process Stopped status detected
			RW	[0]	TI	1'h0	Transmit Interrupt This bit indicates that the packet transmission is complete. Access restriction applies. Self-set to 1 on internal event. Setting 1 clears. Setting 0 has no effect. 0: Transmit Interrupt status not detected 1: Transmit Interrupt status detected