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Horizon Robotics

Sunrise 3.0M (X3M)

Errata

Rev. 1.0

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Revision History

This section tracks the significant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
1.0	April 2021	Initial release

Contents

Tables

1 Introduction

This document contains the silicon errata known at the time of publication for the X3M artificial intelligence processor in supported releases up to.

1.1 Scope

This document describes the errata by Errata ID. Each description includes:

- A unique defect tracking identifier and the current status of the errata.
- Where the implementation deviates from the specification and the conditions under which erroneous behavior occurs.
- The implications of the erratum with respect to typical applications.
- The application and limitations of a workaround where possible.

This document describes errata information that may impact anyone who is developing software that will run on implementations of this X3M product.

1.2 Errata Summary

Table 1-1 below gives a quick reference to all documented device errata of the X3M and their status:

- A = workaround available
- N = no workaround available
- P = partial workaround available

Table 1-1 Summary of Silicon Errata

Errata ID	Errata	Solution	Status
IPU			
ERR0001	IPU configuration failed about ddr_en of DS2 channel.	No fix scheduled	A
ERR0002	Bus hang up during frame drop operation.	No fix scheduled	A
PYM			
ERR0003	Bus hang up during frame drop operation.	No fix scheduled	P
USB			
ERR0004	USB hot plug failed.	No fix scheduled	A

2 Errata

2.1 ERR0001

IPU: IPU configuration failed about ddr_en of DS2 channel

Description

IPU configuration is failed about ddr_en of DS2 channel with shadow register group 2 and 3 selected when the current shadow ready 2 and 3 set.

The ddr_en for shadow register group 2 and 3 selection map wrong ready flag.

Workarounds

Have to set the shadow ready 1 to instead the shadow ready 2 and 3 for ddr_en.

Proposed Solution

No fix scheduled.

2.2 ERR0002

IPU: Bus hang up during frame drop operation

Description

There is a bus write FIFO control bug occurred with corner bus response during frame drop operation.

This bug will stop the write data transfer after write command, and then make stall inside the DDR controller.

Implications

This bug make bus hang up with frame drop operation when the DDR bandwidth is over 65% usage.

Workarounds

To avoid frame drop in busy DDR usage, perform the following procedures:

1. Set bus write FIFO thread pointer to 0x0.
2. Use the safe output image width (buffer depth – 256 pixels) for each scaler as below:
   - Upscale: (buffer depth 4096): 3840x2160.
   - Down scale 0: (buffer depth 1280): 1024x720.
   - Down scale 1: (buffer depth 2048): 1792x1080.
   - Down scale 2: (buffer depth 4096): 3840x2160.
   - Down scale 3: (buffer depth 2048): 1792x1080.
   - Down scale 4: (buffer depth 1280): 1024x720.

Proposed Solution

No fix scheduled.

2.3 ERR0003

PYM: Bus hang up during frame drop operation

Description

There is a failed data transfer protection during frame drop operation. The bus response will hit the corner case when frame drop asserted from other scale channel.

Implications

This bug make bus hang up with frame drop operation when the DDR bandwidth is over 65% usage.

Workarounds

Have to use offline mode to instead online mode to avoid frame drop.

Proposed Solution

No fix scheduled.

2.4 ERR0004

USB: USB hot plug failed

Description

In USB device mode, there is no VBUS detection in current chip ball out to detect external VBUS connected.

Implications

The USB host can't detect the X3M USB device after hot plug.

Workarounds

Have to use a GPIO for the VBUS in detection in USB device mode.

Proposed Solution

No fix scheduled.