X3M Register Reference Manual
PWM

Revision History

Revision	Date	Description
1.0	August-28-2020	Initial Release

PWMx (x = 0, 1, 2)	BASE_ADDR: 0xA500D000, 0xA500E000, 0xA500F000						
	Offset	Register Name	Access	Bits	Field Name	Default Value	Description
	00H	PWM_EN	RW	[31:7]	Reserved		
				[6]	MODE_SEL	1'h0	Mode selection: 0: Normal mode. 1: Simulation mode.
				[5:4]	Reserved		
				[3]	PWM_INT_EN	1'h0	PWM interrupt enable: 0: PWM interrupt generation is disabled. 1: PWM interrupt generation is enabled.
				[2]	PWM2_EN	1'h0	PWM2 channel enable: 0: PWM2 channel is disabled, output low level. 1: PWM2 channel is enabled.
				[1]	PWM1_EN	1'h0	PWM1 channel enable: 0: PWM1 channel is disabled, output low level 1: PWM1 channel is enabled.
				[0]	PWM0_EN	1'h0	PWM0 channel enable: 0: PWM0 channel is disabled, output low level. 1: PWM0 channel is enabled.
	04H	TIME_SLICE	RW	[31:16]	Reserved		
				[15:0]	REG_TIME_SLICE	16'h400	If PWM_INT_EN =1, the PWM generates interrupts periodically. The interrupt period is defined by REG_TIME_SLICE: Interrupt period = Tpwm_mclk * 1024 * REG_TIME_SLICE
	08H	PWM_FREQ	RW	[31:28]	Reserved		
				[27:16]	PWM_FREQ1	12'h400	The frequency of PWM1 output = Fpwm_mclk / PWM_FREQ1. The PWM1 will output high level when configured to 0 or 1.
				[15:12]	Reserved		
				[11:0]	PWM_FREQ0	12'h400	The frequency of PWM0 output = Fpwm_mclk / PWM_FREQ0. The PWM0 will output high level when configured to 0 or 1.

PWMx (x = 0, 1, 2)

BASE_ADDR: 0xA500D000, 0xA500E000, 0xA500F000

Offset	Register Name	Access	Bits	Field Name	Default Value	Description
0CH	PWM_FREQ1	RW	[31:12]	Reserved		
			[11:0]	PWM_FREQ2	12'h400	The frequency of PWM2 output = Fpwm_mclk / PWM_FREQ2. The PWM2 will output high level when configured to 0 or 1.
14H	PWM_RATIO	RW	[31:24]	Reserved		
			[23:16]	PWM_RATIO2	8'h0	The high level ratio to period of PWM2. Duty cycle = PWM_RATIO2/256.
			[15:8]	PWM_RATIO1	8'h0	The high level ratio to period of PWM1. Duty cycle = PWM_RATIO1/256.
			[7:0]	PWM_RATIO0	8'h0	The high level ratio to period of PWM0. Duty cycle = PWM_RATIO0/256.
1CH	PWM_SRCPND	W1C	[31:1]	Reserved		
			[0]	PWM_SRCPND	1'h0	PWM interrupt source pending: For read: 0: The interrupt source is inactive. 1: The interrupt source is active. For write: 0: No effect. 1: Clears the corresponding source.
20H	PWM_INTMASK	RO	[31:1]	Reserved		
			[0]	PWM_INTMASK	1'h0	Mask for the PWM interrupt: 0: Unmasked. 1: Masked.
24H	PWM_SETMASK	WO	[31:1]	Reserved		
			[0]	PWM_SETMASK	1'h0	Sets mask for the PWM interrupt: 0: No effect. 1: Masks the PWM interrupt.
28H	PWM_UNMASK	WO	[31:1]	Reserved		
			[0]	PWM_UNMASK	1'h0	Used to unmask the PWM interrupt: 0: No effect. 1: Unmasks the PWM interrupt.