An Innovative Digital Control Architecture for Low-Voltage, High-Current DC–DC Converters With Tight Voltage Regulation

Stefano Saggini, Massimo Ghioni, *Member, IEEE*, and Angelo Geraci, *Member, IEEE*

***Abstract*—This paper describes an innovative digital control architecture for low-voltage, high-current dc–dc converters, based on a combination of current-programmed control and variable frequency operation. The key feature of the proposed architecture is the low complexity: only two digital-to-analog converters (DACs) with low resolution (7-b) are used for control. An original control algorithm is used to reduce quantization effects to negligible levels, in spite of the low resolution of the DACs. Thanks to this algorithm, both static and dynamic output voltage regulation are improved with respect to traditional digital solutions. Adaptive voltage positioning and active current sharing are inherently provided by the new architecture. A detailed description of the control strategy is given with reference to a single-phase buck converter. Extension to multiphase converters is straightforward. The digital control architecture is experimentally verified on a FPGA-based four-phase prototype buck converter operating at 350 kHz/phase. Output voltage tolerance within $\pm 0.5\%$ is experimentally demonstrated, along with negligible quantization effects and fast transient response. The features and the performance of the proposed architecture make it a valuable candidate for the control of next generation voltage regulator modules.**

***Index Terms*—Current-programmed control, dc–dc switching power converters, digital control.**

I. Introduction

RECENTLY, there has been a growing interest in digital controllers for high-frequency, low-to-medium power dc-dc converters, due to their low power consumption, immunity to noise and analog component variations, ease of integration with other digital systems, ability to implement sophisticated control schemes [1]–[11]. Among the various advantages of digital approach, design flexibility is the most valuable one. The control algorithm is described at the functional level using a hardware description language [very high speed integrated circuit hardware description language (VHDL)]. Sophisticated simulation, synthesis and verification tools are available for translating the VHDL design into standard-cell application specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs). The design can be easily adapted to different technologies or modified to meet a different application or a new set of specifications, thus providing very fast time-to-market.

Manuscript received December 10, 2002; revised August 12, 2003. Recommended by Associate Editor B. Lehman.

The authors are with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, Milano MI 20133, Italy (e-mail: saggini@elet.polimi.it; ghioni@elet.polimi.it; geraci@elet.polimi.it).

Digital Object Identifier 10.1109/TPEL.2003.820543

Most of the digital controllers so far reported are derived from the traditional voltage-mode analog controller [1]–[4], [7]. Basically, an analog-to-digital converter (ADC) is used to digitize the regulated output voltage. The numerical value is processed by a discrete-time proportional-integral-derivative (PID) controller and the result is converted to an analog value by means of a digital pulse width modulator (DPWM). The precision with which a digital controller regulates the output voltage is determined by the resolution of the ADC. In order to avoid steady-state limit cycling, the resolution of the DPWM must be higher than that of the ADC [5].

It can be easily realized that when tight output voltage regulation is required, digital controllers may suffer from excessive complexity and considerable silicon area usage if compared with standard analog solutions, due to the need of high resolution ADCs and DPWMs. From this standpoint, voltage regulator modules (VRMs) represent one of the most challenging applications. Present VRM specifications demand for output currents up to 80 A, along with tight tolerance ($\pm 1\%$ of the nominal output value of about 1.5 V) even in the case of fast current transients (50 A/μs) [12]. Future processor generations are projected to require greater current, up to 100 A, at supply voltages as low as 1 V, with load transient of about 400 A/μs. At this time, digitally controlled VRMs require an ADC with a resolution of at least 9 b, operated at a sampling rate of a few MHz [5]. A DPWM with 10-b resolution or more is needed in order to avoid steady-state limit cycling [5]. Concurrent requirements of high resolution and high operating frequency turn out to be quite expensive in terms of silicon area and dissipated power. Digital controllers based on different architectures have been proposed [8]–[10], but they show similar problems.

A strong reduction of system complexity, die area and dissipated power, while keeping high performance, is therefore a key design goal, especially when high-volume, low-cost solutions are targeted. Some design strategies directed to accomplish this goal have been investigated. A "windowed" ADC is proposed in [6] in order to reduce the ADC resolution. Digital dithering is reported in [6] aiming at reducing the DPWM resolution. A hybrid delay line-counter [2] and a combined ring oscillator-MUX [6] structures are proposed for making a compromise between area and power consumption in DPWM design.

In this paper, we introduce a low-complexity, high-performance digital controller based on a radically different design strategy. The proposed solution combines current programmed control and variable frequency operation. The controller employs only two digital-to-analog converters (DACs) with low resolution (7-b), thus allowing for considerable resource saving

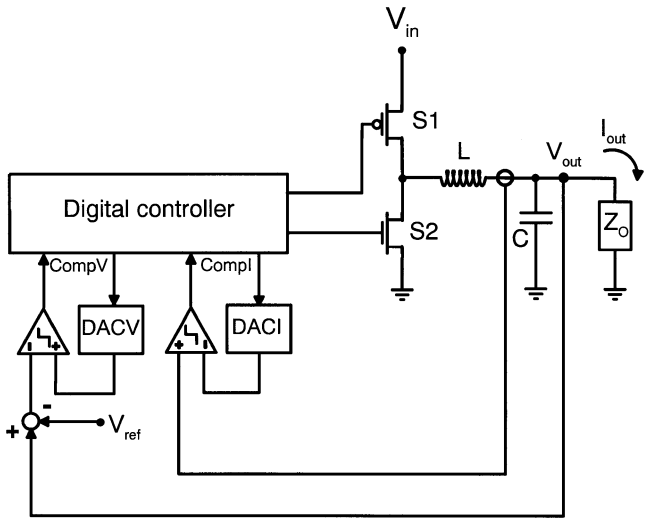

Fig. 1. Simplified block diagram of the control architecture applied to a single-phase buck topology.

[13]. An original control algorithm is used to reduce quantization effects to a negligible level, in spite of the low resolution of the DACs. This makes it possible to improve both static and dynamic output voltage regulation with respect to traditional digital solutions. The new architecture inherently provides some important features like adaptive voltage positioning (AVP) [14] and active current sharing.

The control algorithm has been implemented into a commercially available FPGA device and tested on a prototype four-phase buck converter. Output voltage tolerance well within $\pm 0.5\%$ has been experimentally demonstrated, along with negligible limit cycling effects and fast transient response.

The paper is organized as follows. In Section II, we describe the new architecture and the control algorithm with reference to a single-phase buck converter. Extension to multiphase converters is then easily derived. Section III reports the simulations of the control architecture applied to a four-phase buck converter, performed in the Simulink environment. Experimental results are presented in Section IV.

II. Digital Control Architecture

A single-phase buck topology will be first considered in order to illustrate at best the principle of operation of the new architecture. Extension of the concept to multi-phase topologies will be straightforward.

A. Single-Phase Topology

A block diagram of the new digital controller applied to a single-phase buck converter is shown in Fig. 1.

The proposed architecture combines peak current-mode control and variable frequency operation. The inductor current is sensed and compared to a constant analog value $\mathrm{I_{pk}}$ generated by a first DAC (DACI). $\mathrm{I_{pk}}$ sets the peak inductor current. The error voltage $\mathrm{V_{err}} = (\mathrm{V_{out}} - \mathrm{V_{ref}})$ is compared to the analog signal generated by a second DAC (DACV). DACV generates a bottom voltage level $\mathrm{V_{low}}$ on which a voltage ramp of a given slope is superimposed. The voltage ramp is generated digitally by incrementing the DACV input code at the clock frequency

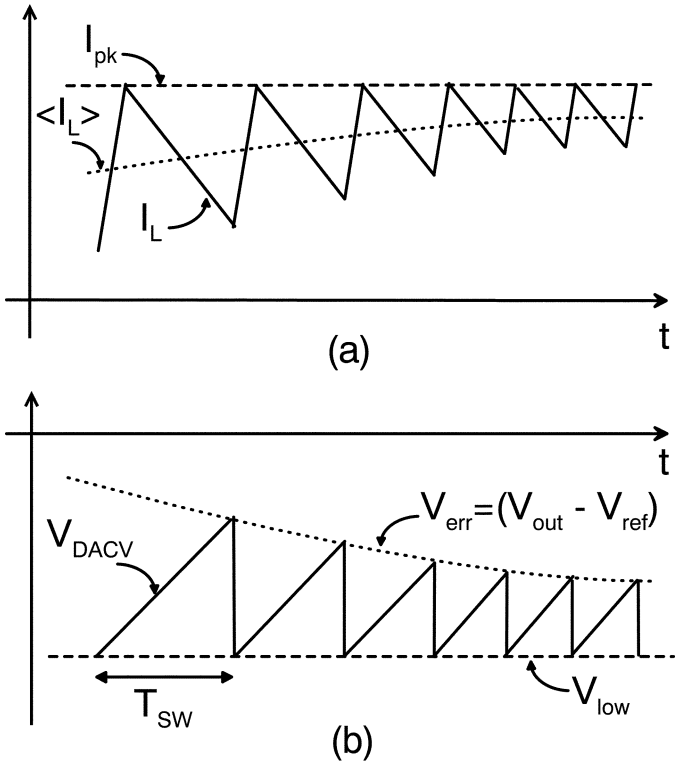

Fig. 2. (a) Current and (b) voltage waveforms during a load transient.

$\mathrm{f_{ck}}$: as soon as the DACV output voltage exceeds $\mathrm{V_{err}}$, the voltage ramp is reset. Based on the status of the logic signal CompI and CompV, generated by the comparators, the digital block provides suitable control signals to the switches S1 and S2. The control laws can be simply summarized as follows:

- when the measured current exceeds $\mathrm{I_{pk}}$ (i.e., CompI ="1"), switch S1 is opened and switch S2 is closed;
- when the DACV output voltage exceeds the error voltage $\mathrm{V_{err}}$ (i.e., CompV ="1"), switch S1 is closed and switch S2 is opened.

The working principle of the controller can be easily understood by looking at Fig. 2 where, for instance, we have considered an increase of the load current $\mathrm{I_{out}}$. Fig. 2(a) shows the inductor current $\mathrm{I_L}$ (solid line) and average inductor current $\langle \mathrm{I_L} \rangle$ (dotted line) as a function of time. The peak current level $\mathrm{I_{pk}}$ set by DACI is also shown (dashed line). Fig. 2(b) shows the corresponding error voltage signal $\mathrm{V_{err}}$ (dotted line) and DACV voltage signal (solid line). For the sake of simplicity, the DACV output voltage has been represented by a continuous function instead of a staircase. The effects due to the quantization of the DACV output will be discussed later

As the load current exceeds the average inductor current, the output voltage value lowers, causing the crossing time between the error voltage and the voltage signal generated by DACV to occur earlier. This makes the instantaneous switching frequency to increase, until the average inductor current value exactly balances the load current. By means of this current self-regulation mechanism, the control system is able to react both to positive and negative load transients. The average current supplied by the converter is largely independent of the selected peak value $\mathrm{I_{pk}}$,

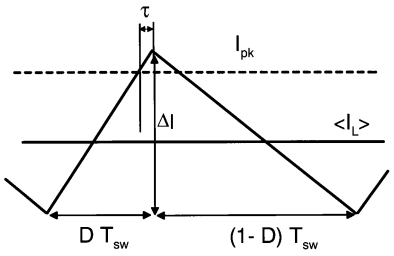

Fig. 3. Detailed representation of the inductor current. Due to the delay, τ, the peak inductor current is actually greater than $\mathrm{I_{pk}}$.

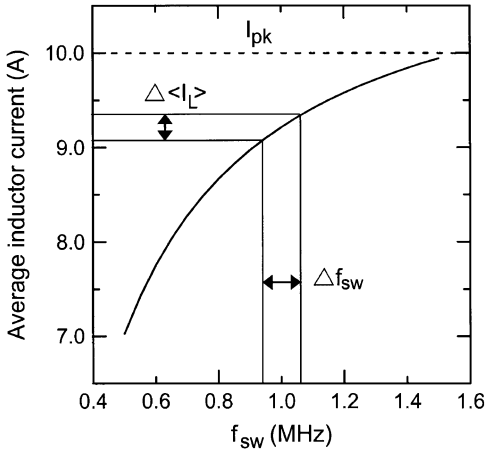

Fig. 4. Average inductor current as a function of switching frequency. $\mathrm{L} = 300$ nH, $\tau = 40$ ns, $\mathrm{D} = 0.125$, $\mathrm{I_{pk}} = 10$ A.

and it self-adapts to the value required by the load by varying the switching frequency.

For the buck converter in continuous conduction mode (CCM), the steady-state average inductor current $\langle \mathrm{I_L} \rangle$ is given by

$$\begin{aligned} \langle \mathrm{I_L} \rangle = \mathrm{I_{out}} &= \mathrm{I_{pk}} - \frac{\Delta \mathrm{I}}{2} + \tau \frac{\mathrm{V_{out}}(1-\mathrm{D})}{\mathrm{L\,D}} \\ &= \mathrm{I_{pk}} - \frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}f_{\mathrm{sw}}} + \tau \frac{\mathrm{V_{out}}(1-\mathrm{D})}{\mathrm{L\,D}} \end{aligned} \tag{1}$$

where $\mathrm{D} = \mathrm{V_{out}}/\mathrm{V_{in}}$ is the converter duty cycle, $\mathrm{f_{sw}}$ is the converter switching frequency, $\Delta \mathrm{I}$ is the current ripple amplitude and τ is the turn-off delay of the high-side switch S1 (see Fig. 3).

If we assume a constant line voltage, $\mathrm{V_{in}}$, it follows that D is constant and $\langle \mathrm{I_L} \rangle$ only depends on $\mathrm{f_{sw}}$ and $\mathrm{I_{pk}}$. As expected, large variations of $\mathrm{f_{sw}}$ are required in order to modulate $\langle \mathrm{I_L} \rangle$ in the range between zero and $\mathrm{I_{pk}}$. In practical systems, the switching frequency modulation must be limited to a small interval, $\Delta \mathrm{f_{sw}}$, centered around a nominal frequency $\mathrm{f_{swo}}$. A plurality of discrete peak current levels $\mathrm{I_{pk}}$ is therefore necessary in order to generate a wide range of inductor currents. As shown in Fig. 4, a continuous range of currents $\Delta \langle \mathrm{I_L} \rangle$, dependent on the allowed frequency variation interval $\Delta \mathrm{f_{sw}}$, is associated to each peak current level $\mathrm{I_{pk}}$. The separation between adjacent values of $\mathrm{I_{pk}}$, i.e., the size of the Least Significant Bit (LSB) generated by DACI, must guarantee the overlap of the corresponding intervals $\Delta \langle \mathrm{I_L} \rangle$.

The DACI resolution can be evaluated once the maximum peak current level $\mathrm{I_{pk\,max}}$ is set. In fact, the size of the LSB generated by DACI s given by

$$\mathrm{LSB_{DACI}} = \frac{\mathrm{I_{pk\,max}}}{2^{\mathrm{n}}} \tag{2}$$

where n is the number of bits.

By differentiating equation (1) with respect to the switching period $\mathrm{T_{sw}}$, we obtain

$$|\Delta \langle \mathrm{I_L} \rangle| = \frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \Delta \mathrm{T_{sw}}. \tag{3}$$

Since the LSB should be less or equal to $|\Delta \langle \mathrm{I_L} \rangle|$ we get

$$\frac{\mathrm{I_{pk\,max}}}{2^{\mathrm{n}}} \leq \frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \cdot \Delta \mathrm{T_{sw}}. \tag{4}$$

Therefore, the minimum number of bit, $\mathrm{n_{min}}$, is given by

$$\begin{aligned} n_{\min} &= \log_2 \left[\frac{\mathrm{I_{pk\,max}} \mathrm{T_{swo}}}{\frac{\mathrm{V_{out}}(1-\mathrm{D})\mathrm{T_{swo}}}{2\mathrm{L}} \cdot \Delta \mathrm{T_{sw}}} \right] \\ &= \log_2 \left[\frac{\mathrm{I_{pk\,max}} f_{\mathrm{swo}}}{\Delta \mathrm{I} \Delta f_{\mathrm{sw}}} \right] + 1 \end{aligned} \tag{5}$$

where $\mathrm{T_{wso}}$ and $\mathrm{f_{swo}}$ are the nominal switching period and frequency and

$$\left| \frac{\Delta \mathrm{f_{sw}}}{\mathrm{f_{swo}}} \right| \simeq \frac{\Delta \mathrm{T_{sw}}}{\mathrm{T_{swo}}}. \tag{6}$$

If we consider, for instance, an application with the following characteristics: $\mathrm{I_{out\,max}} = 15$ A, $\Delta \mathrm{I} = 4$ A; $\tau = 50$ ns; $\mathrm{f_{sw}} = 1$ MHz, $\Delta \mathrm{f_{sw}}/\mathrm{f_{swo}} = \pm 5\%$, we get $\mathrm{I_{pk\,max}} = 15.4$ A [see (1)] and $\mathrm{n_{min}} = 7$.

The digital controller updates the DACI output level by comparing the measured switching period $\mathrm{T_{sw}}$ with the nominal switching period $\mathrm{T_{swo}}$. Measurement can be easily performed by counting the number of clock periods elapsed between the start and stop of the digitally-generated voltage ramp (see Fig. 2). If the difference $(\mathrm{T_{sw}} - \mathrm{T_{swo}})$ stays within the allowed $\Delta \mathrm{T_{sw}}$, no action is taken. Otherwise, the DACI output is varied by a number of levels given by

$$\mathrm{N_{update}} = \mathrm{Int}\{(\mathrm{T_{swo}} - \mathrm{T_{sw}})\mathrm{f_{ck}}\} \tag{7}$$

where $\mathrm{Int}\{\,\}$ denotes taking the upper rounded integer value of the argument.

In practice, the combination of DACV, CompV and the digital controller realizes a voltage-controlled oscillator (VCO), where the oscillation frequency, i.e., the switching frequency of the converter, is controlled by the amplitude of the error voltage, $\mathrm{V_{err}}$. By means of the VCO, the voltage error is converted into a switching period error. The control algorithm updates the peak current level proportionally to the switching period error, with a user-defined dead-zone $\Delta \mathrm{T_{sw}}$. In essence, the digital control implements a proportional algorithm that acts to keep the switching period within the allowed range.

B. Adaptive Voltage Positioning

The adaptive voltage positioning (AVP) technique, also known as "droop function" [14], was introduced to increase

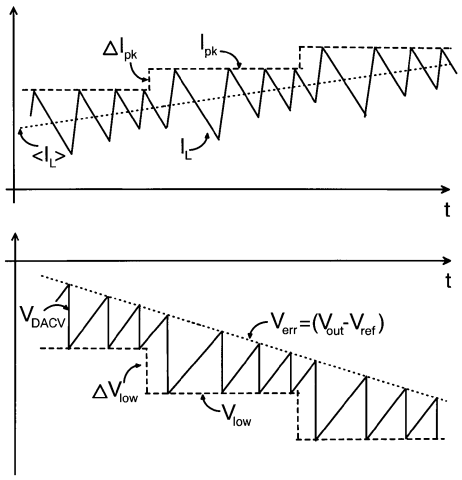

Fig. 5. Mutual tracking of the discrete levels $\mathrm{I_{pk}}$ and $\mathrm{V_{low}}$ during a load transient.

the dynamic voltage regulation performance. According to this technique, the output voltage $\mathrm{V_{out}}$ is positioned at

$$\mathrm{V_{out}} = \mathrm{V_{ref}} - \mathrm{R_{droop}} \mathrm{I_{out}} \tag{8}$$

where the optimal value of $\mathrm{R_{droop}}$ is equal to the equivalent series resistance (ESR) of the filter capacitor.

AVP can be easily included in our control system by forcing any variation of DACI to be tracked by a corresponding variation of DACV. More precisely, if $\mathrm{I_{pk}}$ is increased by $\Delta \mathrm{I_{pk}}$, $\mathrm{V_{low}}$ should be correspondingly decreased by $\Delta \mathrm{V_{low}}$ and vice versa.

It can be easily shown that

$$\begin{aligned} \mathrm{R_{droop}} &= \frac{\Delta \mathrm{V_{low}}}{\Delta \mathrm{I_{pk}}} = \frac{\mathrm{M_{update}}}{\mathrm{N_{update}}} \frac{\mathrm{LSB_{DACV}}}{\mathrm{LSB_{DACI}}} \\ &= \mathrm{K} \frac{\mathrm{LSB_{DACV}}}{\mathrm{LSB_{DACI}}} \end{aligned} \tag{9}$$

where $\mathrm{M_{update}}$ and $\mathrm{N_{update}}$ represent, respectively, the number of levels by which the output of DACV and DACI are updated, and $\mathrm{K} = \mathrm{M_{update}}/\mathrm{N_{update}}$. In the present implementation, the ratio $\mathrm{LSB_{DACV}}/\mathrm{LSB_{DACI}}$ is chosen to match the desired $\mathrm{R_{droop}}$, and both DAC outputs are changed by the same number of levels $(\mathrm{K} = 1)$. If needed, the droop resistance can be easily varied by acting on the digital section of the controller, that is, by varying the parameter K. Fig. 5 shows the mutual tracking of DACI and DACV levels during a load transient.

It must be noted that when AVP is implemented, the assumption of constant output voltage and constant duty cycle made in (1) is not strictly valid, since $\mathrm{V_{out}}$ is load dependent. However, the variation of the output voltage can be considered a second-order effect when typical values of $\mathrm{R_{droop}}$ (a few milliohms) are employed.

In case AVP is not required, the voltage level $\mathrm{V_{low}}$ can be simply kept fixed. However, more sophisticated control algorithms could be devised in order to improve the system response to load transients.

C. Load Regulation

Ideally, if the load current is varied by $\Delta \mathrm{I_{out}}$, the output voltage is expected to vary by

$$\Delta \mathrm{V_{out}} = -\mathrm{R_{droop}} \Delta \mathrm{I_{out}}. \tag{10}$$

In practice, small deviations from ideality arise from the self-regulation mechanism described in Subsection II.B. We showed that small variations of the load current can be accommodated by varying the switching frequency. If the switching frequency stays within a well-defined interval $\Delta \mathrm{f_{sw}}$, DACV and DACI outputs are not changed. In this condition we have [see (3)]

$$\Delta \langle \mathrm{I_L} \rangle = \Delta \mathrm{I_{out}} = -\frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \Delta \mathrm{T_{sw}}. \tag{11}$$

According to (10), this would cause an ideal output voltage variation given by

$$\begin{aligned} \Delta \mathrm{V_{out_{ideal}}} &= \Delta \mathrm{V_{err_{ideal}}} = -\mathrm{R_{droop}} \Delta \mathrm{I_{out}} \\ &= \mathrm{R_{droop}} \frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \Delta \mathrm{T_{sw}}. \end{aligned} \tag{12}$$

By looking at Fig. 2(b), it can be realized that a period variation $\Delta \mathrm{T_{sw}}$ produces an effective error voltage variation given by

$$\Delta \mathrm{V_{err_{effective}}} = \Delta \mathrm{V_{out_{effective}}} = \mathrm{SlopeV} \Delta \mathrm{T_{sw}} \tag{13}$$

where SlopeV is the slope of the voltage ramp.

The maximum error, ε, on the output voltage is therefore given by

$$\begin{aligned} \varepsilon &= (\Delta \mathrm{V_{out_{effective}}} - \Delta \mathrm{V_{out_{ideal}}}) \\ &= \Delta \mathrm{T_{sw}} \left(\mathrm{SlopeV} - \mathrm{R_{droop}} \frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \right). \end{aligned} \tag{14}$$

In principle, the error could be completely canceled by choosing a suitable value for SlopeV. However, suitable values for error cancellation turn out to be much lower than practical ones ($\approx$ a few 10^4 V/s) if typical design parameters are considered (e.g., $\mathrm{R_{droop}} \approx 5\ \mathrm{m\Omega}, \mathrm{V_{out}} \approx 1\ \mathrm{V}, \mathrm{D} \approx 0.1, \mathrm{L} \approx 300\ \mathrm{nH}$). A small error is therefore unavoidable. For instance, a $\pm 0.14\%$ voltage regulation tolerance is to be expected for $\Delta \mathrm{T_{sw}}/\mathrm{T_{swo}} = \pm 5\%, \mathrm{V_{out}} = 1.5\ \mathrm{V}, \mathrm{T_{swo}} = 1\ \mu\mathrm{s}, \mathrm{SlopeV} = 3 \cdot 10^4$ V/s.

D. Line Regulation

Line voltage fluctuations are partially compensated by the feed-forward compensation that is inherently provided by the peak current mode controller.

By differentiating the voltage transfer characteristic of the buck converter, we obtain

$$\Delta \mathrm{V_{out}} = \mathrm{V_{in}} \Delta \mathrm{D} + \mathrm{D} \Delta \mathrm{V_{in}} \tag{15}$$

where $\mathrm{V_{in}}$ is the line voltage.

Line regulation can be easily evaluated by assuming that the output voltage variation is negligible with respect to the right hand side terms of (15) and that the average inductor current variation caused by line fluctuations is negligible. In this case

$$\frac{\Delta \mathrm{V_{in}}}{\mathrm{V_{in}}} \cong -\frac{\Delta \mathrm{D}}{\mathrm{D}} \tag{16}$$

and, by differentiating equation (1)

$$0 \cong -\frac{\mathrm{V_{out}}(1-\mathrm{D})}{2\mathrm{L}} \Delta \mathrm{T_{sw}} + \frac{\mathrm{V_{out}} \mathrm{T_{swo}}}{2\mathrm{L}} \Delta \mathrm{D} + \frac{\tau}{\mathrm{L}} \Delta \mathrm{V_{in}}. \tag{17}$$

By combining (16) and (17), we obtain

$$\Delta T_{sw} \cong -\frac{DT_{swo}}{(1-D)}\frac{\Delta V_{in}}{V_{in}} + \frac{2\tau}{D(1-D)}\frac{\Delta V_{in}}{V_{in}}. \quad (18)$$

By substituting (18) into (13), we finally get

$$\Delta V_{err_{line}} = \Delta V_{out_{line}} = SlopeV\Delta T_{sw} \cong SlopeV\left(-\frac{DT_{swo}}{(1-D)} + \frac{2\tau}{D(1-D)}\right)\frac{\Delta V_{in}}{V_{in}}. \quad (19)$$

Line regulation of $\pm 0.11\%$ is obtained with $\Delta V_{in}/V_{in} = \pm 5\%, V_{out} = 1.5\,V, T_{swo} = 1\,\mu s, \tau = 50\,ns, SlopeV = 3 \cdot 10^4$ V/s.

E. Transient Response

Fig. 6 shows a simplified model of the converter based on (8). In order to obtain a purely resistive output impedance in transient conditions, a low-pass filter with time constant $\tau_f = R_f C_f$ must be included in the voltage feedback loop to remove the ESR zero. A digital filter can be simply designed and implemented in the controller. The output impedance of the converter is given by

$$Z_{out} = Z_1 // Z_2 = \frac{1}{\frac{(1+sC_fR_{droop})}{(1+s\tau_f)R_{droop}} + \frac{sC}{(1+sCESR)}}. \quad (20)$$

By choosing $\tau_f = C \cdot ESR, C_f \ll C$ and $R_{droop} = ESR$, we obtain $Z_{out} \approx R_{droop}$.

The low-pass filter is also needed to make the voltage feedback loop unconditionally stable even for very low ESR values.

It must be pointed out that the model of Fig. 6 is valid until the required slew rate of the average inductor current is not limited by the output voltage and by the value of inductance itself. The worst situation corresponds to a step load transient with amplitude ΔI_{out}. In this case, the following relationship must be verified:

$$\frac{\Delta I_{out}}{\tau_f} \le \frac{V_{out}}{L}. \quad (21)$$

F. Slope Compensation

It is well known that peak current mode control may lead to subharmonic oscillation if $D > 0.5$. This is not an issue in low-voltage, high-current converters, since the bus voltage is quickly moving from 5 V to 12 V or even 48 V due to the quest for better system efficiency. Nevertheless, in some applications conversion from 5 V to 3.3 V or 2.5 V is still required. In these cases, the slope compensation technique [15] can be used to ensure converter stability. In practice, an artificial ramp has to be subtracted to the peak reference value I_{pk}. In the proposed controller, this ramp can be easily generated digitally by decrementing the DACI input code at the clock frequency. As soon as the peak inductor current reaches the value set by DACI the ramp is reset.

G. Startup

At startup, the error voltage falls below V_{low}. In this situation, CompV is always high, and the high side switch is closed. The digital controller automatically increases the DACI output level to $I_{pk\,max}$. When the inductor current reaches this limit the converter is forced to operate in peak current mode at fixed frequency, in order to supply a constant average current. This current charges the output capacitance, causing V_{out} to increase linearly. When the error voltage gets higher than V_{low}, normal operation is restored.

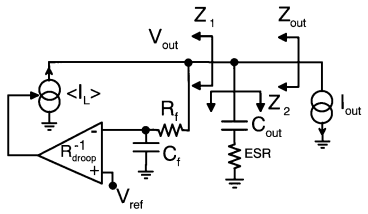

Fig. 6. Simplified model of the dc–dc converter, suitable for load transient analysis.

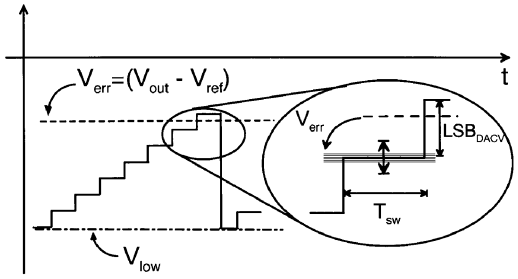

Fig. 7. Quantized voltage ramp. The error voltage oscillates around the discrete levels generated by DACV.

H. Effects Due to the Voltage Ramp Quantization

The voltage ramp generated by DACV is quantized, i.e., it is a staircase having a step width $T_{step} = T_{ck} = 1/f_{ck}$ and a step height given by the LSB of DACV. Since the high-side switch is turned on each time the voltage ramp reaches the error voltage, it turns out that the switching period of the converter is quantized as well. T_{sw} can only assume integer multiple values of the clock frequency. Period quantization translates into current quantization. The separation between two adjacent current levels can be calculated from (3)

$$|(\langle I_L\rangle_m - \langle I_L\rangle_{m-1})| = \Delta\langle I_L\rangle_{min} = \frac{V_{out}(1-D)}{2L}\left(T_{sw_m} - T_{sw_{m-1}}\right). \quad (22)$$

With the following values: $V_{out} = 1.5$ V, $V_{in} = 12$ V, $L = 400$ nH, $(T_{sw_m} - T_{sw_{m-1}}) = T_{ck} = 30$ ns we get $\Delta\langle I_L\rangle_{min} = 50$ mA.

The effects arising from the quantization of f_{sw} can be easily understood by considering steady-state operation. Let's suppose that the voltage error falls between two adjacent levels of DACV, as shown in Fig. 7. In this case, the switching frequency is fixed and therefore the average inductor current has a fixed value as well. If $\langle I_L\rangle$ exactly matches the load current, the converter operates in an unstable equilibrium point. If, for instance, the load current slightly exceeds the average inductor current, the error voltage drops to the next (lower) voltage level generated DACV. In this condition, the error voltage (that is, the output voltage) fluctuates around the DACV voltage level, such that the period of the voltage ramp oscillates between mT_{ck} and $(m+1)T_{ck}$.

In practice, the system experiences a limit cycle where the average inductor current oscillates between two different values separated by $\Delta\langle I_L\rangle_{min}$. The duty cycle of the oscillation self adjusts such that the average inductor current exactly balances the load current. The maximum frequency of oscillation occurs when the load current falls in the middle of two discrete current levels, and it is about a half of the switching frequency of the converter. An exact analysis of the limit cycle effects is currently under development. However, preliminary estimations based on a simplified model of the controller show that the amplitude of the voltage oscillation is approximately given by

$$\Delta V_{out} = \Delta\langle I_L\rangle_{min}\left(\frac{1}{Cf_{sw}} + ESR\right) \tag{23}$$

that is, a hundred of μV with $C = 2$ mF, $ESR = 2$ mΩ, $f_{sw} = 1$ MHz.

Quantization effects can be therefore summarized as follows:

a) the output voltage can only assume discrete values. The difference between two adjacent voltage levels is given by the amplitude of the LSB of DACV, referred to the output. This amplitude is of the order of 1 mV. Discretization of the output voltage is thus negligible;
b) the output voltage is subject to a limit cycle that causes an oscillation around the available discrete levels. However, the amplitude of this oscillation is negligible.

I. Controller Design Criteria

The key parameters of the controller, that is, the resolution of DACI and DACV can be designed according to (2), (5), and (9).

According to (8), V_{ref} is set equal to the nominal output voltage, leading to zero error voltage at zero load current. To guarantee proper system operation, a negative offset voltage should be applied to the DACV output. From a practical point of view, it is more advisable to invert the sign of the error voltage, i.e., $V_{err} = (V_{ref} - V_{out})$ and, correspondingly, to invert the slope of the voltage ramp generated by DACV. Therefore, in the actual system a negative-slope voltage ramp is generated by decrementing the DACV digital input code at the clock frequency. In order to allow correct operation, a digital offset must be applied to DACV such that a positive voltage level V_{low0} is generated at zero load current. V_{low0} is given by

$$V_{low0} = \frac{T_{swo}}{T_{ck}}LSB_{DACV} = \frac{f_{ck}}{f_{swo}}LSB_{DACV}. \tag{24}$$

Starting from V_{low0}, the DACV output voltage is increased as the output current increases.

It must be noted that, according to (24), a number of DAC levels given by f_{ck}/f_{swo} (usually between 15 and 20) is used for generating the voltage ramp; it follows that the dynamic of DACV is correspondingly reduced. This limitation is important when AVP is implemented and it can be easily managed by suitably overestimating $I_{pk\,max}$.

The clock frequency must be sufficiently high to allow the application of the control algorithm specified by (7). Since the switching period is discrete, the minimum width of the allowed switching period variation ΔT_{sw} is given by $2T_{ck}$. Therefore

$$\frac{\Delta T_{sw}}{T_{swo}} \geq \frac{2T_{ck}}{T_{swo}} \tag{25}$$

that can be rewritten as

$$f_{ck} \geq 2\frac{f_{swo}}{\frac{\Delta f_{sw}}{f_{swo}}}. \tag{26}$$

If we consider, for example, $\Delta f_{sw}/f_{swo} = \pm 5\%$ and $f_{swo} = 1$ MHz, we obtain $f_{ck} \geq 20$ MHz. Clock frequency requirements can be easily relaxed by widening the allowed frequency interval Δf_{sw}. We are currently designing a 5-phase controller operating at 5 MHz (1 MHz/phase) with $\Delta f_{sw}/f_{swo} = \pm 7.5\%$ and a system clock frequency of 80 MHz.

Finally, the slope of the voltage ramp is designed such that its amplitude, referred to the output voltage, is comfortably higher than noise and residual voltage ripple (typically, a few tens of millivolts). In the experimental board, the slope is about $3\ 10^4$ V/s.

J. Multi-Phase Topology

A digitally controlled multiphase converter can be simply derived from the single-phase converter described above, by resorting to a master-slave architecture. Each slave (phase) is a buck converter that receives two signals from the master controller: a peak current level signal and a turn-on signal. The slave is operated in peak-current mode: it turns off when the inductor current reaches the fixed peak value I_{pk} and it turns on when it receives the corresponding signal from the master controller. The master controller senses the output voltage level and activates *one* phase each time the error voltage V_{err} intercepts the DACV output voltage. A suitable algorithm must be devised for selecting *which* phase has to be turned on at this specified time. The simplest algorithm for phase activation is based on a circular selection scheme, that is, phases are cyclically turned on. Fig. 8 shows a block diagram of a three-phase master-slave configuration based on this algorithm. The master block includes the digital controller, the D/A converters (DACI and DACV) and a DEMUX that is cyclically scanned for distributing the turn-on signals. If the are N slaves, each slave works at a switching frequency of f_{sw}/N, where f_{sw} is the frequency of the voltage ramp produced by DACV. This architecture is very flexible. An arbitrary number of slave units can be added just by increasing the number of DEMUX outputs.

A second algorithm for phase activation is based on a minimum-current rule; that is, the phase with minimum inductor current is identified and turned on at a specific time. The architecture based on this algorithm is less flexible, since additional hardware for comparing inductor currents is needed in order to select the phase to be activated. Moreover, the master unit must receive the current information from each slave. However, the corresponding overall dynamic response to load variations shows better global performances if compared to the cyclic activation solution.

From a steady-state point of view, both solutions are equivalent. The master controller sets a unique common current reference value for all the phases, thus ensuring active current sharing. Slight current variation between the phases may occur if the inductor values are different. However, (1) shows that even a 30% difference between inductors gives rise to a current unbalance of less than 10%.

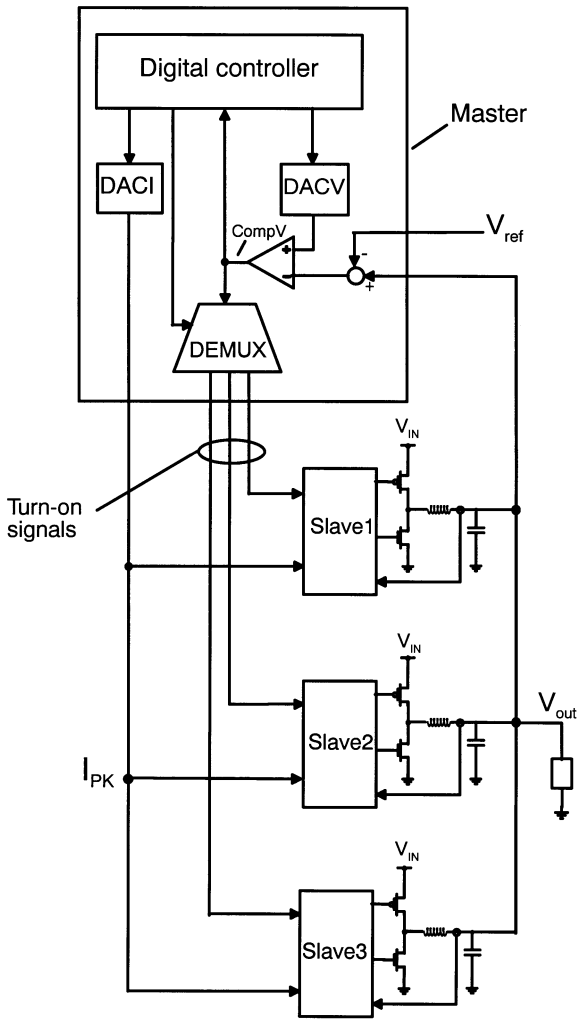

Fig. 8. Simplified block diagram of the control architecture applied to a multi-phase buck topology.

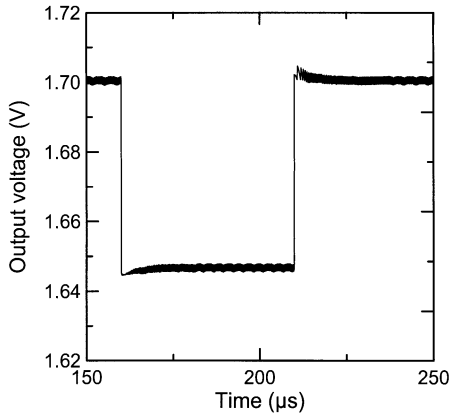

Fig. 9. Simulated output voltage response to a 60 A step load transient.

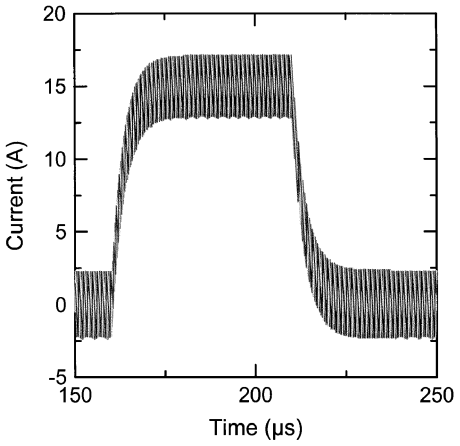

Fig. 10. Simulated response of the inductor phase currents to a 60 A step load transient.

III. Simulations

The overall control architecture applied to a four-phase buck converter has been described in the Simulink environment and extensively simulated in order to verify the analysis and to demonstrate the key features.

As a case study, we have considered a four-phase buck converter complying with VRM 9.0 specifications for desktop systems. Simulations have been performed with the following parameters: $\mathrm{V_{in}} = 12$ V; $\mathrm{V_o}$ variable from 1.1 to 1.8 V; $\mathrm{I_{out\,max}} = 60$ A (15 A/phase); $\mathrm{R_{droop}} = 0.9$ mΩ. In order to point out the ultimate performance of the proposed control architecture, we have considered optimal values for the converter parameters, that is: $\mathrm{L} = 400$ nH, $\mathrm{C} = 4$ mF, $\mathrm{ESR} = 0.9$ mΩ, $\Delta\mathrm{I} = 4.5$ A, $\mathrm{f_{swo}} = 4$ MHz (1 MHz/phase), $\Delta\mathrm{f_{sw}}/\mathrm{f_{swo}} = 10\%, \mathrm{f_{ck}} = 80$ MHz. Both DACI and DACV have a 7-b resolution. In order to verify the robustness of the algorithm particular care has been taken in the definition of the modeled system. In particular, parasitic effects have been considered (e.g., mismatches up to 10% between inductance values and associated parasitic series resistances, mismatches among sense resistances, D/A converter finite settling time and finite computational delay).

Only a few representative simulations are here reported. Fig. 9 shows the output voltage as a function of time during a step load transient of 60 A. The output voltage tolerance is always below $\pm 0.5\%$. The small oscillations clearly visible after the transients arise from the limit-cycle effect described above. As expected, the amplitude of the oscillation is of the order of 100 μV. Fig. 10 shows the phase currents as a function of time. The time constant of the exponential transients corresponds to $\mathrm{C} \cdot \mathrm{ESR} = 3.6\ \mu$s. A magnified view the current leading edge is shown in Fig. 11, where the bolded line represents the peak current level generated by DACI.

IV. Experimental Results

The digital controller was tested on a prototype four-phase buck converter having the following parameters: $\mathrm{C} = 2$ mF, $\mathrm{L_{phase}} = 600$ nH, $\mathrm{R_{droop}} = 1.25$ m$\Omega, \mathrm{f_{sw}} = 1.4$ MHz (350 kHz/phase). The ESR was estimated to be lower than 2 mΩ. The switching frequency was limited by the nonoptimal printed circuit board layout.

The control algorithm was developed in VHDL and then implemented into a FPGA device (Xilinx, Virtex XCV 50) operated at $\mathrm{f_{ck}} = 30$ MHz; the whole digital circuit requires about 2200 equivalent gates. Two D/A converters (BurrBrown

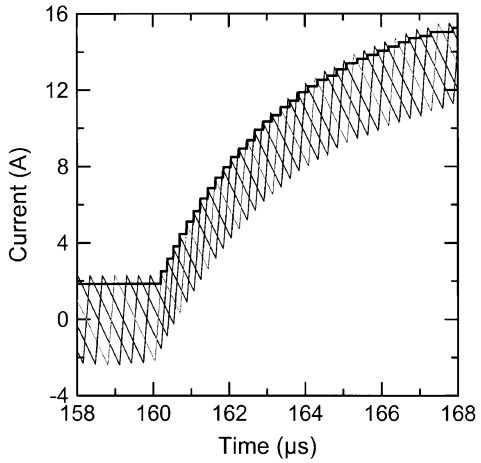

Fig. 11. Magnified view of the current leading edge. The bolded line represents the peak current level generated by DACI.

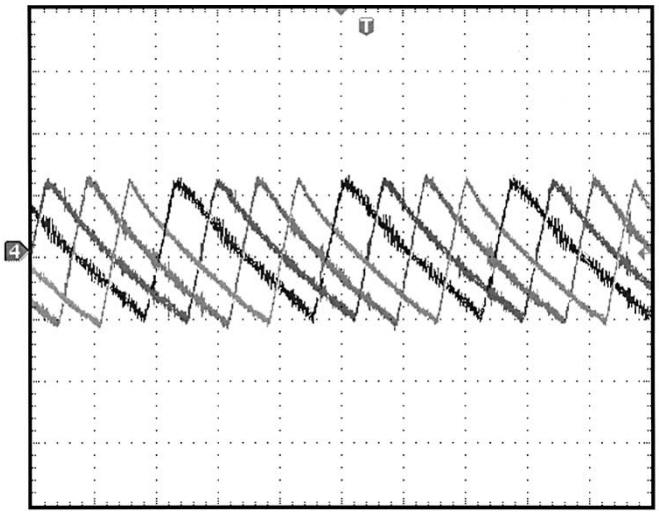

Fig. 12. Phase inductor currents measured at no-load. Time scale: 1 μs/div, vertical scale: 2.5 A/div.

DAC2904) operated at 7 b have been used for implementing DACI and DACV.

Figs. 12 and 13 show respectively the phase inductor currents and PWFM voltage waveforms at the phase nodes measured at no-load. The waveforms are quite clean; no duty cycle instabilities are observable. No substantial difference in the curve shapes is observable by varying the load between 0 and 40 A.

The transient response of the converter was evaluated by using an active load (Chroma mod.631 02) with a maximum sinkable current of 40 A. We have therefore turned-off one phase, in order to push the remaining phases close to their current limit. Fig. 14 shows the voltage ramp produced by DACV and the PWFM voltage waveforms for the three-phase configuration: the cyclical phase activation mechanism is clearly visible. By disabling one phase, the droop resistance is expected to increase by a factor 4/3. This is confirmed by the experimental result reported in Fig. 15, where a voltage step of about 66 mV is generated in response to a load transient from 0 A to 40 A. The shape of the output voltage signal is nearly ideal. The limited current slew-rate and the small undershoot on the trailing edge of the output voltage waveform are due to

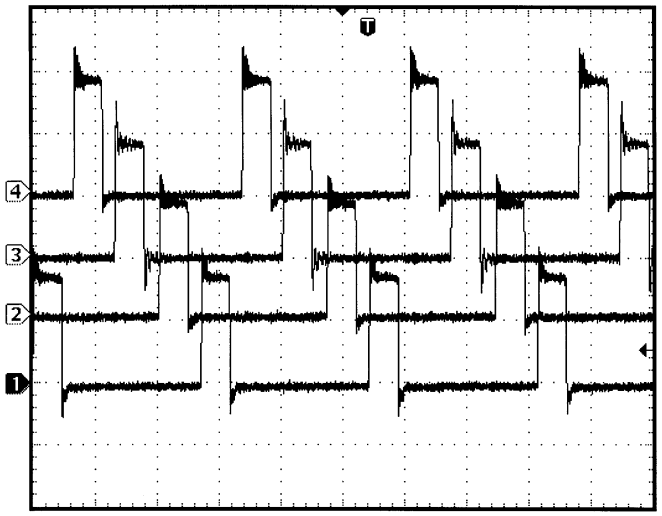

Fig. 13. PWFM waveforms of the four-phase converter measured at no-load. Time scale: 1 μs/div; vertical scale: 5 V/div.

the active load. The board layout has not been optimized either for parasitic reduction or for parasitic equalization among the phases; this may explain the relatively high voltage ripple. Nevertheless, the output voltage tolerance stays within $\pm 0.5\%$.

V. Conclusion

This paper describes a new digital controller for low-voltage, high-current dc–dc switching converters with tight requirements on output voltage regulation. The main features of the controller are:

i) fully reconfigurable digital architecture, with adaptive voltage positioning and active current sharing capabilities;
ii) reduced complexity, due to the use of low-resolution (7-b) DACs;
iii) negligible quantization effects, thanks to an original control algorithm which exploits current programming and variable frequency operation.

It must be pointed out that a traditional digital controller having the same performance would have required a 10-b DPWM and a 9 equivalent bit ADC [6]. Both these circuital blocks are by far more complex and critical and require more space than a 7-b DAC. The proposed architecture is thus suitable for high-volume, low-cost integrated dc–dc controllers.

The control algorithm was developed in VHDL and synthesized to approximately 2200 equivalent gates into a small, commercially available FPGA. For comparison, a simple 32-b full adder requires about 250 equivalent gates. The main parameters of the controller (droop/no-droop, droop value, switching frequency, switching frequency tolerance) are fully programmable. Power management algorithms such as, for example, load dependent phase activation/deactivation, can be easily implemented. The controller can support a serial transmission interface for communicating the system status and the system parameters. This feature is extremely useful for managing complex configurations, where several converters connected in parallel to increase the output current.

The overall control architecture applied to a four-phase buck converter has been simulated and experimentally verified in

order to validate the design approach and demonstrate the key features. Output voltage tolerance within $\pm 0.5\%$ was experimentally demonstrated, along with negligible limit cycling effects and fast transient response.

The features and the performance of the proposed architecture make it a valuable alternative for the control of dc–dc converters dedicated to the supply of next generation DSPs and microprocessors. A fully integrated controller/driver for a 5-phases buck converter is currently under development.

Although specifically designed for low-voltage, high-current buck converters, the digital control architecture described here can be easily adapted to other converter topologies and/or different application fields. The digital nature of the controller makes it possible to quickly customize the design and optimize system performance.

REFERENCES

[1] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE PESC'97 Conf.*, 1997, pp. 21–27.

[2] A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, "High-efficiency multiple-output dc-dc conversion for low voltage systems," *IEEE Trans. VLSI Syst.*, vol. 8, pp. 252–263, June 2000.

[3] A. Prodic, D. Maksimovic, and R. Erickson, "Design and implementation of a digital PWM controller for a high-frequency switching dc-dc power converter," in *Proc. IEEE IECON'01 Conf.*, 2001, pp. 893–898.

[4] A. M. Wu, J. Xiao, D. Markovic, and S. R. Sanders, "Digital PWM control: Application in voltage regulation modules," in *Proc. IEEE PESC'99 Conf.*, 1999, pp. 77–83.

[5] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," in *Proc. IEEE PESC'01 Conf.*, 2001, pp. 465–471.

[6] J. Xiao, A. V. Peterchev, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," in *Proc. IEEE PESC'01 Conf.*, 2001, pp. 38–47.

[7] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital controller IC for dc-dc converter," in *Proc. IEEE APEC'02 Conf.*, 2002, pp. 374–380.

[8] J. A. Abu-Qahouq, M. Pongratananukul, I. Batarseh, and T. Kasparis, "Multiphase voltage-mode hysteretic controlled VRM with DSP control and novel current sharing," in *Proc. IEEE APEC'02 Conf.*, 2002, pp. 663–669.

[9] A. Burstein and A. Schultz, "Method and Apparatus for Digital Voltage Regulation," U.S. Patent 6 100 676, 2000.

[10] A. Burstein, A. Stratakos, W. Clark, D. Lidsky, and C. Sullivan, "Digital Voltage Regulator Using Current Control," U.S. Patent 6 268 716, 2001.

[11] "Special Issue on Digital Control in Power Electronics," *IEEE Trans. Power Electron.*, vol. 18, pp. 293–503, Jan. 2003.

[12] Intel, Inc., "VRM9.1 DC–DC Converter Design Guidelines," Tech. Rep., Intel, Jan. 2002.

[13] S. Saggini, M. Ghioni, A. Geraci, and F. Villa, "Controllore digitale per convertitori dc–dc a commutazione," Italian Patent Application MI 2002A 001539, 2002.

[14] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE APEC'98 Conf.*, 1998, pp. 170–176.

[15] R. W. Erikson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Boston, MA: Kluwer, 2000.

Stefano Saggini was born in Savona, Italy, in 1975. He received the M.S. degree in electronic engineering from the Politecnico di Milano, Italy, in 2002 where he is currently pursuing the Ph.D. degree in information engineering.

His research interests include the design of digital controllers for low-voltage, high-current, dc–dc converters.

Massimo Ghioni (M'91) was born in Monza, Italy, in 1962. He received the Laurea degree in nuclear engineering from the Politecnico di Milano, Italy, in 1987.

Since 1990, he has been with the Department of Electronics and Information, Politecnico di Milano, where he is currently Full Professor of electronics. In 1992, he was Visiting Scientist at the IBM T.J. Watson Research Center, Yorktown Heights, NY, where he worked on silicon photodetectors for integrated optical receivers. He has given contributions to the development of solid-state single-photon detectors and associate electronics for applications in physics, astronomy, and molecular biology. His current research interests include the design of integrated circuits for power amplification and dc–dc conversion.

Angelo Geraci (M'00) was born in Milano, Italy, in 1967. He received the Laurea degree (with honors) in electronic engineering and the Ph.D. degree in electronics and communication engineering from the Politecnico di Milano, Milan, Italy, in 1993 and 1996, respectively.

He has been Assistant Professor with the Department of Electronics and Information (DEI), Politecnico di Milano, since March 1999.