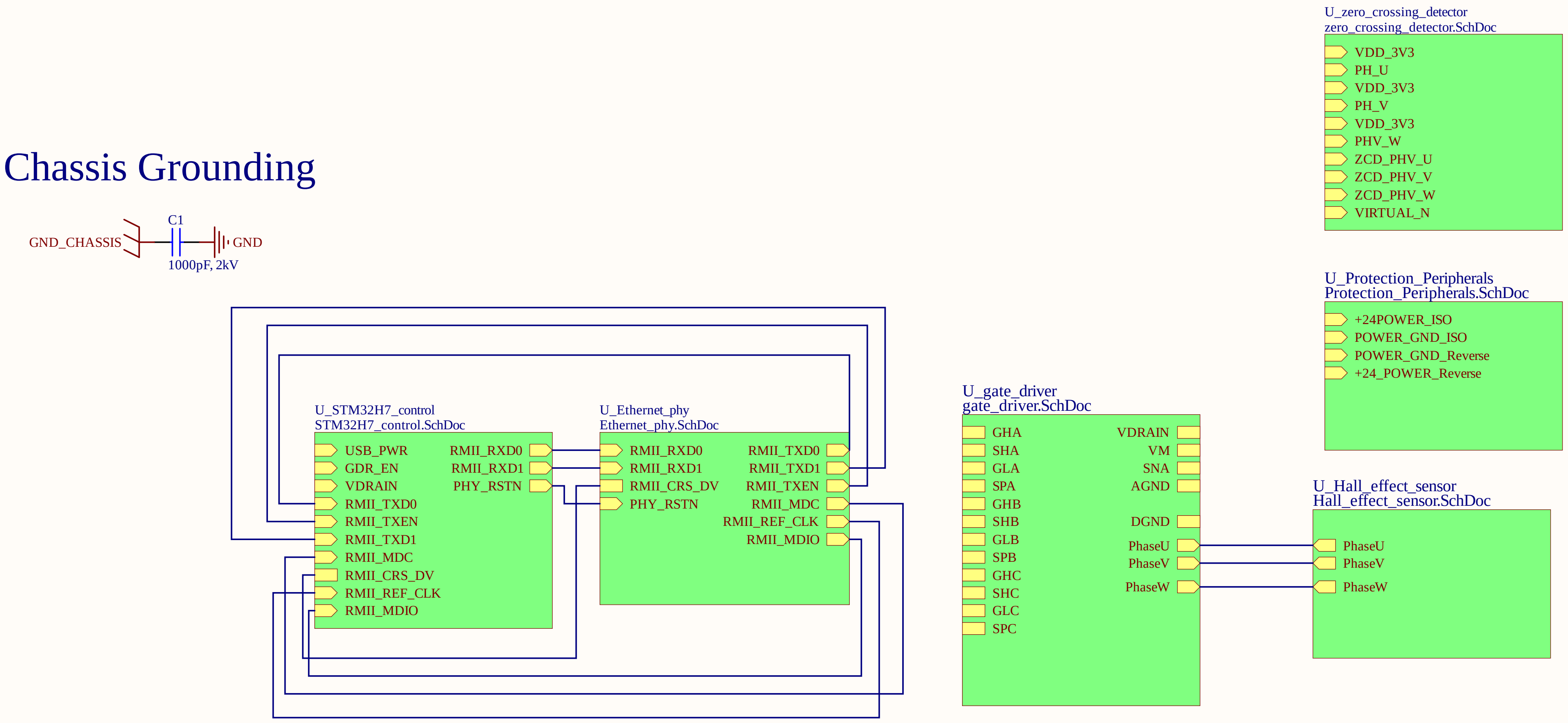
MCAV ESDA ELECTRICAL

Chassis Grounding



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PROJECT

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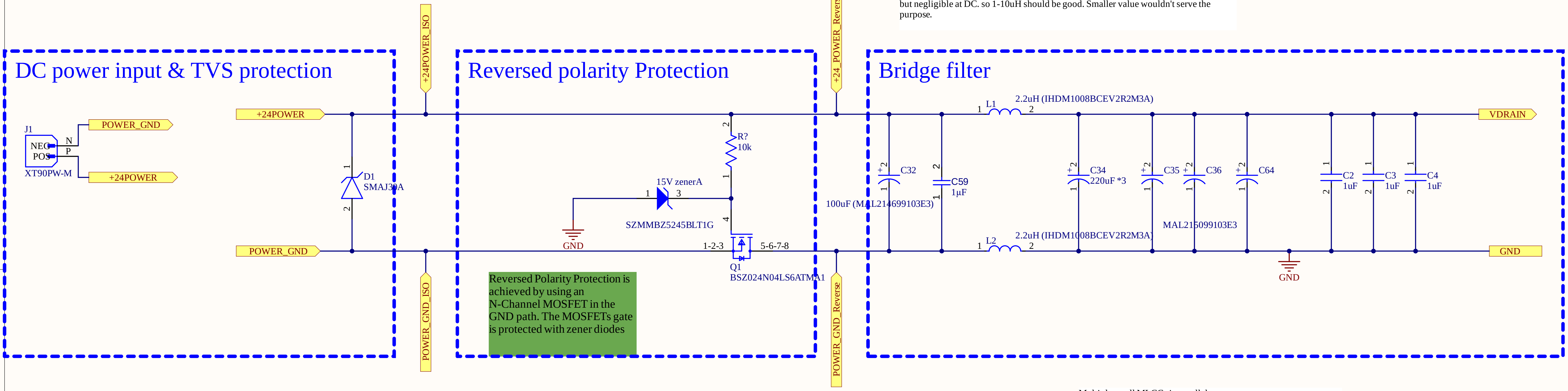
FILE NAME ESC_PCB_V2_Top_Level.SchDoc

SHEET 1 OF 11

3. Inductance value L
Since we are not building a precision filter, we just want some impedance at “fast stuff” but negligible at DC. so 1-10uH should be good. Smaller value wouldn't serve the purpose.



Multiple small MLCCs in parallel:

ESR (effective series resistance) goes down

ESL (effective series inductance) goes down

So the rail looks like a lower-impedance source over a wider frequency range than a single cap could provide.

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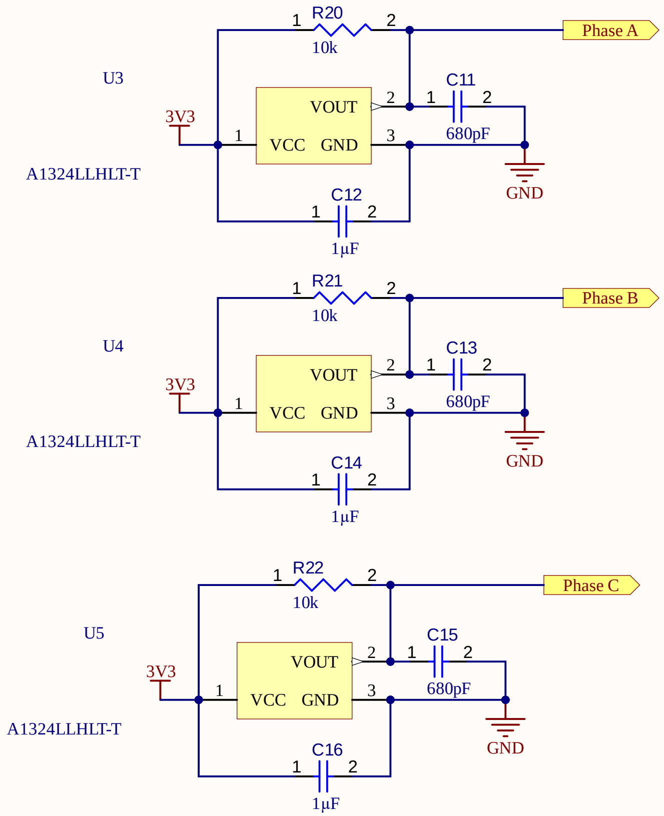
File: Protection_Peripherals.SchDoc		Drawn By:



Hall effect sensor implementation. Different chip symbol model used here and needs to be changed to TMAG5115 from Ti

Table 8-2. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a pin on the TMAG5115 device, but a REF supply-voltage pullup is required for the OUT pin. The OUT pin may be pulled up to V_{CC}.

8.2.1.2.1 Configuration Example

In a 3.3-V system, $3.0V \le V_{ref} \le 3.6$ V. Use Equation 2 to calculate the allowable range for R1.

$$\frac{V_{ref}\ \text{max}}{30\ \text{mA}} \le R1 \le \frac{V_{ref}\ \text{min}}{100\ \mu\text{A}} \tag{2}$$

For this design example, use Equation 3 to calculate the allowable range of R1.

$$\frac{3.4\ \text{V}}{30\ \text{mA}} \le R1 \le \frac{3.2\ \text{V}}{100\ \mu\text{A}} \tag{3}$$

Therefore:

$$120\ \Omega \le R1 \le 30\ \text{k}\Omega \tag{4}$$

After finding the allowable range of R1 (Equation 4), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 5 to calculate the value of C2.

$$2 \times f_{BW}\ (\text{Hz}) < \frac{1}{2\pi \times R1 \times C2} \tag{5}$$

For this design example, use Equation 6 to calculate the value of C2.

$$2 \times 10\ \text{kHz} < \frac{1}{2\pi \times R1 \times C2} \tag{6}$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

A selection of R1 = 10 kΩ and C2 = 680 pF can cause a low-pass filter with a corner frequency of 23.4 kHz.

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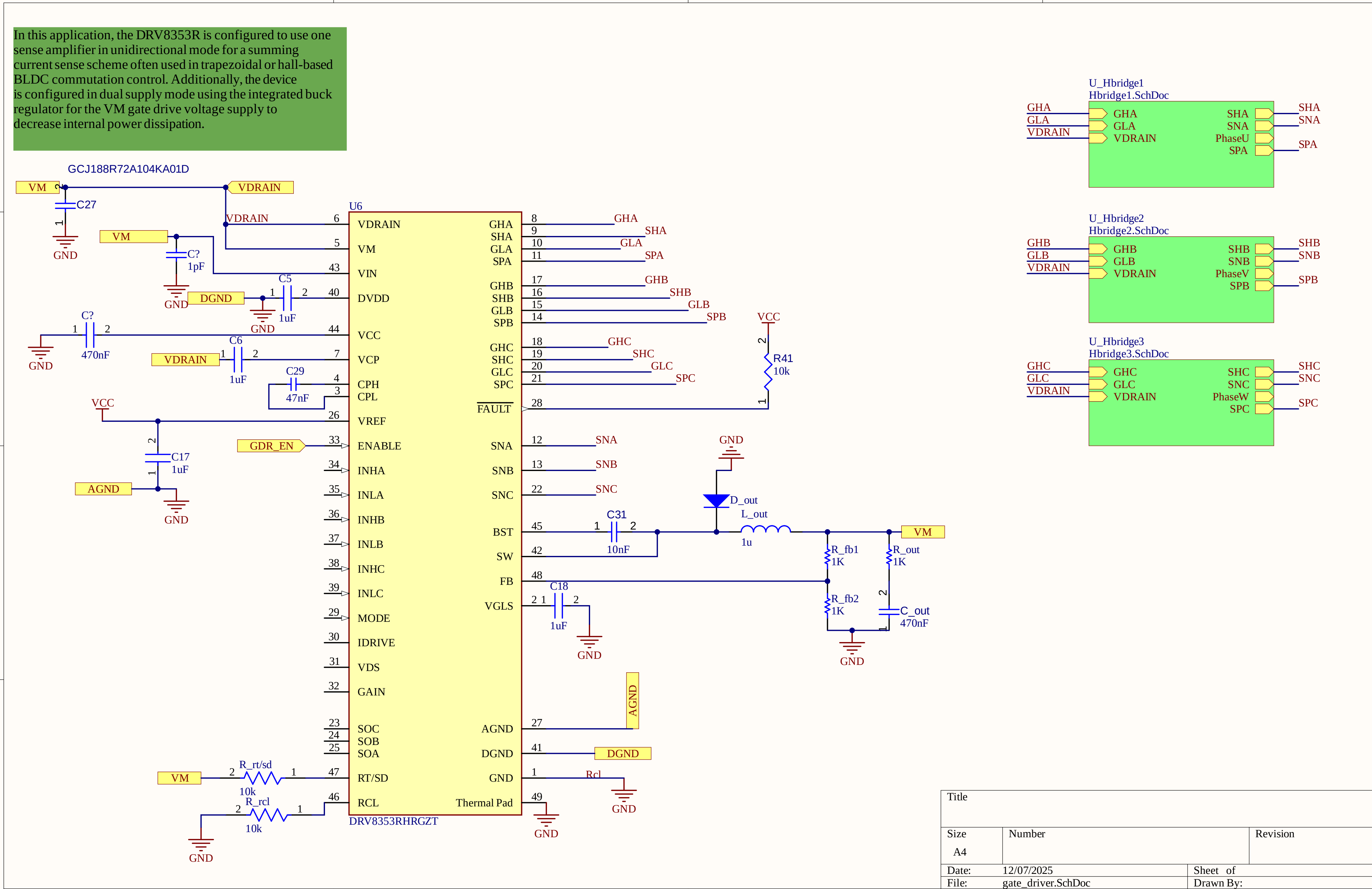
File: Hall_effect_sensor.SchDoc		Drawn By:


In this application, the DRV8353R is configured to use one sense amplifier in unidirectional mode for a summing current sense scheme often used in trapezoidal or hall-based BLDC commutation control. Additionally, the device is configured in dual supply mode using the integrated buck regulator for the VM gate drive voltage supply to decrease internal power dissipation.
GCJ188R72A104KA01D
VM
VDRAIN
C27
GND
U6
DRV8353RHRGZT
VDRAIN
VM
VIN
DVDD
VCC
VCP
CPH
CPL
VREF
ENABLE
INHA
INLA
INHB
INLB
INHC
INLC
MODE
IDRIVE
VDS
GAIN
SOC
SOB
SOA
RT/SD
RCL
GHA
SHA
GLA
SPA
GHB
SHB
GLB
SPB
GHC
SHC
GLC
SPC
FAULT
SNA
SNB
SNC
BST
SW
FB
VGLS
AGND
DGND
GND
Thermal Pad
C? 1pF
C5 1uF
DGND
C? 470nF
C6 1uF
C29 47nF
VCC
C17 1uF
AGND
GDR_EN
R41 10k
C31 10nF
D_out
L_out 1u
R_fb1 1K
R_fb2 1K
R_out 1K
C_out 470nF
C18 1uF
R_rt/sd 10k
R_rcl 10k
Rcl
U_Hbridge1
Hbridge1.SchDoc
PhaseU
U_Hbridge2
Hbridge2.SchDoc
PhaseV
U_Hbridge3
Hbridge3.SchDoc
PhaseW
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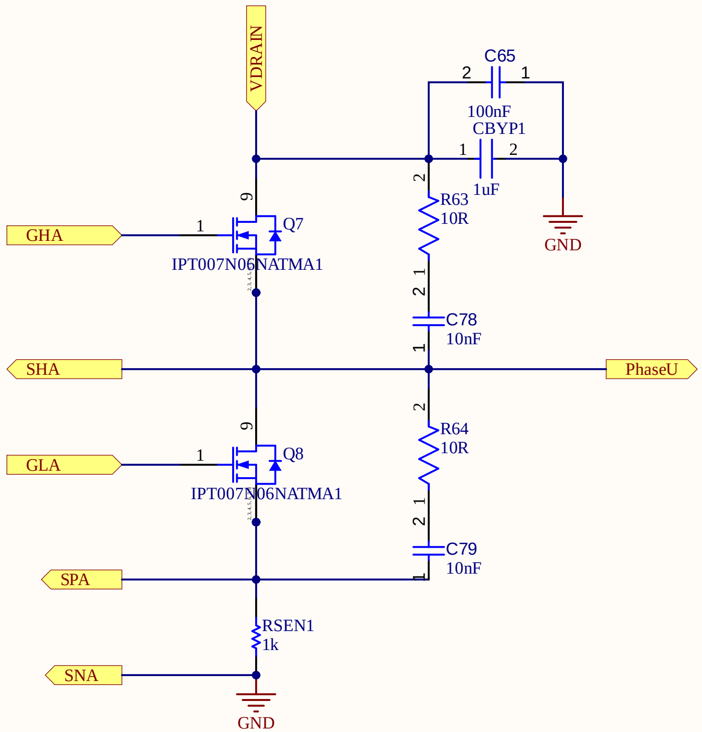

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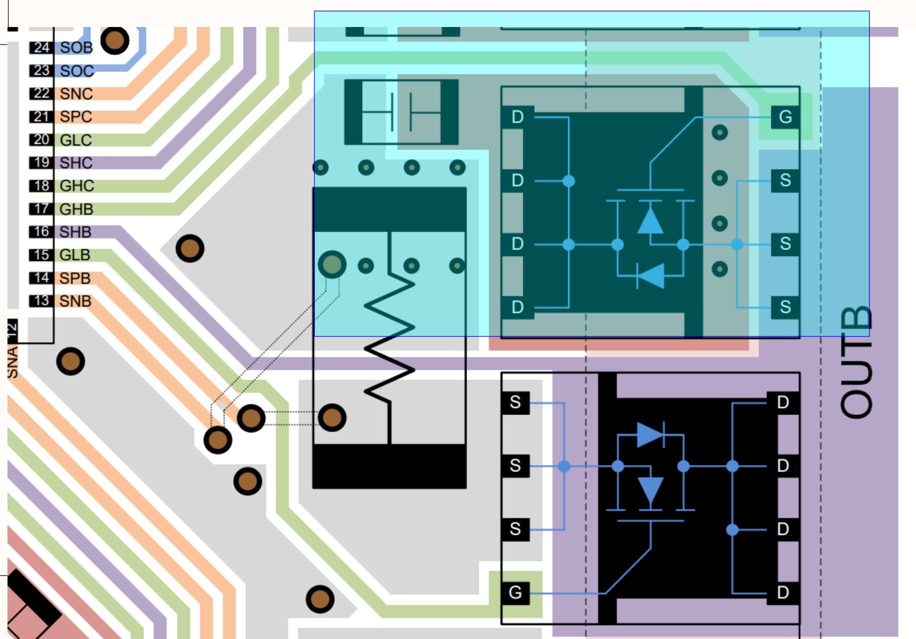
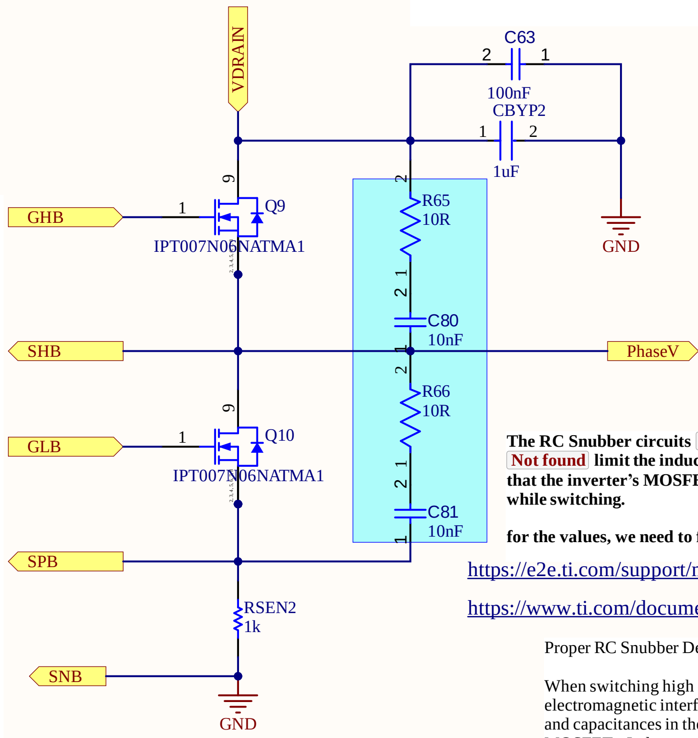
Take a look at the example design from datasheet, I circled the upper half of the bridge, which we can see that a bypass capacitor is connected to ground, which is done on the top right corner on the schematic CBYP2

The other big chunk is the shunt resistor RSEN2 , with its value requiring a double check, which doesn't seem to have a cap in parallel



CBYP2 together with the cap in parallel act as decouplig capacitors, responsible for mid range frequencies and high frequencies respectively. These are just universal values

(might need to look into videos about decoupling capacitors for better options)



The RC Snubber circuits Not found Not found limit the inductive voltage spikes that the inverter's MOSFETs experience while switching.

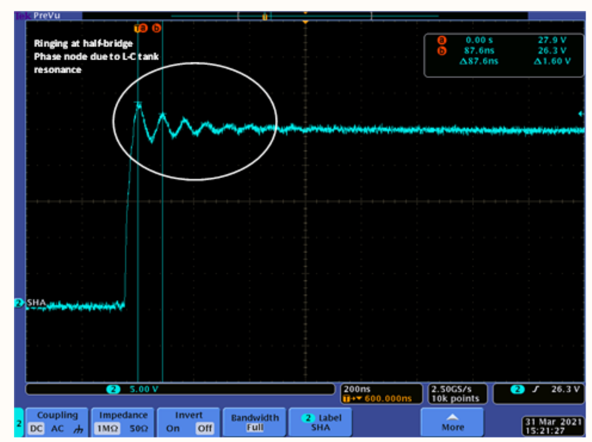
for the values, we need to follow 7-step

https://e2e.ti.com/support/motor-drivers-group/motor-drivers/f/motor-drivers-forum/991693/faq-proper-rc-snubber-design-for-motor-drivers?tisearch=e2e-sitesearch&keymatch=rc%20snu

https://www.ti.com/document-viewer/lit/html/SSZTBC7

Proper RC Snubber Design

When switching high currents through external power MOSFETs to commutate a BLDC motor, ringing can occur, leading to concerns in electromagnetic interference (EMI), circuit jitter, excessive power dissipation, and overstressing components. This is often due to parasitic inductances and capacitances in the Printed Circuit Board (PCB), specifically in the high-current-carrying phase nets between the high-side and low-side MOSFETs. Inductors and capacitors form an inductor-capacitor (L-C) tank circuit, resulting in resonance during switching events.



In order to mitigate the ringing at the phase output, a simple resistor-capacitor (R-C) snubber circuit can be used to "snub", or dampen the oscillations. By removing the oscillations, this will reduce potential EMI and increase the longevity of the MOSFETs by reducing voltage overstress. The R-C snubber is placed in parallel as close as possible to each MOSFET's drain and source connections.

To calculate the resistor (Rsnub) and capacitor (Csnub) values of the R-C snubber circuit, we will use a 7-step procedure that shifts the resonant frequency of the MOSFET ringing to calculate the circuit's parasitic capacitance (C0) and inductance (L). Once those are known, they will be used to derive the values of the R-C snubber. The example shown uses the RC snubber next to the CSD18540Q5B MOSFETs (Qgd = 6.8nC) of the DRV8343-Q1 EVM.

Seven steps to calculate R-C Snubber (with Example)		
Steps	**Description**	**Example**
Step 1	Measure the oscillation frequency (f_o) of the V_{DS} ringing with no RC snubber. See Figure 3.	$f_0 = \frac{1}{82ns} = 12.2\ MHz$
Step 2	Add a capacitor (C_1) in parallel with the rectifier or FET and measure the shifted oscillation frequency (f_1). Select a C_1 value that is several times larger than the rectifier's stated typical capacitance at full-reverse voltage in the datasheet. In this example, the rectifier's capacitance is 22pF, so I chose a 100pF value for C_1. A frequency shift of at least 50% is reasonable. See Figure 4.	$C_1 = 100pF$ $f_1 = \frac{1}{90ns} = 11.1MHz$
Step 3	Calculate the frequency shift ratio: $m = \frac{f_0}{f_1}$	$m = \frac{12.2\ MHz}{11.1\ MHz} = 1.1$

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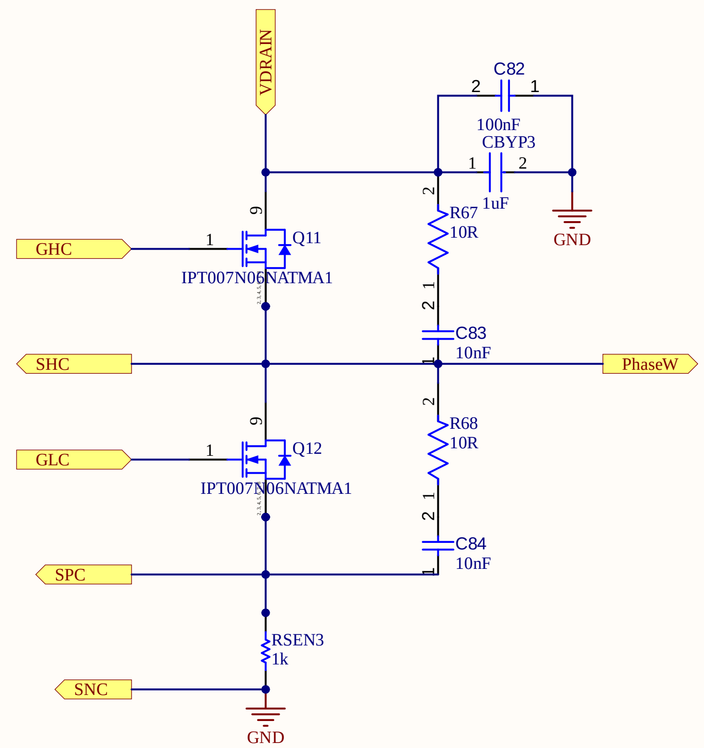
Hbridge2.SchDoc	Drawn By:



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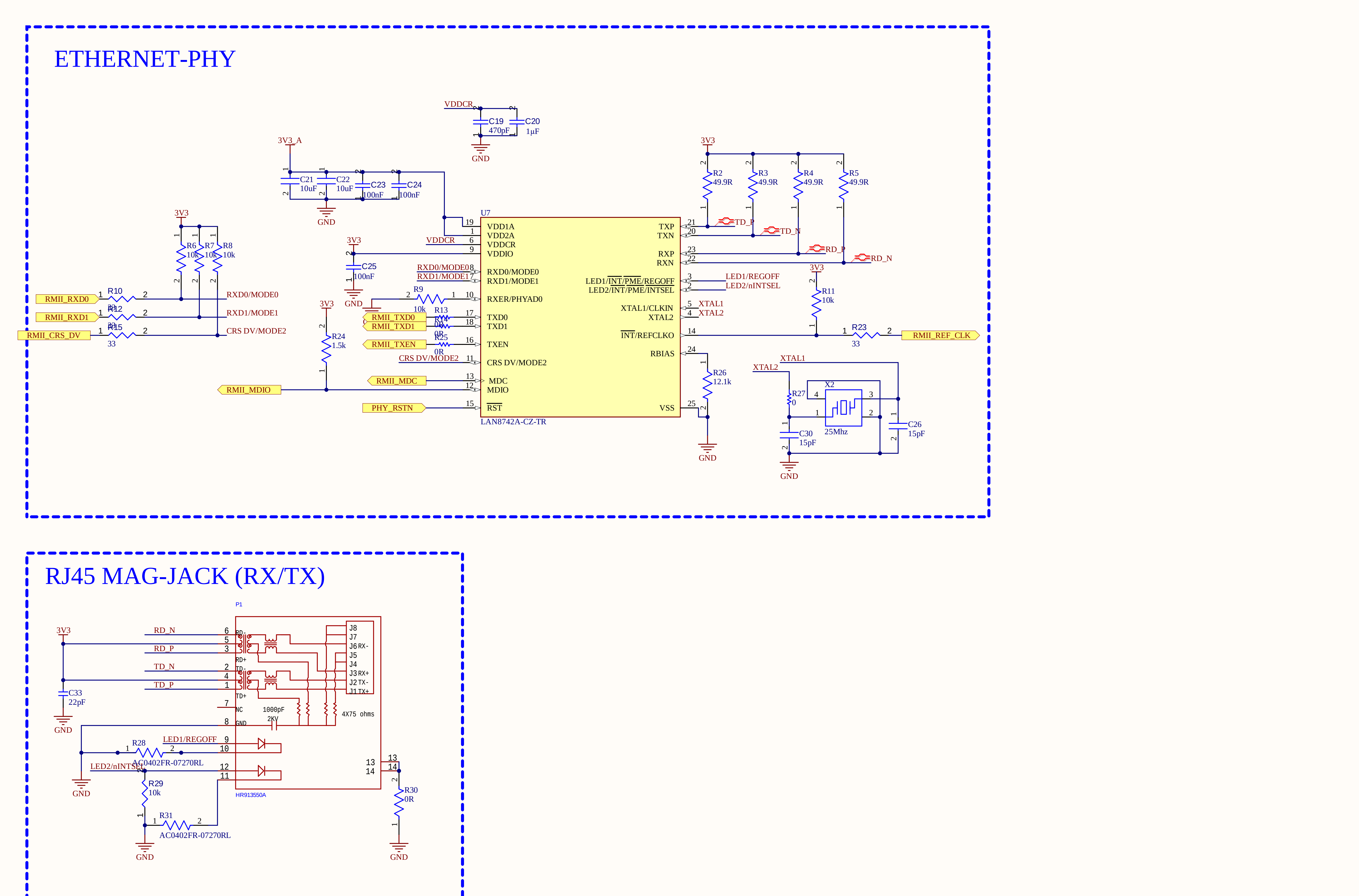

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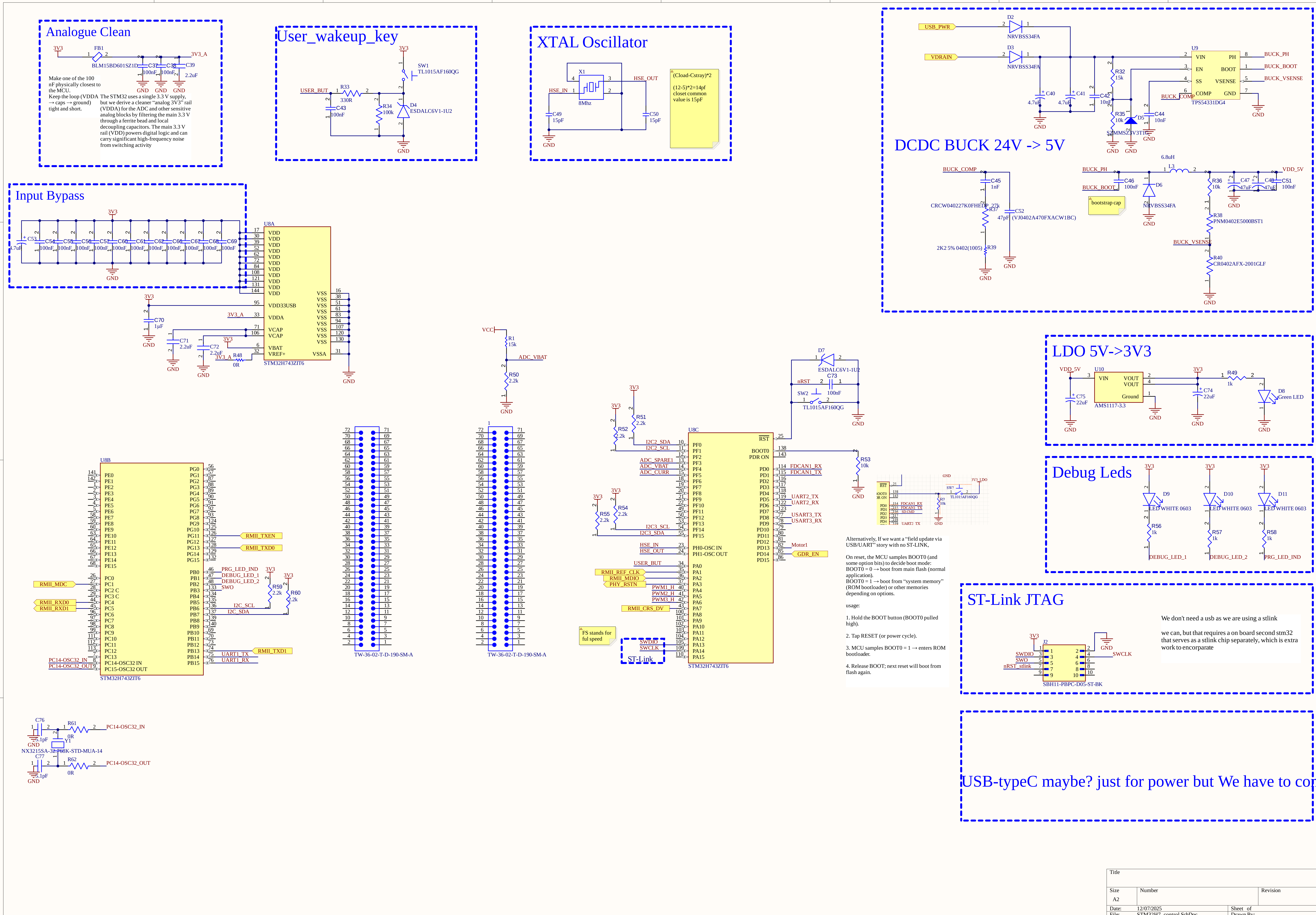

Analogue Clean
Make one of the 100 nF physically closest to the MCU.
Keep the loop (VDDA → caps → ground) tight and short.
The STM32 uses a single 3.3 V supply, but we derive a cleaner "analog 3V3" rail (VDDA) for the ADC and other sensitive analog blocks by filtering the main 3.3 V through a ferrite bead and local decoupling capacitors. The main 3.3 V rail (VDD) powers digital logic and can carry significant high-frequency noise from switching activity
User_wakeup_key
XTAL Oscillator
(Cload-Cstray)*2
(12-5)*2=14pf
closet common value is 15pF
DCDC BUCK 24V -> 5V
bootstrap cap
Input Bypass
LDO 5V->3V3
Debug Leds
STM32H743ZIT6
TW-36-02-T-D-190-SM-A
Alternatively, If we want a "field update via USB/UART" story with no ST-LINK.
On reset, the MCU samples BOOT0 (and some option bits) to decide boot mode:
BOOT0 = 0 → boot from main flash (normal application).
BOOT0 = 1 → boot from "system memory" (ROM bootloader) or other memories depending on options.
usage:
1. Hold the BOOT button (BOOT0 pulled high).
2. Tap RESET (or power cycle).
3. MCU samples BOOT0 = 1 → enters ROM bootloader.
4. Release BOOT; next reset will boot from flash again.
FS stands for ful speed
ST-Link
ST-Link JTAG
We don't need a usb as we are using a stlink
we can, but that requires a on board second stm32 that serves as a stlink chip separately, which is extra work to encorparate
USB-typeC maybe? just for power but We have to consid
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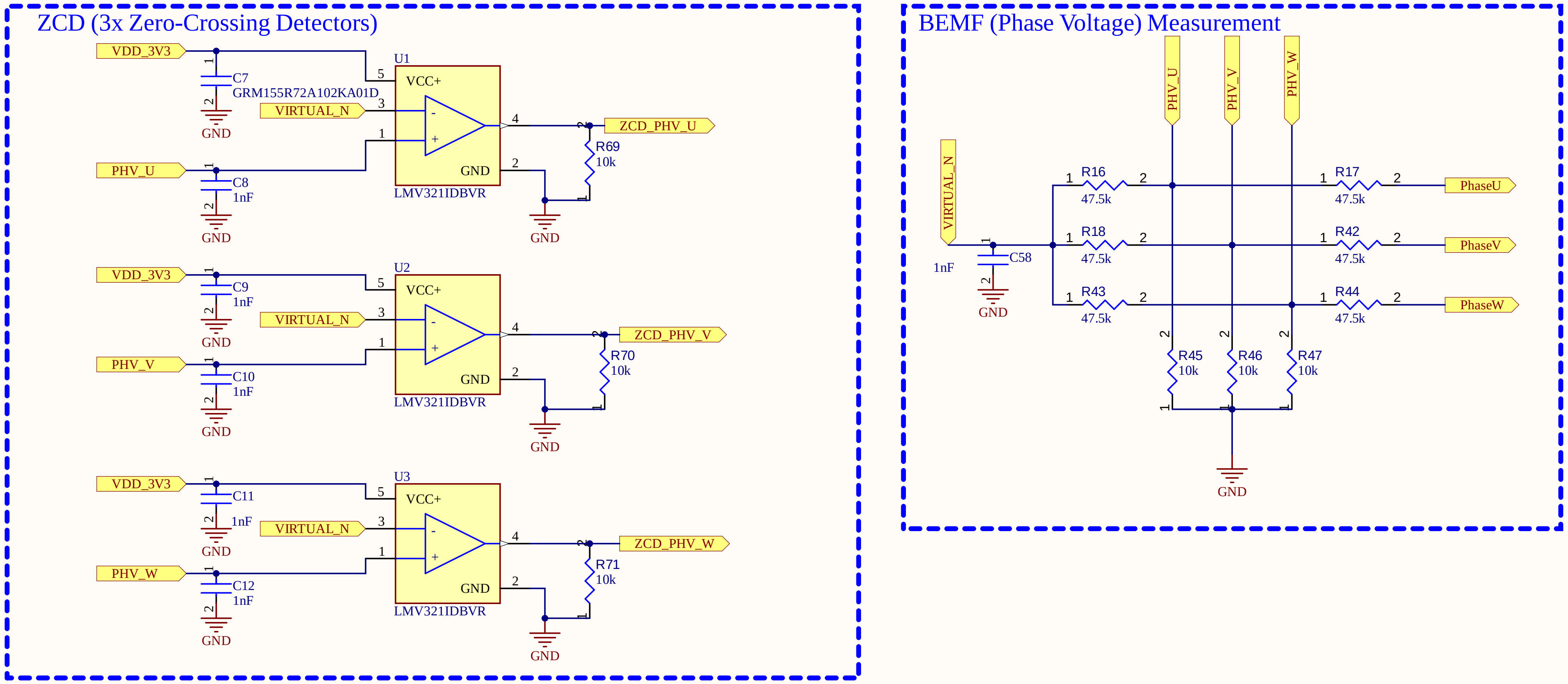

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File:	zero_crossing_detector.SchDoc	Drawn By:	