XIAO ZHONG

Address: 2407 Saratoga dr, state college, PA 16801

(814) 876-2136 | xiaohardwork009@gmail.com | linkedin.com/in/xiao-zhong-6b8b34119

EDUCATION

UNIVERSITY OF PENNSYLVANIA | Philadelphia, PA — August 2021-December 2022
Degree: Master Major: Master of science in Engineering - Electrical Engineering — GPA: 3.6
THE PENNSYLVANIA STATE UNIVERSITY | State College, PA — August 2015-May 2019
Degree: Bachelor Major: Bachelor of science in Engineering- Electrical Engineering | Minor: Math — GPA: 3.4

TECHNICAL SKILLS / CERTIFICATION

Program Language: C, C++, Verilog, Python, Matlab, and Object oriented programming
Robotic skills: Forward and backward algorithm, kalman filter, and policy iteration algorithm
Embedded Skills: stm32fxxx series board programming, arduino programming, and esp32 programming
SOC: Vitis/OpenCL use to validate and program code on ultra96 board CPU and accelerator
Machine learning: Skills:SGD, MLP , CNN, DNN, quantization and pruning skill, and Lottery ticket hypothesis
Network System Skills: Internet packet analysis project , TCP/UDP Analyze using Wireshark and WiFi and LTE Simulations project
Electrical skills: Oscilloscope, multimeter, Cadence circuit design, and basic for VLSI

PROFESSIONAL EXPERIENCE

CANNON INSTRUMENT, Embedded Engineer | State College, PA — May 2019 - June 2021

- Investigated with team of two for Lapping Machine Project including programming UI design and OOP for motor and sensor control, and developing IOT which result in 24-hour automatic working process that eliminate the need for continuous human resource involvement
- Built an individual network system on ESP32 by using console to features including DAC, wifi connection, IOA and web browser, programmed FREERTOS operating system on ESP32 in order to fulfill company future development feature
- Crated Motor testing Case for checking motor statues, including electric design upgrade, component pick and programming for motor control, PWM output, and screen display which increase the development process for product with less mechanical issue (30% error)

ROBOMASTER COMPETITION, Team Lead | State College, PA — November 2017- April 2019

- Designed machine car that can lift up bullet box with pneumatic system and drag another car to specific position, and anothe car that can track target automatically with a bullet shooting system on top with gimbal
- Built a circuit system and implemented code that can use two stm32 boards to communicate and satisfy all machine functions including classic, gimbal system with Freertos

RELATED PROJECT

SYSTEM ON CHIP(SOC), Course Project | Philadelphia, PA — August 2021-December 2021

- Approached thread parallel, compiler optimization and SIMD on Ultra96 board CPU, used automatic vectorization to generate NEON instructions from loops to boost the running speed
- Mapped code on FPGA board to do CPU implementation and used HLS kernel optimization (hardware) to mapped code on accelerator using Vitis and OpenCL, and used Vitis analyzer to observe computation
- Teamed up with two team members to develop a compressor that can receive ethernet input in real time and compress it into memory through various functions. Designed two designs : single ARM processor mapped design and Ultra96 accelerator mapped design from different axis approaches including choice of hardware target,multi thread, loop unrolling,pipeline and data reused. Observed result from Viti s analyzer and successfully boosted the throughput to be 7.09311Mb/s. （eight time faster than before)

COMPUTER ORGANIZATION AND DESIGNATION, Course Project | Philadelphia, PA — January 2022-May 2022

- Designed and implemented a pipelined processor for a simple RISC ISA using Verilog
- Improved the design with architectural techniques used in modern CPU design including superscalar design

DIGITAL INTERGRATE CIRCUITS AND VLSI, Course Project | Philadelphia, PA — August 2022—December 2022

- Explored the design involved realizaion of integrated circuit from device up to the register/subsystem level that includes the study of MOS device characteristics, the critical interconnect and gate characteristics which determine the performance of VLSI circuits, and NMOS/ CMOS logic design
- Designed the circuit-level implementation of a configurable logic block (CLB) comprised of a single basic logic element (BLE) using LUT which includes shift register for input and SRAM to store data by Cadence

WIRELESS COMMUNICATION AND IOT, Course Project | Philadelphia, PA — August 2021—December 2021

- Coded an internet packet analysis tool to capture and do TCP analyze including session count, IP, user traffic bytes sent
- Designed downlink traffic aggregation mechanism at the IP layer to utilize both the LTE and WIFI networks simultaneously. Redesign the throughput aggregation algorithm to increase the throughput
- Implemented and set up an end-to-end IOT monitoring service with LoRA client and LoRaWAN gateway services using simulation in software emulator. Used TTN as network and application server, Thingspeak web as MQTT broker and local

LEADERSHIP

MAIN CHAIR AT CSSA ACADEMIC DEPARTMENT Team Lead | State College, PA — April 2018 – March 2019

- Worked as Chief editor of CSSA 2018 new student guide book
- Led 2018 Chinese new student orientation in 14 main cities in China with at least 50 to 200 new students in each

FOUNDER OF ROBOX CLUB, Team Lead | State College, PA — November 2017 – April 2019

- Built a Robot Team in 2019 Robomaster International Competition and Won the Sixth Place