

CY8CKIT-062S2-AI PSoC™ 6 AI Evaluation Board

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Drawing Numbers

PCBA	121-60699-01
PCB	600-60699-01
FAB DRW	610-60699-01
ASSY DRW	620-60699-01
SCH DRW	630-60699-01

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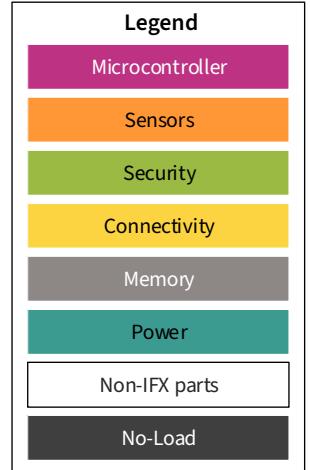
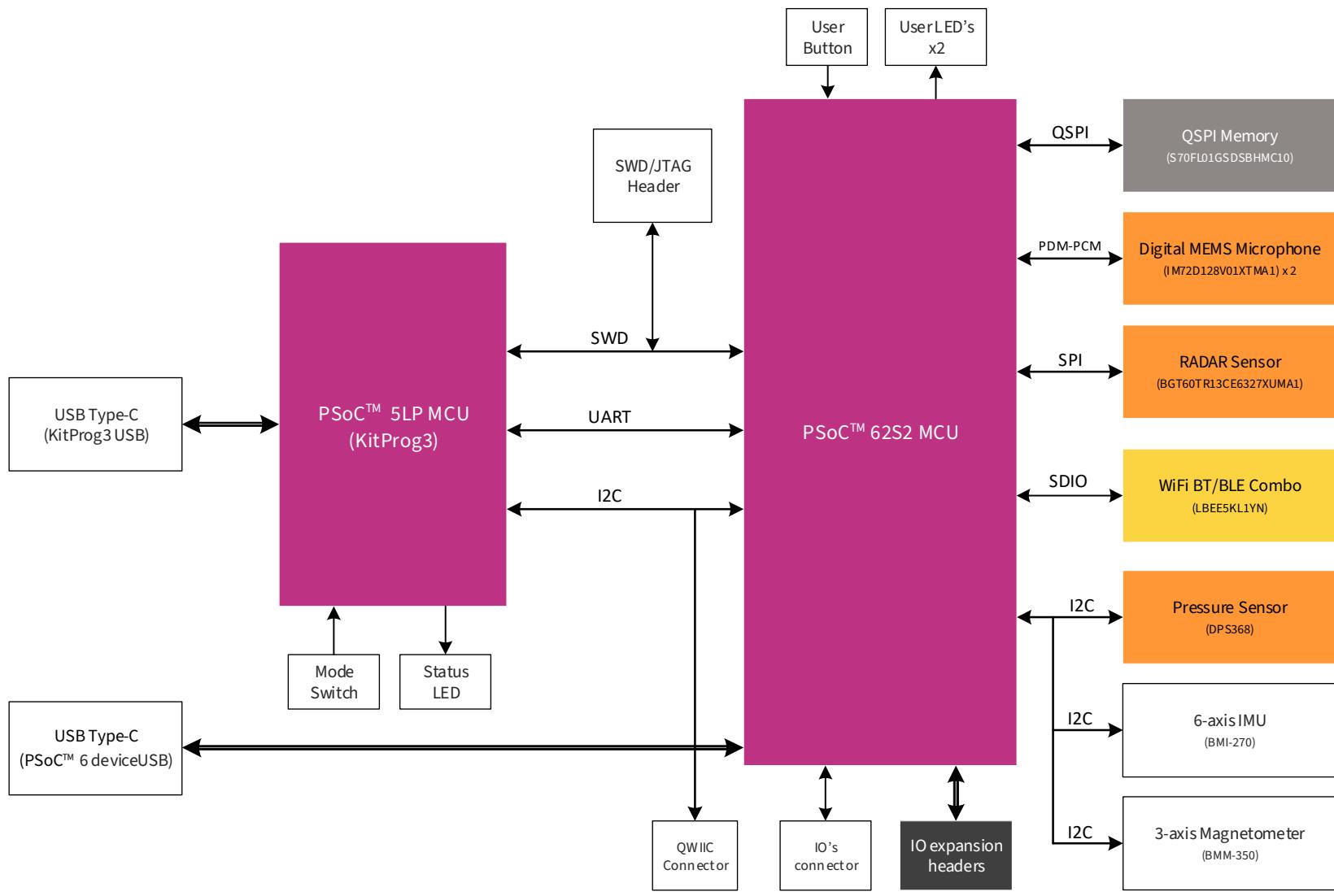


SCH Title : PSoC™ 6 AI Evaluation Board

Page Title: Title Page

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Functional Block Diagram



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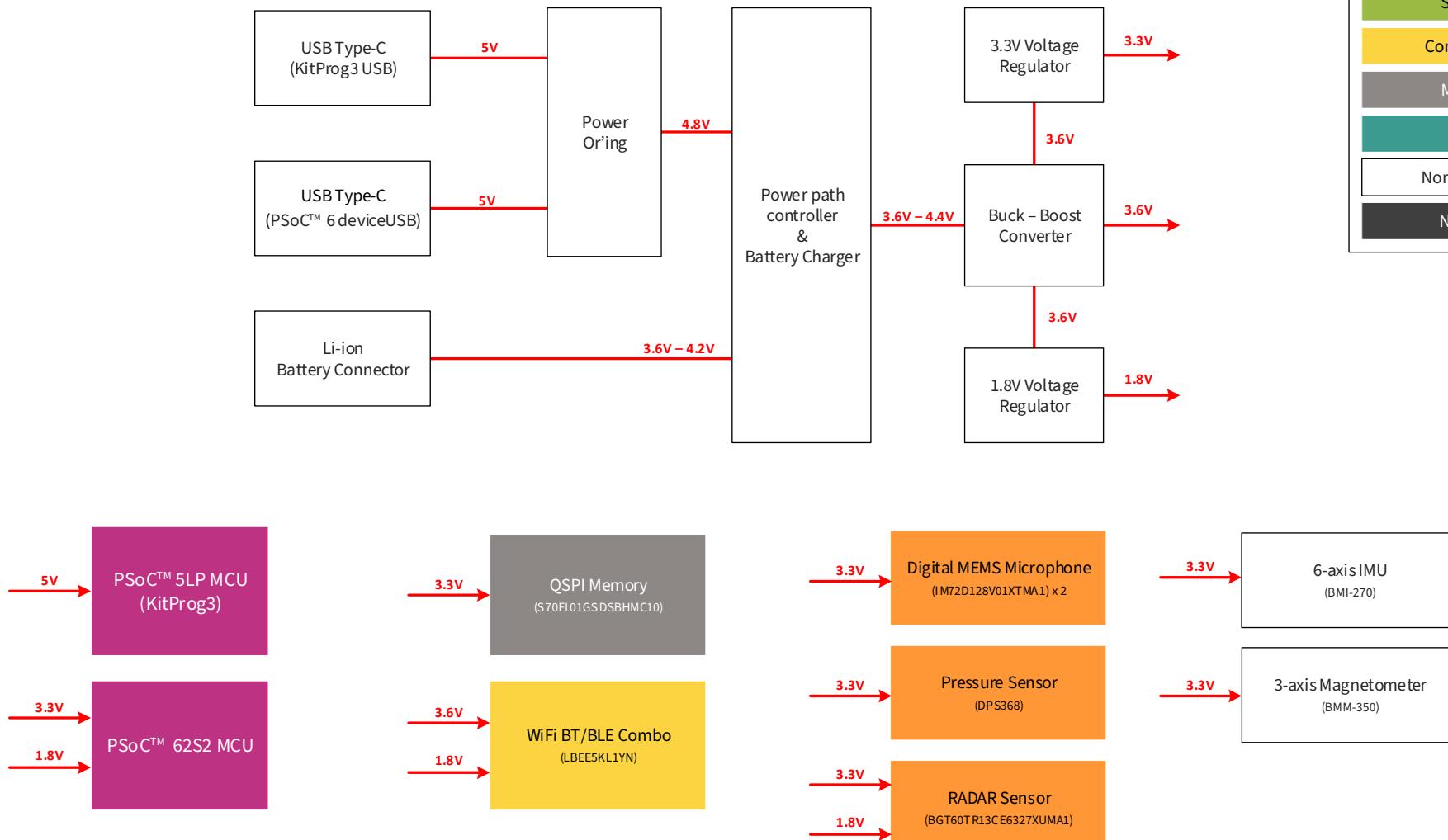
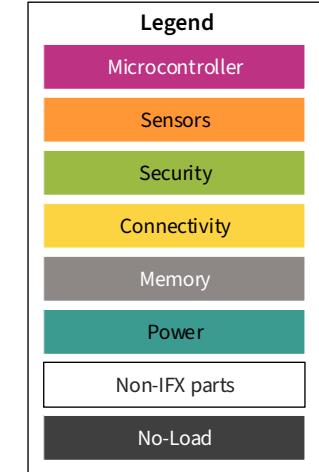
Page Title: Functional Block Diagram

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Power Block Diagram



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Page Title: Power Block Diagram

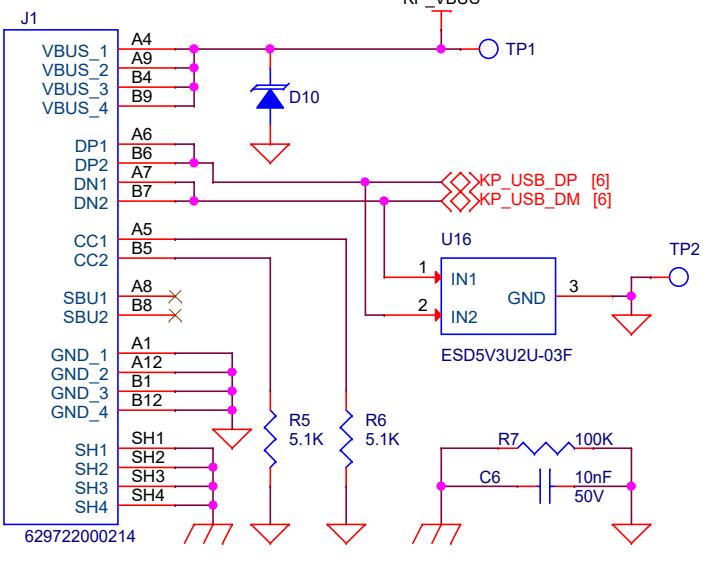


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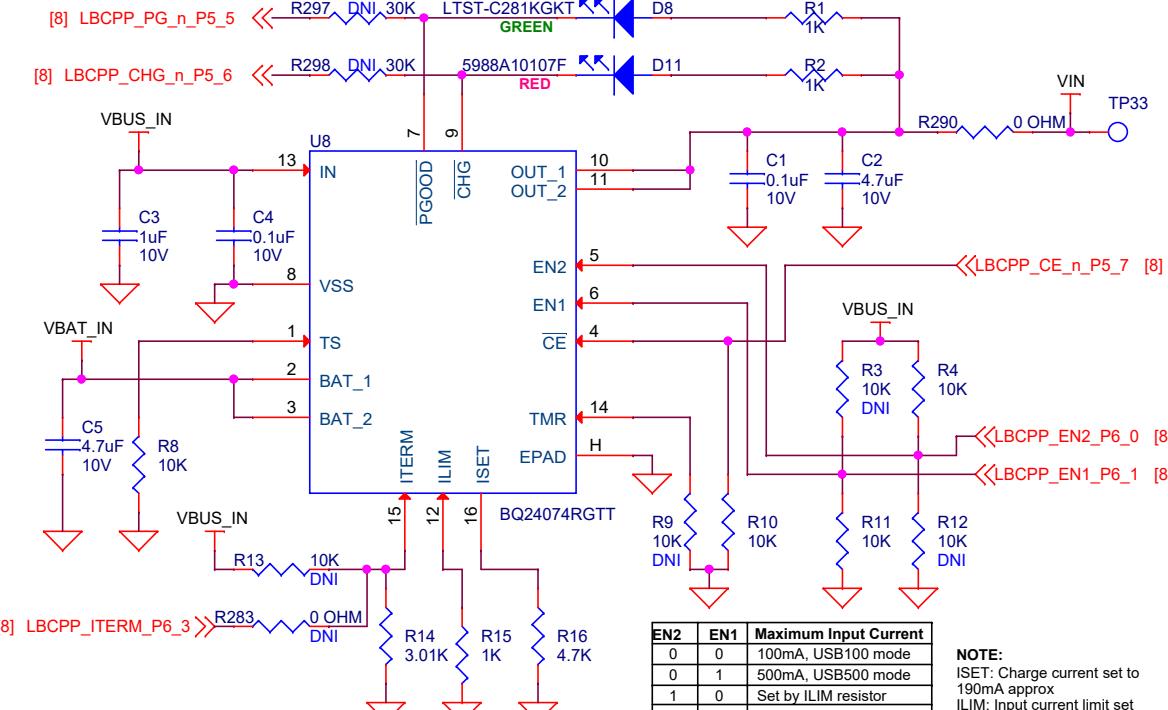
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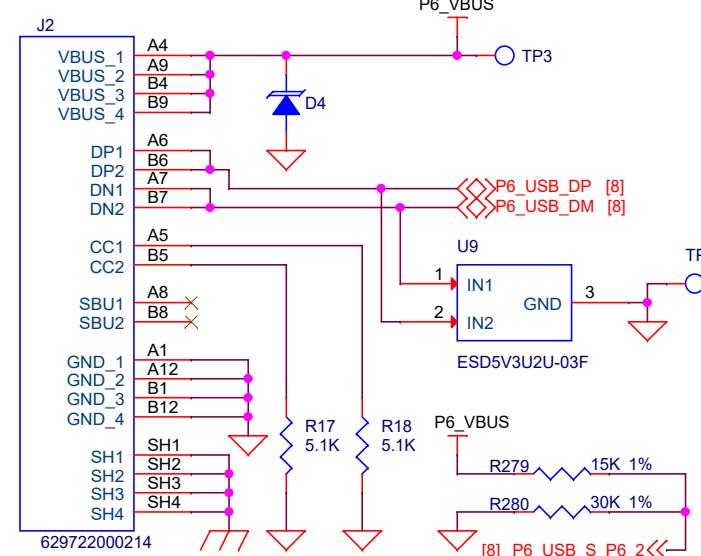
KitProg3 USB Interface and Power Supply



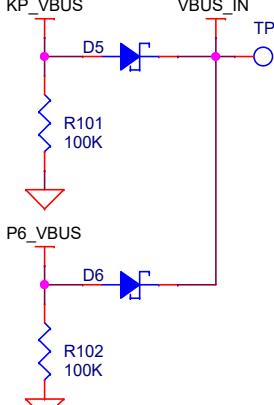
Li-ion Battery Charger and Power path



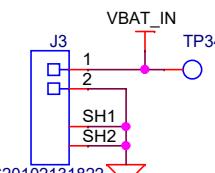
PSoC™ 6 USB Device Interface and Power Supply



Power Supply Or'ing



Li-ion Battery Connector



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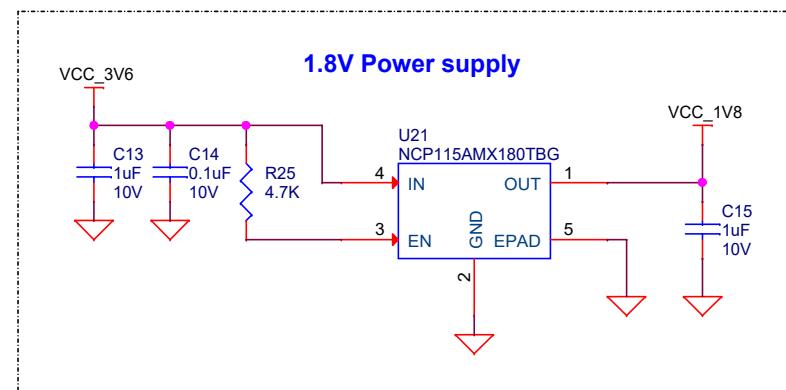
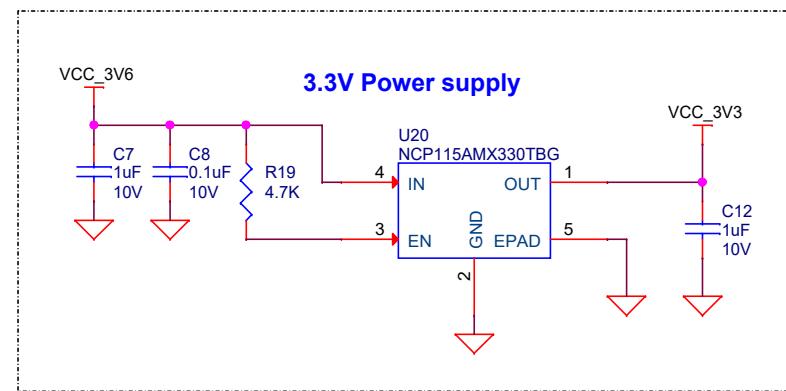
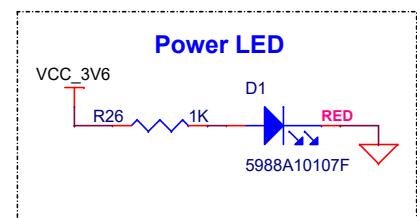
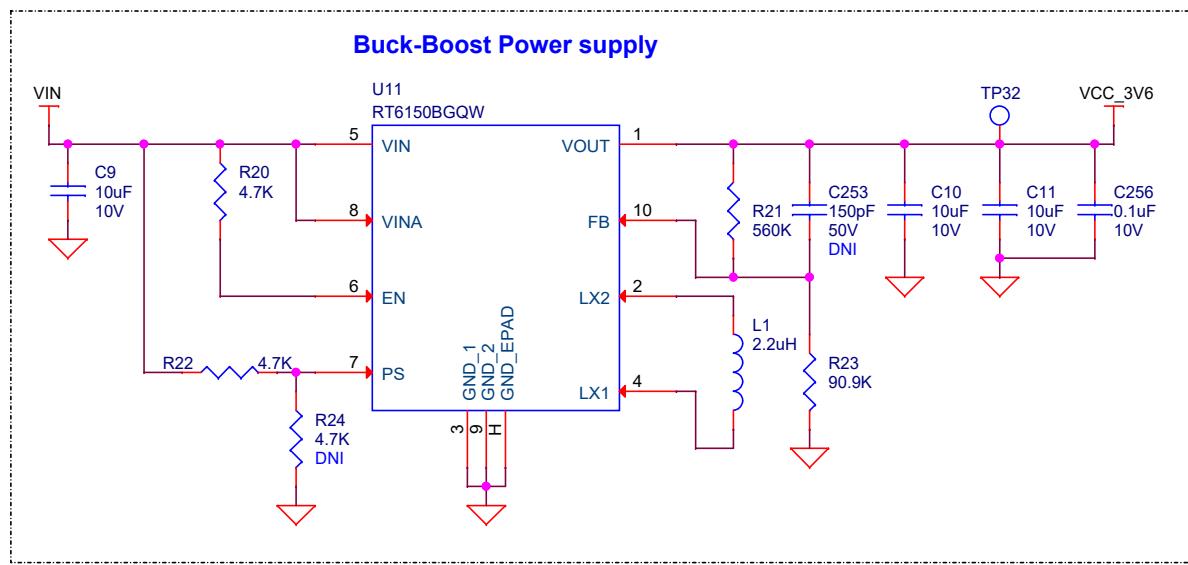


SCH Title : PSoC™ 6 AI Evaluation Board

Page Title: USB and Battery Power Supply Input

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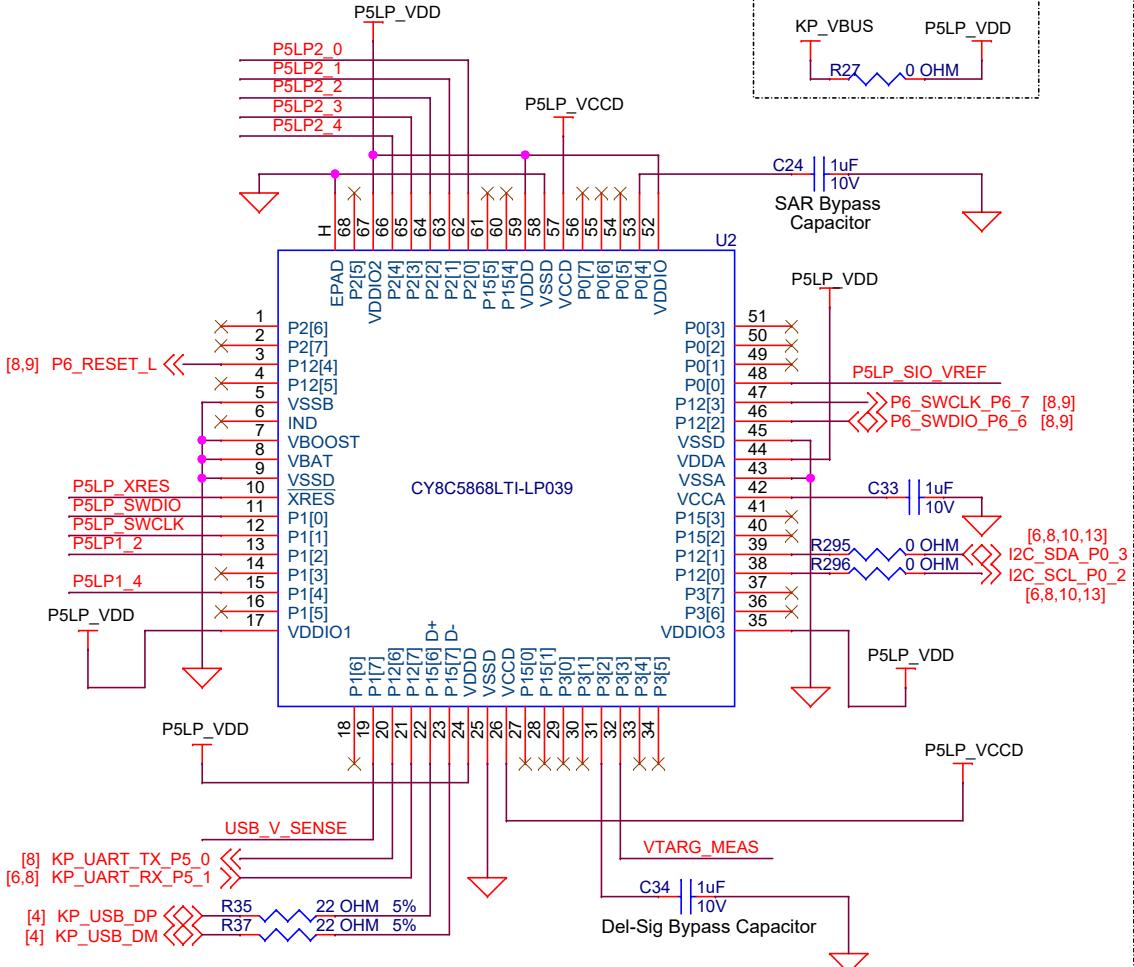
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Page Title: Regulated Voltage Supply

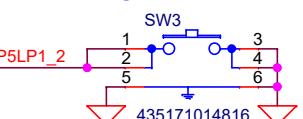
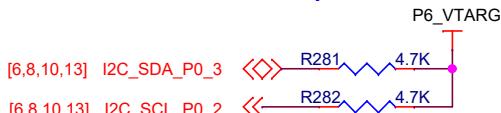
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PSoC™ 5LP based KitProg3**KitProg3 H/W Revision**

P5LP2_0	Bit 0
P5LP2_1	Bit 1
P5LP2_2	Bit 2
P5LP2_3	Bit 3
P5LP2_4	Bit 4

ID = 0x03

Note:
GND is read as binary "1" and floating as "0"

KitProg3 Mode Switch**KitProg3 Status LED****I2C Pull Ups****Legal Disclaimer :**

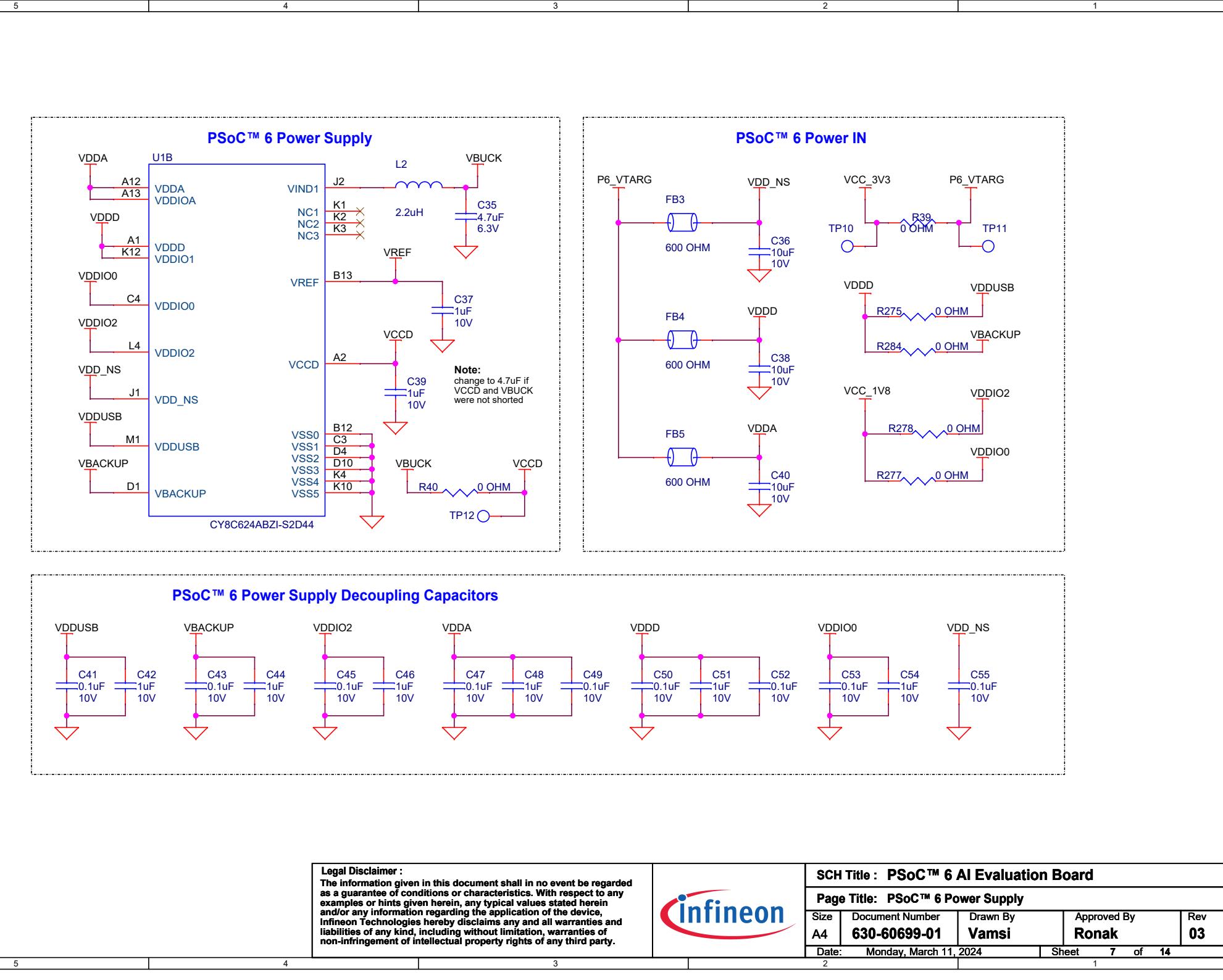
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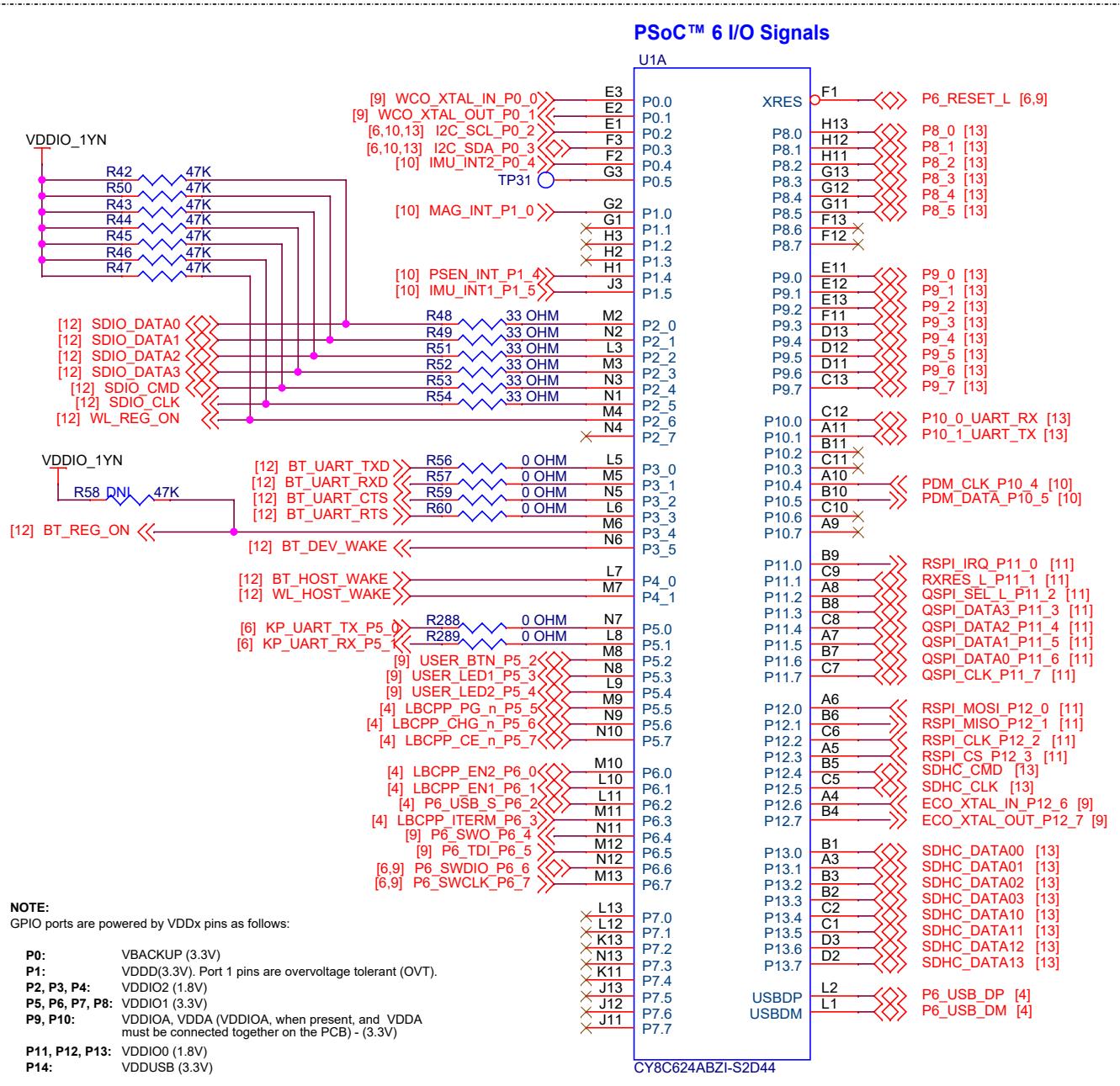
SCH Title : PSOC™ 6 AI Evaluation Board

Page Title: KitProg3 Interface

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PSoC™ 6 I/O Signals


NOTE:

GPIO ports are powered by VDDx pins as follows:

- P0: VBACKUP (3.3V)
- P1: VDDD (3.3V). Port 1 pins are overvoltage tolerant (OVT).
- P2, P3, P4: VDDIO2 (1.8V)
- P5, P6, P7, P8: VDDIO1 (3.3V)
- P9, P10: VDDIOA, VDDA (VDDIOA, when present, and VDDA must be connected together on the PCB) - (3.3V)
- P11, P12, P13: VDDIO0 (1.8V)
- P14: VDDUSB (3.3V)

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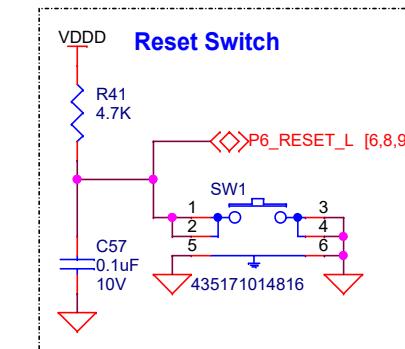
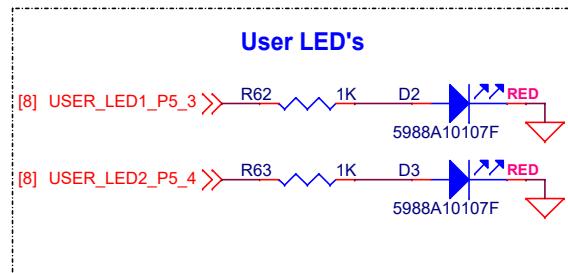
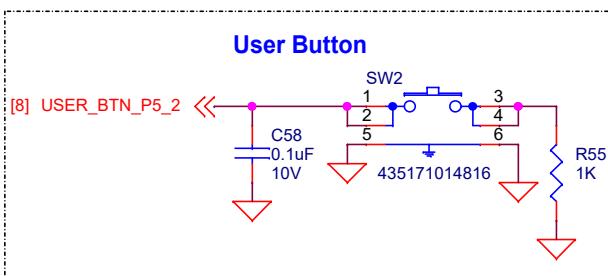
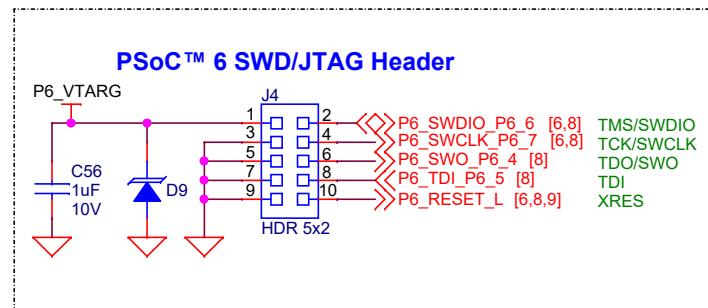
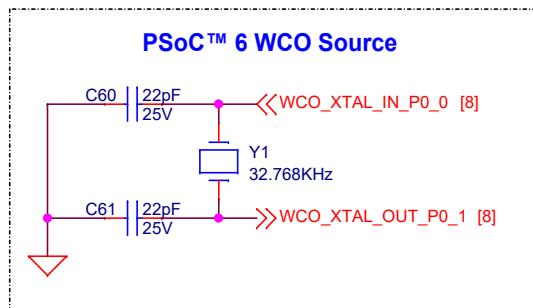
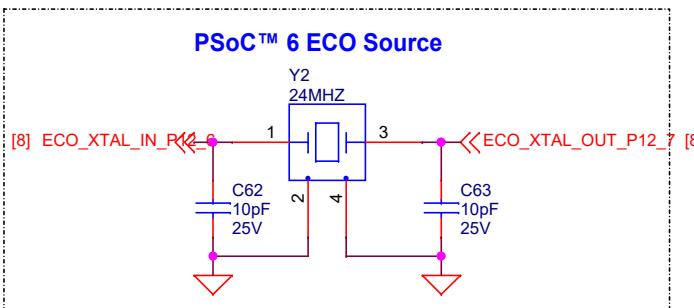
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Page Title: PSoC™ 6 I/O Signals

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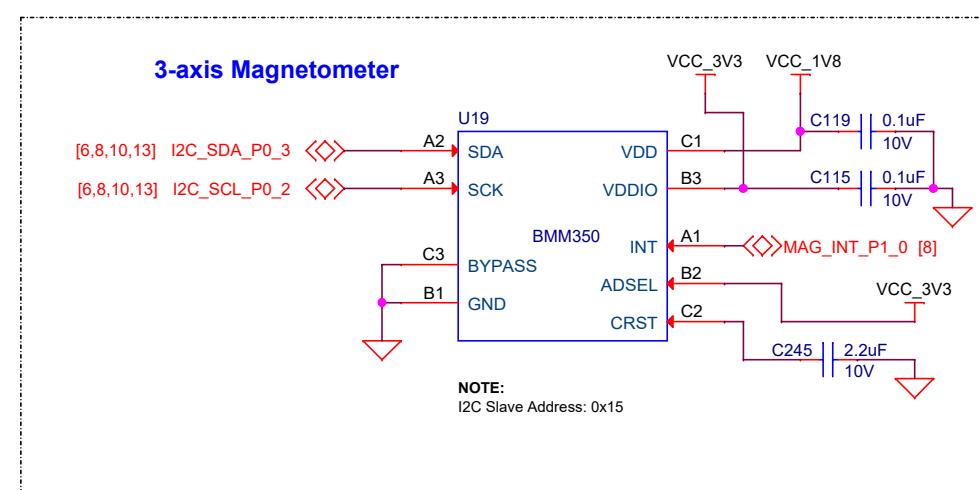
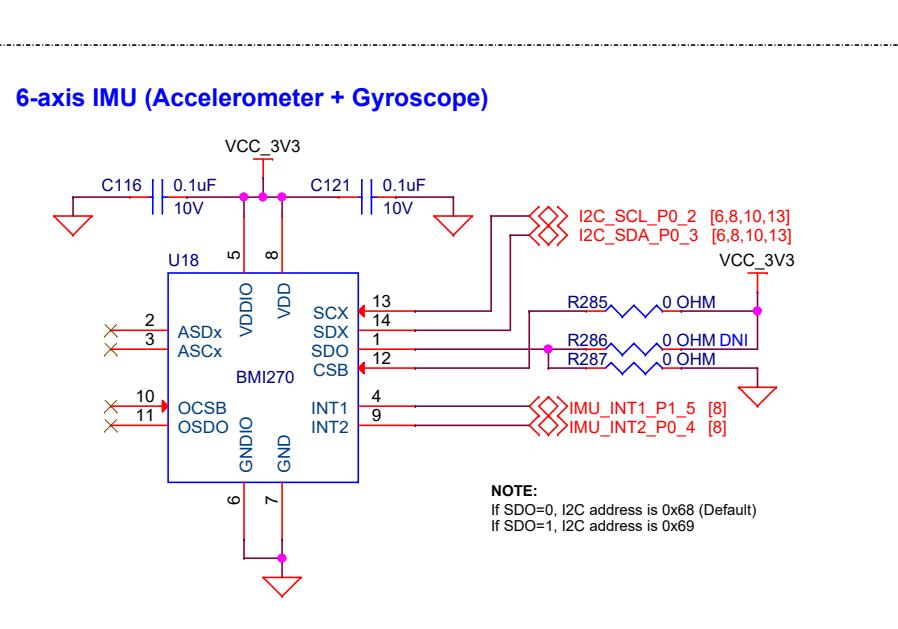
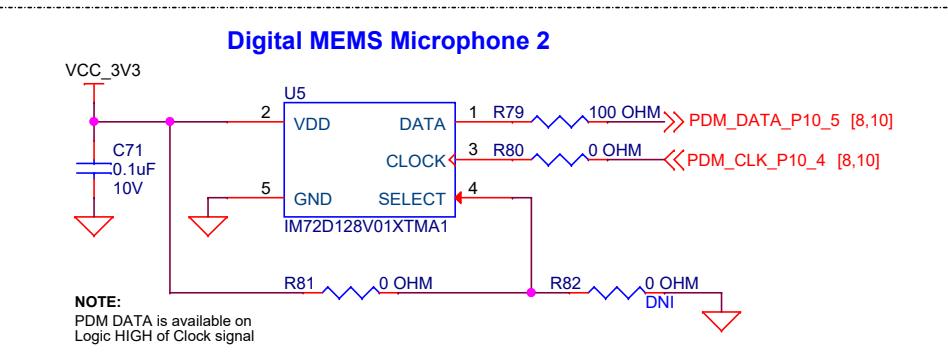
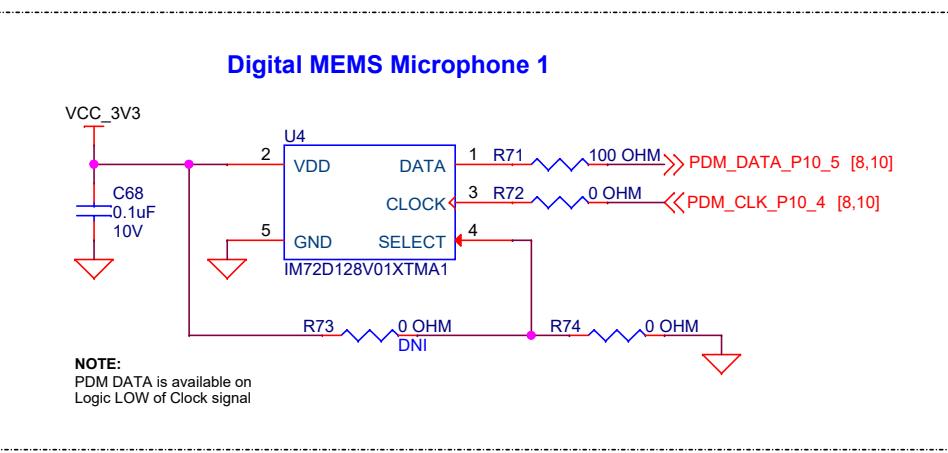
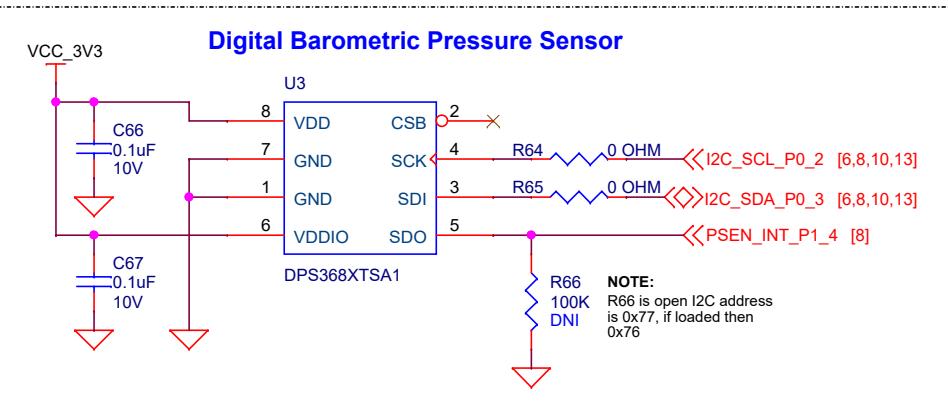
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Page Title: **On-board Peripherals**

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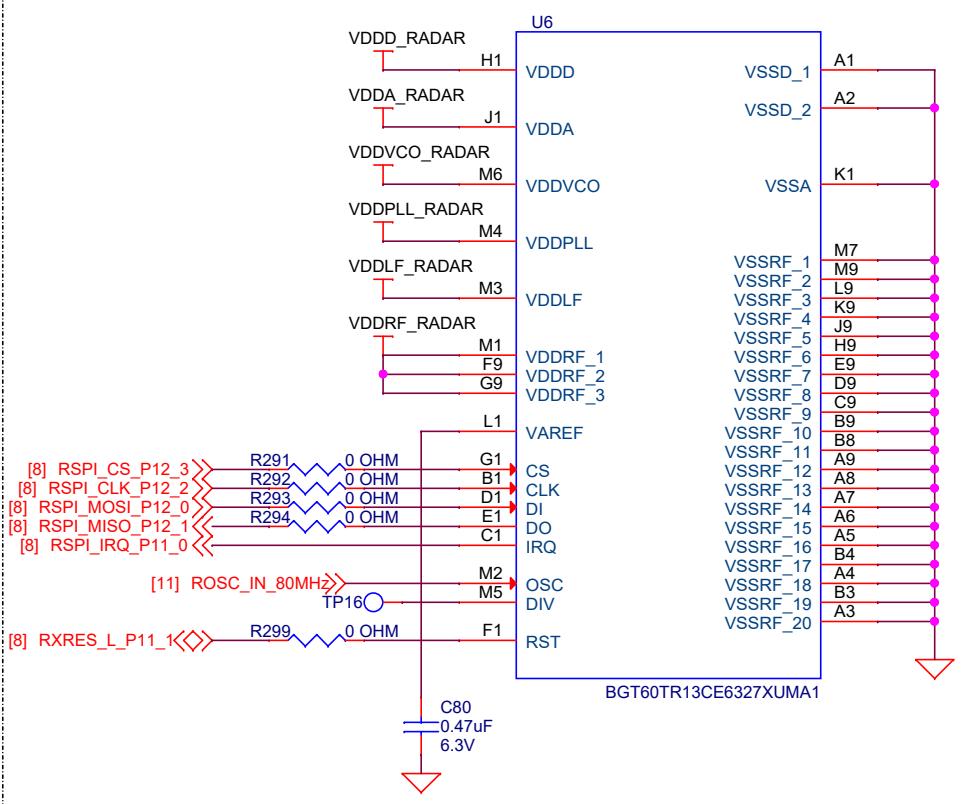


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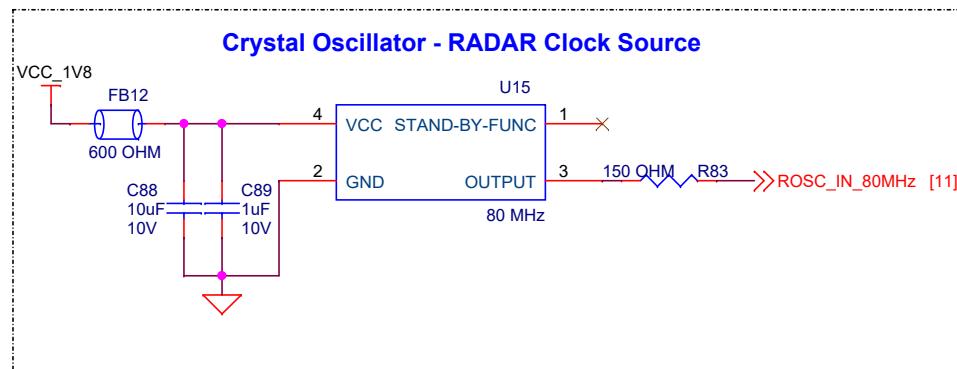
Page Title: IMU, Magnetometer, DMIC's, Pressure sensor

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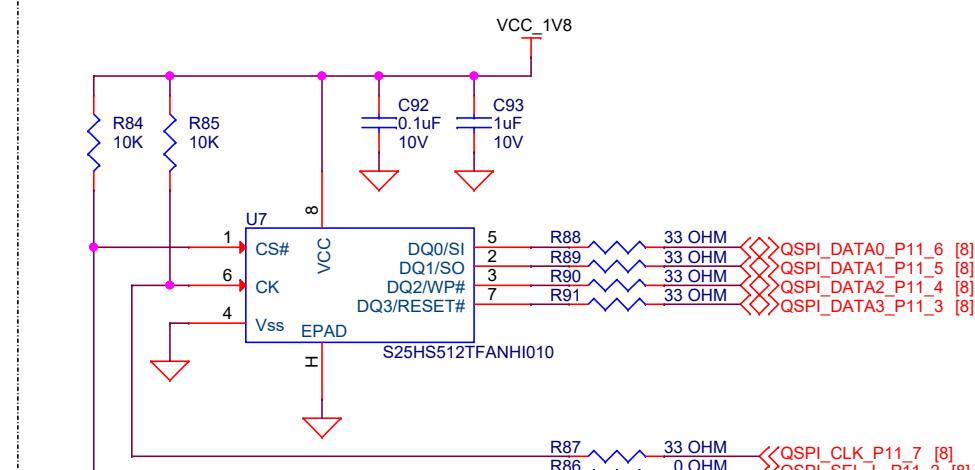
RADAR Sensor



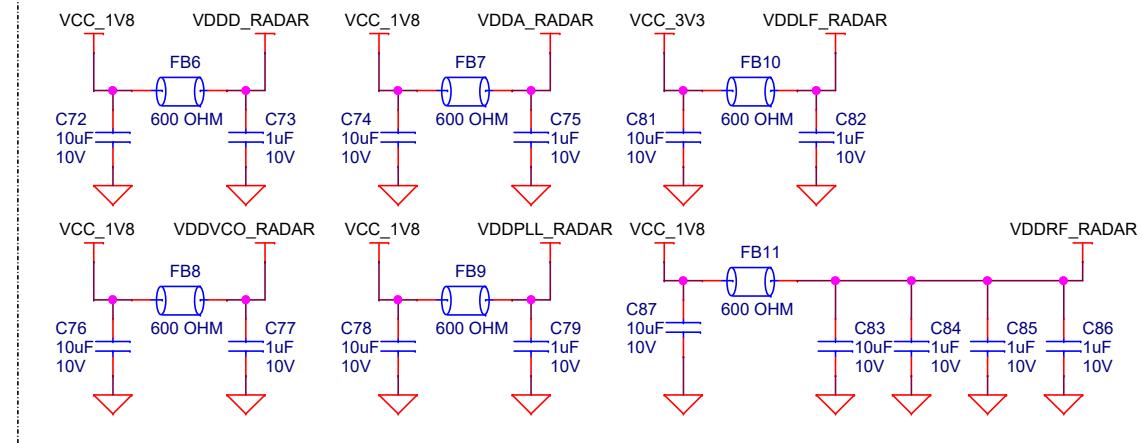
Crystal Oscillator - RADAR Clock Source



QSPI Memory interface



Supply for RADAR Sensor



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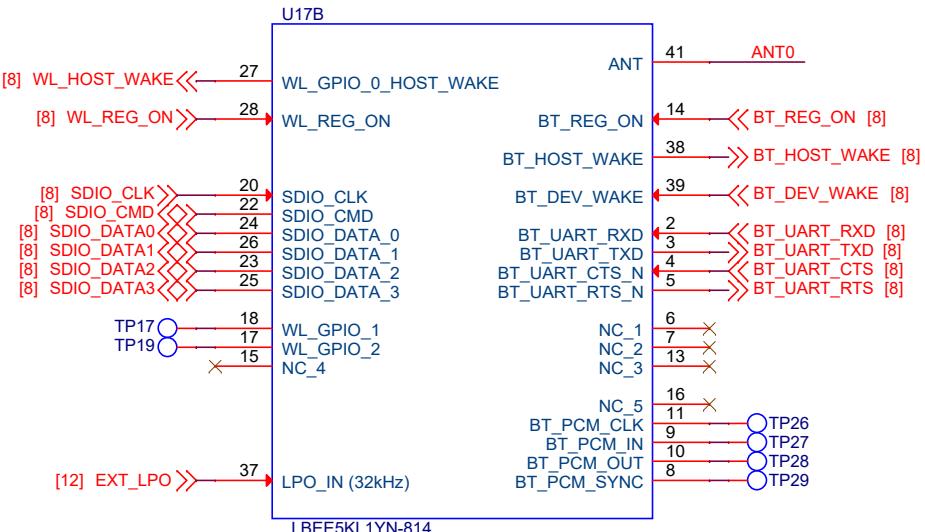
Page Title: QSPI Memory, RADAR Sensor interface

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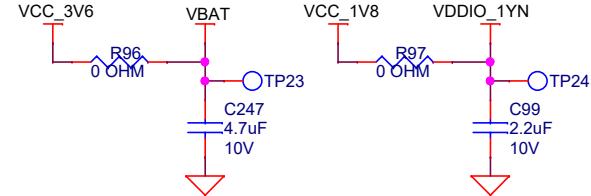
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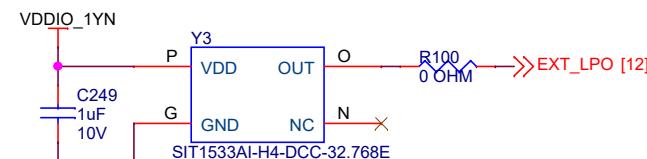
1YN Module Interface Signals



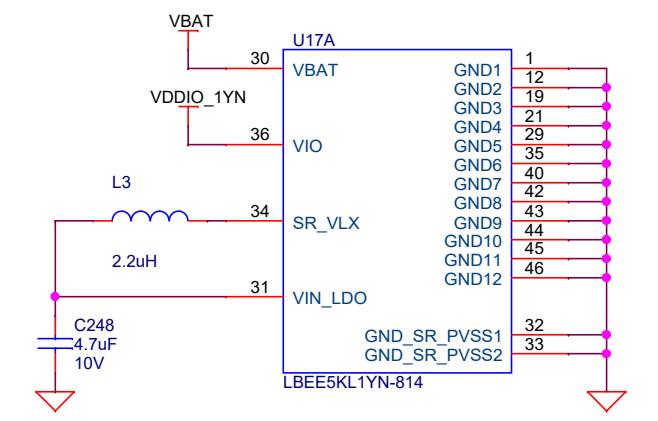
Decoupling Capacitors for 1YN Module



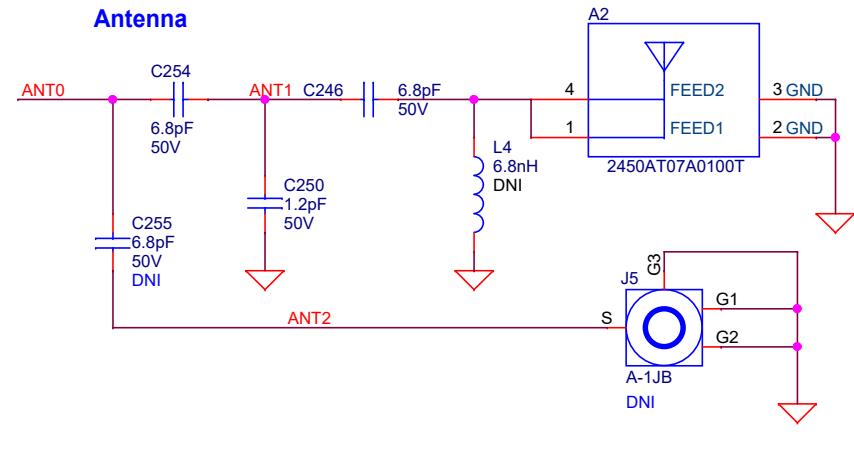
External LPO



Power Supply for 1YN Module



Antenna



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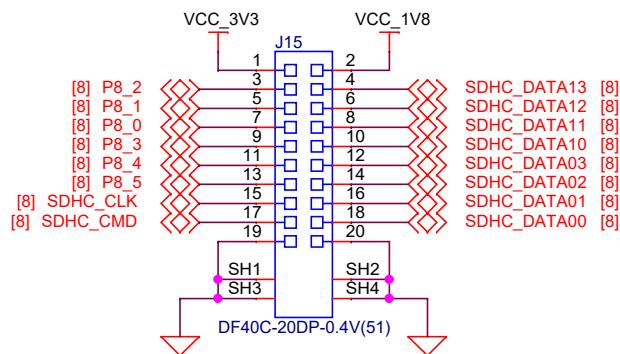
Page Title: **1YN Module Interface (WiFi & BLE)**

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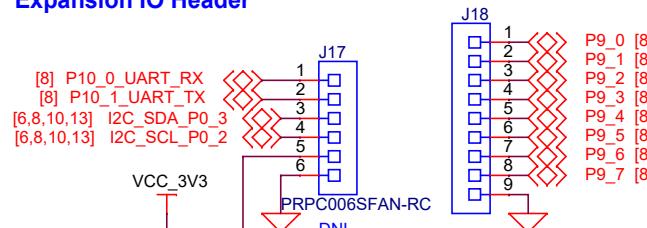
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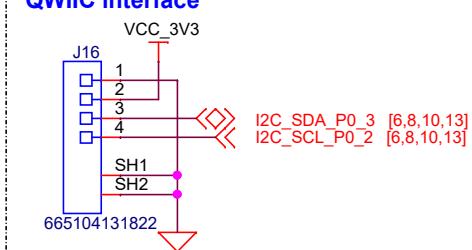
Expansion IO connector



Expansion IO Header



QWIIC interface



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Page Title: IO Expansion, QWIIC and Headers

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REVISION HISTORY

REV	DESCRIPTION OF CHANGE	DATE
0.01	Initial draft schematic	08-11-2023
0.02	Fixing the Open Net issues	13-11-2023
0.03	Updated QSPI memory and added IO expansion header with I2C, UART and SmartIO interface	16-11-2023
01	Initial release	06-12-2023
02	UART signals are updated for J17	06-02-2024
03	Microphone changed to IM72D series	11-03-2024

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