2.5 Gbps CMOS Burst Mode Laser Driver & Limiting Post Amplifier with Digital Set-up, Control & On-chip NVM

Main Features

- 100 mA bias current and 90 mA modulation current output drive capability
- Current DAC output for APD bias control
- Fast burst-mode loop settling time
- On-chip Non-Volatile Memory for storing chip set-up & control data
- Temperature compensated modulation current with on-chip temperature sensor
- True average Tx burst power monitor
- Tx fault detection and safety logic
- Separate and independent Transmitter, Receiver and Digital +3.3 V power supplies

Applications

- GePON & GPON FTTh ONU/ONT
- BOSA-on-Board ONU.

General Description

The NT25L91 is a combined burst mode laser driver and limiting post amplifier designed for fiber optic transceiver modules.

The NT25L91 features an I^2C interface for digital control and set-up and on-chip non-volatile memory to store the control settings. This enables a complete single chip PCB solution for GePON and non-DDMI SFP/SFF optical transceiver modules.

Auto-ranging A/D converters with digitized monitoring and an internal temperature sensor are also provided enabling GPON transceivers and DDMI SFP optical modules to be designed with the addition of a low cost 'digital only' microcontroller.

The NT25L91 includes an on-chip DAC for controlling an external APD bias circuit.

Consuming 99 mA from a 3.3 V supply the NT25L91 is packaged in a 4x4 mm QFN 28 pin RoHS package rated from -40 to +95 °C.

Block Diagram

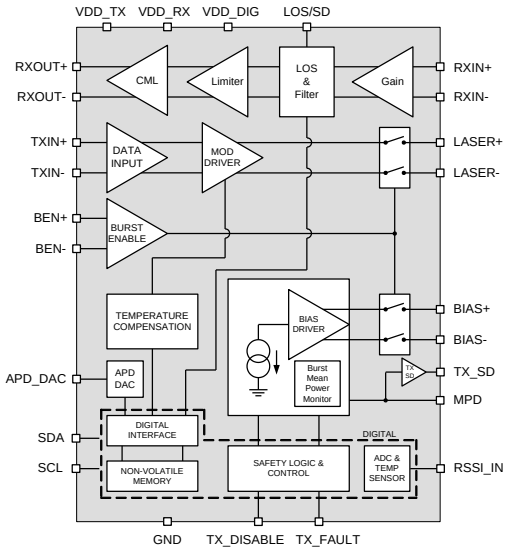

Figure 1 – NT25L91 Functional Block Diagram

Package

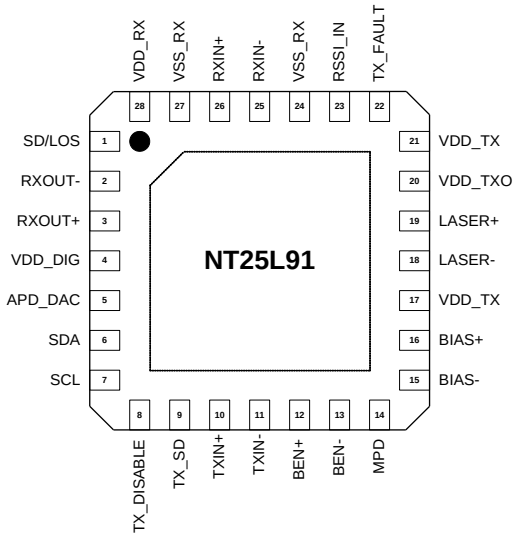

Figure 2 – NT25L91 Package

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Package Diagram & Pin Descriptions

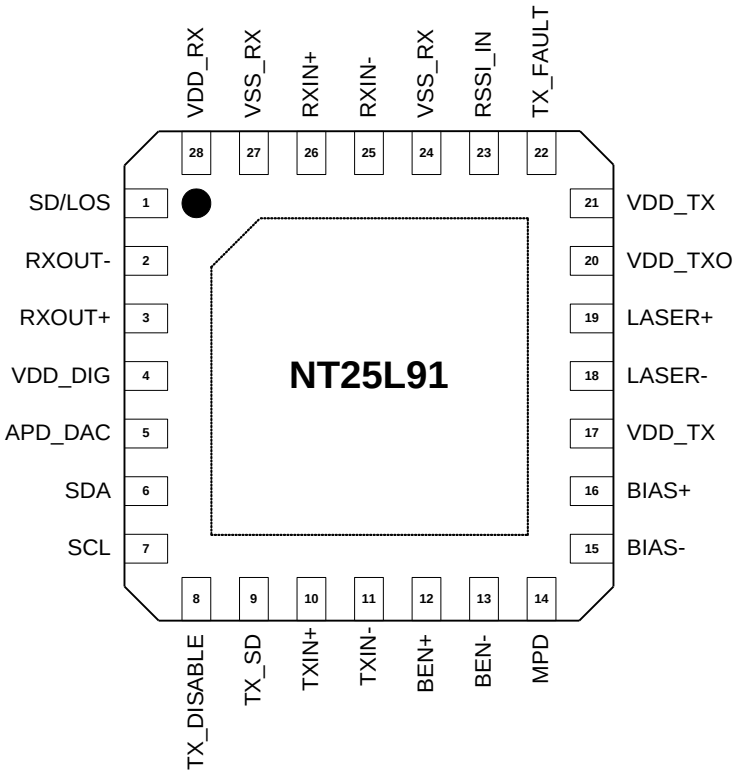


Figure 3 – NT25L91 Package Diagram Here

Table 1 – Package Pin Descriptions

Pin	Name	Function
1	SD/LOS	Signal Detect / Loss of Signal status output. Polarity can be set in NVM. Connect to VDD_RX using a 4k7 to 10k Ω resistor.
2	RXOUT-	Receiver inverting CML data output. Typically AC-coupled.
3	RXOUT+	Receiver non-inverting CML data output. Typically AC-coupled.
4	VDD_DIG	+3.3 V power supply for digital stage. Connect to VDD_RX using suitable power supply filtering.
5	APD_DAC	DAC output. Provides a current sink output for controlling an external APD bias control circuit. DAC is controlled directly via I^2C interface.
6	SDA	Slave I^2C serial data interface connection. On chip 10k Ω pull-up.
7	SCL	Slave I^2C serial clock interface connection. On chip 10k Ω pull-up.
8	TX_DISABLE	TX_DISABLE control input. Active high. Connect to VDD_TX using a 4k7 to 10k Ω resistor.
9	TX_SD	Transmitter signal detect open drain output. Connect to VDD_TX using a 4k7 to 10k Ω resistor. Output is high during Tx transmission.

Pin	Name	Function
10	TXIN+	Transmit data high speed non-inverting input. Internally biased.
11	TXIN-	Transmit data high speed inverting input. Internally biased.
12	BEN+	Burst enable non-inverting input. Internally biased.
13	BEN-	Burst enable inverting input. Internally biased.
14	MPD	Monitor photodiode input for automatic power control.
15	BIAS-	Laser bias current complementary sink. DO NOT use to drive laser. Connect to VDD_TXO via a dummy resistive load of 15 Ω.
16	BIAS+	Laser bias current sink. Always used to drive laser. Connect to laser cathode.
17	VDD_TX	+3.3 V power supply input for transmitter stage.
18	LASER-	Laser modulation inverting current sink. [1]
19	LASER+	Laser modulation non-inverting current sink. [1]
20	VDD_TXO	Laser +3.3 V FET controlled supply voltage output. Internal FET switch controlled by safety logic.
21	VDD_TX	+3.3 V power supply input for transmitter stage.
22	TX_FAULT	TX_FAULT status output. Active high. Open drain output. Connect to VDD_TX using a 4k7 to 10k Ω resistor.
23	RSSI_IN	Receiver signal strength indicator input from preceding transimpedance amplifier (TIA). Current input. Programmable Sink or Source.
24	VSS_RX	Receiver ground connection.
25	RXIN-	Received data inverting input. Use an external 100 Ω resistor to differentially terminate the input to RXIN+.
26	RXIN+	Received data non-inverting input. Use an external 100 Ω resistor to differentially terminate the input to RXIN-.
27	VSS_RX	Receiver ground connection.
28	VDD_RX	+3.3 V power supply input for receiver input stage.
CP	GND	Common ground pad for IC. Also acts as thermal sink for package.

[1] In default mode the LASER+ is used to drive the laser cathode and the LASER- output is connected to VDD_TXO via a dummy load resistor (15 Ω). To enable PCB design flexibility the polarity can be inverted so that the LASER- output can be used to drive the laser cathode and the LASER+ is connected to VDD_TXO via a dummy load resistor (15 Ω). This can be done by setting the TX_MOD_STEER register bit control 6Bh <3> to '1'.

Table 2 – Absolute Maximum Ratings

These are the absolute maximum ratings beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Symbol	Parameter	Rating	Units
V_{DD}	Power supply (V_{DD} to GND)	-0.4 to 4.0	V
T_{stg}	Storage temperature	-65 to +150	°C
T_{Solder}	Soldering temperature (JEDEC J-STD-020C)	260	°C
$V_{IN\_RX\_MAX}$	Maximum receiver differential input (pk-pk)	1600	mV
$RSSI_{MAX}$	Maximum current on RSSI pin	8.0	mA

Table 3 – Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{DD}	Power supply voltage (V_{DD} to GND)	+3.3 ± 10%	V
T_a	Ambient operating temperature	-40 to +95	°C
DR	Data rate	155 to 2700	Mbps
C_{MPD}	Maximum monitor diode capacitance	20	pF
NVM V_{DD}	Supply voltage during NVM programming	3.3 to 3.6	V

Table 4 – Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{DD}	Power supply current [1]		99	119	mA

[1] – Includes receiver output CML termination current. Specified for receiver output swing of 900mVpp. Does not include laser bias and modulation currents. Indicated supply current assumes 20 mA bias and 20 mA modulation currents flowing through laser diode.

Table 5 – Transmitter Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Transmitter Input Stage					
V_{TxIN}, V_{BEN}	Differential input voltage, pk-pk [1]	200		2400	mV
V_{BEN_TTLLOW}	BEN single-ended TTL low input			0.9	V
$V_{BEN\_TTLHIGH}$	BEN single-ended TTL high input	1.9			V
I_{BEN}	Maximum current on BEN pin			20	mA
V_{TxIN_CM}	TxIN Common mode input voltage		V_{DD}–1.32		V
V_{BEN_CM}	BEN Common mode input voltage		1.4		V
Transmitter Bias Stage					
I_{BIAS}	Bias current	1		100	mA
I_{BIAS_OFF}	Bias current disabled			100	µA

Symbol	Parameter	Min.	Typ.	Max.	Units
Acc_{IBIAS}	Bias current setting accuracy [2]	-20	±10	+20	%
$Stab_{APC}$	APC loop setting stability			0.46	dB
Acc_{MON}	MPD current setting accuracy (25°C)	-10		+10	%
I_{MPD}	MPD input current	25		1800	µA
V_{MPD_IN}	Voltage at MPD relative to ground		V_{DD} - 2		V
t_{APC_INIT}	APC loop initialisation time [3]			1.92	µs
V_{LASER}	Laser forward voltage			2.0	V
Laser Modulator Stage					
I_{MOD}	Modulation current	5		90	mA
I_{MOD_OFF}	Modulation current disabled			100	µA
Acc_{MOD}	Modulation current setting accuracy	-15	±10	+15	%
$Stab_{MOD}$	Modulation current temperature stability across operating range	-11	±7	+11	%
T_{RISE} / T_{FALL}	Modulation current rise / fall times [4]		60	80	ps
DJ_{Tx}	Deterministic Jitter, pk-pk [5]		15	40	ps
RJ_{Tx}	Random jitter, rms [6]			1.5	ps
Temperature Compensation Stage					
TSLOPE	TSLOPE setting range	0		7500	ppm/°C
ACC_{SLOPE}	TSLOPE setting accuracy	-1300	± 700	+1300	ppm/°C
VAR_{SLOPE}	TSLOPE variability			±10	%
TCSTART	TCSTART setting range	-40		+95	°C
$ACC_{TCSTART}$	TCSTART setting accuracy		±8		°C
$VAR_{TCSTART}$	TCSTART part-to-part variability			±10	°C
Burst Control Stage					
BEN_{ON}	Burst enable time [7]		5.0	12.8	ns
BEN_{OFF}	Burst disable time [8]		5.0	12.8	ns
$T_{B\_ON\_START}$	Burst on time (fast start-up, 3 bursts)	576			ns
T_{B_ON}	Burst on time (after APC settled)	300			ns
T_{B_OFF}	Burst off time	96			ns
Transmitter Fault and Control Timing					
t_init	From power on or negation of TX_FAULT by TX_DISABLE [9]		39	55	ms
t_off	TX_DISABLE assert time [10]			10	µs

Symbol	Parameter	Min.	Typ.	Max.	Units
t_on	TX_DISABLE de-assert time [11]			1	ms
TX_SD_{DELAY}	TX_SD output delay time [12]		40	200	ns
TX_SD_{VAR}	TX_SD output width variation [12]			100	ns
t_delay	Time from READY set to transmitter output currents enabled [13]		600	900	µs
t_fault	TX_FAULT assert time			100	µs
t_reset	Time TX_DISABLE must be asserted to reset TX_FAULT	10			µs

[1] Internally biased differential inputs. TXIN (+/-) and BEN (+/-) inputs require external high speed termination. See transmitter section for further details.
[2] Ibias setting accuracy applies to operation in bias open loop mode. Accuracy limits valid above 7 mA.
[3] V_{DD} = 3.0V to 3.6V; TX_DISABLE is de-asserted; BEN changes from low to high. Initialisation of automatic power control loop during burst start-up. Time for monitor current to settle to 90% of the target APCSET monitor value within 3 burst on periods.
[4] Rise and Fall times indicated are 20% - 80%.
[5] Deterministic jitter measured with a continuous data pattern (no bursting) of 2^7-1 PRBS + 80 consecutive ones + 2^7-1 PRBS + 80 consecutive zeros at 2.5 Gbps. Includes data dependent jitter and periodic jitter.
[6] Random jitter measured with a 1010 test pattern at 2.5 Gbps.
[7] Assertion of laser bias and modulation currents to within 90% of target values. Valid after APC loop initialised.
[8] De-assertion of laser bias and modulation currents to less than 10% of target values. Valid after APC loop initialised.
[9] Time for NT25L91 transmitter to initialize immediately after power on. Also time to initialize after TX_DISABLE is used to negate a TX_FAULT after a TX_FAULT event has occurred.
[10] Time from rising edge of TX_DISABLE input to when the bias and modulation currents fall below 10% of nominal value.
[11] Time from falling edge of TX_DISABLE input to when the bias and modulation currents rise above 90% of nominal value.
[12] TX_SD delay and variation time measured with respect to BEN timing. See Figure 35 for more details. TX_SD function is derived from actual status of laser bias and modulation currents, not BEN input control. Timing only valid for average photodiode monitor currents I_{MPD} > 100 µA and C_{MPD} < 5 pF. For I_{MPD} < 100 µA and C_{MPD} > 5 pF the maximum TX_SD assert time is 90 ns.
[13] During power up sequence or after a TX_FAULT condition. READY (B4h <4>) is a soft indicator of an internal hardware status flag that indicates the NT25L91 is powered-up correctly and the NVM content has been copied to volatile register memory.

Table 6 – Receiver Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Receiver Input Stage					
V_{RxIN}	Differential input sensitivity, pk-pk [1]		4.0	8.0	mV
$V_{OVERLOAD}$	Differential input overload, pk-pk [1]	1200			mV
V_{RxCM}	Common mode input voltage	1.4	1.5	1.6	V
f_{LFC}	Low frequency cut-on			15	kHz
Receiver Output Stage					
$VOUT_{DIFF00}$	Output Swing (450mV set), pk-pk [2]	350	450	550	mV
$VOUT_{DIFF01}$	Output Swing (900mV set), pk-pk [2]	750	900	1050	mV
$VOUT_{DIFF10}$	Output Swing (1200mV set), pk-pk [2]	1050	1200	1350	mV
$VOUT_{DIFF11}$	Output Swing (1600mV set), pk-pk [2]	1400	1600	1800	mV
$VOUT_{CM}$	Common mode output voltage	1.6	1.8	2.0	V
T_{RISE} / T_{FALL}	Output rise/fall time, No Slew [3]		90	120	ps
	Output rise/fall time, Fast Slew [3]		160	200	ps

Symbol	Parameter	Min.	Typ.	Max.	Units
	Output rise/fall time, Med Slew [3]		320	400	ps
	Output rise/fall time, Slow Slew [3]		1280	1750	ps
DCD_{Rx}	Duty Cycle Distortion, pk-pk		5.5	30	ps
DJ_{Rx}	Deterministic jitter, pk-pk [4]		15	30	ps
RJ_{Rx}	Random jitter, rms [5]		1.9	3	ps
V_{SQU_EN}	Differential output voltage, pk-pk (squelched)			10	mV
Receiver Signal Detect Stage					
V_{LOS}	LOS programming range [6]	10.0		60.0	mV
HYS	LOS Hysteresis programmable Range (optical) [7]	1.0		3.0	dB
VAR_{THRESH}	LOS/SD threshold variation [8]	-0.5		+0.5	dB
SD_{ASSERT}	LOS/SD assert time [9]		11	100	µs
$SD_{DE-ASSERT}$	LOS/SD de-assert time [9]		30	100	µs

[1] Input sensitivity and overload specified for a BER = 1E-10 and a PRBS 2^{23}-1 at 2.5 Gbps.
[2] Differential pk-to-pk output amplitude swing. Measured using a 11110000 square wave pattern. 1200 mVpp and 1600 mVpp settings not advised for use above 622 Mbps.
[3] Measured using a 11110000 square wave for receiver settings shown in Table 18. Between 20%-80% levels.
[4] Deterministic jitter measured with a 2^7-1 PRBS + 80 consecutive ones + 2^7-1 PRBS + 80 consecutive zeros at 2.5 Gbps. Input amplitudes > 20mVpp differential swing.
[5] Random jitter measured with a 1010 test pattern at 2.5 Gbps. input amplitudes > 20 mVpp differential swing.
[6] Differential input. Equivalent to the optical modulation amplitude. Within the specified range the actual LOS level is within 0.5 dB of the target programmed LOS level. The LOS programming range stated is for hysteresis values of 2.5 dB and below. With 3 dB hysteresis the programming range is reduced to 50 mVpp.
[7] $HYS_{Optical} = 10 \times \log_{10}\left(\frac{V_{LOS\_ASSERT}}{V_{LOS\_DEASSERT}}\right)$, LOS Hysteresis can be set by user to 1, 2, 2.5 or 3 dB optical.
[8] Valid across operating temperature range, supply voltage range and wafer fabrication process corners. Across LOS setting range 20d to 60d.
[9] LOS timing measured using open drain LOS output into a 10k Ω resistor pull-up to V_{DD}. From LOS_{ASSERT} threshold +1dB to overload.

Table 7 – Digital Monitoring & Interface Section Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
Digital Diagnostic Monitoring Functions					
I_{APD_DAC}	APD_DAC output current range	0		255	µA
Res_{APD_DAC}	APD_DAC step size resolution		1		µA
V_{APD_DAC}	APD_DAC Headroom Voltage	1.0			V
T_{RANGE}	Temperature sensor range [1]	- 40		+ 95	°C
T_{ACC}	Temperature absolute accuracy		± 2	± 3	°C
TxP_{ADC}	Tx power monitor range [1]	25		1800	µA
TxP_{ACC}	Tx power monitor accuracy [2]		± 10	± 25	%
TxB_{ADC}	Tx bias current monitor range [1]	1		100	mA
TxB_{ACC}	Tx bias current monitor accuracy			± 10	%
TxM_{ADC}	Tx mod current monitor range [1]	5		90	mA
TxM_{ACC}	Tx modulation monitor accuracy			± 10	%
VDD_{ADC}	Supply voltage monitor range [1, 3]	2.6		4.0	V
VDD_{ACC}	Supply voltage monitor accuracy			± 3	%
$RSSI_{ADC}$	RSSI monitor input range [1, 4]	0.1		2048	µA
$RSSI_{ACC}$	RSSI monitor input accuracy		± 10	± 25	%
PO_{RAMP}	Power-On Ramp			100	ms
POR_{DELAY}	Power-On Reset Delay		20	30	ms
T_{TXPWR_VAL}	Length of time sampled MPD value is held on storage capacitor [5]	0.01	10		s
T_{READY}	Time after power-on to READY set		50	100	µs
T_{DDMI_READY}	Time to valid DDMI monitor data			4	ms
I^2C Interface					
F_{SCL}	SCL Clock		400	2000	kHz
t_{LOW}	Low period of SCL clock	250			ns
t_{HIGH}	High period of SCL clock	200			ns
t_{DH}	Data hold time			150	ns
t_{DS}	Data set-up time	100			ns
t_R	Rise time for SDA and SCL			100	ns
t_F	Fall time for SDA and SCL			100	ns
t_{SS}	Set up for STOP condition	100			ns

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{BUF}	Bus free time between a STOP and START condition	200			ns
$C_{I/O}$	Capacitance for each I/O pin			10	pF
Low Speed I/O					
$V_{LOSHIGH}$	LOS/SD status output voltage high [6]	2.0			V
V_{LOSLOW}	LOS/SD status output voltage low [6]			0.4	V
$V_{TX\_FAULT\_H}$	TX_FAULT output voltage high [6]	2.0			V
I_{LOS}	Maximum current on LOS pin			20	mA
$V_{TX\_FAULT\_L}$	TX_FAULT output voltage low [6]			0.4	V
$V_{TX\_SD\_H}$	TX_SD output voltage high [6]	2.0			V
$V_{TX\_SD\_L}$	TX_SD output voltage low [6]			0.4	V
$V_{TX\_DIS\_H}$	TX_DISABLE input voltage high	2.0		V_{DD}	V
$V_{TX\_DIS\_L}$	TX_DISABLE input voltage low	0		0.8	V

[1] Actual monitor operating range is limited to NT25L91 operating conditions. Theoretical monitor reporting range indicated in section 'Internal Diagnostic Monitoring' on page 58.
[2] Represents better than ±1.0 dB error on Tx Power monitor reading.
[3] VDD monitor applies to each separate supply: VDD_TX, VDD_RX, VDD_DIG. Only valid within supply operating range.
[4] RSSI input monitor is a current input. Current input can be sink or source and the current input mode is selected using bit <4> RSSI_POLARITY of register RXSET0 (6Bh).
[5] Time taken for the charge on the Tx Power sampling capacitor to reduce to 50% of its initial value. In the event of a TX_DISABLE or TX_FAULT the Tx Power monitor will report the value held on the Tx Power sampling capacitor and will therefore take a finite time to reduce to zero as the charge stored on the capacitor is dissipated away.
[6] Open drain output pulled high externally using a 4k7 Ω to 10k Ω resistor.

Table 8 – Default Limits

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD_{HIGH_A}	Internal VDD_TX high limit assert		3.9		V
VDD_{HIGH_D}	Internal VDD_TX high limit de-assert		3.8		V
VDD_{LOW_A}	Internal VDD_TX low limit assert		2.7		V
VDD_{LOW_D}	Internal VDD_TX low limit de-assert		2.8		V

Note: In the event that the TX_VDD supply exceeds the limits specified in table 8, the Transmitter output drive currents will be disabled and a non-latching TX_FAULT output will be asserted. If the TX_VDD supply returns to a value within the limits specified then the TX_FAULT will be de-asserted and the transmitter output drive currents will be reinstated.

Typical Operating Characteristics

Typical operating characteristics of the NT25L91 at +3.3 V, 25 °C unless otherwise stated. Receiver terminated into 100 Ω differential load as shown in Figure 50.

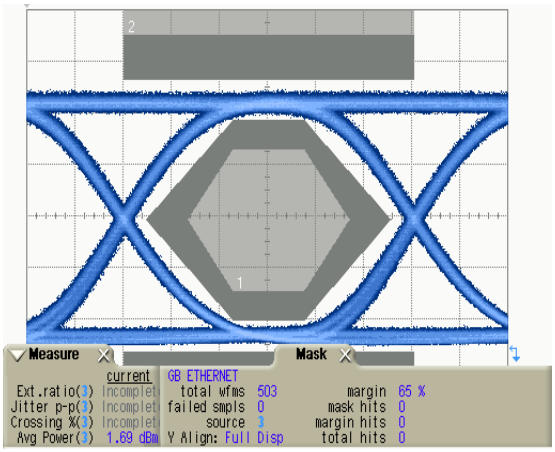


Figure 4 – Tx Optical Eye @ 1.25 Gbps

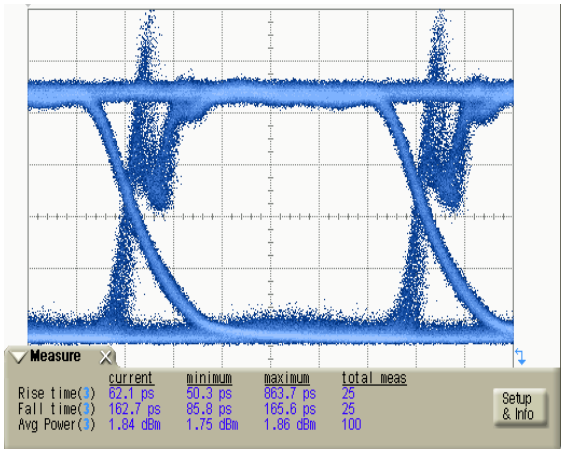


Figure 5 – Tx Unfiltered Optical Eye @ 1.25 Gbps

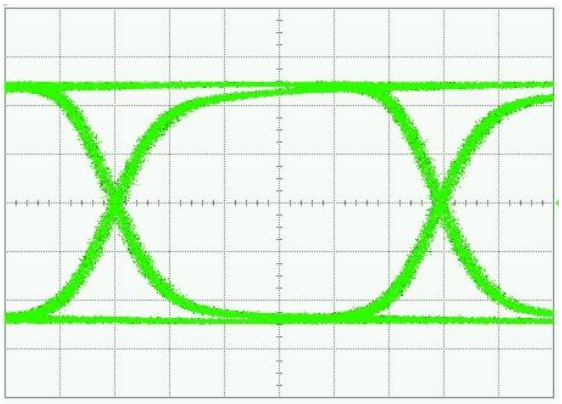


Figure 6 – Rx Single Ended Output @ 2.5 Gbps

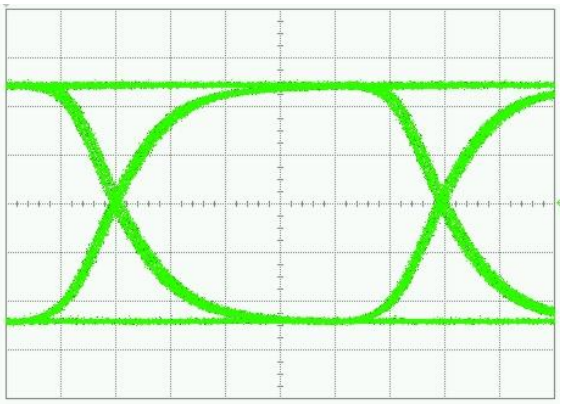


Figure 7 – Rx Single Ended Output @ 1.25 Gbps

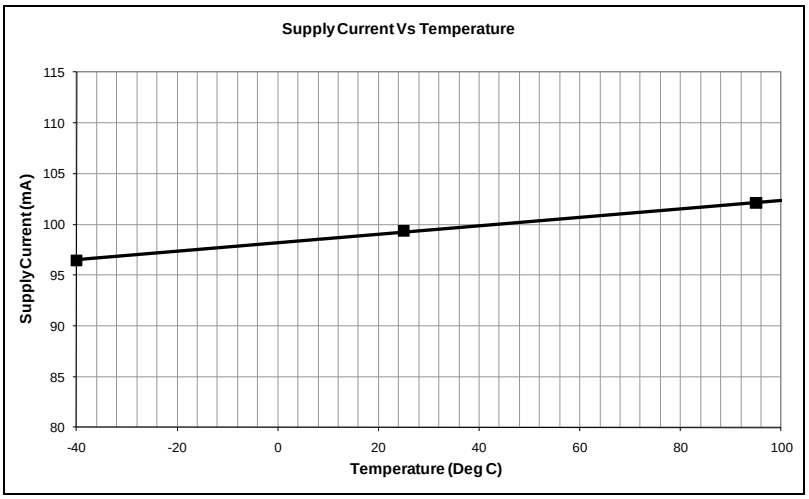


Figure 8 – NT25L91 Typical Supply Current (excluding laser currents)

Functional Block Diagram

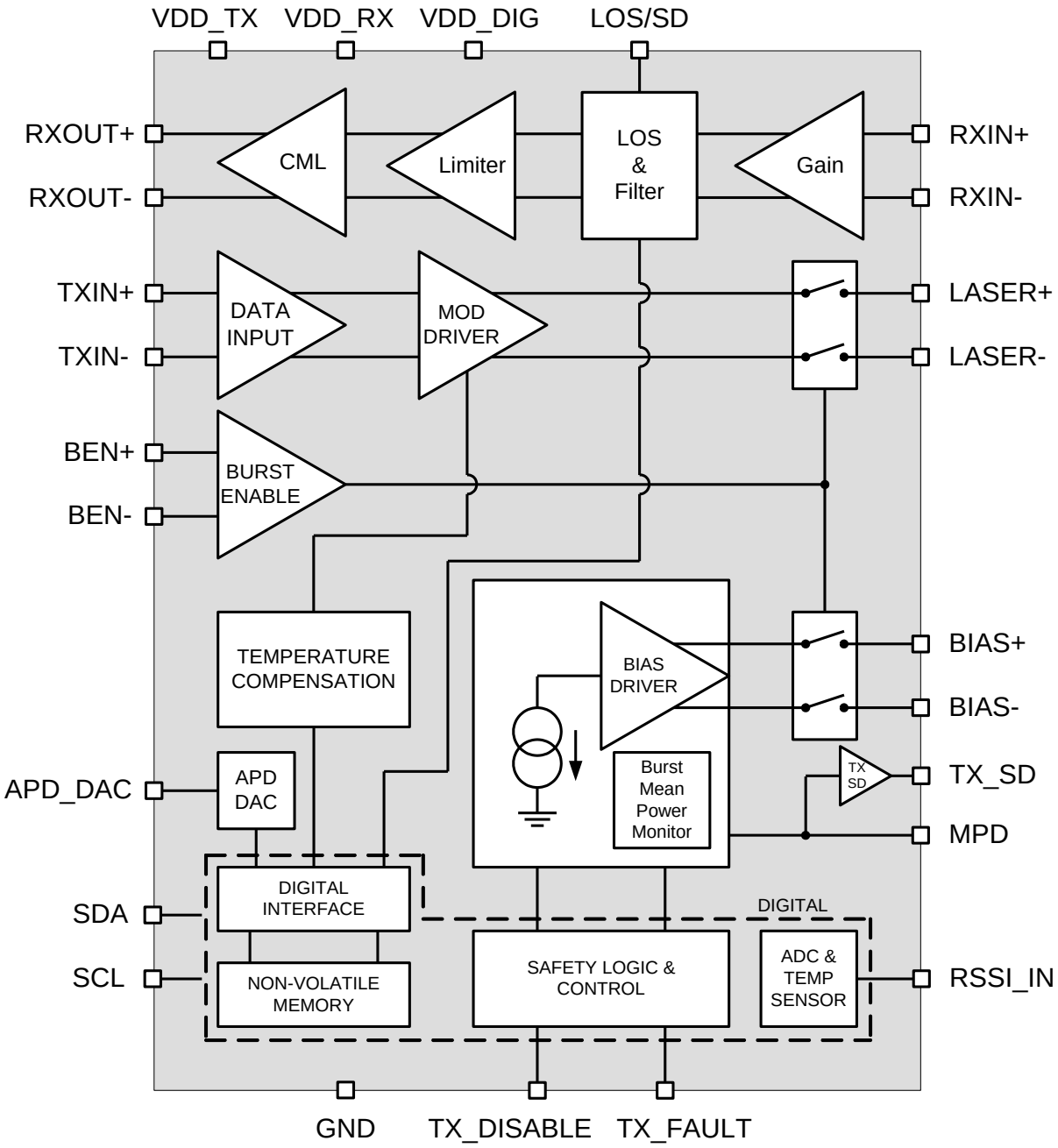


Figure 9 – NT25L91 Functional Block Diagram

The NT25L91 is a pure CMOS combined burst-mode laser driver and limiting amplifier intended for use in both burst-mode and continuous wave (CW), i.e. non-burst, telecom and datacom applications. Both transmitter and receiver signal paths operate up to 2.5 Gbps making the NT25L91 suitable for use in all popular module and protocol applications including BPON, GePON, GPON, OC-3, OC-12, OC-48, GbE, FC and 2xFC transceivers. The NT25L91 is particular suited to BOSA-on-Board ONU applications that can take advantage of the on-chip APD DAC output. In addition the NT25L91 has on-chip Non Volatile Memory (NVM) to store set-up data and is programmed digitally via an I^2C interface. The NT25L91 also includes on-chip sensors and analogue-to-digital converters required for SFF-8472 DDMI monitoring of optical transceivers. The transmitter contains full safety logic control circuitry to meet IEC-60825 eye safety requirements.

Functional Description

Power Supplies and Start-up Sequence

The NT25L91 features three separate power domains: VDD_TX for the transmitter supply, VDD_RX for the receiver supply and VDD_DIG for the digital supply..

VDD_RX and VDD_DIG can be physically connected and powered together whilst the VDD_TX can be powered independently. If VDD_DIG is connected to the VDD_RX then supply filtering components should be used.

The NT25L91 has been designed so that the transmitter supply can be powered independently of the receiver and digital supplies. This enables the user to power down the transmitter during normal operation whilst continuing to operate the receiver and digital circuits. This feature has been specifically included for use in PON ONU applications.

Recommended filtering and de-coupling of the NT25L91 power supplies is shown in the applications section of this document.

The NT25L91 power-up sequence is shown in Figure 10 below and assumes VDD_TX and VDD_RX are powered at the same time as VDD_DIG.

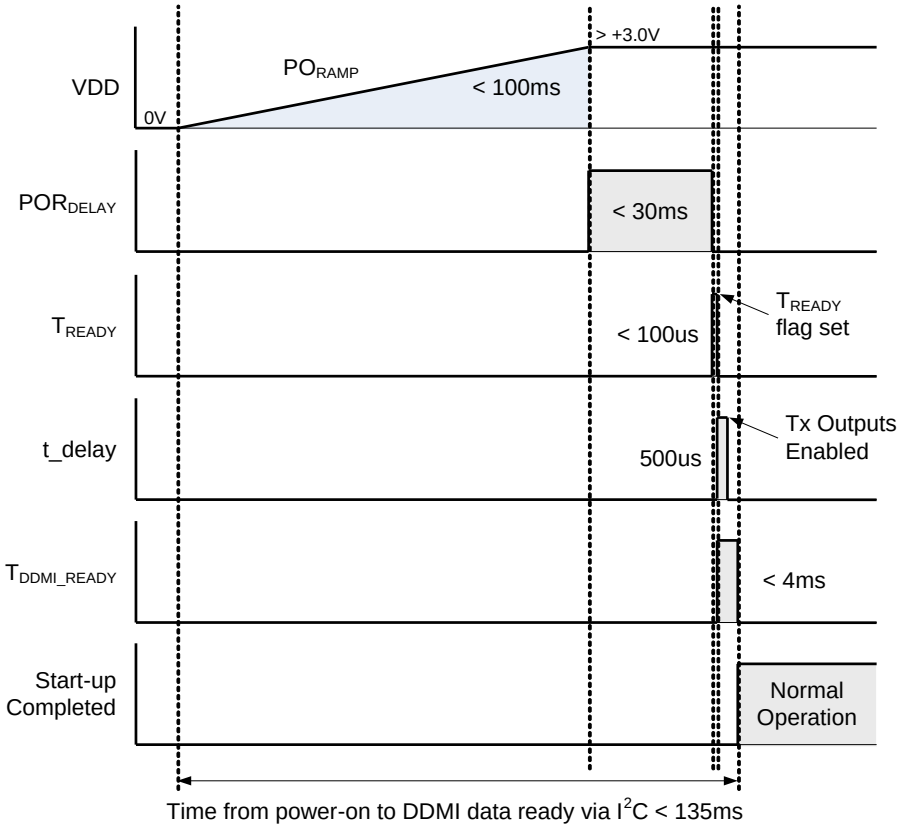


Figure 10 – NT25L91 Power-up timing sequence

The NT25L91 has an on-chip power-on reset circuit to guarantee that the IC powers up correctly. The digital functions, I^2C interface and non-volatile memory within the NT25L91 are controlled by a digital state machine. During the period before T_{READY} is set the transmitter outputs will be disabled and the receiver outputs will be squelched. The LOS output will be asserted high. The POR assert level is typically 2.3 V with a hysteresis of around 100 mV.

Start-up Sequence

The start up sequence for the NT25L91 is shown in the flow chart diagram below.

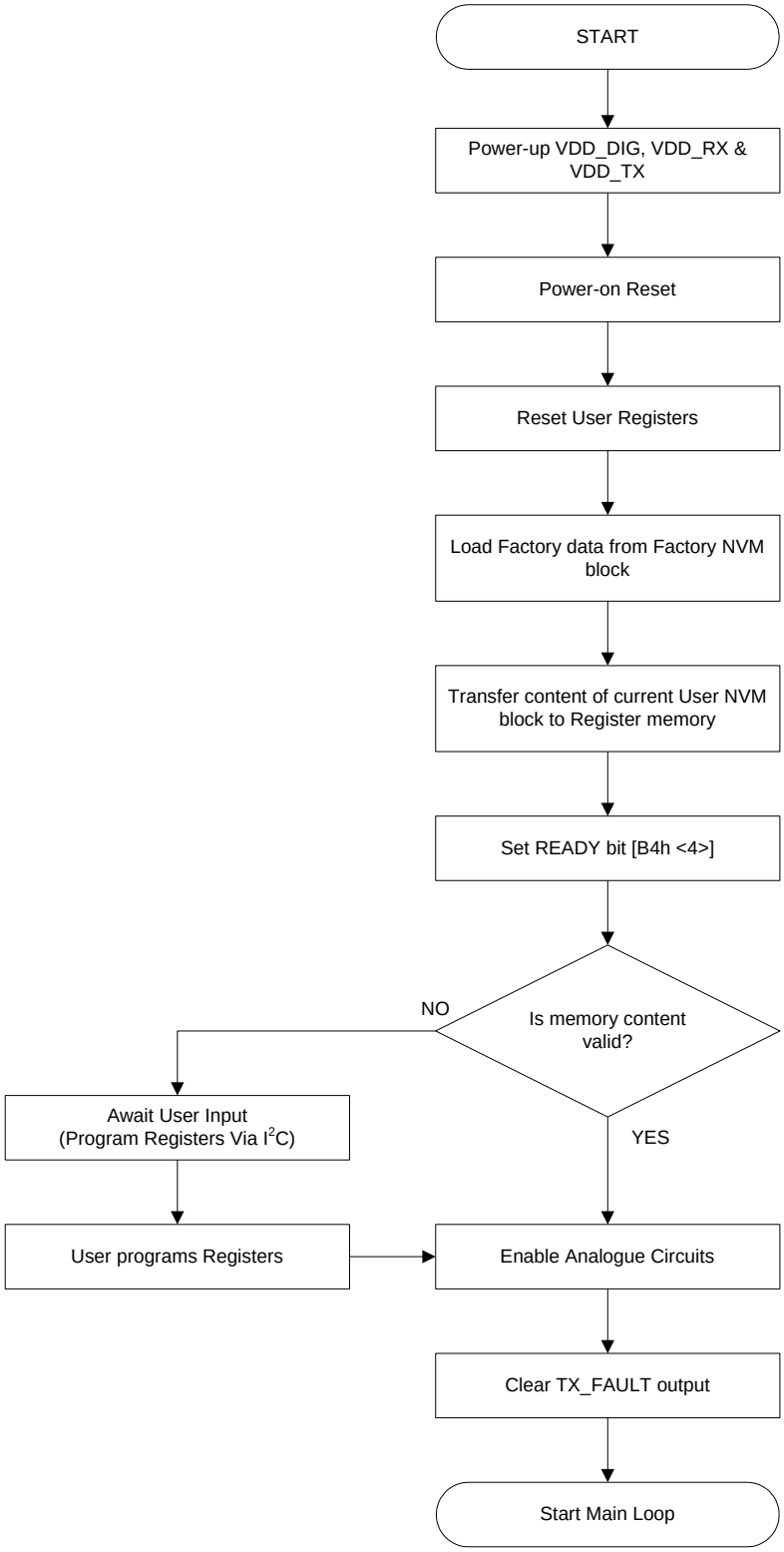


Figure 11 – NT25L91 Power-on Control Loop

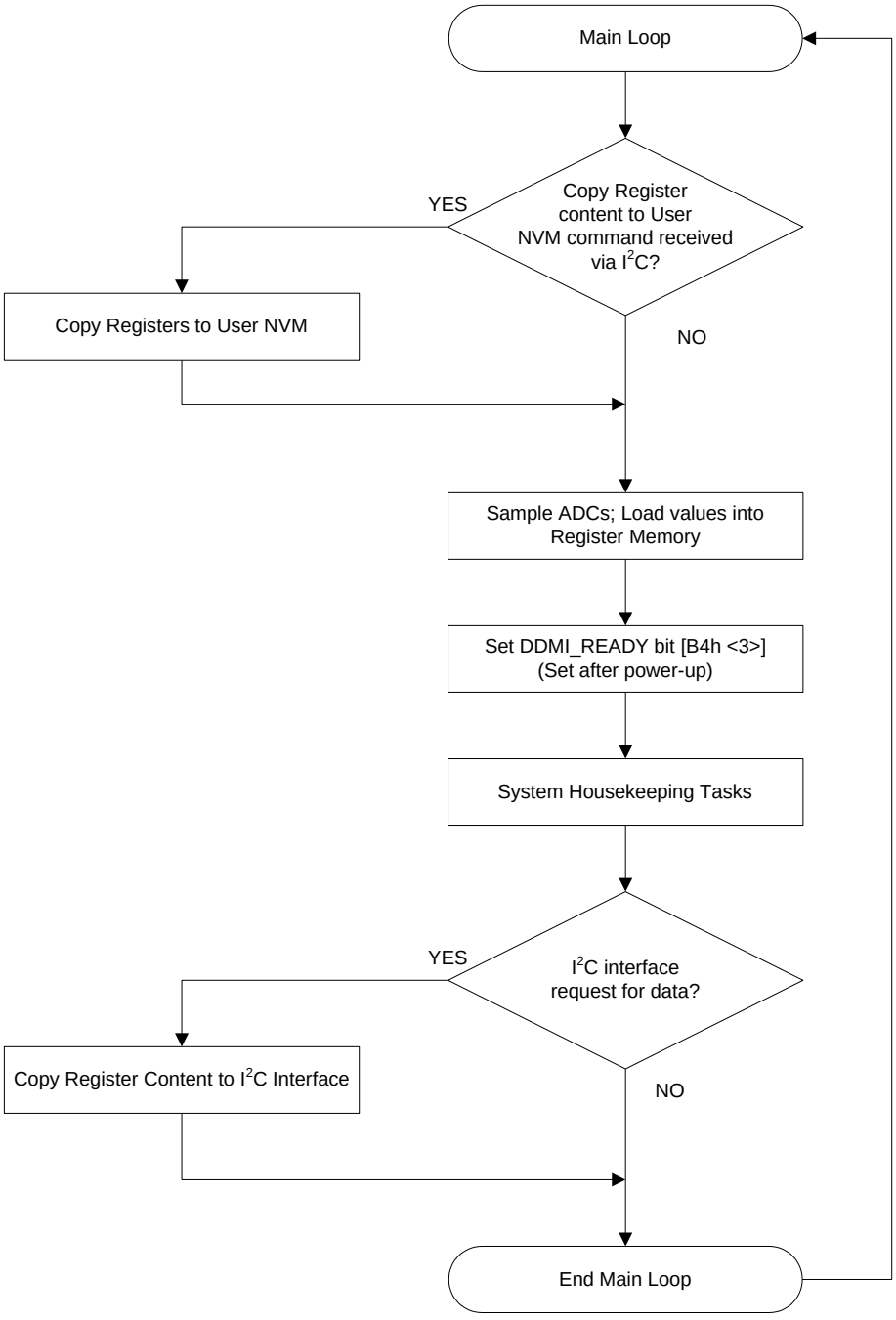


Figure 12 – NT25L91 Main Control Loop

Transmitter Features

The NT25L91 transmitter consists of an internally biased differential input stage that can be DC coupled or AC coupled depending on the mode of operation, a temperature compensated modulation current output driver, a burst mode controlled high current bias driver and a burst control input stage. The transmitter also contains sophisticated eye safety circuitry to comply with single point failure transmitter faults as per IEC-60825 requirements.

Transmitter Input Stage

The transmitter data inputs and the burst enable control inputs are high speed internally biased differential inputs that are typically externally terminated with PECL or CML loads.

The transmitter data input stage can be either DC coupled (burst-mode operation) or AC coupled (standard CW transceivers) and is internally biased. Input termination may be required for CML or LVPECL applications. The input stage consists of a limiting gain block that allows the NT25L91 to work with a range of input signals from 200 mVpp to 2400 mVpp including standard LVPECL inputs.

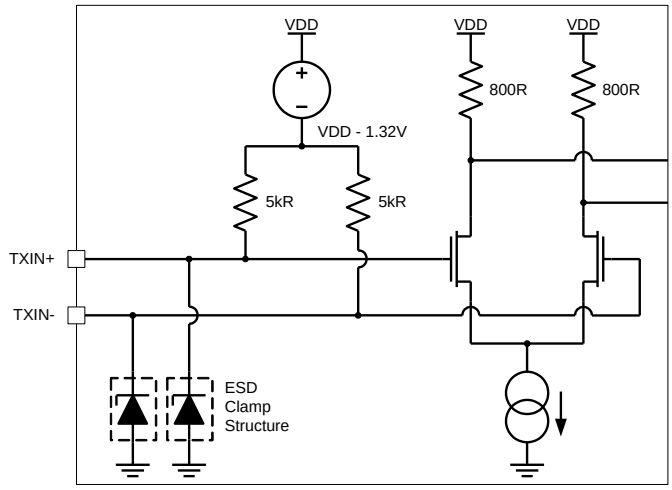


Figure 13 – NT25L91 Transmitter Data Input Internal Biasing

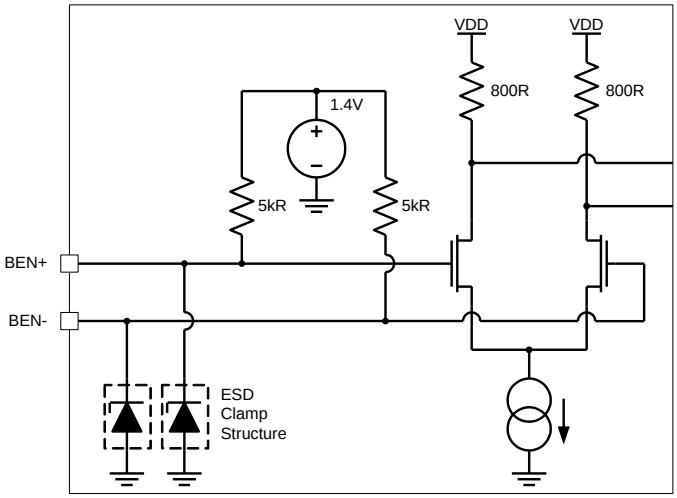


Figure 14 – NT25L91 Transmitter Burst Enable Input Internal Biasing

The burst enable inputs can be used either differentially or single ended depending on the termination scheme being used. The diagrams below indicate the correct termination methods for LVPECL, CML and LVTTL signaling schemes. The burst enable inputs should always be DC coupled for correct operation.

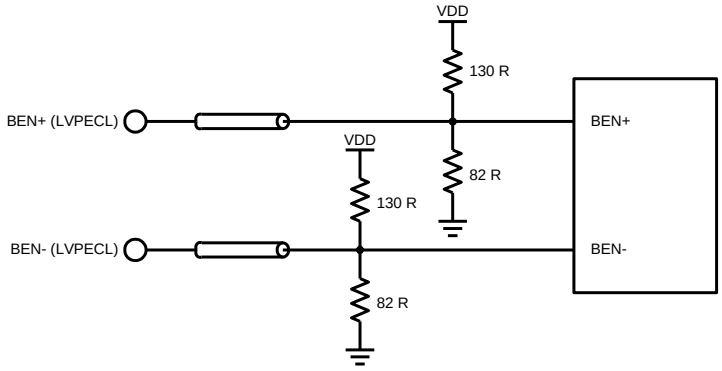


Figure 15 – NT25L91 BEN input termination: Differential LVPECL

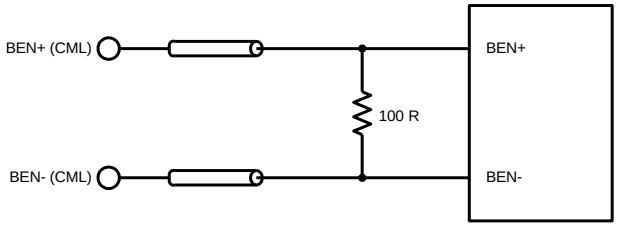


Figure 16 – NT25L91 BEN input termination: Differential CML

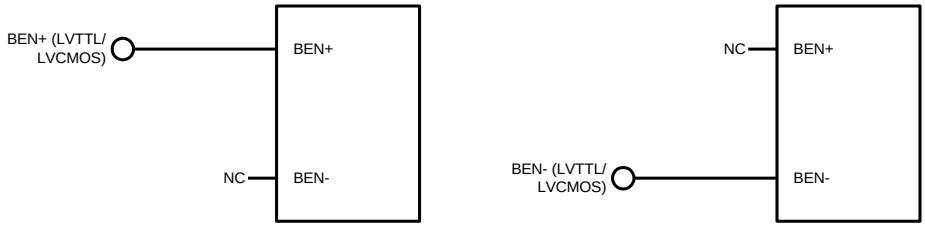


Figure 17 – NT25L91 BEN input termination: Single Ended LVTTL/LVCMOS

For electrical evaluation and characterization of the NT25L91 transmitter modulation outputs the test circuit shown in Figure 18 below is used.

The test circuit provides a DC coupled evaluation environment for the LASER+ and LASER- high speed modulation outputs with characteristic load impedance of 10 Ω. When measuring the output rise and fall times the differential output capacitor C_{DIFF} is not fitted. When output overshoot is being measured, the differential output capacitor CDIFF is fitted to represent a typical laser capacitance.

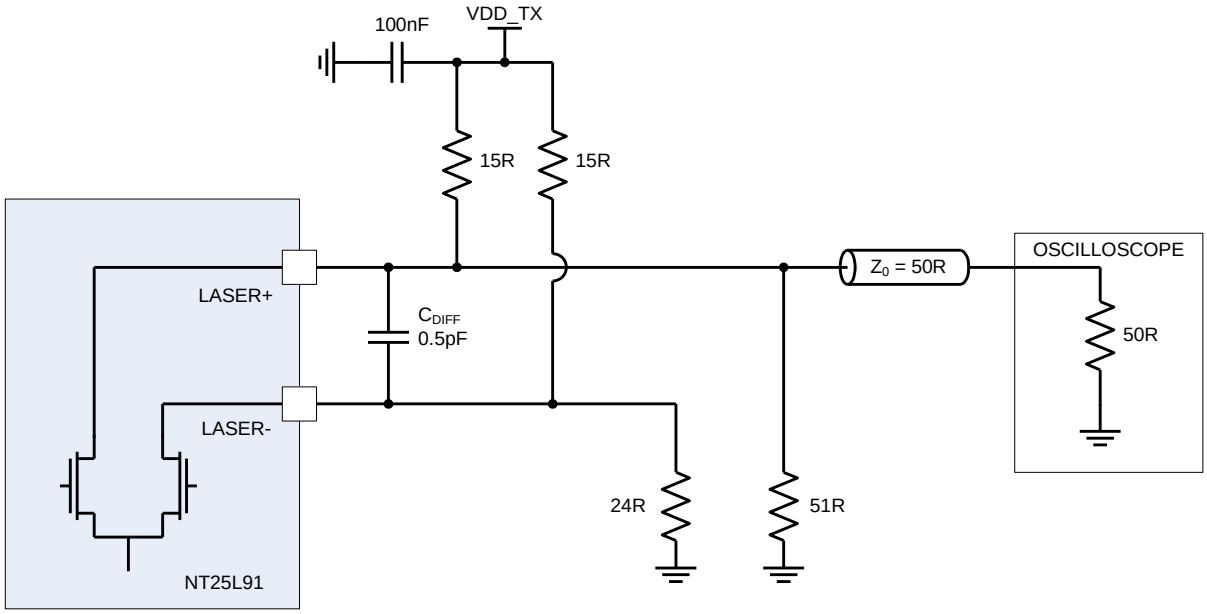


Figure 18 – NT25L91 Transmitter high speed modulation output evaluation circuit

Modulation Stage

The modulator stage comprises of a switched current source capable of switching up to 90 mA of modulation current through either the LASER+ or LASER- outputs. The modulation current is set digitally and is temperature compensated for laser efficiency changes over temperature and lifetime.

For correct burst-mode operation and fast laser turn on times the laser modulation outputs must be DC coupled to a common anode laser. The outputs can be either DC or AC coupled for non-burst applications such as standard SFP modules.

In the absence of input data, or the data inputs floating, the laser outputs will sink 50% of the modulation current through each pin, LASER+ and LASER-.

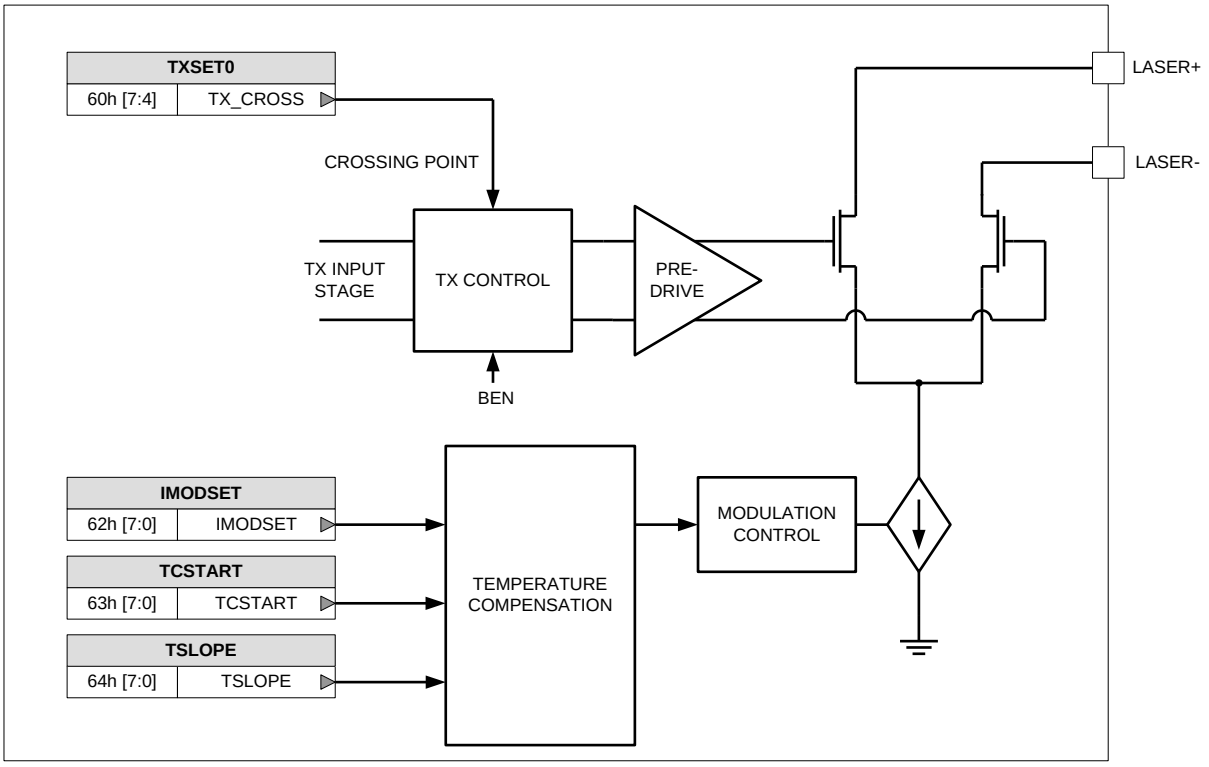


Figure 19 – NT25L91 Transmitter Modulation Stage Diagram

The NT25L91 modulator outputs are driven by the transmitter differential data input signal (TXIN+/TXIN-) and also controlled by the burst control inputs (BEN+/BEN-). The LASER+ output will sink modulation current if a logic one is transmitted through the TXIN data path and the BEN control path is enabled high. Use the TX_MOD_STEER (6Bh <3>) bit to invert the modulation current steering for flexible PCB design. The modulation output crossing point can be adjusted using the TX_CROSS control in the TXSET0 register.

The modulation current is derived from three controllable current sources which are accessed using the registers IMODSET, TCSTART and TSLOPE. The characteristic of each of the three current sources and how they are combined together to derive the total modulation current is described in the following section.

The NT25L91 modulation current can be programmed directly and simply, using only the IMODSET register. This will apply a constant modulation current depending on the register value set and detailed under the IMODSET Register DAC section. The registers TCSTART and TSLOPE should be programmed to 00h in this case. The user then has direct control of the modulation current using the IMODSET register via the I^2C interface.

Temperature Compensation Stage

The modulation output current is controlled using a digital temperature compensation computer that can be set-up to match the laser diode being driven and compensate for changes in laser efficiency over temperature and life time.

A temperature compensation stage within the modulation controller provides a method of adjusting the modulation current based on the ambient temperature and pre-set laser characteristics. The laser temperature compensation is programmed digitally and can function ‘stand alone’ without the need for an external microcontroller or memory.

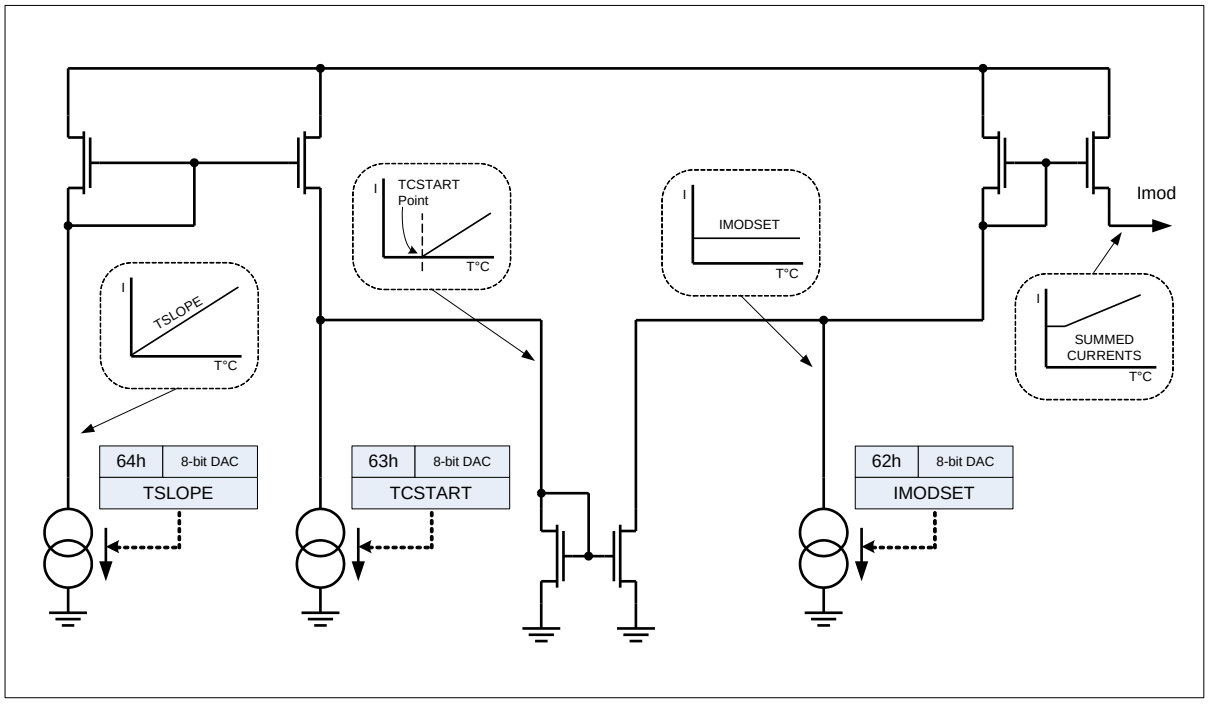


Figure 20 – NT25L91 Temperature Compensated Modulation Control

The NT25L91 temperature compensation circuit shown in Figure 20 uses three DACs to set the overall modulation current based on two different modulation current functions summed together.

The IMODSET register sets a modulation current that remains constant over temperature and voltage. IMODSET can be programmed by the user to set the room temperature modulation current before any temperature dependant currents are added.

The TSLOPE register is used to program a temperature varying current which is then added to the constant current set with IMODSET. The temperature varying current follows a linear gradient where the gradient is set by the TSLOPE DAC. The temperature at which this current starts to be added to the constant current is controlled by the TCSTART register.

IMODSET

The IMODSET register controls the constant portion of modulation current via a true 8-bit logarithmic DAC which follows the relationship described by the equation below:

$$I\_IMODSET\ (mA) = [0.4009 \times e^{(0.0217 \times IMODSET)}] - 0.04mA$$

The chart below shows actual modulation current plotted against the IMODSET register value.

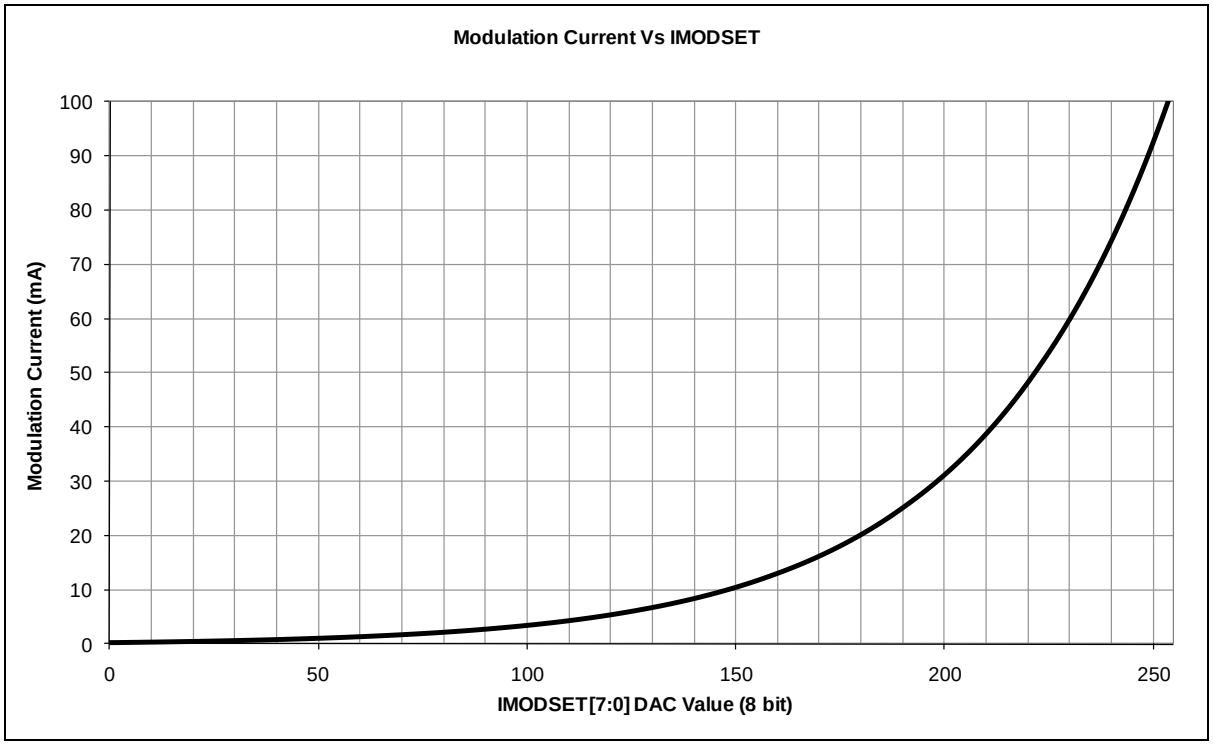


Figure 21 – NT25L91 IMODSET Register Value versus Modulation Current Output

The use of an 8-bit logarithmic DAC for setting the constant portion of modulation current means that the step-size resolution can be kept constant over the entire modulation current range and enables the user to set the modulation current to very small values, accurately. The modulation output drive stage is rated to 90mA but the DAC allows modulation currents up to 100mA to be programmed but this is not recommended for long-term operation.

TSLOPE

The TSLOPE register sets a temperature varying modulation current that can be added to the constant modulation current set by IMODSET. The TSLOPE register controls an 8-bit linear DAC that sets the slope of the temperature controlled current source. The current is a function of temperature and the TSLOPE register value set, as follows:

$$I\_TSLOPE\ (mA) = 0.288 * (1 + (MAX_{TSLOPE} * (T - 25°C))) * TSLOPE$$

Where, MAX_{TSLOPE} is the maximum selectable temperature slope allowed = 0.007500
This is the maximum SLOPE setting range given in ppm divided by 1.0E+6 [7500 ppm/°C / 1.0E+6]

T is the current ambient temperature in °C

TSLOPE is the actual register DAC value {0 to 255}

This leads to the following formula for calculating the actual temperature gradient slope:

Slope (mA/°C) = 0.002160 * TSLOPE

The chart in Figure 22 below shows the actual TSLOPE current plotted against temperature for various TSLOPE values and Figure 23 shows the slope value set by TSLOPE versus register code.

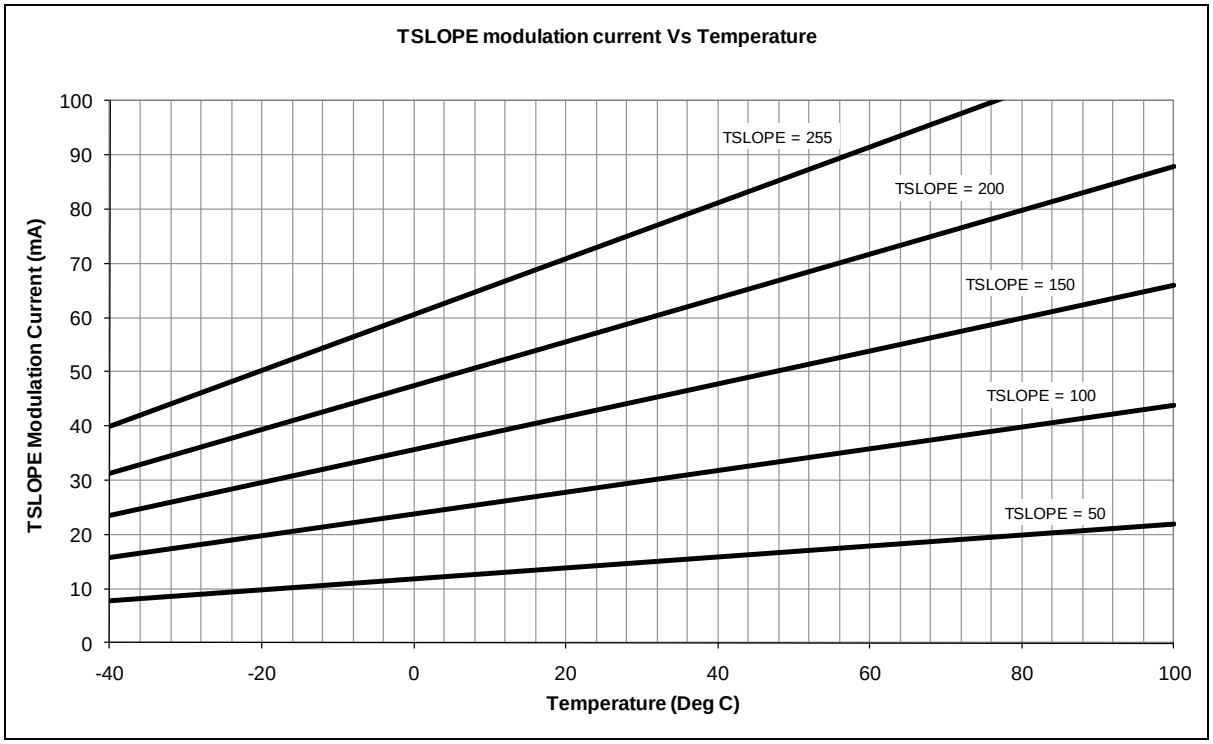


Figure 22 – NT25L91 TSLOPE Modulation Current versus Temperature

The TSLOPE register is used in conjunction with the TCSTART register so that the desired temperature varying slope is applied from a specific temperature starting point.

TCSTART

The TCSTART register controls an 8-bit DAC that sets the current value at which the TSLOPE current actually starts to contribute to the total modulation current. The TCSTART current start point is:

I_TCSTART (mA) = 0.32 * TCSTART

Where TCSTART is the actual register DAC value {0 to 255}

This describes the point at which the TSLOPE current will effectively start to contribute to the overall modulation current as TSLOPE and TCSTART are related as follows:

Temperature Compensated Current (mA) = I_TSLOPE – I_TCSTART

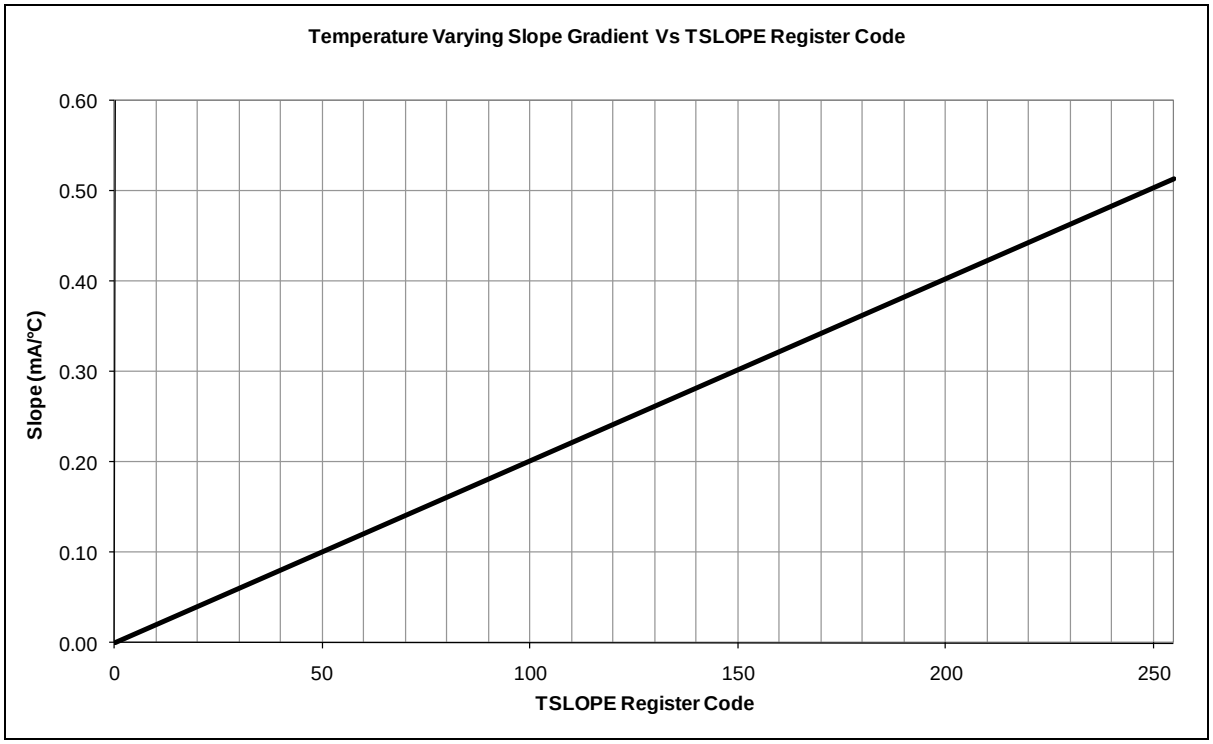


Figure 23 – NT25L91 TSLOPE gradient 'Slope' versus TSLOPE Register Value

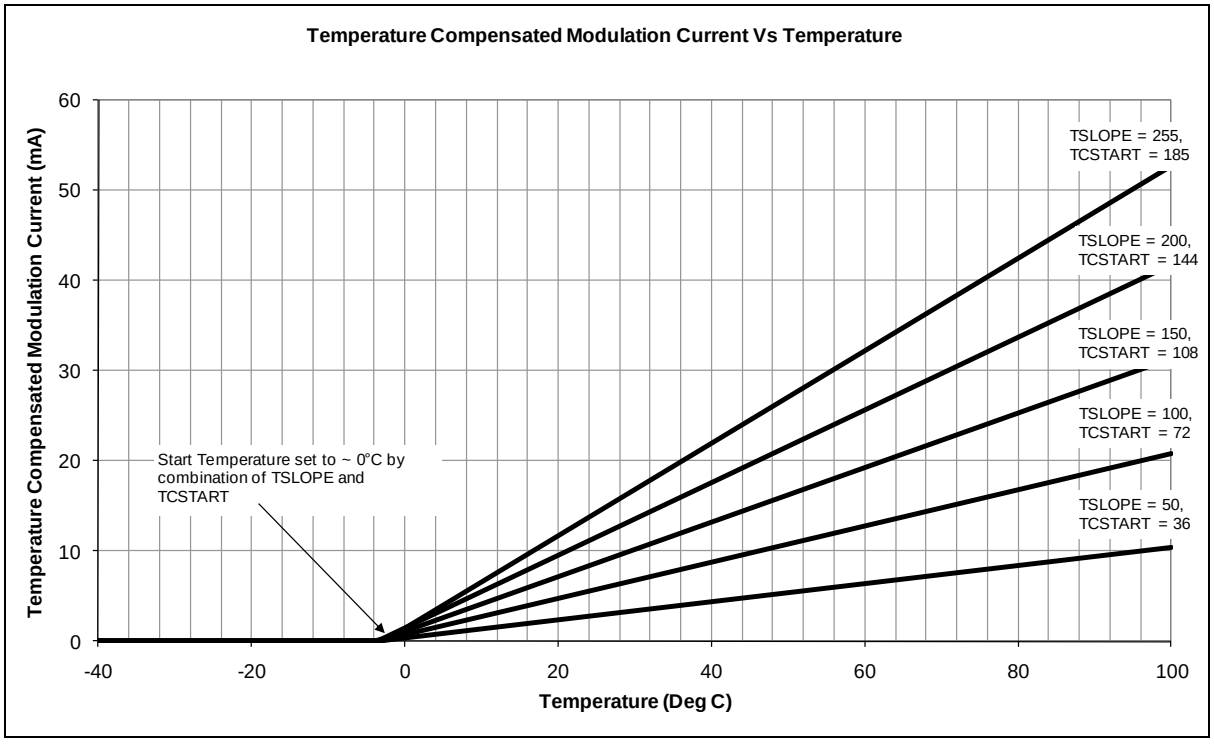


Figure 24 – NT25L91 Temperature Compensated Modulation Current Vs Temperature

Combining the Currents Together

The modulation currents derived from the above temperature compensation control registers are combined together in the on-chip temperature compensation stage to provide a single modulation current to the laser.

The currents are mathematically combined as:

Total Modulation Current (mA) = I_IMODSET + (I_TSLOPE – I_TCSTART)

From this equation we can see that setting registers TSLOPE and TCSTART to 00h results in a modulation current set only by IMODSET. It is possible to use combinations of IMODSET and TSLOPE with TCSTART to produce an overall modulation current that matches the required laser modulation current very well and therefore provides excellent control of extinction ratio over temperature, as shown in Figure 25 and Figure 26.

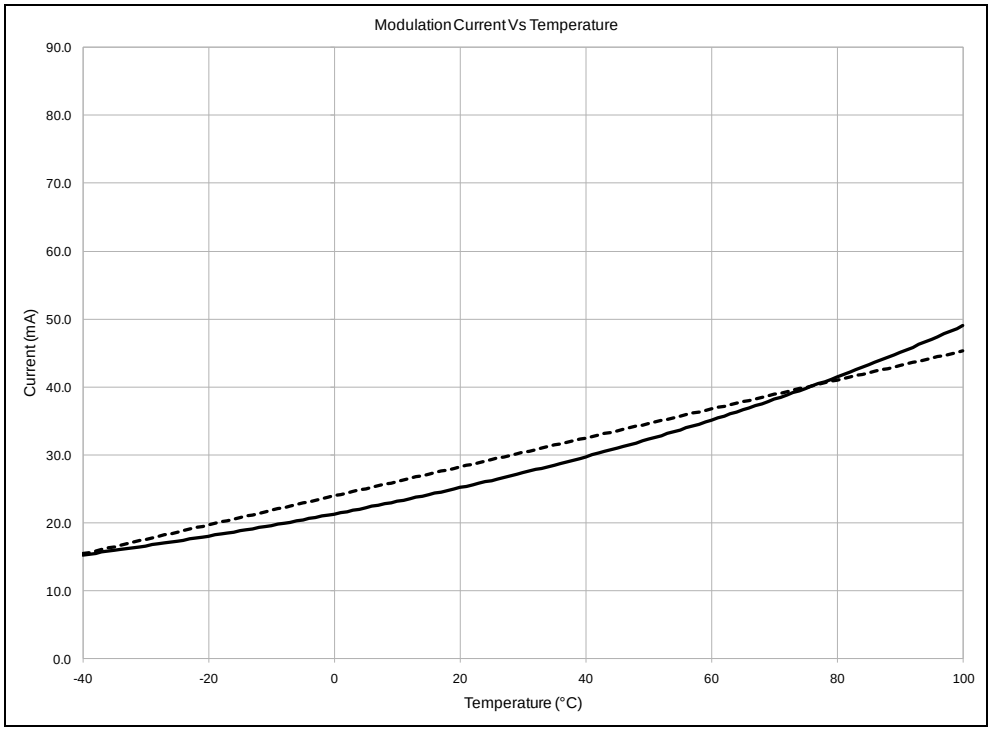


Figure 25 – Actual Laser Modulation Current (solid) Vs Compensated Modulation Current (dashed)

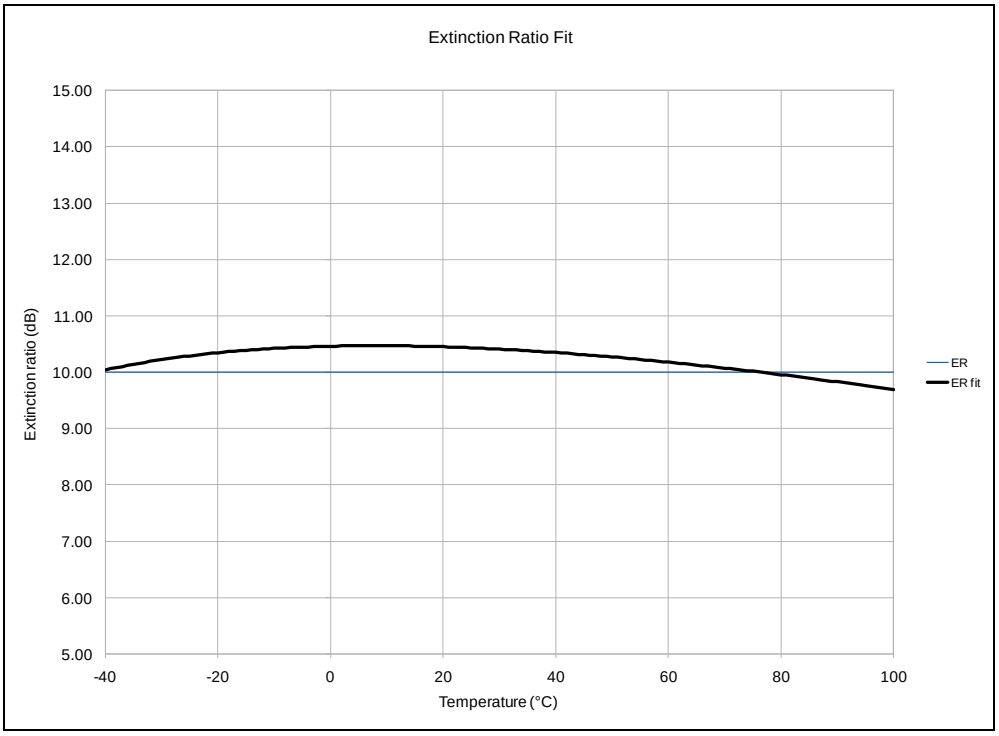


Figure 26 – Extinction Ratio Control Using Temperature Compensated Modulation Current

Bias Stage

The bias stage features a digital automatic mean power control loop that sets the mean output power and maintains this power over temperature and supply voltage changes. Bias currents of up to 100 mA can be achieved. The bias stage can operate in both burst and non-burst modes as a result of the digital control loop implemented in the NT25L91. The actual bias current can be programmed directly, via the BIASDAC register, or indirectly by setting a reference target monitor current for the automatic power control loop to maintain by adjusting the bias current internally.

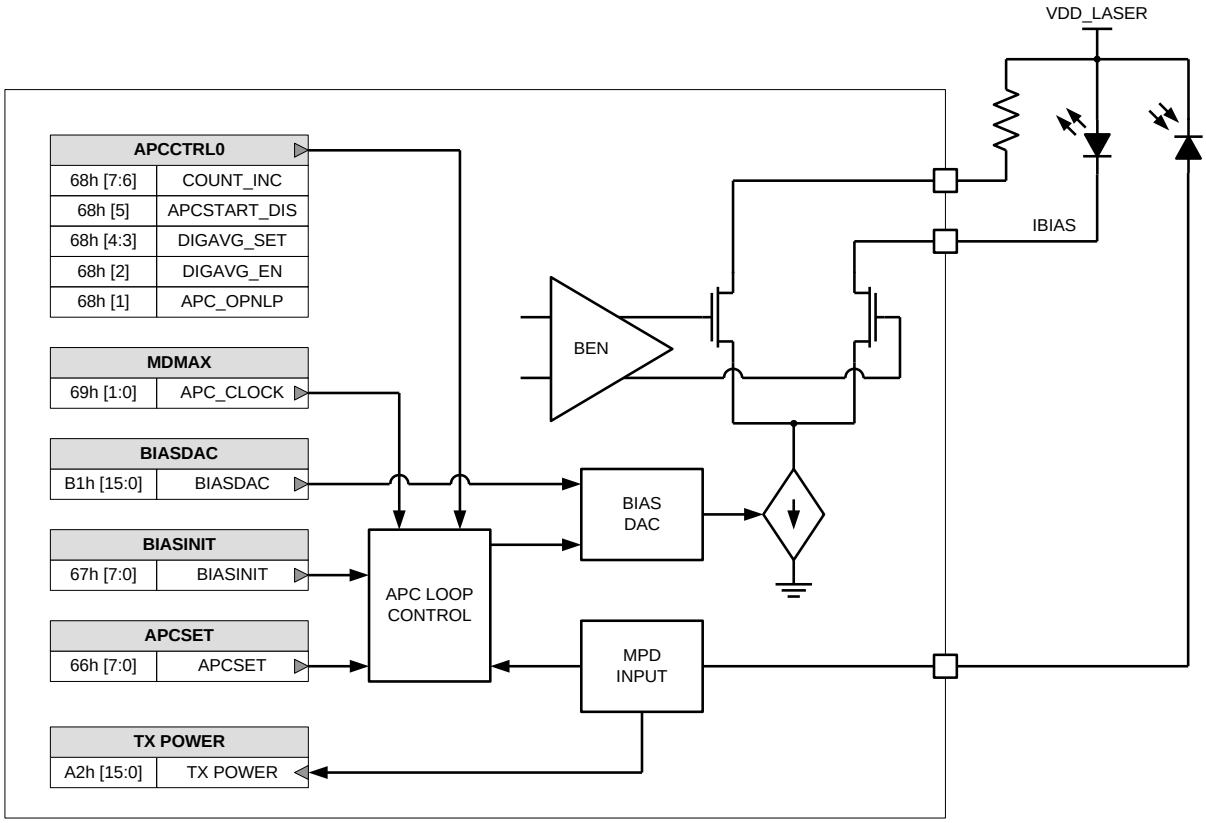


Figure 27 – NT25L91 Bias Stage Diagram

The bias stage comprises of several control registers which are detailed below.

APCSET

The APCSET register controls a pseudo logarithmic 8-bit DAC that is a piece-wise linear approximation to the exponential function:

Target Monitor Photodiode Current (µA) = $(7.4\mu A * 2^{(APCSET/32)}) + 1$

The APCSET register allows the user to set a target monitor photodiode current which is used during closed loop mean power feedback control. The NT25L91 internally adjusts the bias current so that the actual monitor photodiode current is equal to the target monitor photodiode current set by APCSET.

The target monitor photodiode current can be programmed from 7.4 µA up to 1800 µA as shown in Figure 28 and, as the function is logarithmic, the resolution is the same from the lowest to highest monitor current. This enables precise setting of transmitter output power even for low optical power requirements.

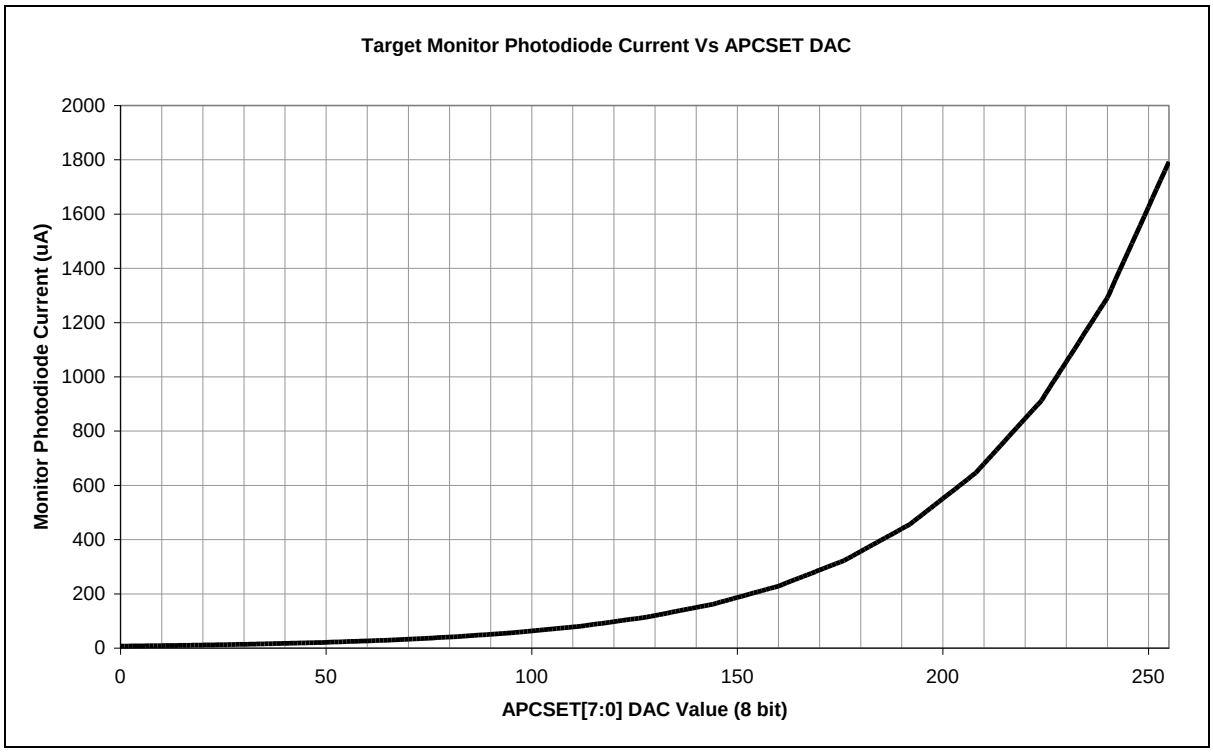


Figure 28 – NT25L91 Target Monitor Photodiode Current Vs APCSET Code

BIASDAC

The BIASDAC register is a 16-bit register that controls a 10-bit pseudo logarithmic DAC. Therefore only the upper 10 bits of the register are actually used to program the DAC, the remaining lower 6 bits should be set to zero. The BIASDAC register is actually programmed using two 8-bit registers, BIASDAC MSB (B1h) and BIASDAC LSB (B2h), so only the upper 2 bits of BIASDAC LSB are utilised.

The contents of both BIASDAC MSB and BIASDAC LSB are only transferred to the DAC when BIASDAC LSB is written. This is done to ensure that all bias DAC updates occur in a single step, even when a new value requires both registers to be changed

Lower Range	Upper Range	BIASDAC MSB (B1h)								BIASDAC LSB (B2h)							
0000h	FFC0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.8 mA	102.8 mA	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0

Table 9 – BIASDAC 16-bit register mapping

The bias current output can be calculated in Excel or similar using the following formula:

Bias Current (mA) = [(1/128) * (0.4mA*2^n) * ((BIASDAC+1)-(128*n))] + (0.4mA*2^n) + 0.4mA

Where BIASDAC is the actual BIASDAC decimal code {0 to 1023} and n = int(BIASDAC/128)

When operating in closed loop feedback mode the NT25L91 internally controls the bias current using the APCSET target value. The BIASDAC is used to set the actual bias current when the NT25L91 is used in open loop mode. Open loop mode is enabled by setting APCCTRL0 register APC_OPNLP to '1' (68h<1>). The default value for APC_OPNLP is 0 which sets the feedback to closed loop.

The BIASDAC register is in the volatile memory area, rather than non-volatile, as this is intended to be controlled using an external microcontroller for applications that require more advanced control of the bias current.
The relationship between BIASDAC code and the bias current output is shown in Figure 29.

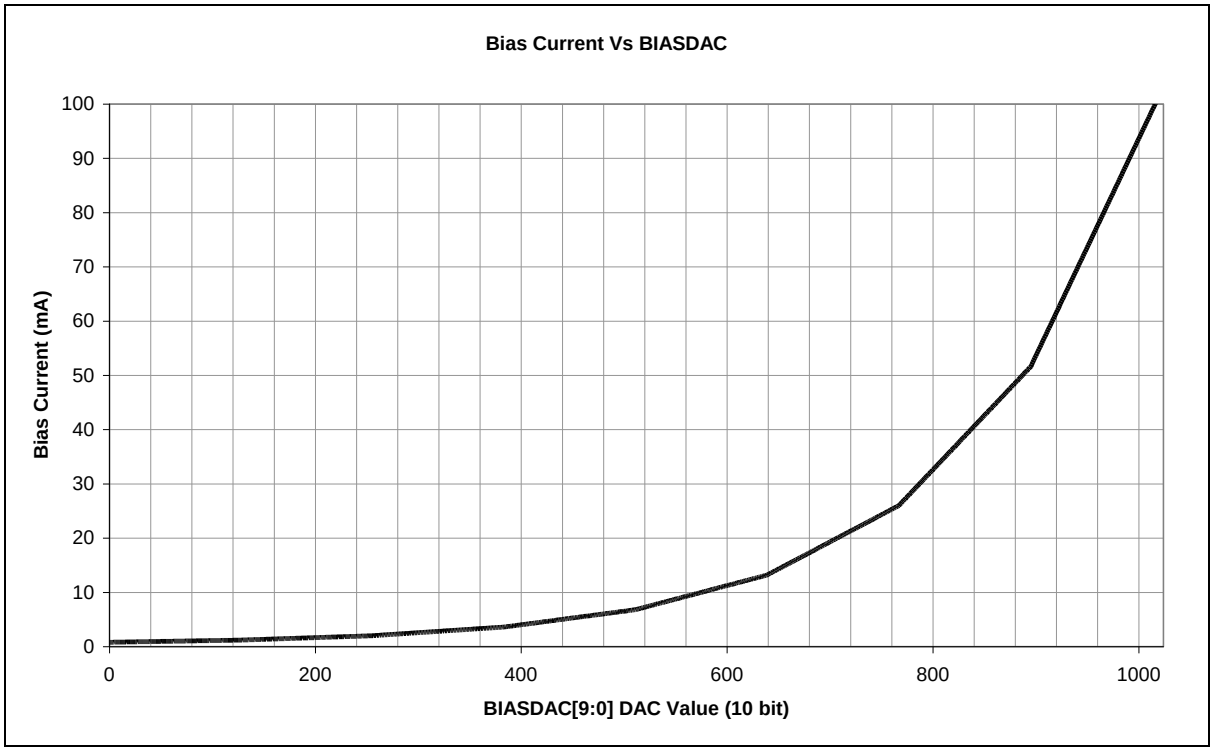


Figure 29 – NT25L91 Bias Current Vs BIASDAC Code

Burst Control Stage

The NT25L91 features a sophisticated burst controlled automatic feedback loop that allows the mean power loop to respond quickly to burst enable inputs and turn the bias and modulation currents on in less than 12.8 ns.

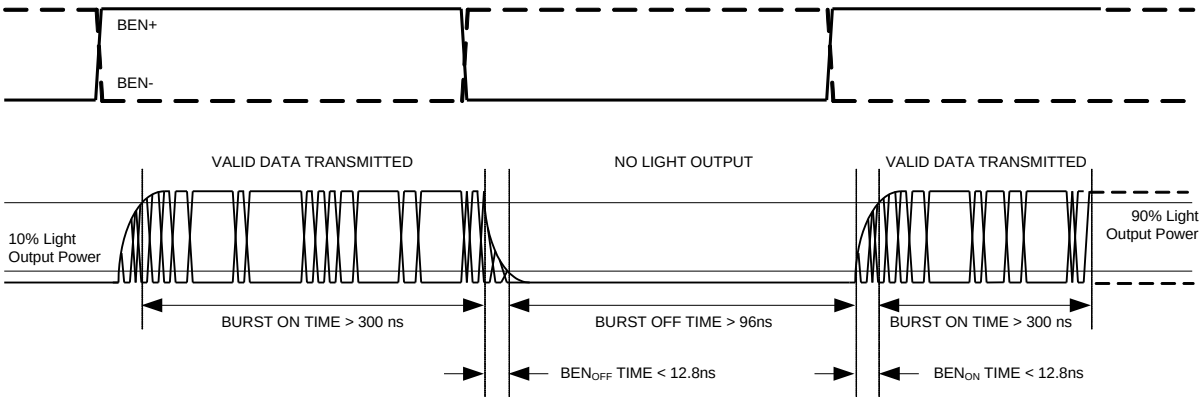


Figure 30 – Burst Control Timing

The burst controller also features a fast start-up algorithm that can set the correct laser mean power within three burst on cycles as shown in Figure 31.

The digital APC loop that provides fast start-up for burst-mode operation can be optimised for various applications using the control registers shown in Figure 27, specifically APCCTRL0 and MDMAX registers.

APC_CLOCK

APC_CLOCK is a 2-bit control for the speed of the oscillator used to clock the APC loop. By default the APC_CLOCK is set to the fastest programmable rate of 6.5 MHz. During APC start-up, the fastest rate of 6.5 MHz is always applied in order to meet the GPON start-up timing requirements shown in Figure 31.

The APC_CLOCK sets the steady state APC loop sampling rate. Reducing the APC_CLOCK rate effectively reduces the loop sampling rate which can be useful for low data rate applications (below 622Mbps) to reduce base line wander effects. The APC_CLOCK is changed by setting the relevant bits in register MDMAX as shown in the table below.

Register MDMAX 69h <1:0>		Divider Value	Nominal Clock Rate	Nominal Loop Time Constant
APC_CLOCK_1	APC_CLOCK_0			
0	0	1	6.5 MHz	154 ns
0	1	÷ 16	406 kHz	2.46 µs
1	0	÷ 64	101 kHz	9.85 µs
1	1	÷ 256	25 kHz	39.4 µs

Table 10 – APC_CLOCK Settings

The fast start-up speed can be changed by setting LOOP START in register TXSET0 60h <3> to '1'. When LOOP START is set to '1' the APC loop will use the current APC_CLOCK rate during start-up as well as during normal steady state operation. It is not recommended to change the fast start-up rate when using the NT25L91 in burst-mode applications.

The fast start-up algorithm can be disabled completely by setting APCSTART_DIS to '1'. APCSTART_DIS can be found in register APCCTRL0 68h <5>. If APCSTART_DIS is set to '1' then the APC fast start-up algorithm is not used and instead the bias current is set to the current BIASINIT value. Once the BIASINIT value has been loaded then the APC loop goes straight into standard integration mode and the APC loop samples at the current APC_CLOCK rate. If the current BIASINIT value is zero then the APC loop waits until the BIASINIT is programmed with a non-zero value before applying any bias current. This effectively holds the transmitter in a disabled state until the BIASINIT value is programmed.

DIGAVG_SET

DIGAVG_SET is a 2-bit control used to set the amount of digital average applied to the APC loop. The function is enabled by setting the DIGAVG_EN bit to '1'. The default for the NT25L91 is digital averaging disabled. When not used (i.e. default) the APC loop makes a decision to increment or decrement the bias current DAC by one bit step on every clock cycle. If the digital averaging function is enabled then the APC loop decision is taken less frequently on multiples of the APC loop clock rate as shown in the table below.

Register APCCTRL0 68h <4:2>			Clock Cycles Counted	Time Constant for 6.5 MHz Clock
DIGAVG_EN	DIGAVG_SET_1	DIGAVG_SET_0		
0	x	x	1	154 ns
1	0	0	32	4.92 µs
1	0	1	64	9.85 µs
1	1	0	128	19.7 µs
1	1	1	256	39.4 µs

Table 11 – APC Loop Digital Averaging Settings

For non-burst mode low data rate applications the APC loop performance can be optimised by reducing the APC clock rate using the APC_CLOCK function. For burst-mode applications the APC loop performance can be optimised better by applying the full APC loop clock rate of 6.5 MHz and then using the digital averaging function DIGAVG_SET to alter the loop response time.

Fast Start-up Algorithm

The NT25L91 uses a four stage fast start-up algorithm to enable the transmitter output to reach the desired optical output conditions within GPON timing requirements. The four stages are shown in Figure 31 and described below in detail.

- Stage 1: The bias current is set to 0.5 x Modulation Current. The modulation current is a function of IMODSET + (TSLOPE – TCSTART).
- Step 2: The bias current is increased by linearly ramping, or incrementing, the BIASDAC by the number of steps defined in COUNT_INC for each clock period. The bias current output will actually ramp non-linearly as the BIASDAC function is pseudo logarithmic.
- Step 3: Once the linear ramp phase has incremented the bias current such that the actual monitor current is greater than the target monitor current, set by APCSET, then a binary search phase is initiated. The binary search alters the bias current to achieve an actual monitor current that is within one bit value of the target monitor current.
- Step 4: The final stage is APC loop integration mode. The APC loop samples the monitor current at a loop clock rate defined by APC_CLOCK and makes a decision on the sampled monitor current to increment or decrement the BIASDAC value in order to maintain the monitor current at the target value defined in the APCSET register.

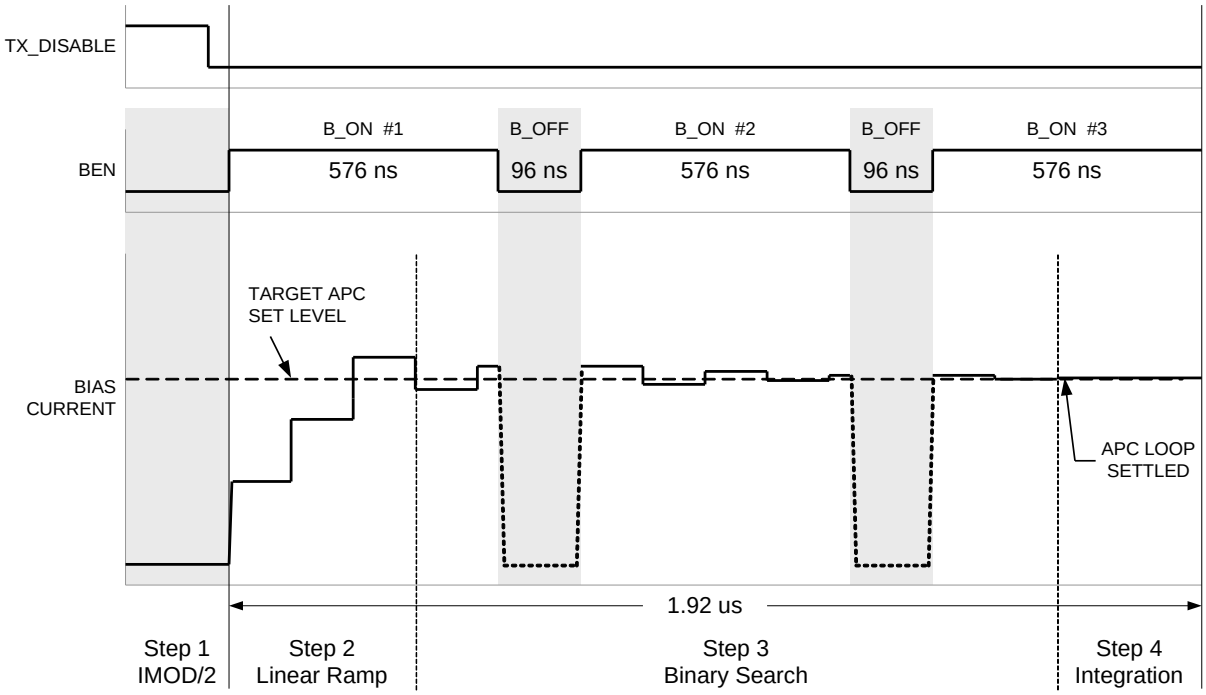


Figure 31 – APC Loop Start-Up Timing in Burst Mode

COUNT_INC

The COUNT_INC function is a 2-bit control for adjusting the step size of the bias current during the linear ramp phase of the fast start-up algorithm as shown in Figure 31. The COUNT_INC control is located in the upper two bits of the APCCTRL0 register at 68h <7:6>.

The COUNT_INC function is used to change the ramp step size in stage 2 of the fast start-up algorithm. The default value is 64 bits and means that the BIASDAC will be incremented by 64 bits for each ramp step during the linear ramp stage. Smaller step sizes can be programmed as shown in the table below.

Register APCCTRL0 68h <7:6>		Step Value
COUNT_INC_1	COUNT_INC_0	
0	0	64 bits (default)
0	1	32 bits
1	0	16 bits
1	1	8 bits

Table 12 – COUNT_INC Setting Values

BIASINIT

BIASINIT is an 8-bit register that enables the user to program an initial bias current to aid fast start-up times during burst operation. When BIASINIT is used, the fast start-up algorithm uses this value at stage 1 of the search. The BIASDAC current value can be calculated in Excel or similar using the following formula:

Initial Bias Current (mA) = [(1/32) * (0.4mA*2^n) * ((BIASINIT+1)-(32*n))] + (0.4mA*2^n) + 0.4mA

Where BIASINIT is the actual DAC decimal code {0 to 255} and n = int(BIASINIT/32)

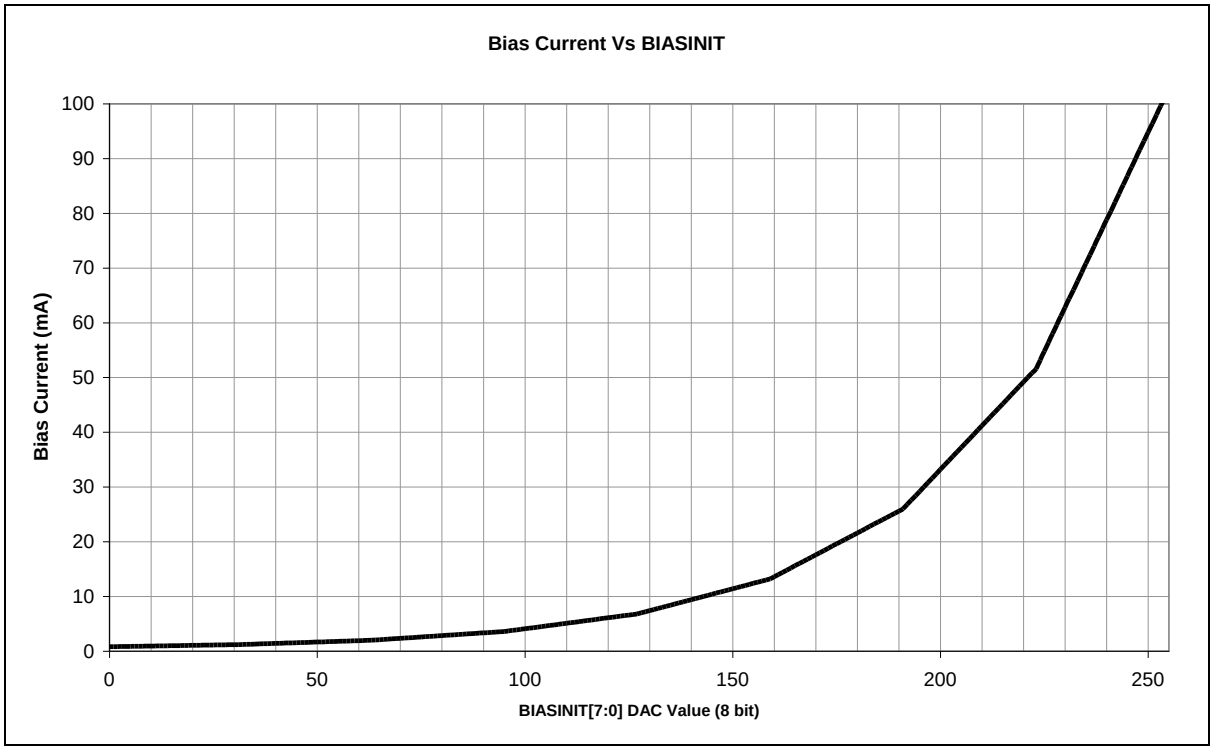


Figure 32 – NT25L91 Bias Current Vs BIASINIT Code

BIASMAX

The BIASMAX function is provided to allow the user to set a maximum bias current limit beyond which a TX_FAULT condition will be asserted. The BIASMAX function is programmed through register 6Ah <7:0> and provides an 8-bit control for setting the upper bias current. The NT25L91 is designed to produce bias currents up to 100 mA. To set the upper limit of BIASMAX to the maximum protected limit of 100 mA, program register 6Ah to value FEh.

If BIASMAX is set to FFh then the NT25L91 will apply no upper limit to the bias current output stage.

In the case where the BIASMAX limit is exceeded then a latched TX_FAULT will assert and the transmitter bias and modulation currents will be disabled until the TX_FAULT condition is reset by toggling the TX_DISABLE input. If the bias current persists in exceeding the BIASMAX limit then the TX_FAULT will repeatedly assert until the bias current falls below the BIASMAX limit.

The BIASMAX DAC is a pseudo logarithmic 8-bit DAC made up of 8 ranges of 32 values. The DAC output can be calculated in Excel or similar using the following formula:

Bias Current Maximum (mA) = [(1/32) * (0.4mA*2^n) * ((BIASMAX+1)-(32*n))] + (0.4mA*2^n) + 0.4mA

Where BIASMAX is the actual DAC decimal code {0 to 255} and n = int(BIASMAX/32)

Note: Setting BIASMAX to FFh disables the BIASMAX limit function.

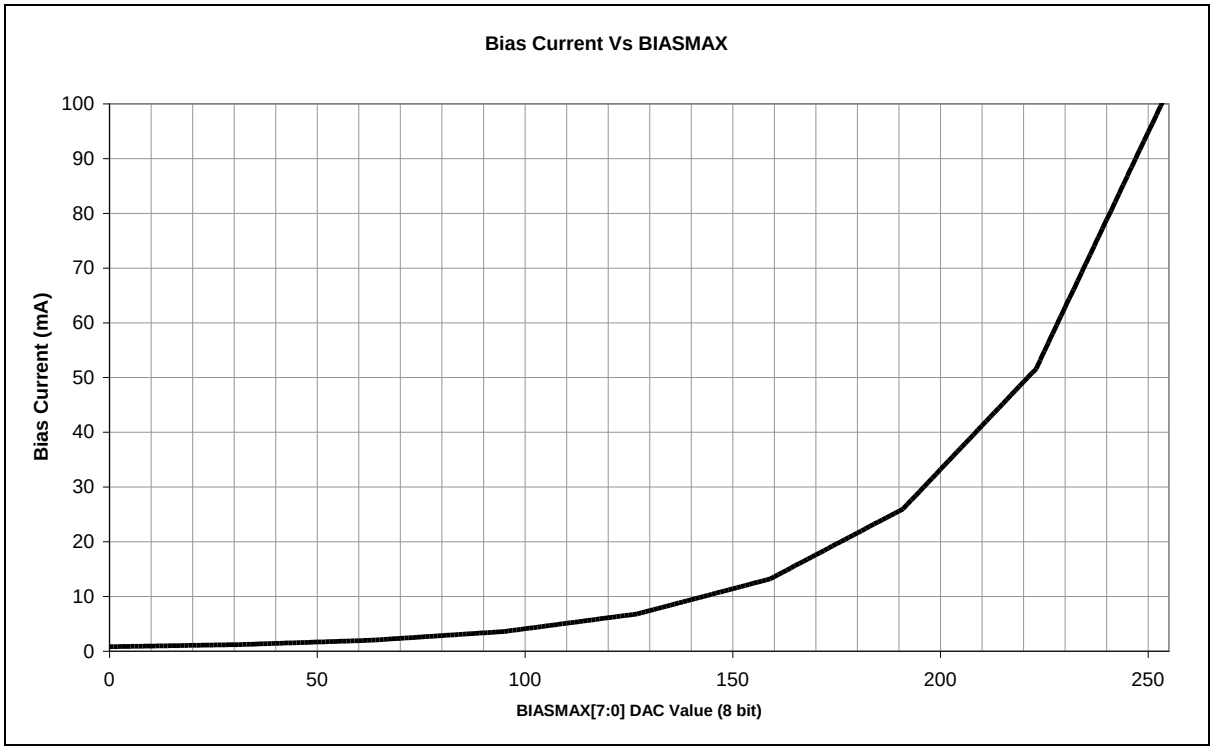


Figure 33 – NT25L91 Bias Current Maximum Limit Vs BIASMAX Code

MDMAX

The MDMAX function is provided to allow the user to set a maximum monitor photodiode current limit beyond which a TX_FAULT condition will be asserted. The MDMAX function is programmed through register 69h <7:2> and provides a 6-bit control for setting the upper monitor photodiode current. The NT25L91 is designed to operate with monitor photodiode currents up to 1800 µA. If the MDMAX register is set to FCh then no limit is applied and the monitor current could go above 1800 µA, w hich is outside of the NT25L91 operating specification.

To set the upper limit of MDMAX to the maximum protected limit of 2016 µA, program register 69h to value F8h. The lower two bits of this register also control the APC_CLOCK and therefore the value programmed must consider both the MDMAX and APC_CLOCK functions when using this register.

In the case where the MDMAX limit is exceeded then a latched TX_FAULT will assert and the transmitter bias and modulation currents will be disabled until the TX_FAULT condition is reset by toggling the TX_DISABLE input. If the monitor current persists in exceeding the MDMAX limit then the TX_FAULT will repeatedly assert until the monitor current falls below the MDMAX limit.

The MDMAX DAC is a 6-bit linear DAC with values as follows:

Maximum Monitor Current (uA)= 32 * (MDMAX+1)

For values of MDMAX < 63. Where MDMAX = 63, no upper limit will be applied to the MPD current.

Note: Setting MDMAX to FCh disables the MDMAX limit function.

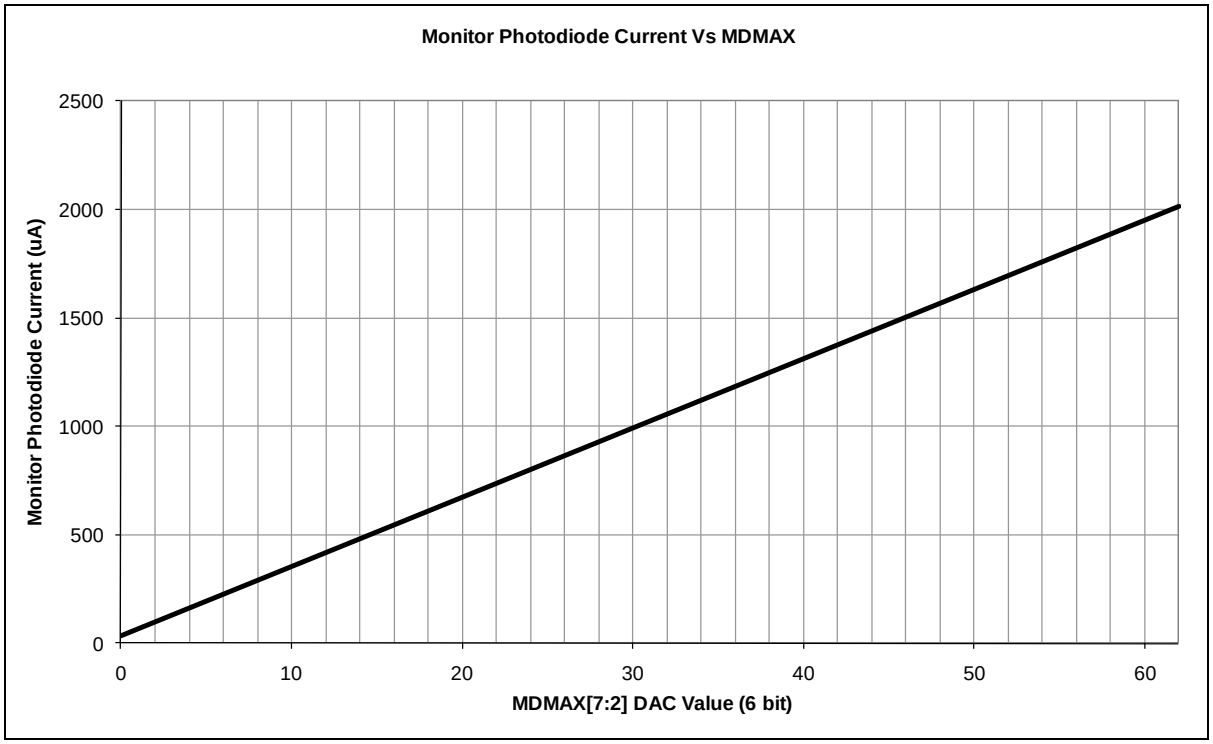


Figure 34 – NT25L91 Monitor Photodiode Current Maximum Limit Vs MDMAX Code

Transmitted Signal Detect Status Output

The NT25L91 features a TX_SD open drain status output pin to indicate whether the laser is currently activated or disabled. The NT25L91 uses the monitor photodiode current to ascertain whether the laser is transmitting light. The actual monitor photodiode current (I_{MPD}) is compared with the mean target monitor current (I_{MPD_APCSET}). If the actual monitor current is greater than 0.105x the target mean monitor current then TX_SD will be asserted. The TX_SD circuitry has been designed to cope with long runs of zeroes found in standard SONET and GPON patterns. The diagram below shows the timing associated with the TX_SD function. The polarity of the TX_SD function can be inverted by setting bit 3 (TX_SD_POL) of register 61h (TXSET1) to '1'.

As the TX_SD function is derived directly from the monitor photodiode current it will assert high as soon as the photocurrent detected is greater than 0.105x the target monitor current. Therefore during the initial average power control start-up sequence when the NT25L91 is searching for the correct mean power level, the TX_SD will be asserted as shown in Figure 36.

During power-up and initialisation the TX_SD output will remain de-asserted. The TX_SD output asserts after the transmitter is activated.

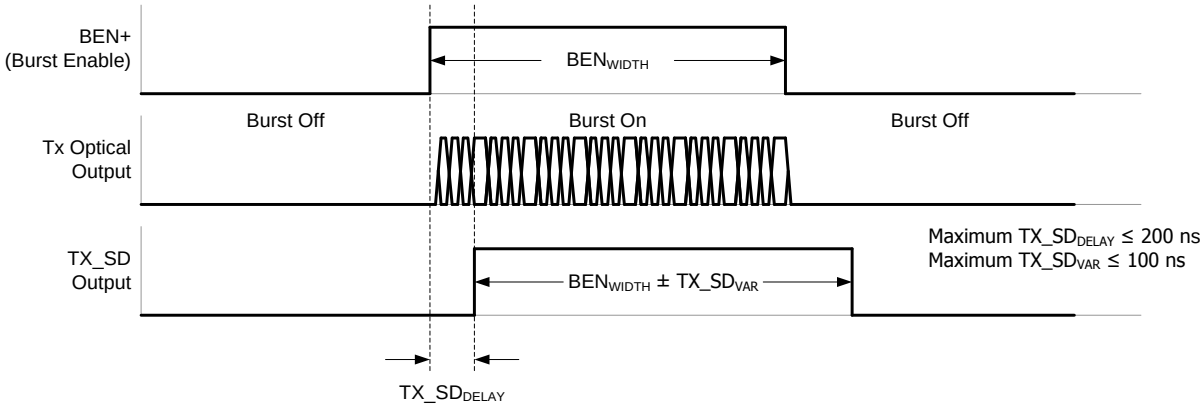


Figure 35 – NT25L91 TX_SD Timing Diagram

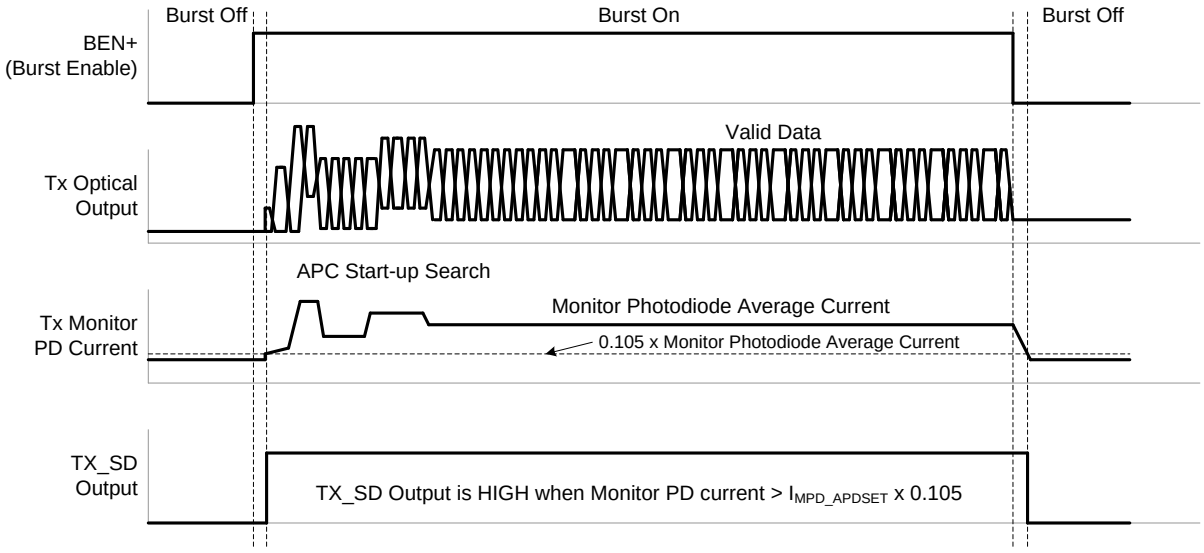


Figure 36 – NT25L91 TX_SD Function during APC Start-up Search Condition

GPON Power Levelling

The NT25L91 features a GPON Power Levelling mode which can automatically reduce the transmitted output power by 3dB and 6dB as required by the ITU GPON standard. This function is controlled by the upper two bits of the CONTROL0 register in volatile memory and is intended to be used in conjunction with an external microcontroller. The table below shows how the GPON power levelling function operates.

Register CONTROL0 B0h <7:6>		GPON Power Level	MPD Current (APCSET)	Modulation Current
GPON_1	GPON_0			
0	0	0 dB (default)	x 1.0	x 1.0
0	1	-3 dB	x 0.5	x 0.5
1	1	-6 dB	x 0.25	x 0.25
1	0	Not Used	-	-

Table 13 – GPON Power Levelling Function

If GPON power levels of -3 dB or -6 dB are programmed then the NT25L91 automatically reduces the target APC monitor current and modulation current by 50% or 75% respectively. This results in a reduction in optical transmitted power of -3 dB or -6 dB whilst maintaining the correct extinction ratio and temperature compensated modulation current. It is expected that the GPON power level settings will not be changed during actual data transmission.

Tx Crossing Point Adjust

The transmitter crossing level can be adjusted using the TX_CROSS control in register TXSET0 <7:4>. This gives a 4-bit control over the transmitter crossing point. The crossing point is adjusted by varying the pulse width of the transmitter eye from approximately -45 ps to + 45 ps. Adjusting the pulse width essentially shortens or lengthens the one-level period as shown in Figure 37. The nominal setting for TX_CROSS to achieve a 50% crossing point is 07h. The crossing adjustment control will have greatest effect when the data period is shortest at 2.5 Gbps. For data rates lower than 2.5 Gbps the crossing point adjustment will result in less aggressive variation in the crossing point.

The change in one-level pulse width versus the crossing point adjust control code TX_CROSS is shown in Figure 38.

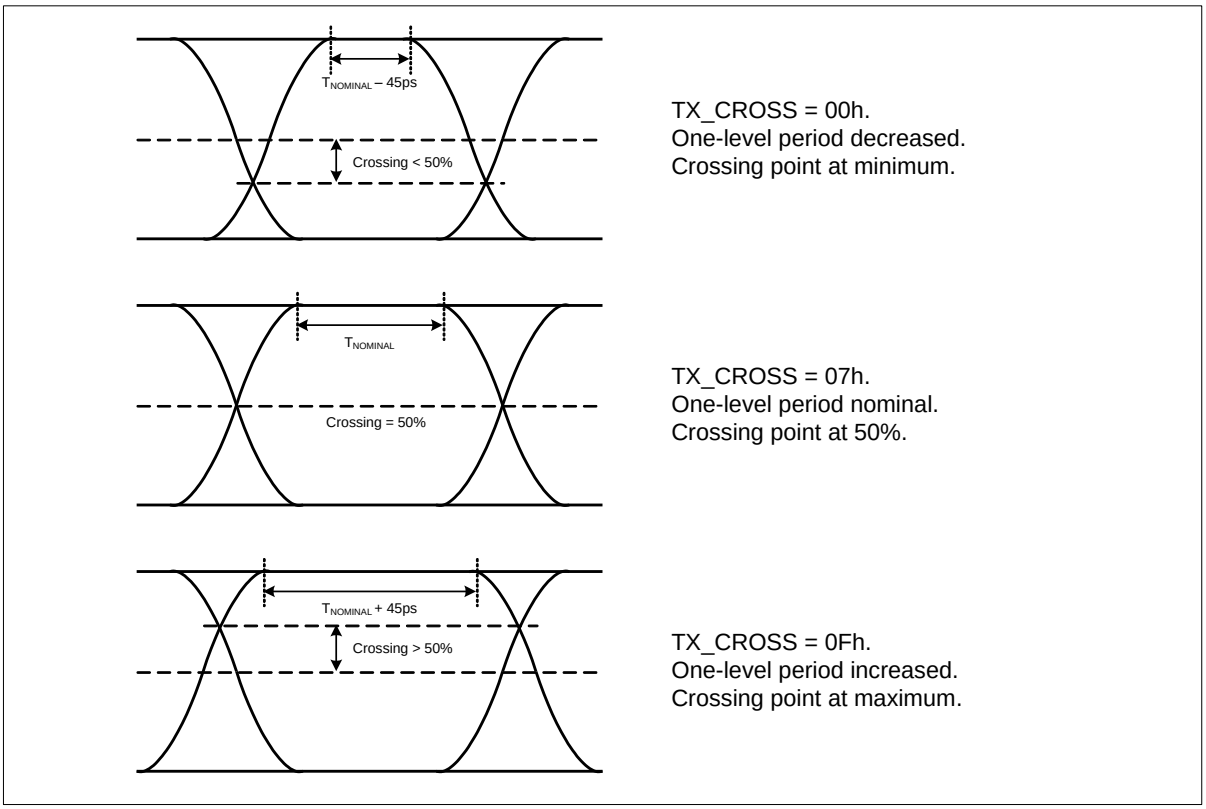


Figure 37 – NT25L91 Tx Crossing Point Adjustment using TX_CROSS

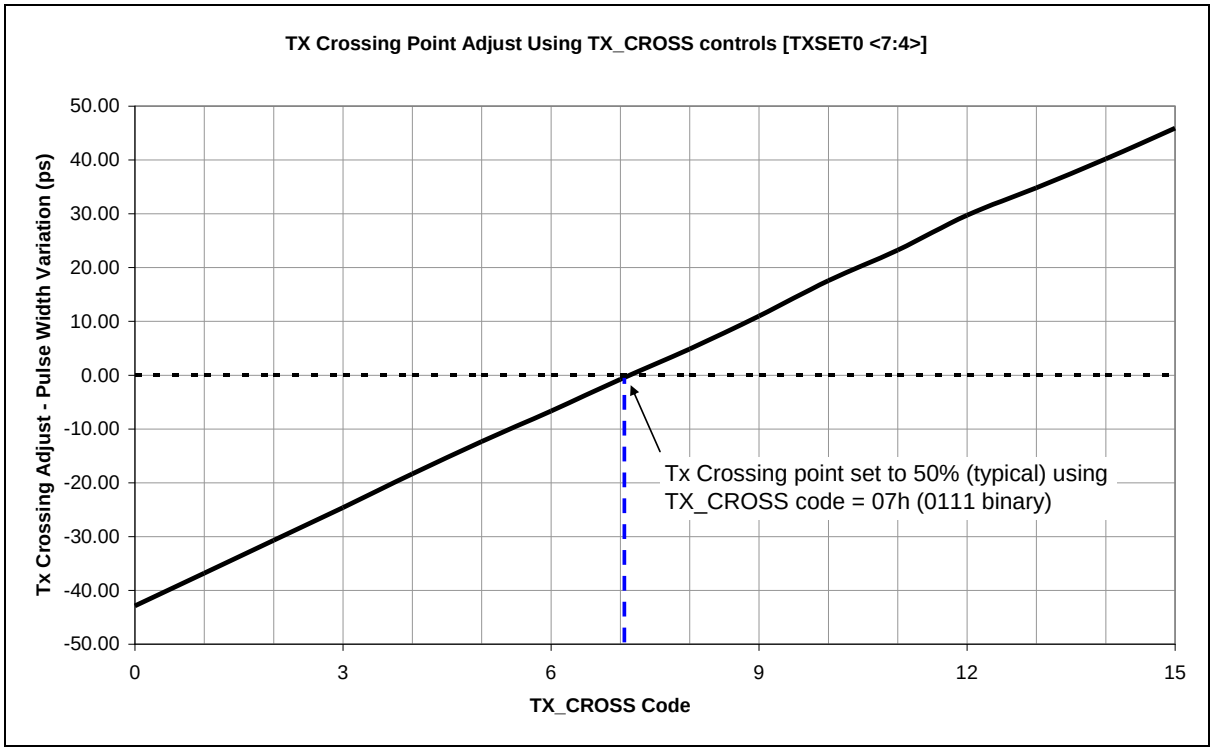


Figure 38 – NT25L91 Tx Crossing Point pulse width variation versus TX_CROSS

Eye Safety Stage

The NT25L91 features in-built IEC-60825 Eye Safety circuitry that can be programmed as required for the target application.

The NT25L91 includes a TX_DISABLE hardware input and software control via I^2C and a TX_FAULT hardware open drain output with software pin status indicator.

Programmable maximum bias and monitor current limits provide both eye safety and laser end-of-life (EOL) alarms.

A VDD supply monitor can disable the transmitter should VDD_TX go above or below factory limits (see Table 8).

The APC loop is protected by a single-point of failure check such that any opens or shorts to the APC loop cause a TX_FAULT condition as required by IEC-60825. The NT25L91 circuit response to single point failures is shown in Table 14.

If an APC fault occurs, then the TX_FAULT open drain output will be switched and pulled high by an external pull-up resistor (typically 4k7 Ω to 10k Ω). In the same instance, the bias and modulation currents will be internally disabled to turn off the laser. An internal FET switch is also included on-chip to turn off the positive to supply to the attached laser diode, VDD_TXO.

In the case of an APC loop fault, the TX_FAULT output can only be reset and the outputs enabled again by either cycling the NT25L91 power supply or by toggling the TX_DISABLE input for duration greater than 10 µs.

The NT25L91 safety logic circuit diagram is shown in Figure 39. The safety logic can be completely disabled by setting FAULT_INHIBIT to ‘1’. Any latched faults can be changed to non-latching faults by setting LATCH_INHIBIT to ‘1’. The supply voltage monitor can also be disabled such that any over or under voltage events on TX_VDD do not cause a TX_FAULT condition by setting VDD_FAULT to ‘1’.

Finally, the NT25L91 features a watchdog timer function for use with external microcontrollers. If an external microcontroller is used to constantly update the NT25L91, for example when supplying bias and modulation control using a look-up table, then the user may want to protect the NT25L91 from a microcontroller failure by using the watchdog function. If the watchdog is enabled (by default it is disabled) by setting WATCHDOG_EN to ‘1’ then the external microcontroller must repeatedly update the WATCHDOG register B3h with the value FFh every 100ms so that the watchdog counter does not cause a TX_FAULT condition. The watchdog counter will trigger a TX_FAULT if the timer is allowed to count down from FFh to 00h.

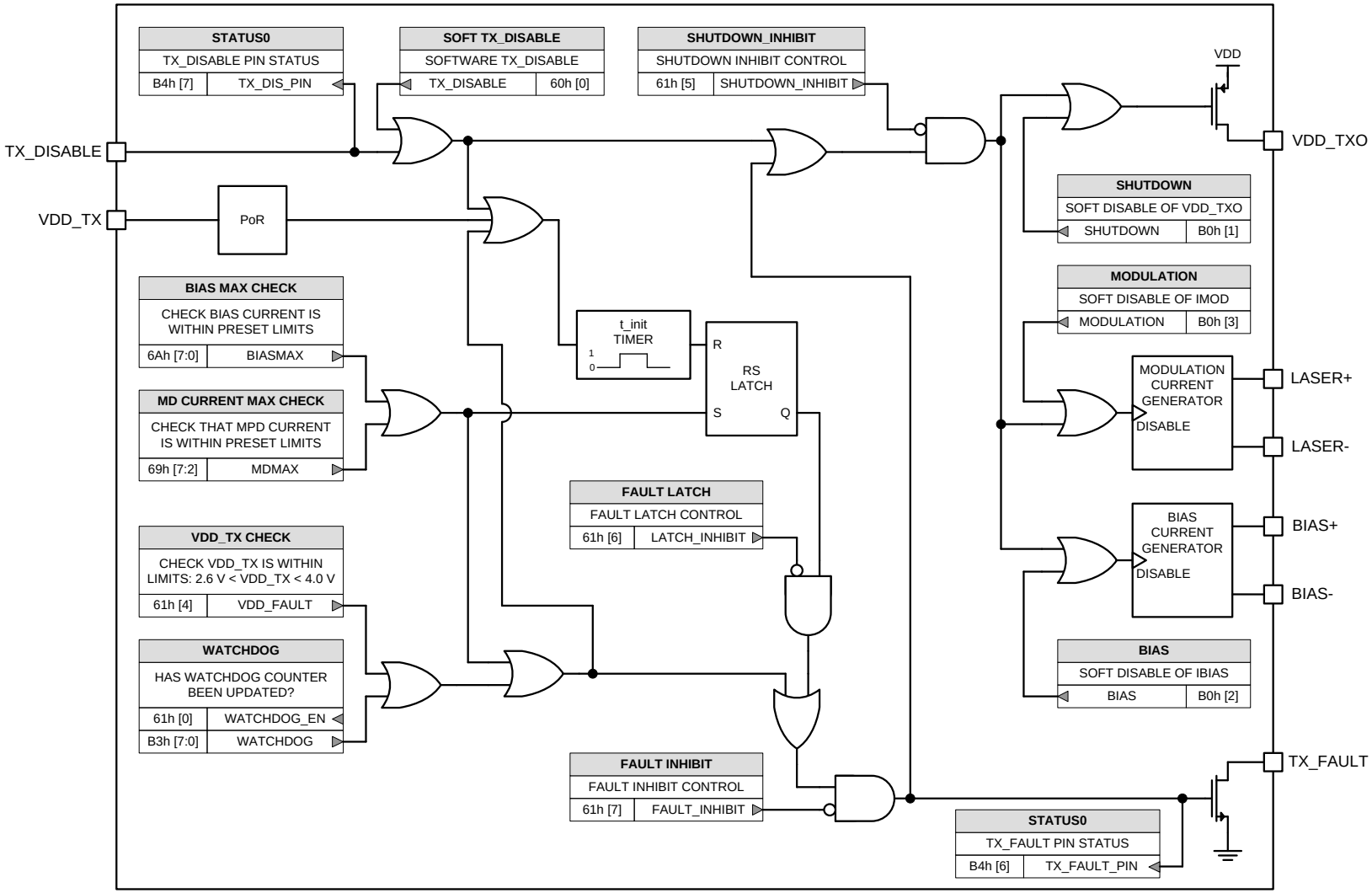


Figure 39 – NT25L91 Safety Logic Control Circuit

Table 14 – Circuit Responses to Single Point Failures

The table below shows the NT25L91 responses to single point failures at each pin:

PIN	NAME	SHORT TO VDD_TX	SHORT TO GND	OPEN
1	SD/LOS	None. Excessive SD/LOS current. Could cause internal damage to circuits.	None	None
2	RXOUT-	None. Could cause internal damage to circuits.	None. Could cause internal damage to circuits.	None
3	RXOUT+	None. Could cause internal damage to circuits.	None. Could cause internal damage to circuits.	None
4	VDD_DIG	None.	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	IC not powered correctly. Tx will not function.
5	DCAP	None. Excessive supply current. Could cause internal damage to circuits.	None. Excessive supply current. Could cause internal damage to circuits.	None
6	SDA	None. Communications will not function.	None. Communications will not function.	None
7	SCL	None. Communications will not function.	None. Communications will not function.	None
8	TX_DISABLE	Tx disabled.	None	Tx disabled.
9	TXIN+	None	None	None
10	TXIN-	None	None	None
11	TX_SD	None. Excessive TX_SD current. Could cause internal damage to circuits.	None	None
12	BEN+	None	None	None
13	BEN-	None	None	None
14	MPD	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.
15	BIAS-	None. Increases chip power dissipation.	None.	None.
16	BIAS+	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.	TX_FAULT asserted (latching). Bias and modulation currents disabled.
17	VDD_TX	None	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	IC not powered correctly. Tx will not function.
18	LASER-	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	TX_FAULT asserted (latching). Bias and modulation currents disabled. Applies only if DC connected to Laser.	None
19	LASER+	TX_FAULT asserted (latching). Bias and modulation currents	TX_FAULT asserted (latching). Bias and modulation currents	None

PIN	NAME	SHORT TO VDD_TX	SHORT TO GND	OPEN
		disabled. Applies only if DC connected to Laser.	disabled. Applies only if DC connected to Laser.	
20	VDD_TXO	None. No disconnection of laser anode from supply if VDD_TXO not used.	TX_FAULT asserted (latching). Bias and modulation currents disabled if connected to laser anode. CAUTION: Shorting to GND will cause IC damage.	TX_FAULT asserted (latching). Bias and modulation currents disabled if connected to laser anode.
21	VDD_TX	None	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	IC not powered correctly. Tx will not function.
22	TX_FAULT	None. Excessive TX_FAULT current. Could cause internal damage to circuits.	None	None
23	RSSI_IN	None	None	None
24	VSS_RX	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	None	None
25	RXIN-	None	None	None
26	RXIN+	None	None	None
27	VSS_RX	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	None	None
28	VDD_RX	None	None. IC short circuit. IC malfunction.	None. IC malfunction.
CP	GND	IC short circuit. Tx disabled. Non-latching TX_FAULT output attempted during IC malfunction.	None	IC not grounded correctly. IC may not function correctly.

Assumes MDMAX and BIASMAX are not inhibiting.
Assumes all safety logic circuits are enabled.
BIAS+ output should always be used to drive the laser for correct eye safety operation. BIAS- is only a dummy complementary bias output and does not have internal eye safety protection.

Safety Logic Timing

The following diagrams show the NT25L91 responses to TX_FAULT conditions during start-up and normal operation in the presence of specific faults.

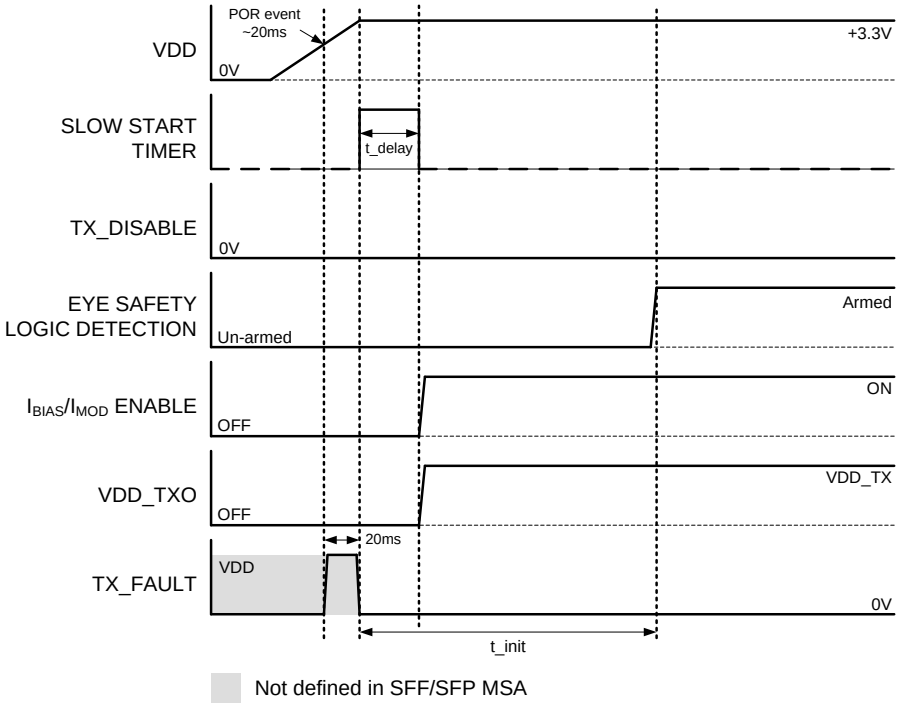


Figure 40 – Power-up Timing Sequence

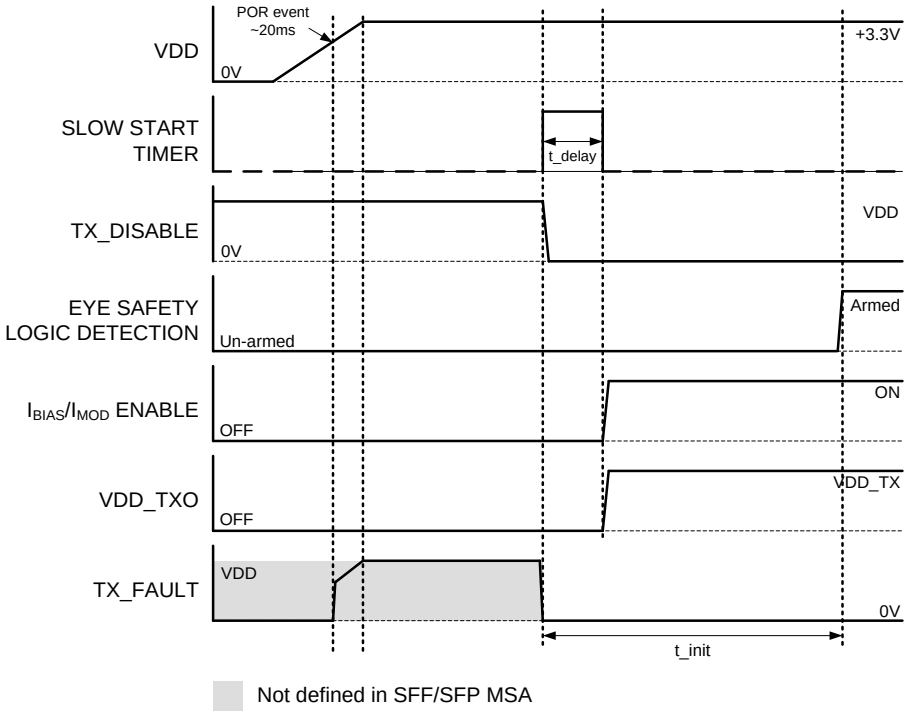


Figure 41 – TX_DISABLE Held High During Power-up Timing Sequence

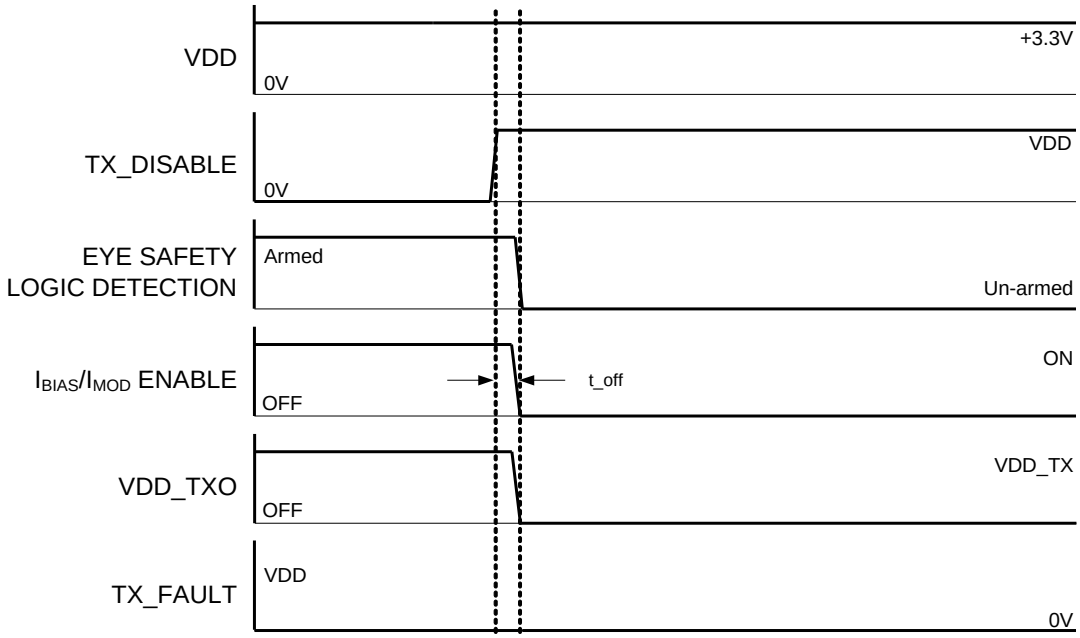


Figure 42 – TX_DISABLE Held High During Normal Operation

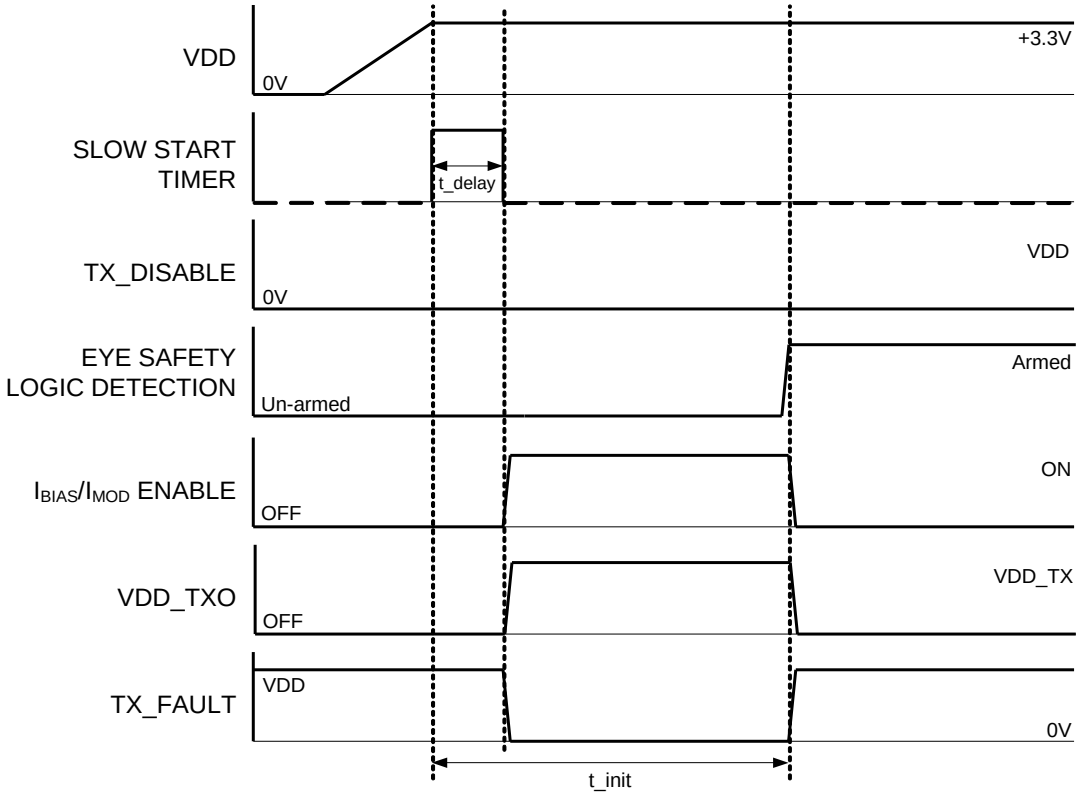


Figure 43 – APC Loop Error during Power-up Causing TX_FAULT

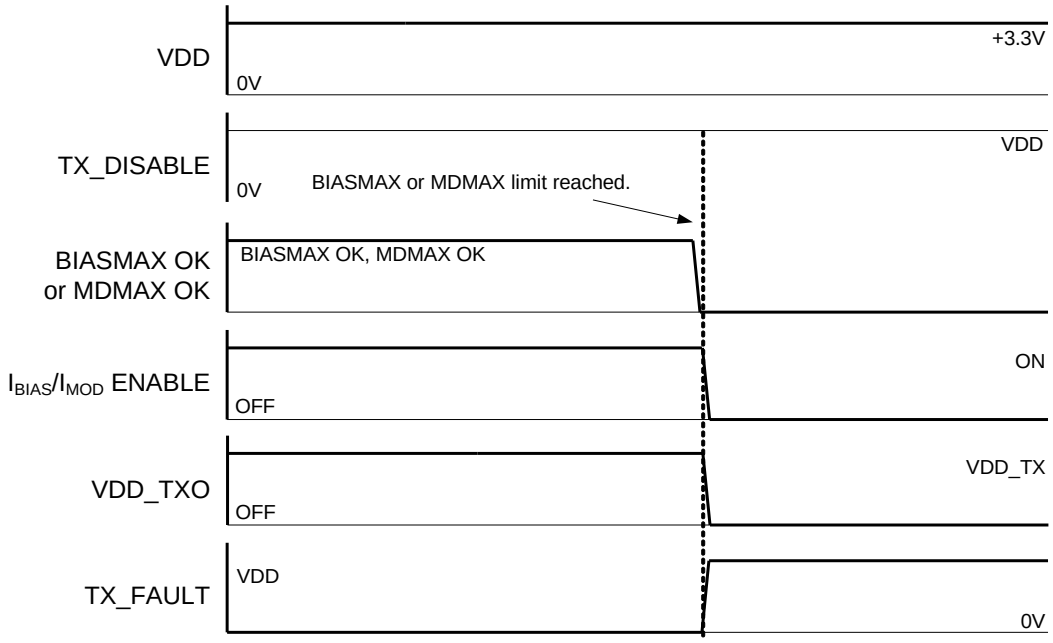


Figure 44 – BIASMAX or MPMAX current limit exceeded causing TX_FAULT

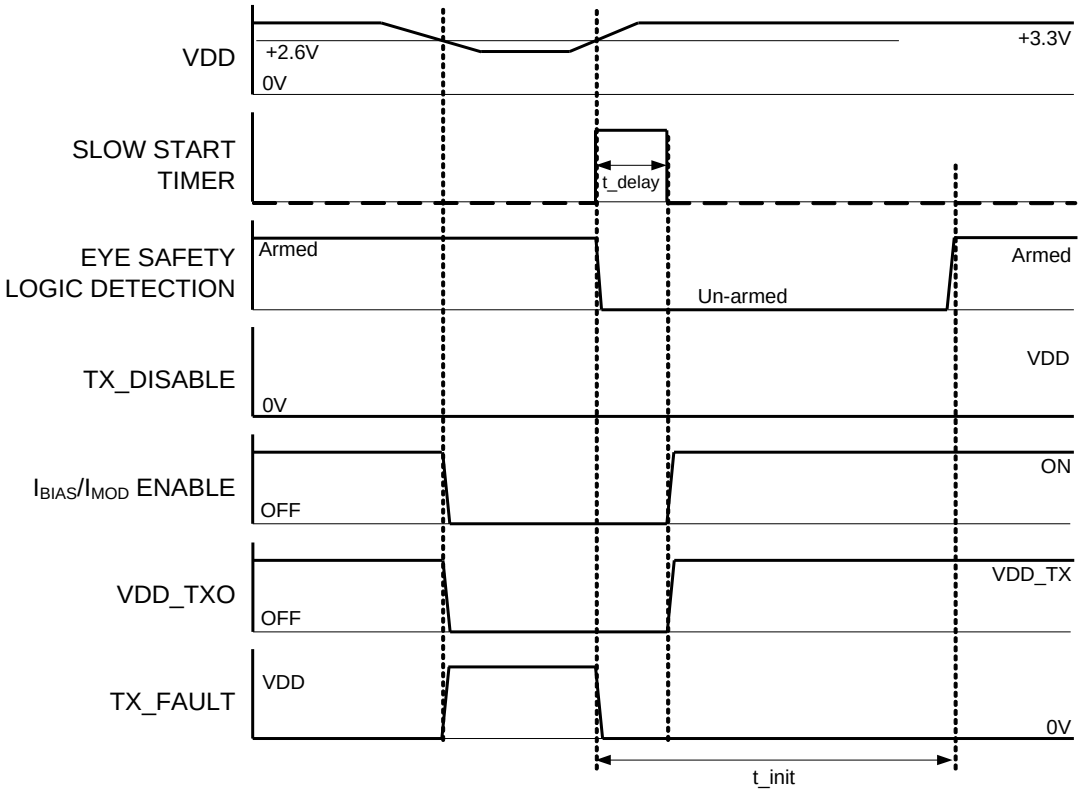


Figure 45 – VDD drops below default limit causing a non-latching TX_FAULT

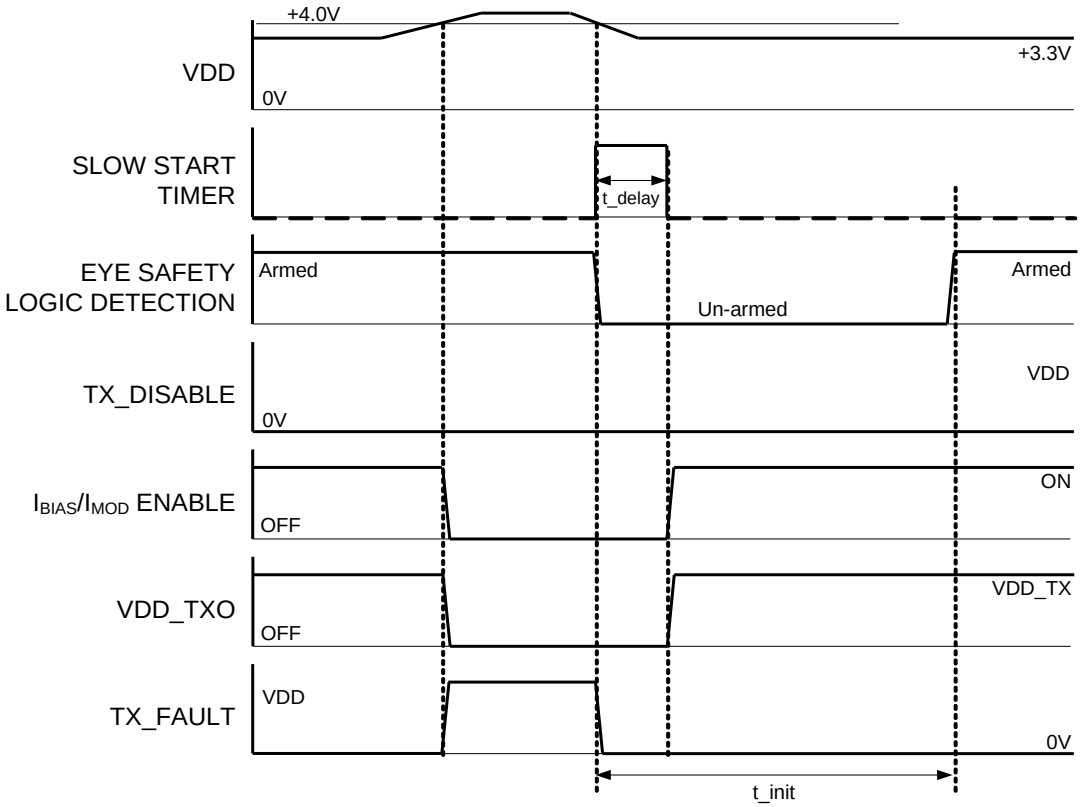


Figure 46 – VDD exceeds default limit causing a non-latching TX_FAULT

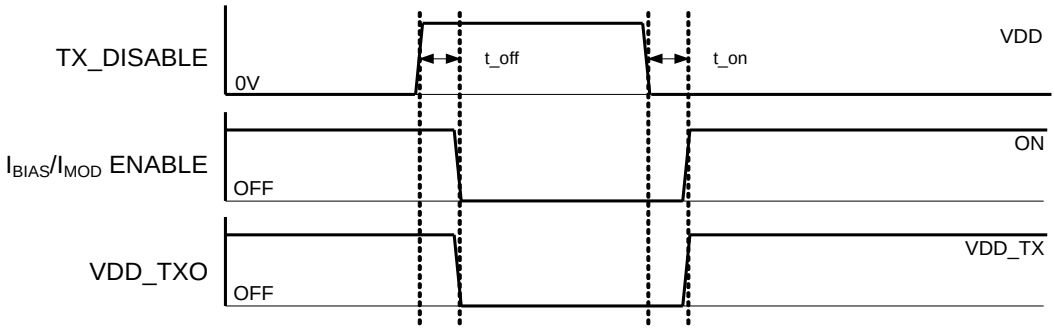


Figure 47 – TX_DISABLE asserted under normal operation

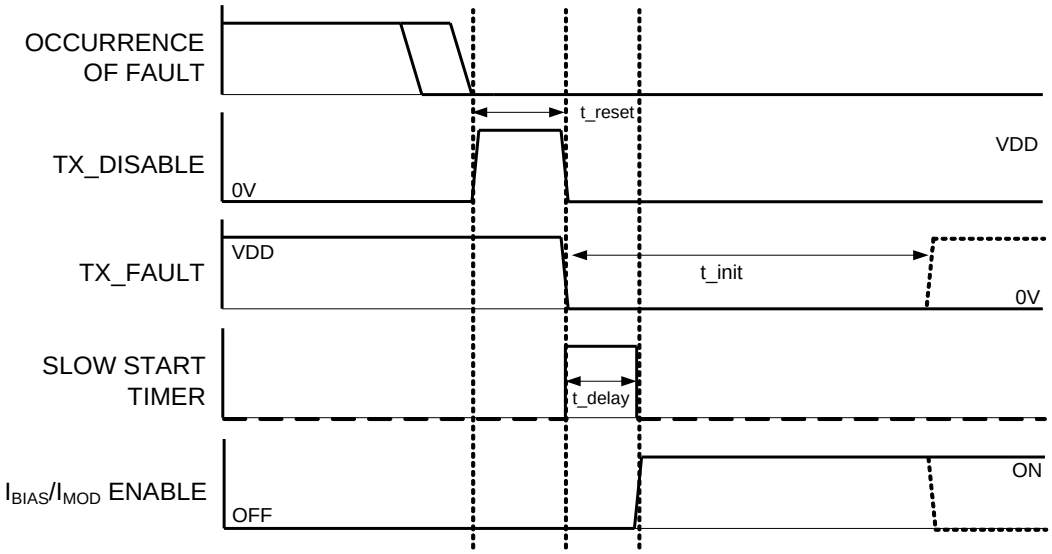


Figure 48 – Clearing of TX_FAULT by toggling of TX_DISABLE

Receiver Features

The NT25L91 features a limiting receiver with CML differential output stage. The signal path operates from 155 Mbps to 2.7 Gbps and has selectable receiver bandwidth settings to improve sensitivity in lower data rate applications. The receiver section also contains a signal detect function with polarity selectable status output indicator.

Receiver Input Stage

The NT25L91 data inputs are internally biased via 6.5k Ω resistors to a common mode voltage of 1.5V. The receiver inputs should be differentially terminated with an external 100 Ω resistor between RXIN+ and RXIN-. Typically the data inputs would be AC coupled to the preceding transimpedance amplifier (TIA) IC. The data input stage is designed to be driven differentially and is sensitive to input voltages as low as 4.0 mV peak-to-peak. The data input stage is shown below.

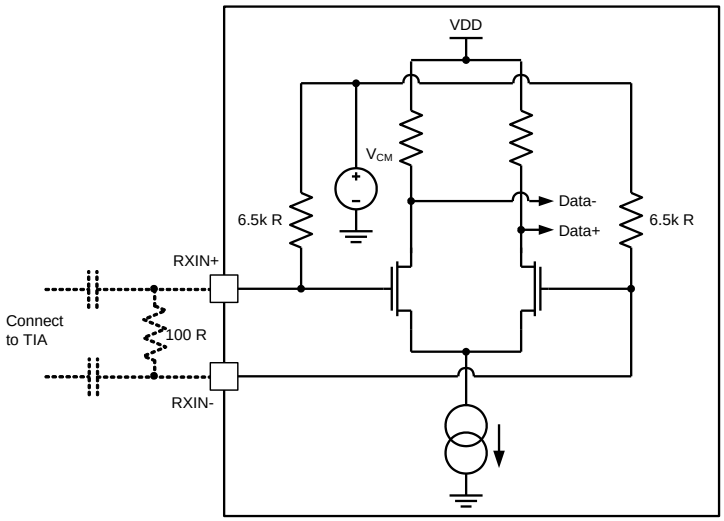


Figure 49 – Receiver Input Stage

Receiver CML Output Stage

The NT25L91 data outputs are CML compliant and may be terminated using an AC-coupled differential termination scheme. A typical AC-coupled 100 Ω termination scheme is shown below.

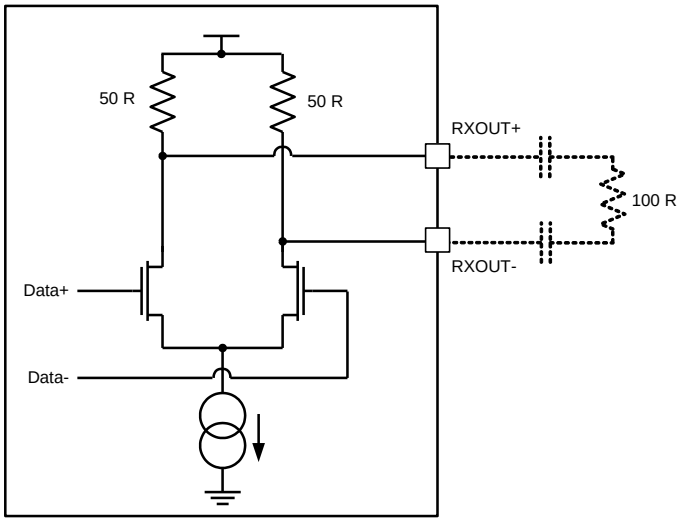


Figure 50 – Receiver Output Stage

Receiver Digital Control Functions Block Diagram

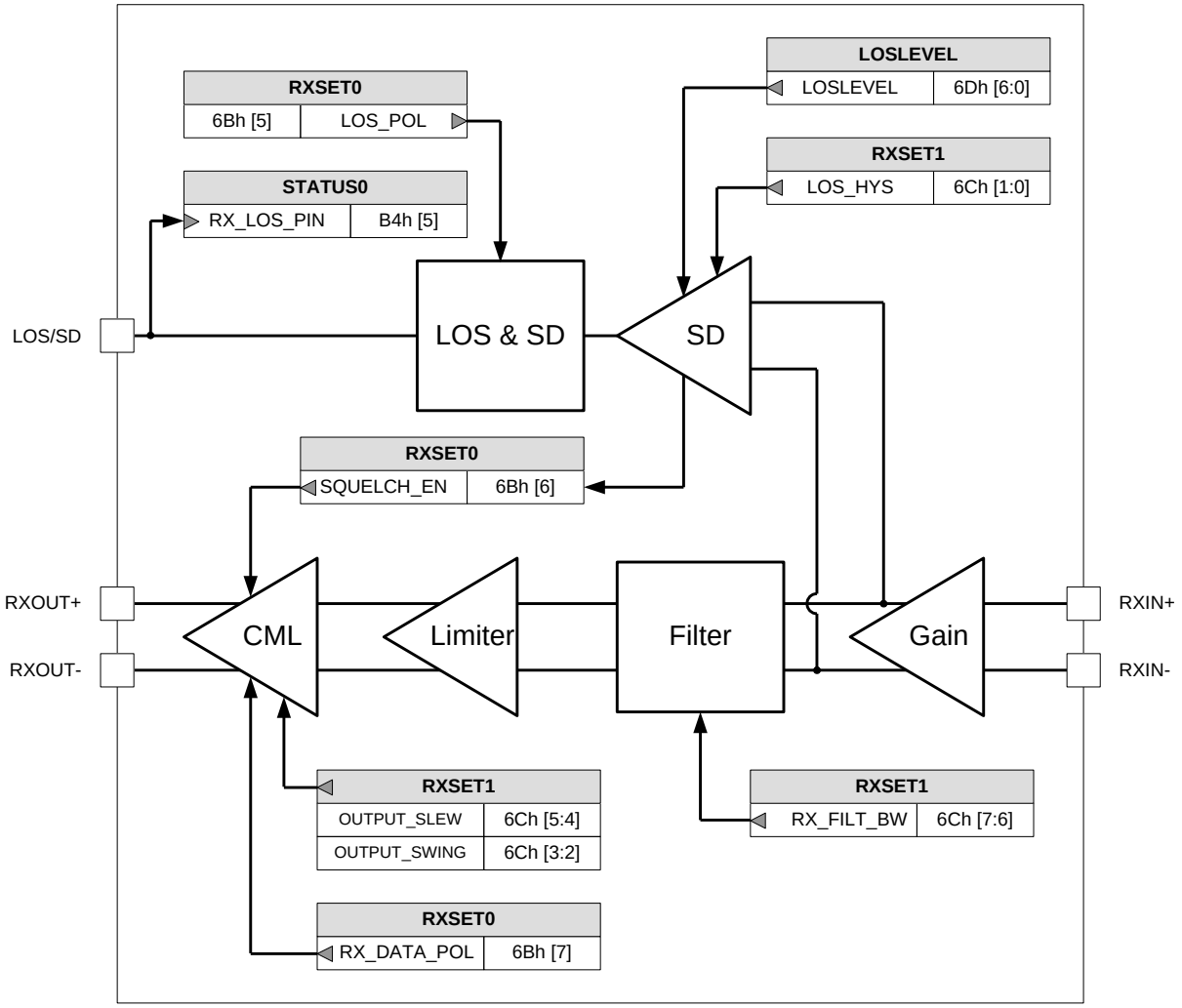


Figure 51 – NT25L91 Receiver Digital Control Functions

Receiver Data Output Polarity Invert Function

The receiver data output polarity can be inverted by setting bit 7 of RXSET0 (6Bh) to '1'.

Receiver Data Output Amplitude Control

The NT25L91 has a programmable CML output stage that allows four different amplitudes to be selected using the register RXSET1. The levels available are shown in Table 15.

Register RXSET1 6Ch <3:2>		Output Swing	Target Data Rate
OUTPUT_SWING_1	OUTPUT_SWING_0		
0	0	450 mVpp (default)	2.5 Gbps
0	1	900 mVpp	1.25 Gbps / 2.5 Gbps
1	0	1200 mVpp	622 Mbps
1	1	1600 mVpp	155 Mbps

Table 15 – NT25L91 Receiver Output Amplitude Control

Although the NT25L91 default for OUTPUT_SWING is <0:0> resulting in a 450 mVpp swing it is expected that the majority of applications will use the second setting of 900 mVpp output swing for GE-PON, GPON and SFP applications above 622 Mbps. The 1200 mVpp and 1600 mVpp output swings are not recommended for use with applications above 622 Mbps.

Receiver Data Output Slew Control

The CML output slew rate can also be adjusted to optimise the receiver data output rise and fall times for the specific application. The possible settings are shown in the table below.

Register RXSET1 6Ch <5:4>		Slew Selected	Typical 20%-80% Rise/Fall times	Target Output Amplitude
OUTPUT_SLEW_1	OUTPUT_SLEW_0			
0	0	OFF (Default)	90 ps	900 mVpp
0	1	FAST	160 ps	900 mVpp
1	0	MEDIUM	320 ps	1200 mVpp
1	1	SLOW	1280 ps	1600 mVpp

Table 16 – NT25L91 Receiver Output Slew Control

Receiver Filter Stage

The receiver signal path contains a digitally programmable bandwidth filter which limits the upper cut-off frequency to one of three settings enabling the signal path sensitivity to be optimised for the data rates shown in the table below.

Register RXSET1 6Ch <7:6>		Receiver Rate Setting
RX_FILT_BW_1	RX_FILT_BW_0	
0	0	2.5 Gbps (default)
0	1	1.25 Gbps
1	0	622 / 155 Mbps
1	1	622 / 155 Mbps

Table 17 – NT25L91 Receiver Bandwidth Settings

Setting RX_FILT_BW to either <1 :0 > or <1 :1> results in the same filter setting which can be used for 622 Mbps or 155 Mbps applications.

Optimising the Receiver Signal Path Settings

The NT25L91 provides control over the receiver signal path for output amplitude, slew rate and filter rate setting. Below is a table with recommended settings for all of these controls for specific data rates and applications.

Data Rate	Application	Rate Setting	Amplitude	Slew Rate
2.5 Gbps	GPON, SFP, SFF	2.5 Gbps	900 mVpp	OFF
1.25 Gbps	GE-PON, SFP, SFF	1.25 Gbps	900 mVpp	FAST
622 Mbps	SFP, SFF	622 / 155 Mbps	1200 mVpp	MEDIUM
155 Mbps	SFP, SFF	622 / 155 Mbps	1600 mVpp	SLOW
Multi-Rate	155M – 2.5G SFP	2.5 Gbps	900 mVpp	OFF

Table 18 – Optimised Receiver Signal Path Settings

Signal Detect/Loss of Signal Stage

The NT25L91 features a CMOS open drain signal status output that is polarity selectable as a LOS or an SD status output. A signal status function is implemented on-chip that uses a peak detector to determine the input modulation amplitude and then compares this with a tuneable reference level, set by the digital interface. If the input amplitude falls below the preset level then the status output is asserted. The assert to de-assert hysteresis can be programmed to be between 1.0 dB to 3.0 dB optically.

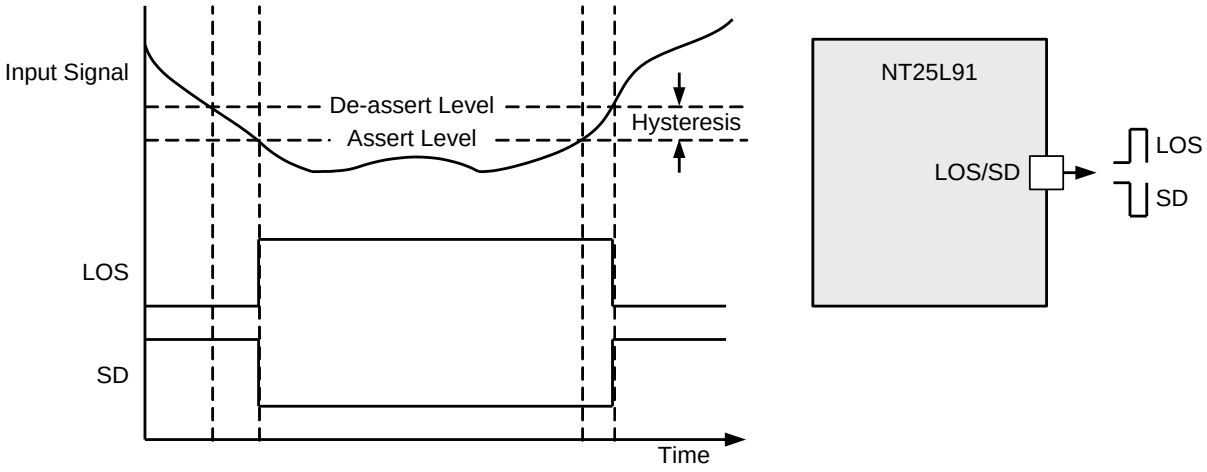


Figure 52 – Receiver Signal Detect Operation

Setting the LOS Assert Level

The LOS signal assert level is set using the register LOSLEVEL at 6Dh. This controls a 7-bit linear DAC to set the LOS assert threshold and covers the range 0 mVpp to 127 mVpp and is described by the formula below:

LOS Assert Level (mVpp) = 1 mV * LOSLEVEL <6:0>

The LOS is designed to work across the differential signal input range of 10 mVpp to 60 mVpp (see Table 6 for details). The programming range is shown graphically in Figure 53.

Setting the LOS Hysteresis

The LOS hysteresis can be set to one of four levels using register RXSET1. Details are shown in the table below. Figure 54 shows the LOS Assert and De-Assert levels graphically for all Hysteresis settings.

Register RXSET1 6Ch <1:0>		**Hysteresis (Optical)**
LOS_HYS_1	**LOS_HYS_0**	
0	0	1 dB (default)
0	1	2 dB
1	0	2.5 dB
1	1	3 dB

Table 19 – LOS_HYS Settings

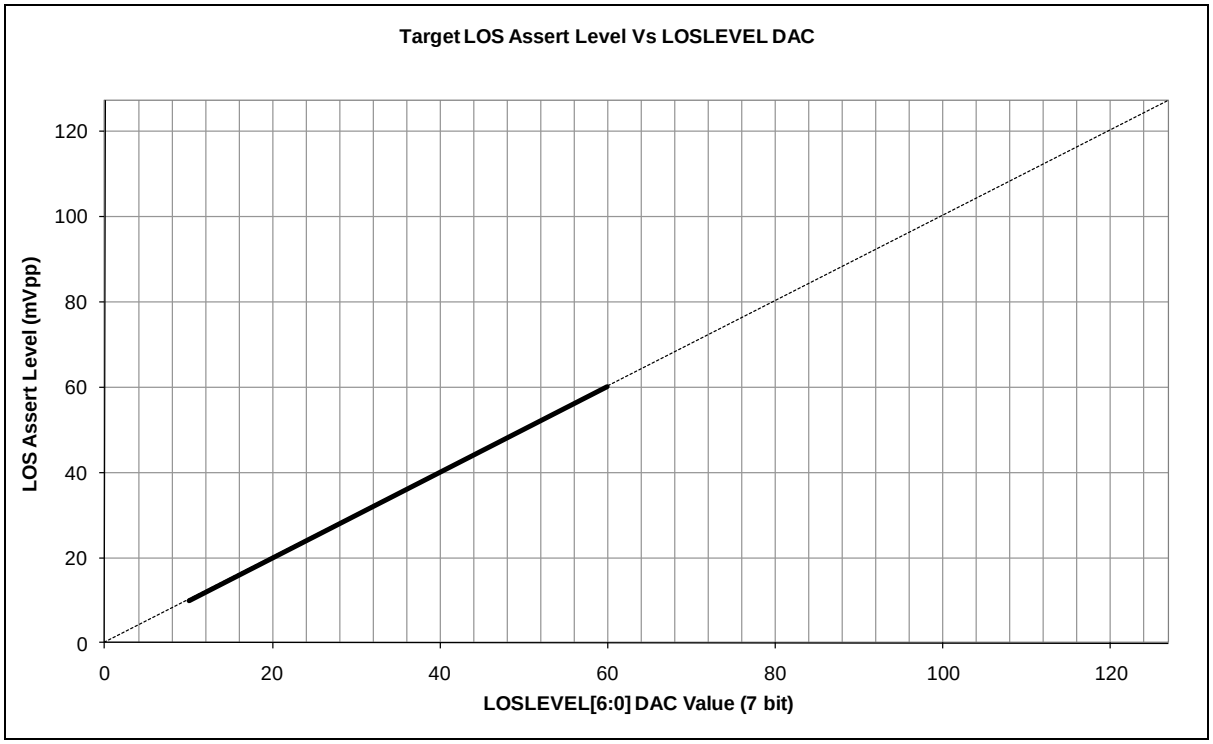


Figure 53 – NT25L91 LOS Assert Setting

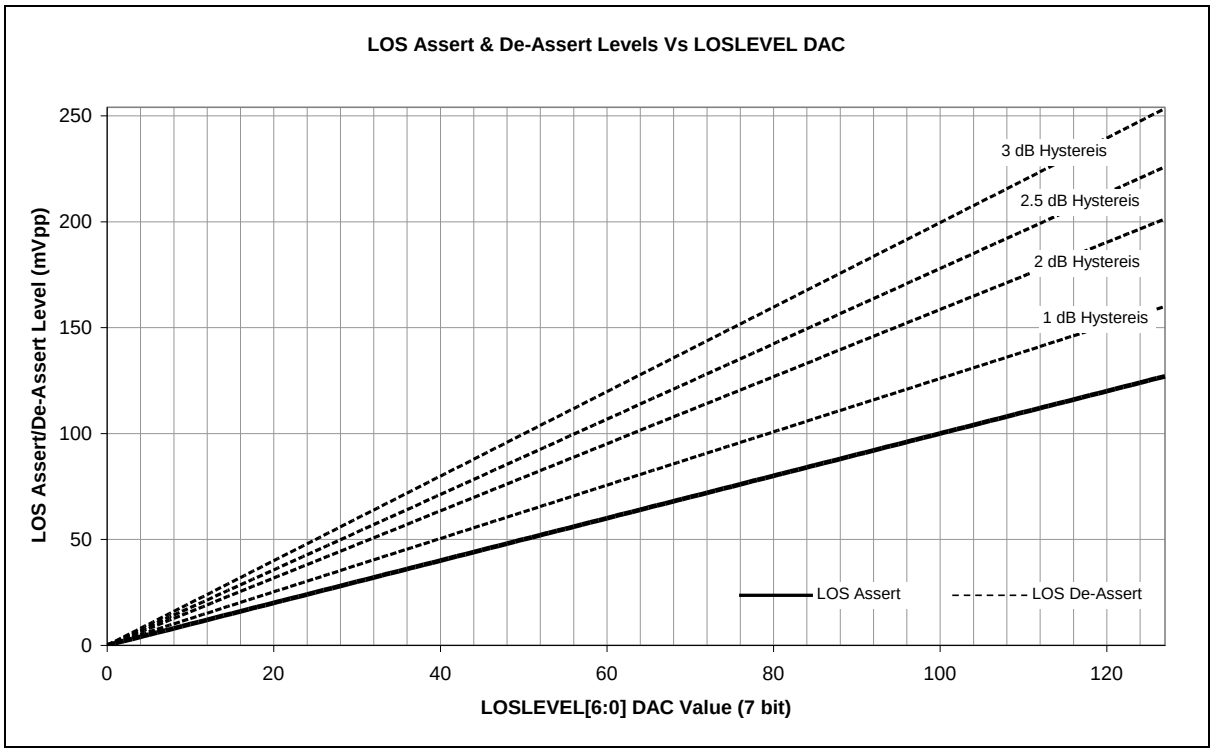


Figure 54 – NT25L91 LOS Assert & De-Assert Levels with Hysteresis

LOS/SD Output Polarity

The LOS/SD pin is an open drain status output that is typically pulled high with a 4.7k to 10k Ω resistor to VDD_RX. The polarity of this output can be changed from Loss of Signal (default) to Signal Detect by setting bit 5 of register 6Bh RXSET0.

Receiver Output Squelch Function

The receiver outputs can be squelched during a Loss of Signal condition. To enable squelching of the outputs the 'SQUELCH_EN' bit (Bit 6 of register 6Bh) should be set to '1'. The receiver outputs will be set to the mid-point of their nominal levels when squelched.

APD_DAC Output Function

The NT25L91 includes an on-chip DAC for controlling an external Avalanche Photo Diode (APD) bias circuit. The DAC is a current sink output that can be used directly as a current output control or, by means of an external resistor and current mirror, a control voltage output.
The DAC is a 8-bits wide with a step size resolution of 1 µA. The full scale output current is typically 255 µA. The APD_DAC is controlled via the I2C interface by setting the byte in register 65h.

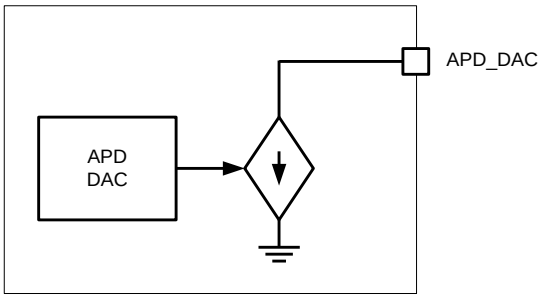


Figure 55 – APD_DAC Sink Output

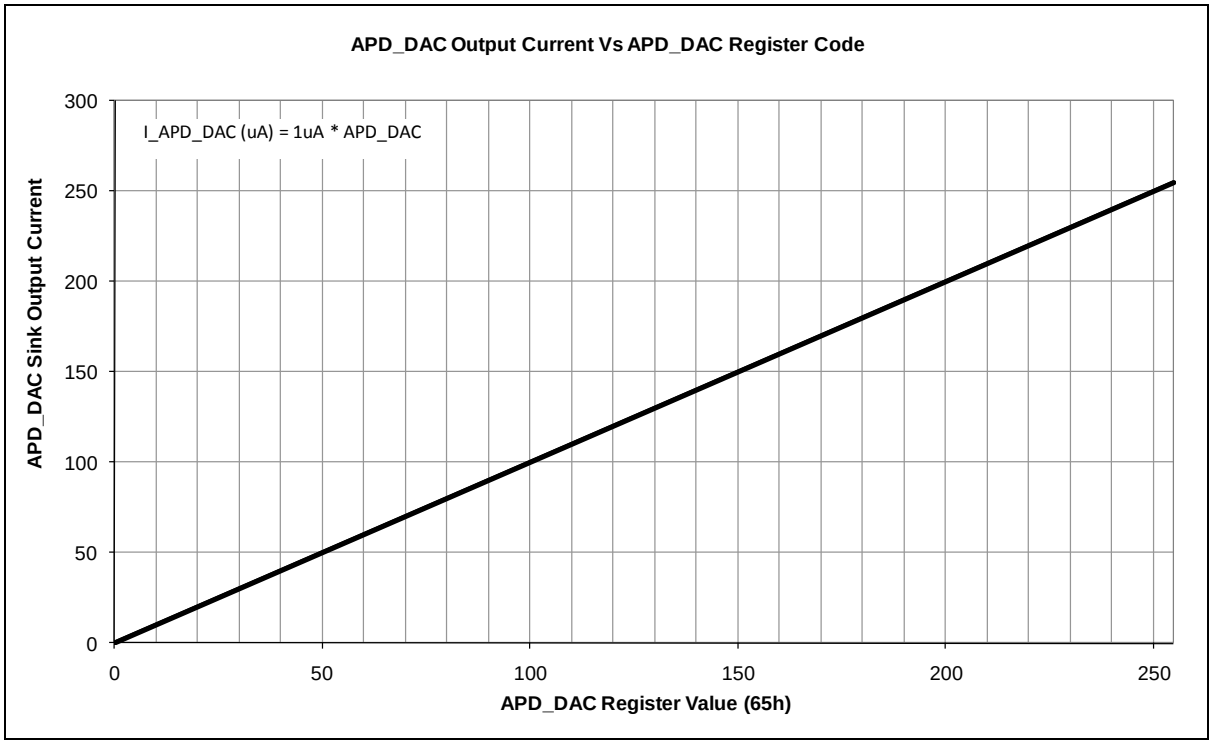


Figure 56 – APD_DAC Sink Output Current Register Control Characteristics

Digital Control & Monitoring Features

The NT25L91 is set-up, programmed and controlled via an I^2C digital interface. Registers in the NT25L91 are used to control the various analogue functions within the IC. The contents of the registers related to the IC's configuration are stored in non-volatile memory to allow the IC to function from power-up without the requirement for external memory or control from an external microcontroller. The NT2L90 registers can be found at I^2C address A8h.

Digital I^2C Interface

The I^2C interface is a slave interface responding to read and write requests from an external master interface on a host controller. The SDA and SCL interface lines are internally pulled-up to VDD with 10k Ω resistors to reduce off chip components. The interface can function at data transfer rates of up to 2 Mbps and will comfortably support the standard 100 kHz mode and 400 kHz fast mode.

An I^2C transaction is contained within a frame that is preceded by a start condition and completed by a stop condition. A start condition is defined by the host master pulling the SDA line low whilst the SCL line is high. A stop condition is defined by the host master releasing the SDA to transition low to high whilst the SCL line remains high.
The master interface has control of the bus during a framed transaction. The NT25L91 allows repeat start conditions in which the master may send multiple frames delimited by a start condition before finally sending a stop condition. This allows the master to send multiple frames without releasing control of the bus.

During a framed data transaction, data is transferred from master to slave or slave to master by clocking data on the bus. A data bit is valid during a clock low to high transition whilst the SDA state may only change when the SCL line is low. Data is arranged as 8 bits followed by an acknowledge (ACK) bit. The acknowledge bit is controlled by the recipient of the data by holding the SDA line low to acknowledge the correct receipt of a data byte. A not-acknowledged (NACK) bit can be signalled by leaving the SDA line floating during the 9th SCL clock cycle. A not-acknowledge can be used to indicate several conditions depending on the nature of the transaction and data content.

Address Decoding

After a start condition from the master indicates the beginning of a frame, the master must then send an address byte to the slave. The address byte is formatted as shown in Figure 57. The first seven bits contain the address of the target slave device with the msb first. The eighth bit indicates the type of transaction required: a '0' indicates a write (master writes to slave) and a '1' indicates a read (master reads from slave). If no slave on the bus matches the address sent, then the SDA line will be left floating and therefore the master receives a NACK back. The master must then send a stop condition. If a slave does appear on the bus with the target address then it must pull down the SDA line thus sending an acknowledge back to the master at which point communication between master and slave can proceed depending on the type of transaction requested – write or read.

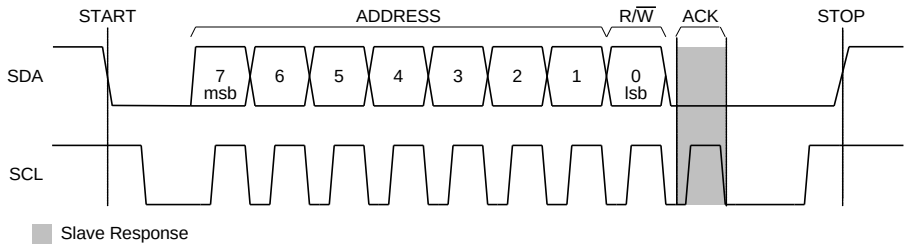


Figure 57 – I^2C Address Decoding

Write Transaction

A write transaction is shown below in Figure 58. Communication is initiated by the master driving the I^2C bus with a start condition. The master then signals the 7-bit slave address followed by a write bit, indicating that the master intends to write data to the slave. The slave then acknowledges the master by holding down the SDA line (shown in grey). The master then proceeds to write data on to the bus, 8-bits wide with MSB first, and then receives an acknowledge from the slave (again, in grey). The diagram below shows the first byte of data and acknowledge followed by a stop condition. In reality the master is likely to send several data bytes along the bus before terminating the transaction frame. A typical single register write would involve the master sending a start condition; the 7-bit slave address and write bit; the first data byte would contain the register address to be written to; the second data byte would contain the data to be written; finally a stop condition would be sent by the master.
The NT25L91 allows multiple consecutive registers to be written to by incrementing an internal register address pointer with the initial register address being set by the first data byte sent by the master. The proceeding data byte is written to this register address and any further data bytes are written to the incremental register address.

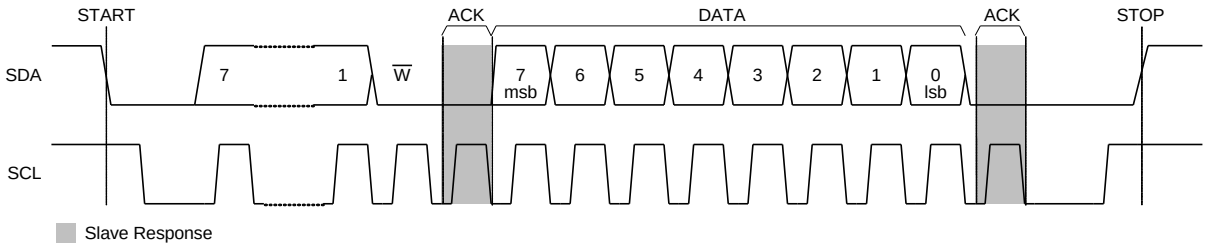


Figure 58 – I^2C Write Transaction

Read Transaction

Figure 59 below shows a read transaction. The master sends the slave address followed by a read request bit which is subsequently acknowledged by the slave (the first grey bit). The slave then responds by placing data onto the bus (shown in grey) from the current memory location held in the register address pointer. The master will then hold down the SDA line to acknowledge (shown in white) the successful receipt of the data byte. The process can continue until the master terminates the communication with a stop condition.

To read data from random register addresses the master must first send write to the slave followed by the register address to be read from and a stop condition. The master can then initiate a read frame and the slave will read out consecutive data bytes starting from the register address indicated in the previous write frame.

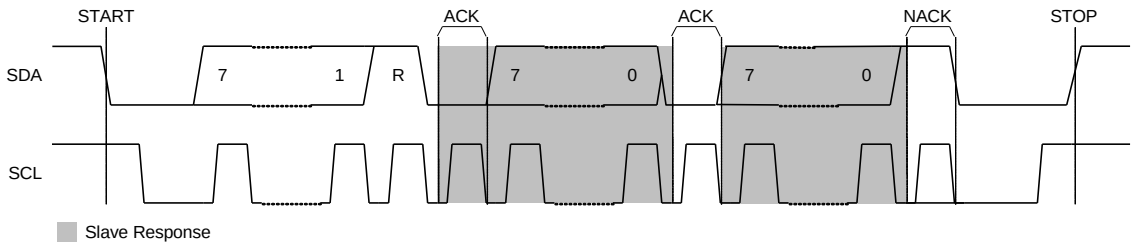


Figure 59 – I^2C Read Transaction

Memory Map

The NT25L91 contains both volatile and non-volatile memory and both types of memory can be accessed through register locations addressed via the I²C serial interface. The registers and memory organisation are shown in the figure below.

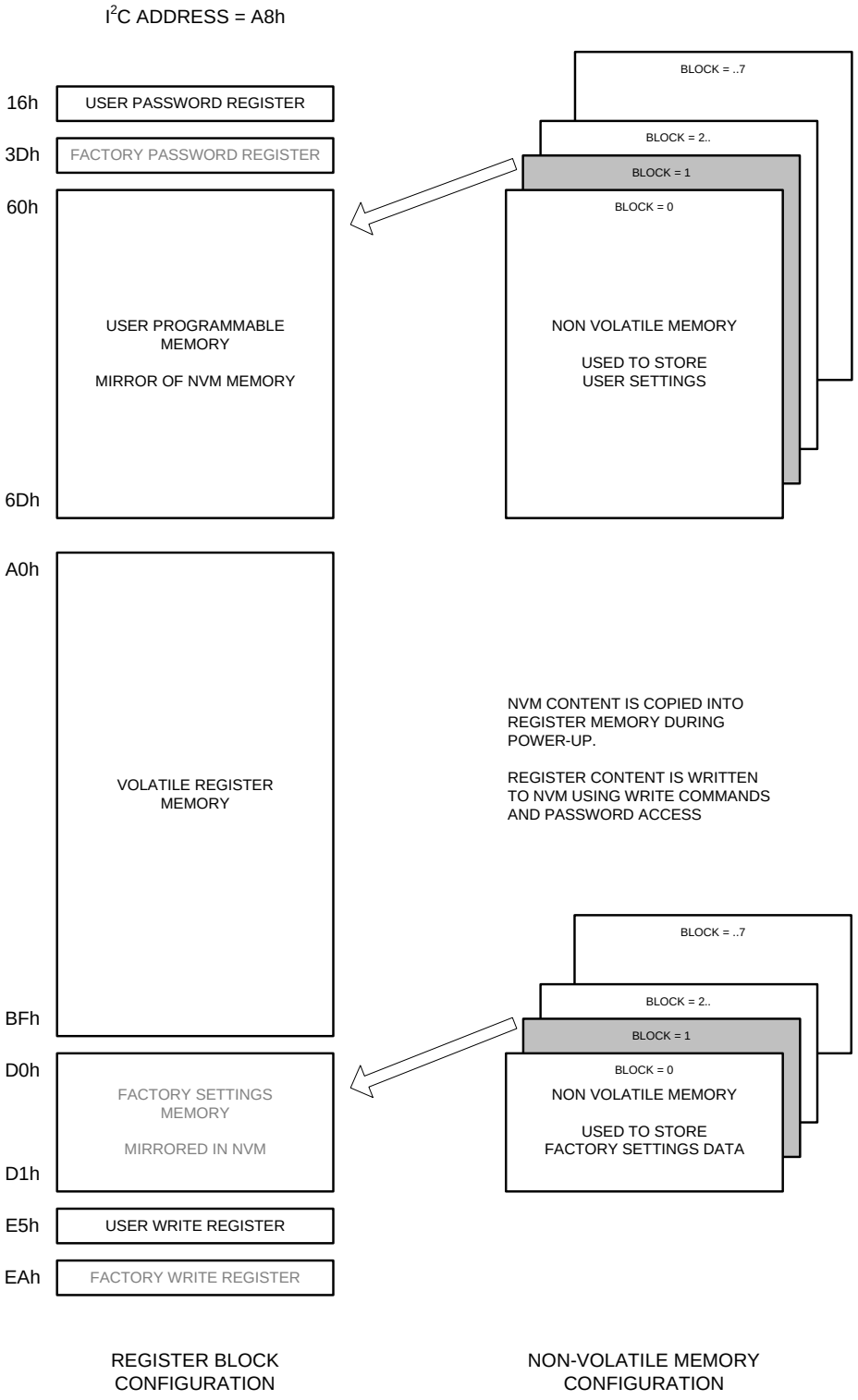


Figure 60 – NT25L91 Register & Memory Structure

Registers from 60h to 6Dh are used to control the internal functions of the NT25L91, such as the transmitter temperature compensation. The registers are volatile and can be overwritten at any time via the I^2C interface. The content of registers 60h to 6Dh can be permanently stored in non-volatile memory so that the NT25L91 can reload the register settings after power-up. This allows the user to write to the registers 60h through 6Dh and change the contents as required. When the user is satisfied the current register content is correct then the content can be copied to non-volatile memory for later recall. The non-volatile memory is organized as eight blocks of 14 bytes of one-time program (OTP) memory. Only one of the eight blocks is active at any one time. This allows the NT25L91 to be re-programmed up to eight times before the OTP memory blocks are full. A full description of how to set up the user registers and program their content to NVM is described later.

The user register space from A0h to BFh contains mainly status registers for reading. Some of the registers in this space can be written to and are used to control some special functions within the IC (such as GPON power leveling) but these registers are not backed up in NVM and so must be re-programmed on every power-up (by an external microcontroller for example).

Registers D0h and D1h contain factory settings that are also stored in NVM and recalled on power-up.

Register 16h is used in conjunction with register E5h to permanently copy the content of the user register space (60h to 6Dh) into the next available user NVM block. These registers are volatile memory.

Finally, Register 3Dh is used in conjunction with register EAh to permanently copy the content of the factory register space (D0h to D1h) into the next available factory NVM block. These registers are volatile memory. These registers are detailed here for information as they are only required during factory programming of the ICs internal factory settings.

Copying User Register area to NVM

The contents of the user register area (60h to 6Dh) can be copied into non-volatile memory by sending I^2C commands to initiate the copy. Once a copy is initiated the register contents are copied into the next available NVM memory block one bit at a time - there are eight available one-time programmable (OTP) blocks in the NT25L91 in total. The entire copy procedure should take no longer than 2.56s. During this time the NT25L91 will hold the SDA and SCL lines low to indicate the NT25L91 is busy. The I^2C copy command procedure is show in the figure below:

1. Write the User password byte to register 16h

2. Write the User program command to register E5h

3. Contents of Registers 60h to 6Dh are now internally transferred to next blank NVM memory block.

Figure 61 – NT25L91 Volatile Register Copy to User NVM

The NT25L91 will automatically select the next free NVM memory block to program. The current ‘active’ NVM memory block can be monitored by reading the content of register B5h ‘SYSTEM STATUS’ where bits <2:0> contain the current NVM block number in binary.

The supply voltage to the NT25L91 should be at least **3.3V** at the VDD_DIG pin to guarantee successful writing of the register content into NVM.

Internal Diagnostic Monitoring

The NT25L91 contains a multi-channel 9-bit auto-ranging A/D converter to digitise the following analogue monitors within the IC: supply voltage, transmitter bias current, transmitted output power. The NT25L91 also contains an on-chip temperature sensor which is also digitised using the A/D converter. In conjunction with an external RSSI monitor input, the NT25L91 can digitise the received average power. These monitor values are available in digital 16-bit format via the I^2C slave interface allowing the user to construct a complete digital diagnostic monitoring interface (DDMI) optical transceiver compliant to the SFF-8472 standard in conjunction with an external microcontroller. An external microcontroller is required to process the digitised A/D values and respond to host commands as per the SFF-8472 standard requirements.

In addition to the five monitored functions for SFF-8472, the NT25L91 also provides a digitised monitor of the transmitter modulation current.

Mapping of the ADCs into Register Memory

The NT25L91 digital diagnostic monitors are mapped into 16-bit registers from A0h through to AFh. These are described in Table 20 below.

Register Address	Register Description	Content
A0h	TEMP MSB	Temperature monitor 16-bit register
A1h	TEMP LSB	
A2h	TX POWER MSB	Tx transmitted power monitor 16-bit register
A3h	TX POWER LSB	
A4h	TX BIAS MSB	Tx bias current monitor 16-bit register
A5h	TX BIAS LSB	
A6h	TX MOD MSB	Tx modulation current monitor 16-bit register
A7h	TX MOD LSB	
A8h	RX POWER MSB	Rx RSSI input power 16-bit register
A9h	RX POWER LSB	
AAh	VDD_TX MSB	Tx Supply Voltage monitor 16-bit register
ABh	VDD_TX LSB	
ACh	VDD_RX MSB	Rx Supply Voltage monitor 16-bit register
ADh	VDD_RX LSB	
AEh	VDD_DIG MSB	Digital Supply Voltage monitor 16-bit register
AFh	VDD_DIG LSB	

Table 20 – ADC Monitor Register Locations

A description of each of the six monitors is now provided detailing how to decode each of the 16-bit values.

Temperature Monitor

The temperature monitor can theoretically report temperature from -53.7 °C through to 133.7 °C although this is well beyond the absolute maximum operating range of the NT25L91 IC.

The 9-bit ADC value is mapped to the upper 9 bits of the TEMP register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of (133.7 °C + 53.7 °C) / 65536 = 0.00286 °C/bit with a reporting resolution of ± 0.37 °C.

Lower Range	Upper Range	TEMP MSB (A0h)								TEMP LSB (A1h)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-53.7 °C	133.7 °C	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 21 – Temperature Monitor mapping to TEMP Register

To calculate the temperature from the TEMP register value use the formula below:

Temperature (°C) = TEMP * (187.4 °C / 65536) – 53.7 °C

Tx Power Monitor

The NT25L91 transmitted power monitor reports the mean transmitter output power as follows: (1) In non-burst operation the monitor is directly proportional to the mean transmitted output power derived from the monitor feedback current which is constantly maintained by the automatic power control loop. (2) In burst mode operation the monitor is derived from the averaged monitor photocurrent during successive burst-on periods. During a burst-off period, the transmitted power is assumed to be zero and therefore excluded from the averaging function. A voltage proportional to the monitor current is generated internally within the IC and sampled with a capacitor C_{SAMPLE} only when BEN is high. For non-burst operation, BEN is always tied high.

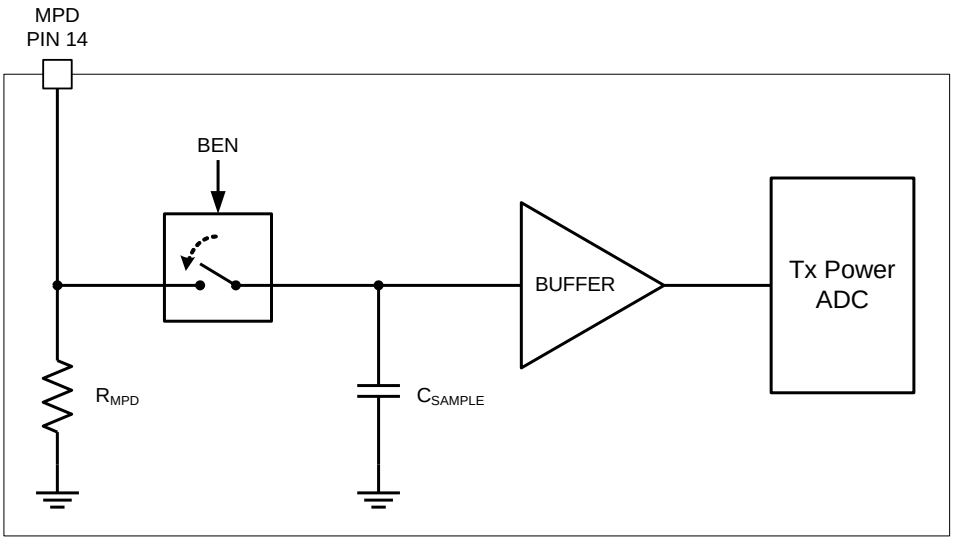


Figure 62 – NT25L91 Burst Tx Power Monitor Functional Diagram

The Tx power monitor can report the monitor photodiode current from 0.0 µA through to 1800.0 µA.

The 9-bit ADC value is auto-ranged and mapped to three different areas in the 16-bit TX POWER register depending on the target monitor photodiode current value. The upper three bits of the TX POWER register are always zero. This gives an equivalent LSB value of 112.5 µA / 512 = 0.22 µA/bit.

Lower Range	Upper Range	TX POWER MSB (A2h)								TX POWER LSB (A3h)							
0000h	1FF0h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 µA	112.5 µA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
112.5 µA	450.0 µA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
450.0 µA	1800.0 µA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0

Table 22 – Tx Power Monitor mapping to TX POWER Register

The TX POWER register therefore should be interpreted as follows:

Monitor Photodiode Diode Current (µA) = TX POWER * (112.5 µA / 512)

The Tx power monitor resolution depends on the actual photodiode current. For currents less than 112.5 µA the resolution will be ± 0.22 µA. For currents between 112.5 µA and 450 µA the resolution will be ± 0.88 µA. For currents between 450 µA and 1800 µA the resolution will be ± 3.52 µA.

Tx Bias Current Monitor

The Tx bias current monitor can report the transmitter bias current from 0.0 mA through to 204.8 mA although the NT25L91 is designed to provide up to 100 mA of bias current.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit TX BIAS register depending on the actual bias current value. Therefore the TX BIAS register utilises all 16-bits of the register. This gives an equivalent LSB value of 1.6 mA / 512 = 3.125 µA/bit.

Lower Range	Upper Range	TX BIAS MSB (A4h)								TX BIAS LSB (A5h)							
0000h	FFFFh	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 mA	1.6 mA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
1.6 mA	6.4 mA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
6.4 mA	25.6 mA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
25.6 mA	102.4 mA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
102.4 mA	204.8 mA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 23 – Tx Bias Current mapping to TX BIAS Register

The TX BIAS register therefore should be interpreted as follows:

Tx Bias Current (mA) = TX BIAS * (1.6 mA / 512)

The Tx bias current monitor resolution depends on the actual bias current. For currents less than 1.6 mA the resolution will be ± 3.125 µA. For currents between 1.6 mA and 6.4 mA the resolution will be ± 12.5 µA. For currents between 6.4 mA and 25.6 mA the resolution will be ± 50 µA. For currents between 25.6 mA and 102.4 mA the resolution will be ± 0.2 mA. For currents between 102.4 mA and 204.8 mA the resolution will be ± 0.4 mA. In practice the TX BIAS value should never result in a value equivalent to 100 mA or greater. Therefore bit 15 of TX BIAS register will likely always remain zero.

Tx Modulation Current Monitor

The Tx modulation current monitor can report the transmitter modulation current from 0.0 mA through to 204.8 mA although the NT25L91 is designed to provide up to 90 mA of modulation current.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit TX MOD register depending on the actual modulation current value. Therefore the TX MOD register utilises all 16-bits of the register. This gives an equivalent LSB value of 1.6 mA / 512 = 3.125 µA/bit.

Lower Range	Upper Range	TX MOD MSB (A6h)								TX MOD LSB (A7h)							
0000h	FFFFh	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 mA	1.6 mA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
1.6 mA	6.4 mA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
6.4 mA	25.6 mA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
25.6 mA	102.4 mA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
102.4 mA	204.8 mA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 24 – Tx Modulation Current mapping to TX MOD Register

The TX MOD register therefore should be interpreted as follows:

Tx Modulation Current (mA) = TX MOD * (1.6 mA / 512)

The Tx modulation current monitor resolution depends on the actual modulation current. For currents less than 1.6 mA the resolution will be ± 3.125 µA. For currents between 1.6 mA and 6.4 mA the resolution will be ± 12.5 µA. For currents between 6.4 mA and 25.6 mA the resolution will be ± 50 µA. For currents between 25.6 mA and 102.4 mA the resolution will be ± 0.2 mA. For currents between 102.4 mA and 204.8 mA the resolution will be ± 0.4 mA. In practice the TX MOD value should never result in a value equivalent to 90 mA or greater. Therefore bit 15 of TX MOD register will likely always remain zero.

Rx Power Monitor

The NT25L91 features a receiver signal strength indicator (RSSI) input for monitoring the current from an external RSSI output from a trans-impedance amplifier (TIA) such as the Semtech NT24L50.
The RSSI input monitor can be configured to accept both Sink (default) or Source output monitors from the preceding TIA. The polarity of the RSSI input is configured to Source mode by setting bit 4 of register 6Bh [RXSET0] to '1'. This activates an internal current mirror which changes the input polarity. The maximum current handing capability of the RSSI pin is 8 mA.

The output from the internal RSSI current mirror is fed into an auto-ranging analog-to-digital converter that can digitise TIA monitor currents from 90 nA up to 2 mA – equivalent to an average optical input power range of -40 dBm to +3 dBm (assuming 0.9 A/W responsivity). The digitised RSSI monitor input is stored in registers A8h and A9h as the RX POWER MSB and RX POWER LSB respectively, forming a 16-bit raw ADC value for SFF-8472 processing and reporting using an external microcontroller.

The auto-ranger operates continuously and before every ADC sample cycle. This guarantees that the ADC digitised output is monotonic with RSSI input monitor current.

A 10nF capacitor should be connected between the RSSI pin input and ground to reduce noise at the RSSI monitor node as shown in Figure 63.

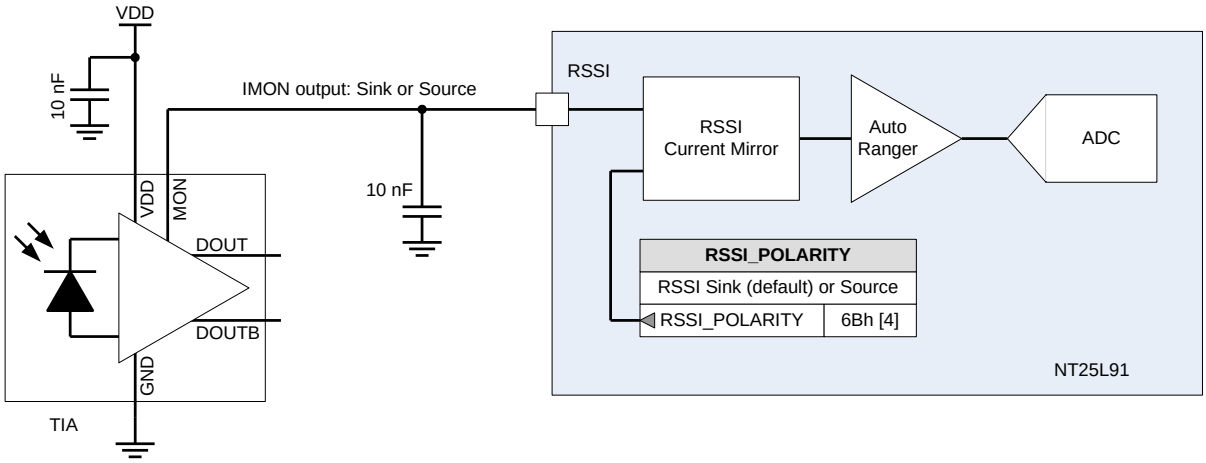


Figure 63 – NT25L91 RSSI Monitor A/D Input

The Rx Power monitor can report the RSSI current from 0.0 µA through to 2048 µA.

The 9-bit ADC value is auto-ranged and mapped to five different areas in the 16-bit RX POWER register depending on the actual RSSI current value. Therefore the RX POWER register utilises all 16-bits of the register. This gives an equivalent LSB value of 16 µA / 512 = 0.03125 µA/bit.

Lower Range	Upper Range	RX POWER MSB (A8h)								RX POWER LSB (A9h)							
0000h	FFFFh	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 µA	16 µA	0	0	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0
16 µA	64 µA	0	0	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0
64 µA	256 µA	0	0	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0
256 µA	1024 µA	0	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0
1024 µA	2048 µA	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 25 – Rx Power mapping to RX POWER Register

The RX POWER register therefore should be interpreted as follows:

Rx Power [*RSSI*] Current (mA) = RX POWER * (16 µA / 512)

The Rx Power current monitor resolution depends on the actual RSSI current. For currents less than 16 µA the resolution will be ± 31.25 nA. For currents between 16 µA and 64 µA the resolution will be ± 125 nA. For currents between 64 µA and 256 µA the resolution will be ± 500 nA. For currents between 256 µA and 1024 µA the resolution will be ± 2 µA. For currents between 1024 µA and 2048 µA the resolution will be ± 4 µA.

Tx Supply Voltage Monitor

The Tx Supply Voltage monitor can report the supply voltage from 2.5 V through to 4 V.

The 9-bit ADC value is mapped to the upper 9 bits of the VDD_TX register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 4V / 65536 = 61 µV/bit with a reporting resolution of ± 7.81 mV.

Lower Range	Upper Range	VDD_TX MSB (AAh)	VDD_TX LSB (ABh)

0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	4.0 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 26 – Tx Supply Voltage mapping to VDD_TX Register

To calculate the Tx supply voltage from the VDD_TX register value use the formula below:

Tx Supply Voltage (V) = VDD_TX * (4 V / 65536)

Rx Supply Voltage Monitor

The Rx Supply Voltage monitor can report the supply voltage from 2.5 V through to 4 V.

The 9-bit ADC value is mapped to the upper 9 bits of the VDD_RX register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 4V / 65536 = 61 µV/bit with a reporting resolution of ± 7.81 mV.

Lower Range	Upper Range	VDD_RX MSB (ACh)								VDD_RX LSB (ADh)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	4.0 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 27 – Rx Supply Voltage mapping to VDD_RX Register

To calculate the Rx supply voltage from the VDD_RX register value use the formula below:

Rx Supply Voltage (V) = VDD_RX * (4 V / 65536)

Digital Supply Voltage Monitor

The Digital Supply Voltage monitor can report the supply voltage from 2.5 V through to 4 V although in practice if the digital supply voltage goes below 3.0 V or above 3.6 V then it is outside of the recommended operating range of the NT25L91 IC and the monitor readings will not be reliable.

The 9-bit ADC value is mapped to the upper 9 bits of the VDD_DIG register with the lower 7 bits always being set to zero. This gives an equivalent LSB value of 4V / 65536 = 61 µV/bit with a reporting resolution of ± 7.81 mV.

Lower Range	Upper Range	VDD_DIG MSB (AEh)								VDD_DIG LSB (AFh)							
0000h	FF80h	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0.0 V	4.0 V	d8	d7	d6	d5	d4	d3	d2	d1	d0	0	0	0	0	0	0	0

Table 28 – Digital Supply Voltage mapping to VDD_DIG Register

To calculate the Digital supply voltage from the VDD_DIG register value use the formula below:

Digital Supply Voltage (V) = VDD_DIG * (4 V / 65536)

Register Map & Functional Description

The NT25L91 registers are located at I^2C address A8h.

Non-volatile memory password registers

16h	USER NVM PASS			This register must be programmed with a pre-defined password to enable programming of the on-chip user NVM. Write '64h' to enable user NVM programming.
Byte	Name	Type	PoR	
	USER_NVM_PASS	R/W	00h	

3Dh	FACTORY NVM PASS			This register must be programmed with a pre-defined password to enable programming of the on-chip factory settings NVM. Factory use only.
Byte	Name	Type	PoR	
	FACT_NVM_PASS	R/W	00h	

Non-volatile memory User Registers

60h	TXSET0			Register for setting general transmitter parameters.
Bit	Name	Type	PoR	
7	TX_CROSS_3	R/W	0	Sets Tx output crossing point adjust. 16 settable values. Set to 07h (0111 binary) for normal operation.
6	TX_CROSS_2	R/W	0	
5	TX_CROSS_1	R/W	0	
4	TX_CROSS_0	R/W	0	
3	LOOP_START	R/W	0	Set to '1' to apply a slow APC loop start. Value determined by APC_CLOCK control.
2	TX_DATA_POL	R/W	0	Set to '1' to invert the Tx data polarity.
1	BURST_POL	R/W	0	Set to '1' to invert the burst control polarity input.
0	TX_DISABLE	R/W	0	Set to '1' to disable the transmitter outputs

61h	TXSET1			Register for setting general transmitter parameters.
Bit	Name	Type	PoR	
7	FAULT_INHIBIT	R/W	0	Set to '1' to inhibit on-chip eye safety circuitry.
6	LATCH_INHIBIT	R/W	0	Set to '1' to inhibit latching of TX_FAULTs.
5	SHUTDOWN_INHIBIT	R/W	0	Set to '1' to inhibit shutdown of transmitter currents during a TX_FAULT.
4	VDD_FAULT	R/W	0	Set to '1' to inhibit over or under voltage conditions generating a TX_FAULT.
3	TX_SD_POL	R/W	0	Set to '1' to invert the TX_SD output polarity.
2	BEN_ON	R/W	0	Set to '1' to permanently force continuous non-burst operation. Allows Tx to be set-up during module manufacture without biasing burst inputs.
1	POWER_SAVE	R/W	0	Saves power by turning off modulation and bias currents completely during Tx BEN de-assert periods.
0	WATCHDOG_EN	R/W	0	Set to '1' to enable the watch dog counter function for use with external MCUs.

62h	IMODSET			Temperature independent modulation current. Sets the constant amount of modulation current applied to the laser over temperature.
Byte	Name	Type	PoR	
	IMODSET	R/W	00h	

63h	TCSTART			Sets the start current at which the temperature dependent modulation current is applied to the laser.
Byte	Name	Type	PoR	
	TCSTART	R/W	00h	

64h	TSLOPE			Controls the gradient of the temperature dependent modulation current added at the TCSTART point. If TSLOPE is set to zero, then no temperature dependent modulation current is added.
Byte	Name	Type	PoR	
	TSLOPE	R/W	00h	

65h	APD_DAC			APD_DAC control register. Used to set the DAC sink output current.
Byte	Name	Type	PoR	
	APD_DAC	R/W	00h	

66h	APCSET			Sets the Automatic Power Control loop target level. Represents a digitized amount of target monitor photodiode current.
Byte	Name	Type	PoR	
	APCSET	R/W	00h	

67h	BIASINIT			Sets the initial target bias current value to enable extremely fast burst start-up. Set this value to the typical or minimum bias current value required during normal operation.
Byte	Name	Type	PoR	
	BIASINIT	R/W	00h	

68h	APCCTRL0			Register for applying APC settings.
Bit	Name	Type	PoR	
7	COUNT_INC_1	R/W	0	Sets the APC loop digital control counter step size value for binary searching.
6	COUNT_INC_0	R/W	0	
5	APCSTART_DIS	R/W	0	Set to ‘1’ to inhibit the APC fast start algorithm
4	DIGAVG_SET_1	R/W	0	Sets the amount of digital averaging applied to the digital APC loop.
3	DIGAVG_SET_0	R/W	0	
2	DIGAVG_EN	R/W	0	Set to ‘1’ to enable APC loop digital averaging.
1	APC_OPNLP	R/W	0	Set to ‘1’ to disable the APC loop and program the bias DAC directly.
0	RESERVED	R/W	X	Reserved bit used for NVM block control.

69h	MDMAX			Sets maximum value of monitor photodiode feedback current allowed.
Bit	Name	Type	PoR	
7	MD_MAX_5	R/W	0	Sets the maximum allowed monitor feedback diode current. 32 uA to 2016 uA settable range (63 x 32 uA steps). If the set value is exceeded, then a TX_FAULT condition occurs. Setting all bits (7:2) to ‘1’ disables the MDMAX limit function and inhibits the TX_FAULT response for currents greater than 2016 uA.
6	MD_MAX_4	R/W	0	
5	MD_MAX_3	R/W	0	
4	MD_MAX_2	R/W	0	
3	MD_MAX_1	R/W	0	
2	MD_MAX_0	R/W	0	
1	APC_CLOCK_1	R/W	0	Sets the sampling rate of the APC loop. 6.5 MHz is the default clock sampling rate.
0	APC_CLOCK_0	R/W	0	

6Ah	BIASMAX			Sets maximum value of bias current allowed. Sets the maximum allowed bias current in using a pseudo logarithmic DAC with a maximum allowed bias current of 102 mA. If the value is exceeded, then a TX_FAULT condition occurs. Programming FFh will disable the BIASMAX limit function and inhibits the TX_FAULT response for currents greater than 102 mA.
Byte	Name	Type	PoR	
	BIASMAX	R/W	00h	

6Bh	RXSET0			Receiver control register 0
Bit	Name	Type	PoR	
7	RX_DATA_POL	R/W	0	Set to '1' to invert the receiver output polarity
6	SQUELCH_EN	R/W	0	Set to '1' to enable squelching of the receiver data outputs under a LOS condition.
5	LOS_POL	R/W	0	Set to '1' to invert the output polarity of LOS and provide a Signal Detect (SD) status output.
4	RSSI_POLARITY	R/W	0	Set to '1' to change the RSSI input polarity from Sink (default) to Source.
3	TX_MOD_STEER	R/W	0	Set to '1' to invert the modulation current steering during a BEN de-assert. This allows the user flexibility in choosing either the LASER+ or LASER- to drive the laser cathode.
2	TX_MOD_SQUELCH	R/W	0	Set to '1' to squelch the transmitter modulation currents in the absence of input data at TXIN.
1	TEMP_DIS	R/W	0	Set to '1' to disable the on-chip temperature sensor.
0	ADC_DIS	R/W	0	Set to '1' to disable the internal ADC operation.

6Ch	RXSET1			Receiver control register 1
Bit	Name	Type	PoR	
7	RX_FILT_BW_1	R/W	0	Sets receiver bandwidth: 00 = 2.5 Gbps, 01 = 1.25 Gbps, 10 & 11 = 622/155 Mbps.
6	RX_FILT_BW_0	R/W	0	
5	OUTPUT_SLEW_1	R/W	0	Sets the receiver CML slew rate: 00 = OFF, 01 = FAST, 10 = MEDIUM, 11 = SLOW.
4	OUTPUT_SLEW_0	R/W	0	
3	OUTPUT_SWING_1	R/W	0	Controls CML output swing amplitude: 00 = 450mVpp, 01 = 900mVpp, 10 = 1200mVpp, 11 = 1600mVpp.
2	OUTPUT_SWING_0	R/W	0	
1	LOS_HYS_1	R/W	0	Controls LOS hysteresis (Optical): 00 = 1dB, 01 = 2dB, 10 = 2.5dB, 11 = 3dB.
0	LOS_HYS_0	R/W	0	

6Dh	LOSLEVEL			Sets LOS Assert level. 7-bit value
Bit	Name	Type	PoR	
7	LOS_SLOPE_COMP	R/W	0	Set to '1' to apply a 2dB temperature dependent slope.
6:0	LOSLEVEL	R/W	0	Sets LOS Assert level: 0 mVpp to 127 mVpp.

General User Registers (Volatile)

A0h	TEMP MSB			Holds MSB of digitized temperature sensor from ADC. 8-bit value.
Byte	Name	Type	PoR	
	TEMPMSB	R	N/A	

A1h	TEMP LSB			Holds LSB of digitized temperature sensor from ADC. 8-bit value.
Byte	Name	Type	PoR	
	TEMPLSB	R	N/A	

A2h	TX POWER MSB			Holds MSB of digitized Tx Power from monitor PD ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXPOWERMSB	R	N/A	

A3h	TX POWER LSB			Holds LSB of digitized Tx Power from monitor PD ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXPOWERLSB	R	N/A	

A4h	TX BIAS MSB			Holds MSB of digitized Tx bias from ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXBIASMSB	R	N/A	

A5h	TX BIAS LSB			Holds LSB of digitized Tx bias ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXBIASLSB	R	N/A	

A6h	TX MOD MSB			Holds MSB of digitized Tx modulation ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXMODMSB	R	N/A	

A7h	TX MOD LSB			Holds LSB of digitized Tx modulation ADC. 8-bit value.
Byte	Name	Type	PoR	
	TXMODMSB	R	N/A	

A8h	RX POWER MSB			Holds MSB of digitized receiver signal strength indicator ADC. 8-bit value.
Byte	Name	Type	PoR	
	RXPOWER MSB	R	N/A	

A9h	RX POWER LSB			Holds LSB of digitized receiver signal strength indicator ADC. 8-bit value.
Byte	Name	Type	PoR	
	RXPOWER LSB	R	N/A	

AAh	VDD_TX MSB			Holds MSB of digitized Tx supply voltage ADC. 8-bit value.
Byte	Name	Type	PoR	
	VDD_TX MSB	R	N/A	

ABh	VDD_TX LSB	Holds LSB of digitized Tx supply voltage ADC.

Byte	Name	Type	PoR	8-bit value.
	VDD_TX LSB	R	N/A	

ACh	VDD_RX MSB			Holds MSB of digitized Rx supply voltage ADC. 8-bit value.
Byte	Name	Type	PoR	
	VDD_RX MSB	R	N/A	

ADh	VDD_RX LSB			Holds LSB of digitized Rx supply voltage ADC. 8-bit value.
Byte	Name	Type	PoR	
	VDD_RX LSB	R	N/A	

AEh	VDD_DIG MSB			Holds MSB of digitized digital supply voltage ADC. 8-bit value.
Byte	Name	Type	PoR	
	VDD_DIG MSB	R	N/A	

AFh	VDD_DIG LSB			Holds LSB of digitized digital supply voltage ADC. 8-bit value.
Byte	Name	Type	PoR	
	VDD_DIG LSB	R	N/A	

B0h	CONTROL0			Control0 register.
Bit	Name	Type	PoR	
7	GPON_1	R/W	0	Set GPON power level: 00 = 0dB (default) 01 = -3dB, 11 = -6dB, 10 = Not Used.
6	GPON_0	R/W	0	
5	RX_PWR_DWN	R/W	0	Set to ‘1’ to power down the receiver section.
4	TX_PWR_DWN	R/W	0	Set to ‘1’ to power down the transmitter section.
3	MODULATION	R/W	0	Set to ‘1’ to inhibit modulation current.
2	BIAS	R/W	0	Set to ‘1’ to inhibit bias current.
1	SHUTDOWN	R/W	0	Set to ‘1’ to activate FET shutdown of VDD_TXO
0	BEN_TOGGLE	R/W	0	Indicates activity on BEN input pin.

B1h	BIASDAC MSB			Sets open loop bias current. Register 65h bit 1 must be set to ‘1’ to use in open loop mode.
Byte	Name	Type	PoR	
	BIASDACMSB	R/W	00h	

B2h	BIASDAC LSB			Sets open loop bias current. Register 65h bit 1 must be set to ‘1’ to use in open loop mode.
Byte	Name	Type	PoR	
	BIASDACLSB	R/W	00h	

B3h	WATCHDOG			Watchdog counter register. If the watchdog is enabled then this register must be constantly loaded with the value FFh as the internal counter decrements down to 00h. If the register reaches 00h then the NT25L91 will disable the transmitter outputs and assert a non-latching TX_FAULT.
Byte	Name	Type	PoR	
	WATCHDOG	R/W	00h	

B4h	STATUS0			Status0 register
Bit	Name	Type	PoR	
7	TX_DIS_PIN	R	0	Reports the status of the TX_DISABLE pin (1 = HIGH, 0 = LOW)
6	TX_FAULT_PIN	R	0	Reports the status of the TX_FAULT pin (1 = HIGH, 0 = LOW)
5	RX_LOS_PIN	R	0	Reports the status of the LOS pin (1 = HIGH, 0 = LOW)
4	READY	R	0	IC sets bit to '1' when the IC is powered up correctly and ready.
3	DDMI_READY	R	0	IC sets bit to '1' when DDMI data is ready
2	ADDR_ADC_2	R/W	0	Select ADC to be addressed.
1	ADDR_ADC_1	R/W	0	
0	ADDR_ADC_0	R/W	0	

B5h	STATUS1			Status1 register
Bit	Name	Type	PoR	
7	NVM_CHECK_OK	R	0	Indicates successful programming of NVM.
6	NVM_WRITE_DONE	R	0	Indicates NVM write cycle completed.
5	CAL_2	R	0	Status of the NVM block used for holding calibration data. These bits contain the current NVM block being accessed.
4	CAL_1	R	0	
3	CAL_0	R	0	
2	USER_2	R	0	Status of the NVM block used for holding user data. These bits contain the current NVM block being accessed.
1	USER_1	R	0	
0	USER_0	R	0	

B6h	CONTROL1			Control1 register
Bit	Name	Type	PoR	
7	LEVEL_DET_EN	R/W	0	Set to '1' to remove default TX_IN± input threshold of 25mVpp differential.
6	BENLEV_DET_EN	R/W	0	Set to '1' to remove default BEN± input threshold of 25mVpp differential.
5	MOD_LIMIT_DIS	R/W	0	Set to '1' to disable the modulation overcurrent limit. Default limit is 102mA.
4		R	0	
3		R	0	
2		R	0	
1		R	0	
0		R	0	

Factory Setting Non-Volatile Memory Registers

D0h	FACTORY NVM			Factory set NVM
Byte	Name	Type	PoR	
	FACTORY NVM	R/W	00h	

D1h	FACTORY NVM			Factory set NVM
Byte	Name	Type	PoR	
	FACTORY NVM	R/W	00h	

Non-volatile memory program registers

E5h	USER NVM PRGM			This register must be written with a pre-defined code to program the on-chip user NVM. Write ‘C6h’ to initiate programming of NVM.
Byte	Name	Type	PoR	
	USER_NVM_PRGM	R/W	00h	

EAh	FACTORY NVM PRGM			This register must be written with a pre-defined code to program the on-chip factory NVM. Factory use only.
Byte	Name	Type	PoR	
	FACT_NVM_PRGM	R/W	00h	

Applications Information

Applications

The following applications circuit diagrams show how the NT25L91 can be used in several different fiber optic transceiver applications.

GePON FTTh ONU Transceiver Module

The application schematic below shows how the NT25L91 can be configured for use in a GePON transceiver module. The NT25L91 can be used without any additional external memory or microcontrollers as GePON applications generally do not require digital diagnostic monitoring functionality and the NT25L91 can be digitally programmed during module assembly via the I^2C interface and set-up values stored in the on-chip NVM.

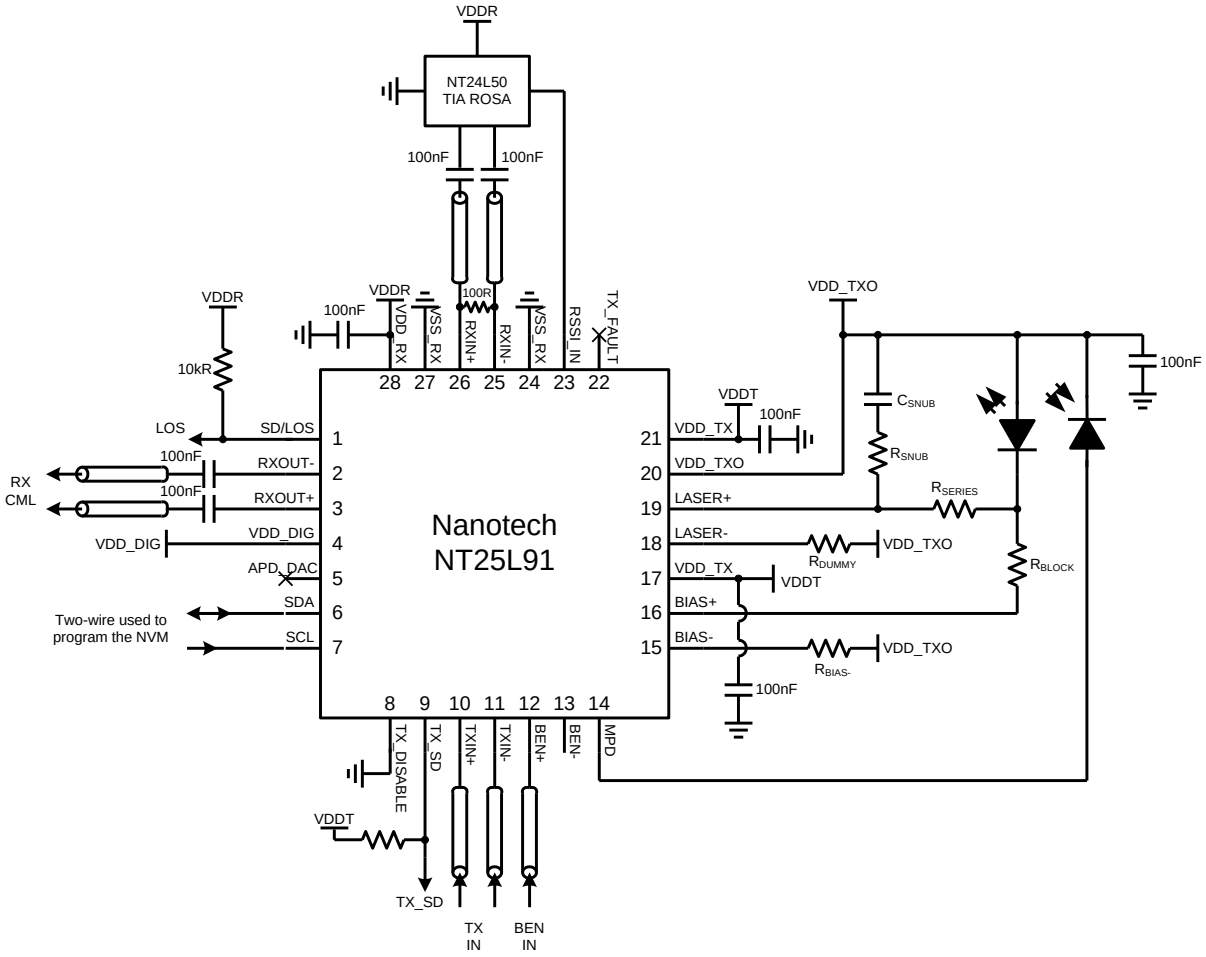


Figure 64 – Typical GePON Module Application Using NT25L91

GPON FTTh ONU Transceiver Module

The application schematic below shows how the NT25L91 can be configured for use in a GPON transceiver module. In this application for a GPON Tri-Plexer module the NT25L91 is used in conjunction with an external microcontroller that features digital and analogue I/O. The NT25L91 is shown using an external temperature sensor, in additional to the internal sensor, allowing accurate monitoring of the temperature local to the tri-plexer laser. The external microcontroller provides the external I^2C data interface to the module host interface and processes digital diagnostic data obtained by reading the digital memory of the NT25L91. In addition the external microcontroller is used to set-up and control a video amplifier for CATV signal reception.

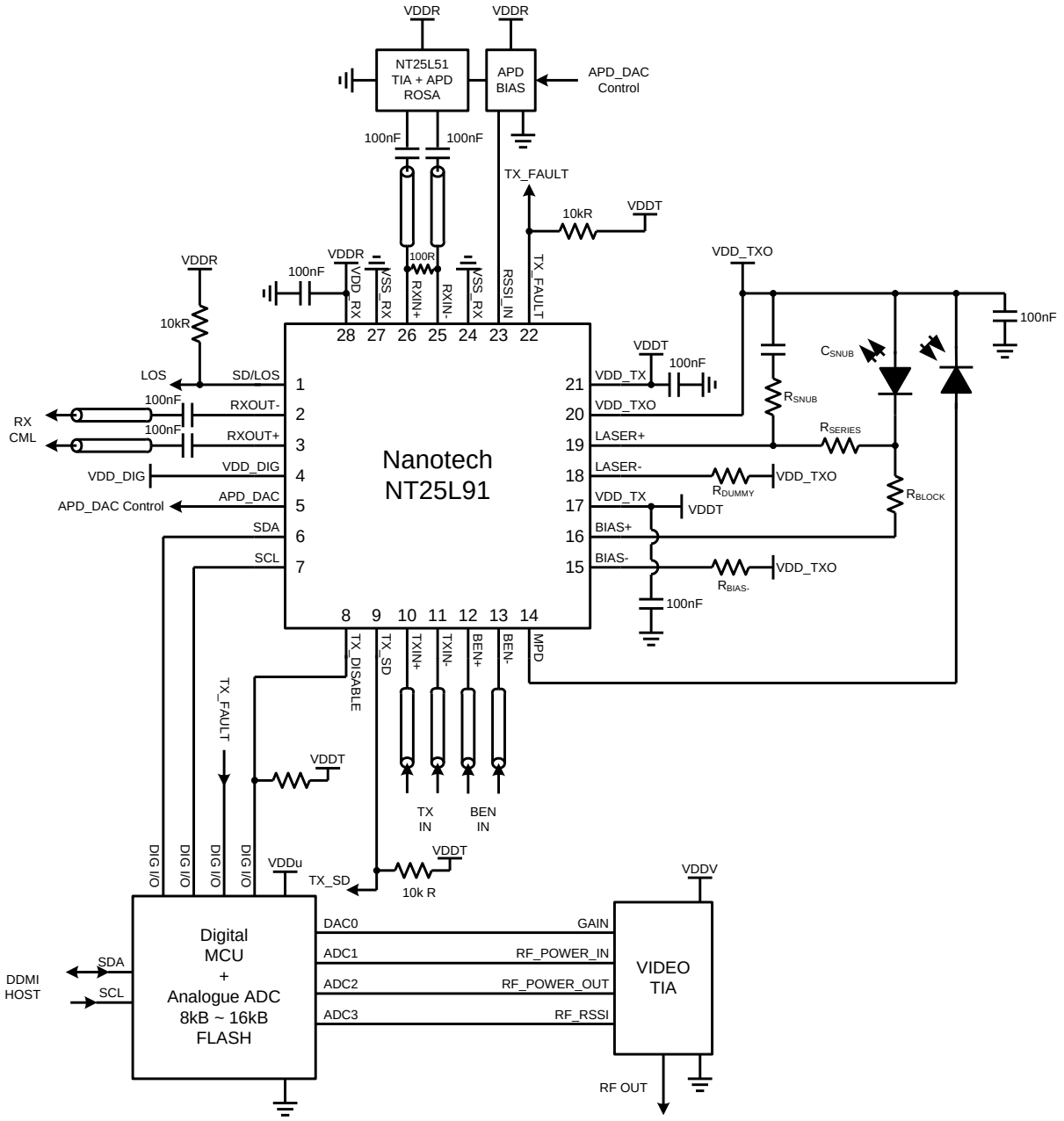


Figure 65 – Typical GPON Module Application Using NT25L91

GPON APD BOSA-on-Board Application

The application schematic below shows how the NT25L91 can be configured for use in a GPON ONU BOSA-on-Board application. The NT25L91 is controlled via the I_2C interface from the ONU GPON MAC SoC or microcontroller. The example below shows an APD based receiver, using Semtech's NT25L51 TIA + APD in a BOSA, where the APD control voltage is provided by an external switching boost regulator that is controlled via the NT25L91's on-chip APD_DAC output.

An alternative, non APD, solution could use Semtech's NT25L59 high sensitivity 2.5 Gbps TIA. In this case the APD_DAC output is not used.

The NT25L91 mean power control loop is used to set and maintain the transmitter output power whilst the extinction ratio control can be provided either by the NT25L91's on-chip temperature compensated modulation current control or by using modulation current Look-Up Tables stored on the GPON SoC set via the I^2C interface.

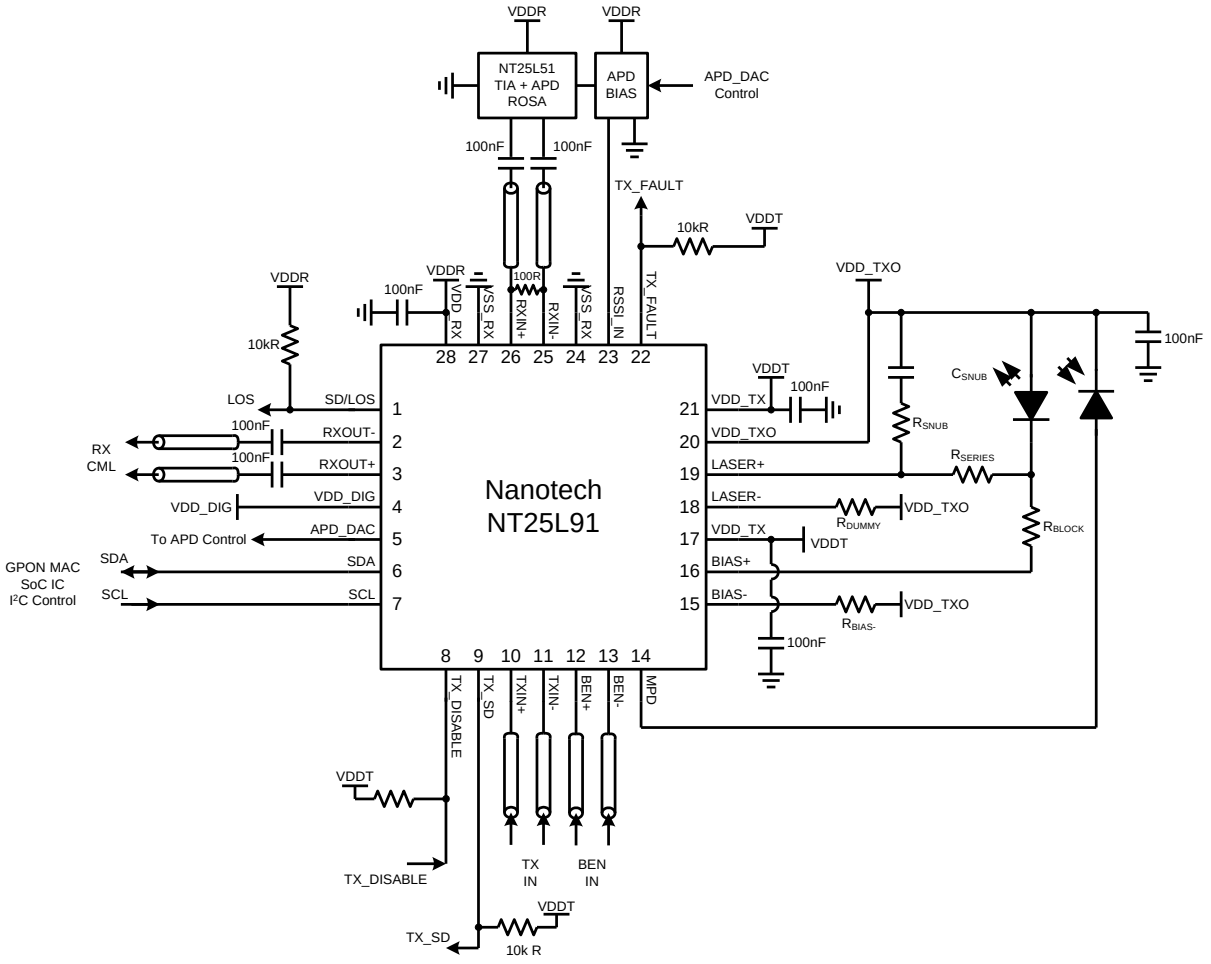


Figure 66 – Typical GPON ONU BOSA-on-Board Application Using NT25L91

SFP DDMI Transceiver Module

The application schematic below shows how the NT25L91 can be configured for use in a GbE SFP DMMI transceiver module. The NT25L91 is used in conjunction with an external microcontroller that features some digital I/O only. The microcontroller provides the external I^2C data interface to the module host interface and processes digital diagnostic data obtained by reading the digital memory of the NT25L91.

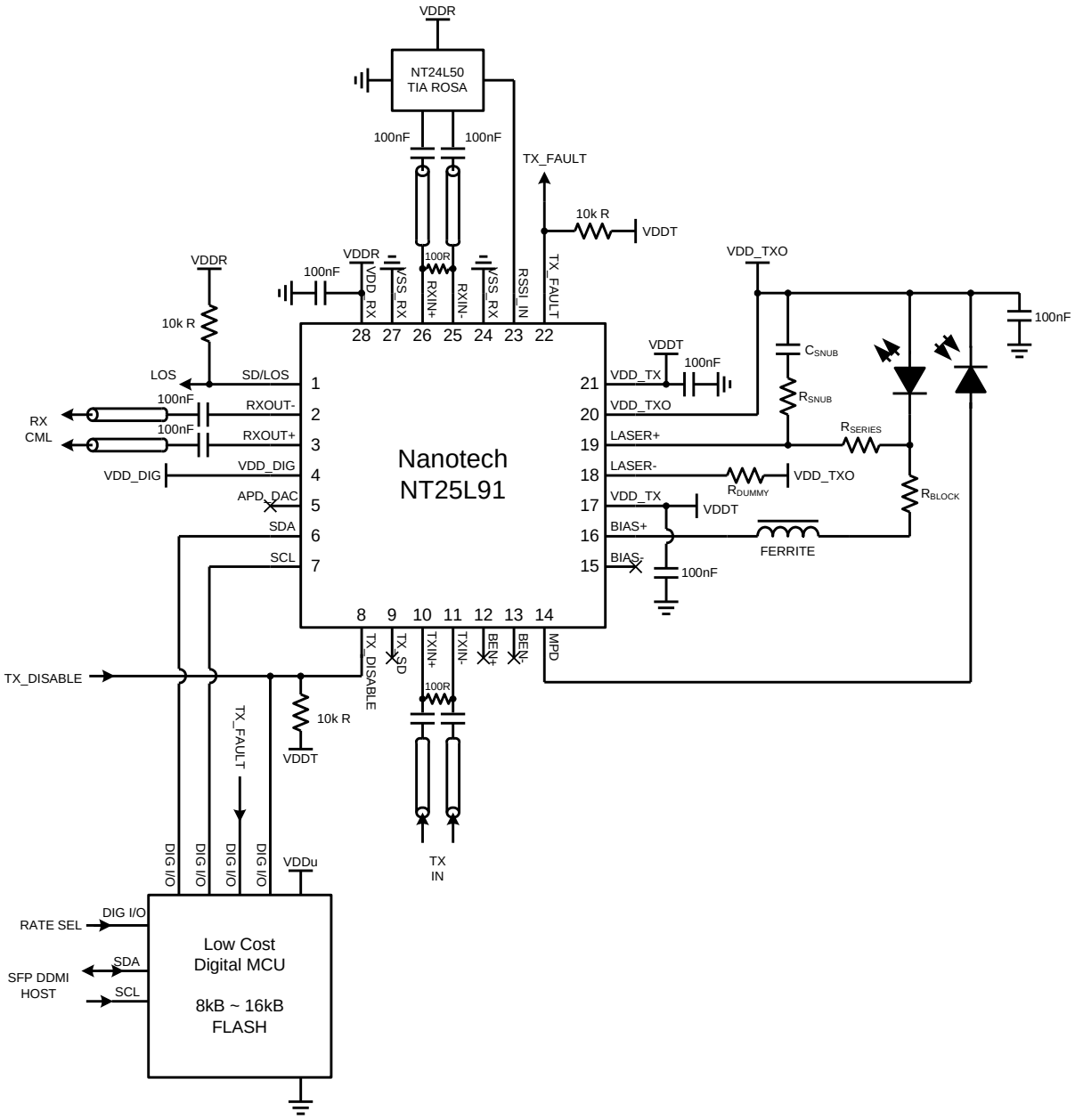
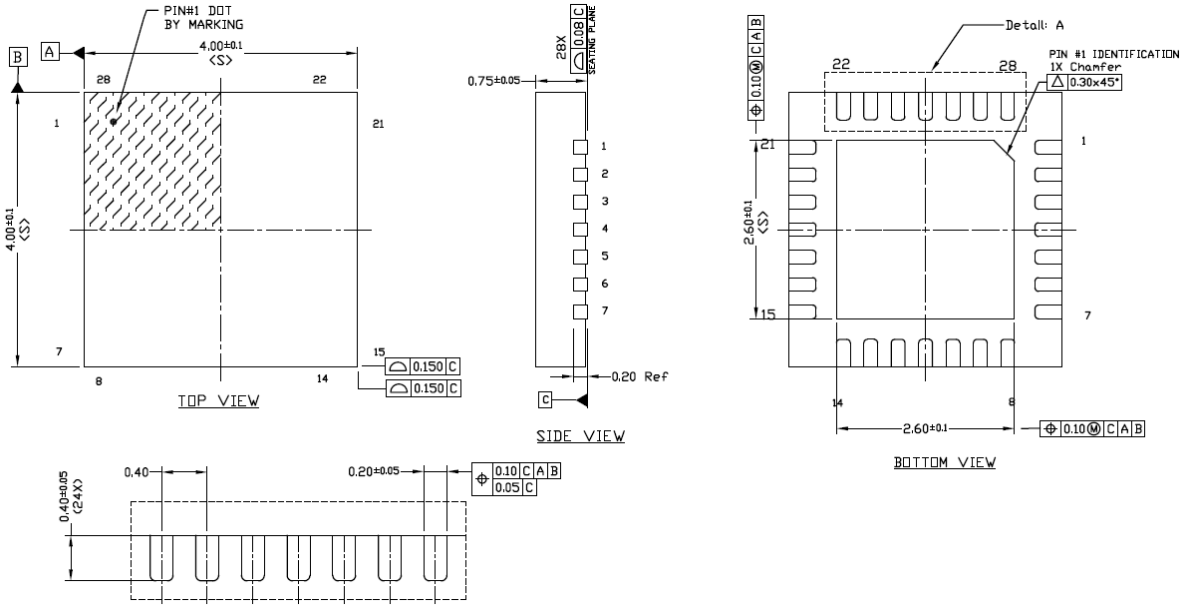


Figure 67 – Typical GbE SFP DDMI Module Application Using NT25L91

Package Information

QFN 28-pin, 4 x 4 mm, 0.4 mm pitch



Dimensions in mm

Figure 68 – 4 mm x 4 mm QFN 28 Lead Mechanical Package Drawing

Table 29 – Ordering Information

Part Number	Package
NT25L91-QFN	4 mm x 4 mm QFN 28 in Trays
NT25L91-QFN-TR	4 mm x 4 mm QFN 28 on Tape & Reel

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