



Latch-up TESTING REPORT

Applicant/Department: Nations Technologies Inc.			
Product: N32G030C8L7		LOT:	
Case NO: S210319134		Quantity: 9 ea	
Test Item: Latch-up (LU)		Package/Pin Count: LQFP48	
Application Date: 2021/3/19		Date Finished: 2021/3/30	
Reference: JESD78E		Temperature: 85 ± 5 °C Humidity: 55 ± 5%	
Test Instrument: MK2(SN0204336)		Calibration Due Date: 2020/09/02~2021/09/01	
Test Voltage: 1.5*VDDmax			
Failure Criteria:			
If absolute Inom is ≤ 25 mA, then absolute Inom + 10 mA is used Or If absolute Inom is >25mA, then > 1.4X absolute Inom is used			
Trigger Current:	±100mA	Minimum Pass Level = ±	±100mA
Trigger Voltage:	/	Minimum Pass Level = ±	/
Vsupply Over Voltage:	1.5*VDDmax	Minimum Pass Level = ±	+7.5V

NOTE 1: ESD/latch-up test is employed as one of qualification tests for electronic products. However, the pass / fail results of this test can NOT be taken as go/no-go criteria for IC tape-out and mass production. Before and after ESD/latch-up test(s), complete parametric and functional testing (F/T) are essential for determining pass/fail of the tested products. (References: Page 9, AEC-Q100-003-Rev-E-2003; and Page 15, ESDA-JEDEC JS-001-2017).

NOTE 2: MA-tek sample storage policy is 14 days after the test data delivery. Prolonged storage can be arranged per client's request.

WE HEREBY CERTIFY THAT:

The test(s) was/were conducted according to test conditions provided by customer. Testing was performed on calibrated and JEDEC-ESDA qualified ESD instruments. The quality and comprehensiveness of this test(s) were delivered by qualified personnel.

Tested by	Reviewed by	Approved by
Joe_Xu	Fly-Fei	Zhen-zhu

CERTIFICATE of APPROVAL INDEPENDENT TESTING LABORATORY:

ISO9001:2015 Certificate Registration No. 20001845 QM08, issued by UL DQS Inc.
IEC/IECQ17025 Certificate No. IECQ-L ULTW 09.0009, approved by Certification Body (CB): UL Registered Firm





实验室管理公正性声明 Impartiality

为维护实验室的公正性，保护检测活动的独立性，本实验室声明：

1. 遵守国家法律、法规和认可机构的要求，执行分析检测服务；
2. 坚持独立检测、独立判断，保持和发展认可的分析检测能力；
3. 坚持公平、公正、对所有客户一视同仁的分析检测服务原则；
4. 不从事与客户送检产品相关的研发、生产、销售等活动；
5. 不接受有违分析检测公正性的投资赞助和代理要求，不介入客户之间的市场竞争和利益冲突；
6. 维护客户的权利，保护客户的所有权和专利权不受侵犯。

保护客户机密信息和所有权的承诺 Confidentiality

实验室承诺保护客户的机密信息和所有权。客户提供的分析检测方法、技术要求和图面文件、说明书以及委托合约和协议等与分析检测有关的所有文件及受检样品、检测结果均列入实验室保密范畴，以及保护客户所有权的完整性。在主持能力验证和分包检测时，也为参加实验室及客户的检测数据及结果保密。



TABLE OF CONTENTS

1. TEST SUMMARY
2. PIN ASSIGNMENT
3. ESD TESTING CONDITIONS
4. RAW DATA
5. APPENDIX-1 (PASS/FAIL CRITERIA)
6. APPENDIX-2 (ESD INSTRUMENTATION AT MA-TEK)

**1. TEST SUMMARY**

IT CLASS: II NOTE: Class I - Latch-up testing performed at room temperature. Class II - Latch-up testing performed at maximum ambient rated temperature for the device. Level: A Level A - The failure criteria as defined in JEDEC. Level B - Special failure criteria. Supplier shall provide definition of failure criteria used.	Trigger Model	Test Pin	Sample	Passing Current or Voltage
	+IT	+IT_IO_85C	3	Pass(+100mA)
	-IT	-IT_IO_85C	3	Pass(-100mA)
	Vsupply Over voltage test	OV_VDD_85C	3	Pass(+7.5V)

NOTE: Red color in raw data indicates failed pins, if any.

**2. Pin ASSIGNMENT**

Pin Group	PAD Pins
VDD	1,24,48
VSS	8,23,47
IO	2-7,9-22,25-46



3. ESD TEST CONDITIONS

Positive Current Trigger
Negative Current Trigger
Over Voltage Supply Test

VDD= 5V
GND= 0V

Clamp= 200mA

Vclamp= +7.5V/-2.5V (IO5V pins)

**4. Raw Data - 2**

Positive Current Trigger_+100 (Unit:mA) 85C								
Test Pin Fail Current	#1	#2	#3	Test Pin Fail Current	#1	#2	#3	
VDD	/	/	/	IO	Pass	Pass	Pass	
VSS	/	/	/					

Negative Current Trigger_-100 (Unit:mA) 85C								
Test Pin Fail Current	#4	#5	#6	Test Pin Fail Current	#4	#5	#6	
VDD	/	/	/	IO	Pass	Pass	Pass	
VSS	/	/	/					

Vsupply Over voltage test_+7.5 (Unit:V) 85C								
Test Pin Fail Voltage	#7	#8	#9	Test Pin Fail Voltage				
VDD	Pass	Pass	Pass					

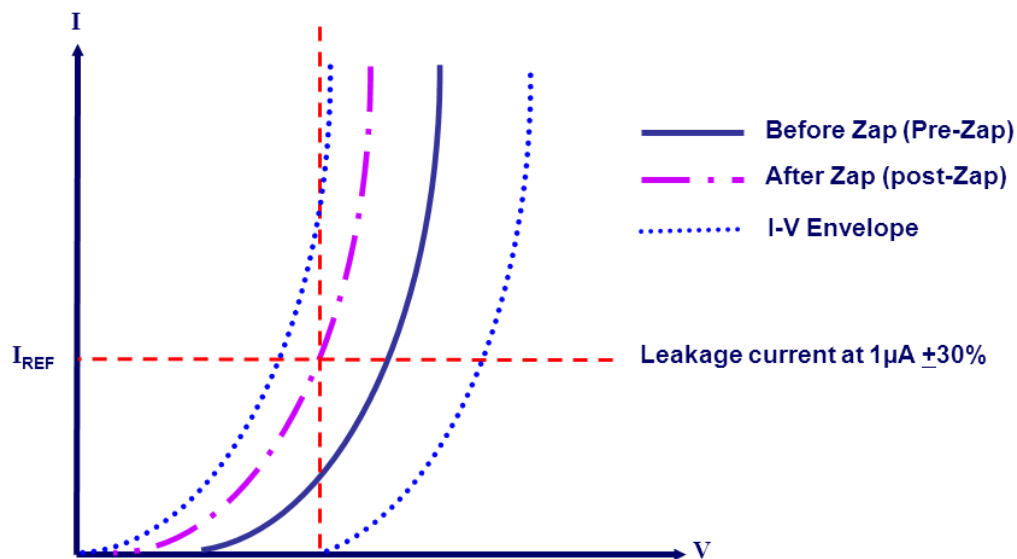
5. APPENDIX-1 (PASS/FAIL CRITERIA)

FAILURE CRITERIA

If absolute I_{nom} is ≤ 25 mA, then absolute $I_{nom} + 10$ mA is used
Or If absolute I_{nom} is > 25 mA, then $> 1.4X$ absolute I_{nom} is used.

Note

For custom designed ESD testing customers may select variation in I_{dd} , and leakage current as criteria to determine pass/fail results of ESD testing.

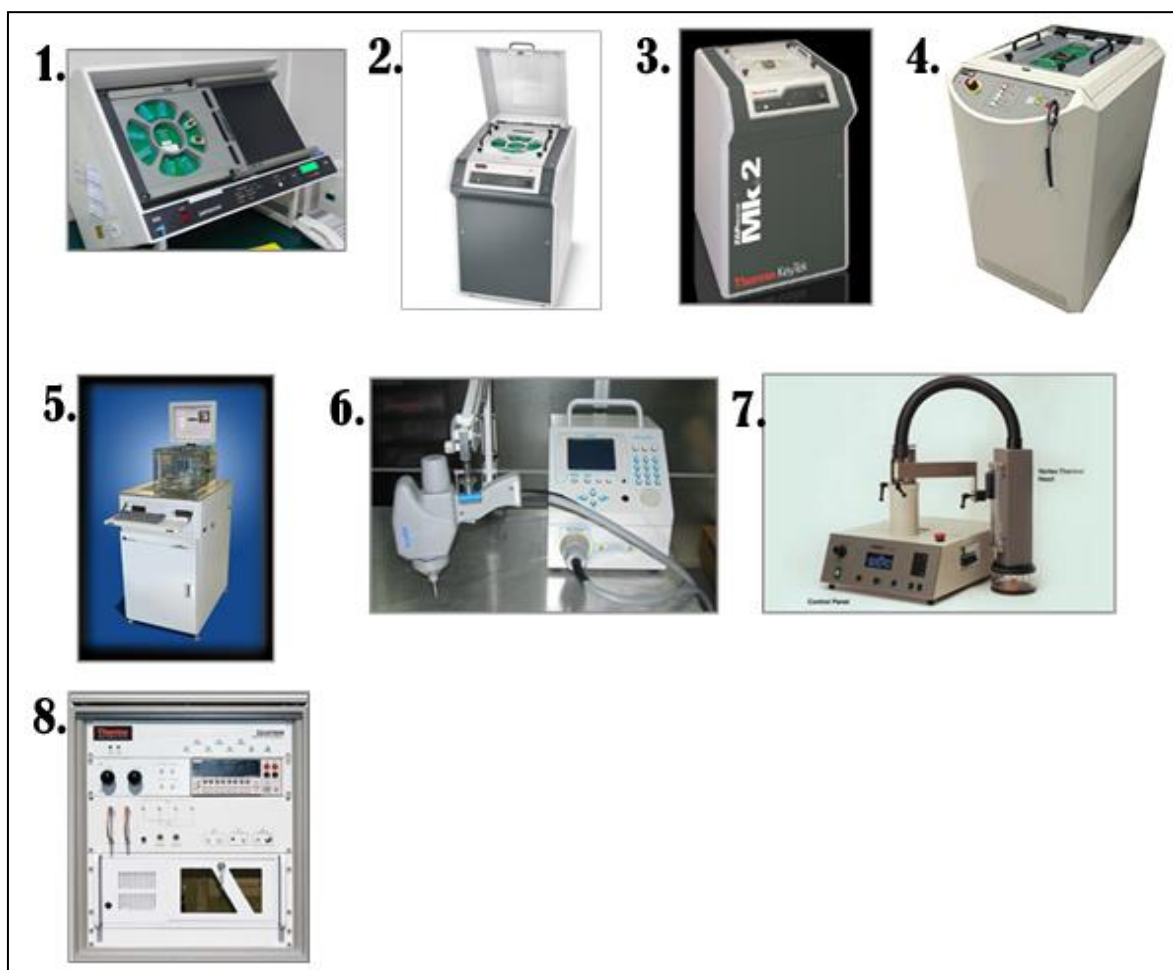


Pass/Fail Criteria:

Variation of Leakage Current and I-V Shift in Pre-Zap and Post-Zap curves

6. APPENDIX-2 (ESD INSTRUMENTATION AT MA-TEK)

No.	Test Tools	Vendors	System Specification
1	Zapmaster	Thermo Keytek	256 Pin Count, ESD Pulse 50 V to 8 KV
2	MK1	Thermo Scientific	256 Pin Count, ESD Pulse 10 V to 8 KV
3	MK2	Thermo Keytek	768 Pin Count, ESD Pulse 10 V to 8 KV
4	MK4	Thermo Scientific	2304 Pin Count, ESD Pulse 10 V to 8 KV
5	CDM Tester	Oryx Orion	100 V to 2 KV
6	ESD Gun	Noiseken	Voltage = 1 KV to 30 KV
7	High Temp. Test Module	Thermonics	Maximum temperature = 150°C.
8	TLP Tester	Thermo Scientific	Voltage = 1 V to 2 KV, Current = 10 nA to 40 A





DISCLAIMER:

1 This report is proprietary to the client and may not be copied, reproduced or referred (whether in whole or in part) to any other party by any means without the prior written consent of MA-tek.

本報告非經本公司事前書面同意，不得複製、轉載、提述(全部或部份內容)於他人。

2 The information contained in or referred to in this report is based solely on information, data and/or samples provided to MA-tek by the client. All of the contents of this report shall be treated as a whole. Any single page of this report shall not be used or interpreted separately.

本報告僅針對客戶提供的試樣作出技術分析，報告中的任意頁次不可以被拆解來單獨使用。

3 This report shall be used as technical reference only. Unless with the prior written consent of MA-tek, this report shall not be used for any other purpose, especially in legal disputes, nor be evidenced as MA-tek's opinions for any specific case.

本報告僅限於作技術參考，非經本公司事前書面之同意，此報告不得用於訴訟案件，亦不得做為本公司就具體個案表示意見之證明。

