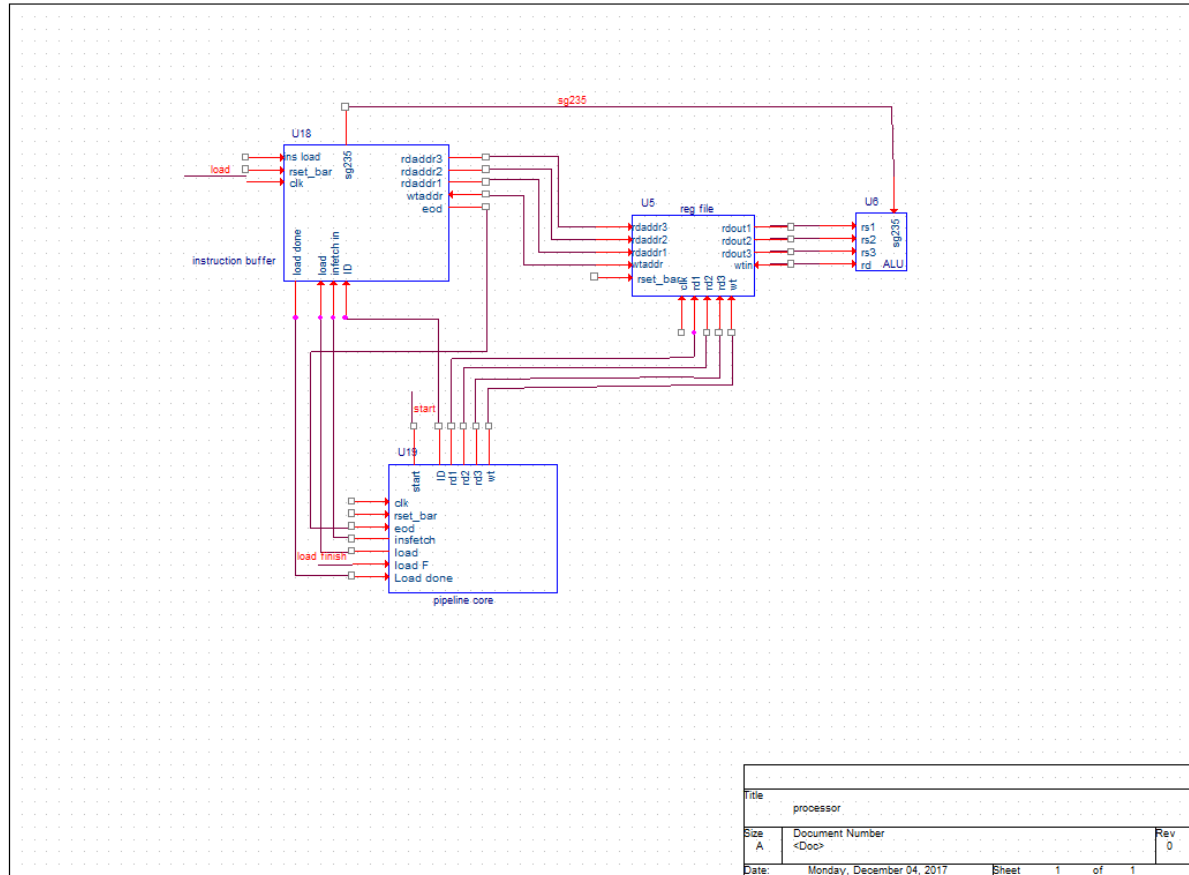
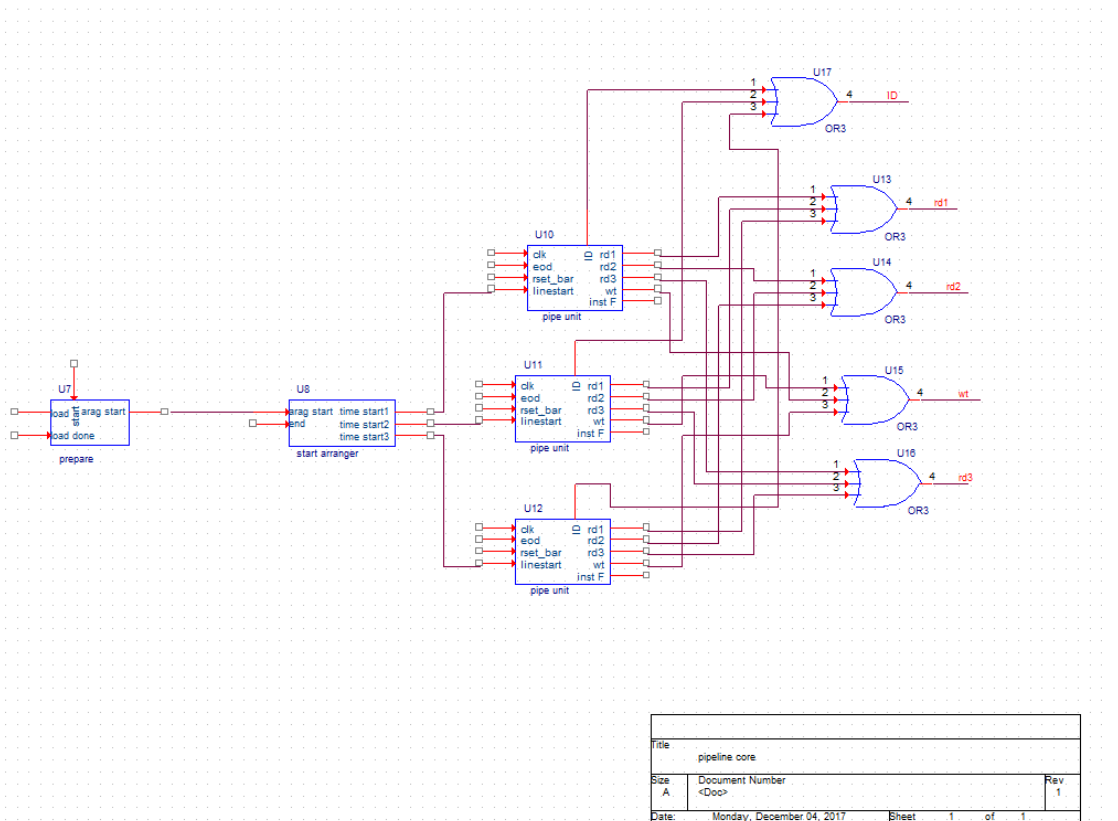
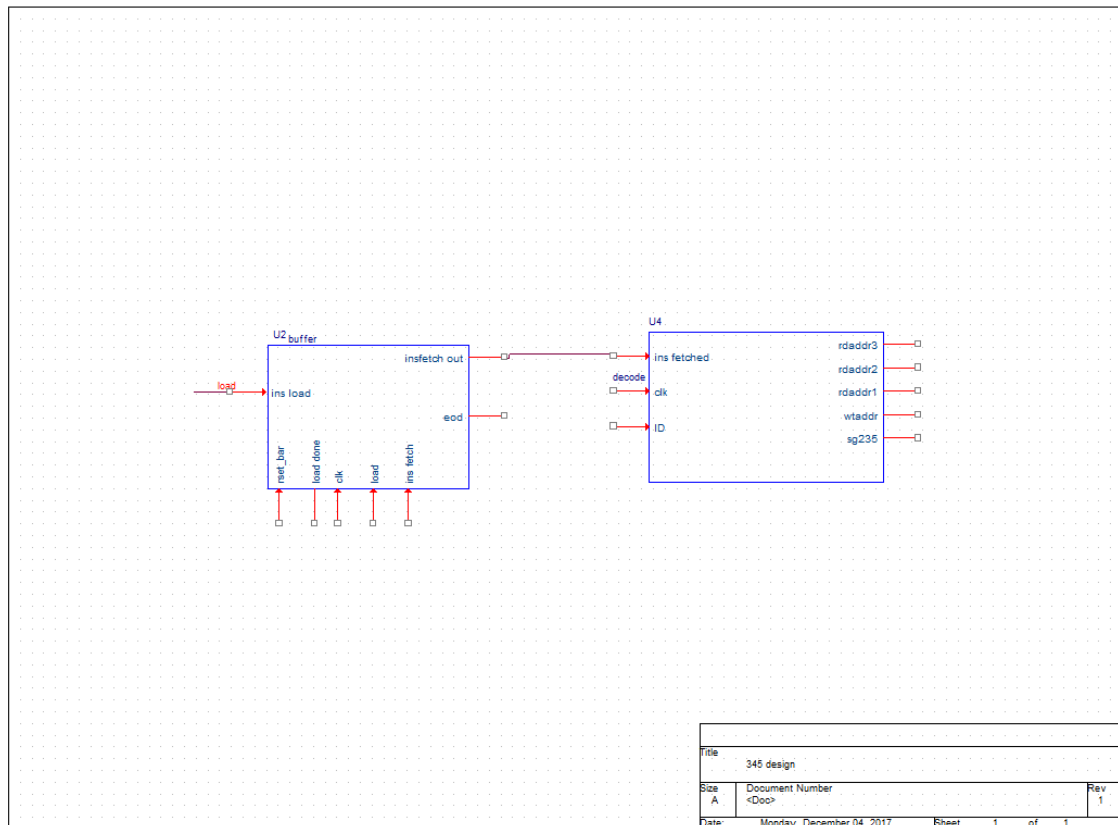

ESE 345 Final Project Report
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Project goal:

To learn a use of VHDL/Verilog hardware description language and modern CAD tools for the structural and behavioral design of the triple-stage pipelined multimedia unit with a reduced set of multimedia instructions similar to those in the Sony Cell SPU and Intel SSE architectures.

Unit block diagram:



Design procedure:

1. Read the design material and understand the whole structure and function of the final design.
2. Design started with draft diagram. We determine how many and what kind of input and output each component have. We determine what kind of subunit should the instruction buffer and pipeline core hold. We combined the IF/ID register and EX/WB register with time sequence. instruction buffer will fetch instruction and hold for one clock cycle. A Decode register was implemented to decode a fetched instruction and send to register file and. It is also driven by clock edge, so it allows the register file and the pipeline core to hold same decoded instruction for one clock cycle. These two designs act as the same way as IF/ID register and EX/WB register. After designed the block diagram of each unit and the time sequence relationship between each unit, we start to code each unit in Active HDL with VHDL language. The register file was coded first. Instruction buffer followed. Then the ALU. Instruction buffer and register file were tested using simulator. Every single instruction was tested using simulator for ALU. The pipeline core was coded in the last. A preparer and a start arranger were coded first. Preparer was used to control the instruction loading and response to the instruction loading finish. The start arranger was used to arrange the start sequence of three pipe line stages. Three pipe line unit was designed using finite state machine. At last, a structural architecture was used to combine three pipeline units and a preparer and a start arranger together to become the pipeline core. After we got all units, we used structural architecture to combine them all together to get the processor. Small helper entity like edge detector and 3to1 or gate was designed to help control signals delivered properly.
3. An instruction convertor was designed to convert hand typed instruction in certain format into machine code for the processor to use. We used python to code the instruction convertor.
4. To test and print the result of the processor, we designed a testbench. The testbench load instruction file in machine language (the output of instruction convertor), start the processor and print processor running status each 0.5ns after the first pipeline started. Our processor clock frequency was set at 1 GHZ. So one clock period is 1ns. The reason why we choose to print status each 0.5 ns is because that we set the write register file each half clock period. It is needed for our design to complete the write back and ALU calculation within one clock cycle. Since at the beginning of EXE stage, ALU immediately calculate the result according to opcode and operands and place the result on wtout output. While at the start of EXE stage, the register also write the value on wtout output into register, and that value was the value of last clock cycle. So we changed the register file writing frequency, to allow it write again during the EXE stage to complete the correct write back process.
5. Proper instruction sequence was designed to test the performance of our processor. We used the matrix multiplication to test the MA, li, bcw instructions and parallel data processing ability as professor recommended during the lecture. We also used another instruction file to test all of other instructions provided by this processor. And for some special instruction with signed number and value limitation, we designed a third instruction file to test those ability of the processor. When design the instruction combinations, we can't use instruction like MA to use a value from a register and write back to the same register. Since the processor we implement realized the dataforwarding function to allow the read and write to same register within the same cycle read out the new written value.

All VHDL source code and testbenches:**Instruction buffer:**

```
--Xiaomin Yuanchang
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use ieee.numeric_std.all;

entity instruction_buffer is
    port(
        rset_bar: in std_logic;
        clk: in std_logic;
        eod: out std_logic;
        load: in std_logic;
        loaddone: out std_logic;
        instructionLoad: in std_logic_vector(23 downto 0);
        instructionFetched: out std_logic_vector(23 downto 0);
        insfetch: in std_logic
    );
end;

architecture behavior of instruction_buffer is

    type memory is array(0 to 31) of std_logic_vector(23 downto 0);
    signal mem : memory;
    begin
        process(clk,rset_bar)
            variable PC : integer range 0 to 32;
            variable loadCount: integer range 0 to 32;
            begin
                if rset_bar = '0'then
                    PC := 0;
                    loadCount :=0;

                elsif rising_edge(clk) then
                    if load = '1'then
                        eod <= '0';
                        mem(loadCount) <= instructionLoad;
                        loadCount := loadCount + 1;
                        if loadCount = 32 then

                            loaddone <= '1';
                        else
```

```
        loaddone <= '0';
    end if;

    elsif insfetch = '1' then

        instructionFetched <= mem(PC);
        PC := PC + 1;

        if PC = loadCount - 2 then
            eod <= '1';
        end if;

        if PC = loadCount then

            PC := 0;
            loadCount := 0;
        end if;
    elsif loadCount > 0 then
        loaddone <= '1';
    end if;
end if;
end process;
end;
```

decode:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
```

entity decode is

```
    port(
        instructionFetched: in std_logic_vector(23 downto 0);
        ID: in std_logic;
        clk: in std_logic;
        sg235: out std_logic_vector(18 downto 0);
        rdaddr3: out std_logic_vector(4 downto 0);
        rdaddr2: out std_logic_vector(4 downto 0);
        rdaddr1: out std_logic_vector(4 downto 0);
        wtaddr: out std_logic_vector(4 downto 0)
    );
end;
```

```

architecture behavioral of decode is
begin
    process(clk)
        variable inskeep : std_logic_vector(23 downto 0);
    begin
        if rising_edge(clk) then

            if ID = '1' then
                inskeep := instructionFetched;
            end if;

            sg235 <= inskeep(23 downto 5);
            rdaddr3 <= inskeep(19 downto 15);
            rdaddr2 <= inskeep(14 downto 10);
            rdaddr1 <= inskeep(9 downto 5);
            wtaddr <= inskeep(4 downto 0);
        end if;
    end process;
end;

```

instructionBuffer:

```

library ieee;
use ieee.std_logic_1164.all;
use pack.all;
entity InstructionBuffer is
    port(
        rset_bar: in std_logic;
        clk: in std_logic;
        eod: out std_logic;
        load: in std_logic;
        loaddone: out std_logic;
        instructionLoad: in std_logic_vector(23 downto 0);
        insfetch: in std_logic;
        ID: in std_logic;
        sg235: out std_logic_vector(18 downto 0);
        rdaddr3: out std_logic_vector(4 downto 0);
        rdaddr2: out std_logic_vector(4 downto 0);
        rdaddr1: out std_logic_vector(4 downto 0);
        wtaddr: out std_logic_vector(4 downto 0)
    );
end;

```

architecture structural of InstructionBuffer is
 signal instruction: std_logic_vector(23 downto 0);

```
begin
```

```
instruction_buffer: entity instruction_buffer
  port map(
    rset_bar=>rset_bar,
    clk=>clk,
    eod=>eod,
    load=>load,
    loaddone=>loaddone,
    instructionLoad=> instructionLoad,
    instructionFetched=>instruction,
    insfetch=>insfetch
  );
```

```
decode: entity decode
  port map(
    instructionFetched=>instruction,
    ID=>ID,
    clk=>clk,
    sg235=>sg235,
    rdaddr3=>rdaddr3,
    rdaddr2=>rdaddr2,
    rdaddr1=>rdaddr1,
    wtaddr=>wtaddr
  );
```

```
--probes
instructionp <= instruction;
```

```
end architecture;
```

Registerfile:

```
--Xiaomin Yuanchang
```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
use ieee.numeric_std.all;
```

```
entity registerfile is
```

```
  port(
    check: in std_logic;
    checkout: out std_logic_vector(63 downto 0);
    wt: in std_logic;
    wtin: in std_logic_vector(63 downto 0);
    rd1: in std_logic;
```



```

    rd2: in std_logic;
    rd3: in std_logic;
    rdout1: out std_logic_vector(63 downto 0);
    rdout2: out std_logic_vector(63 downto 0);
    rdout3: out std_logic_vector(63 downto 0);
    rdaddr1: in std_logic_vector(4 downto 0);
    rdaddr2: in std_logic_vector(4 downto 0);
    rdaddr3: in std_logic_vector(4 downto 0);
    wtaddr: in std_logic_vector(4 downto 0);
    clk: in std_logic;
    rset_bar: in std_logic
  );
end;

architecture behavioral of registerfile is
  type memory is array(0 to 31) of std_logic_vector(63 downto 0);
  signal regfile : memory;
begin
  process( rset_bar, clk)
    variable checkcount: integer range 0 to 32;
  begin
    if rset_bar = '0' then
      checkcount:= 0;
      for i in regfile'range loop
        regfile(i)<=(others => '0');
      end loop;
    end if;
    --elsif rising_edge(clk) then
      if wt = '1' then
        regfile(to_integer(unsigned(wtaddr)))<= wtin;
      end if;

      if rd1 = '1' then
        rdout1 <= regfile(to_integer(unsigned(rdaddr1)));
      end if;

      if rd2 = '1' then
        rdout2 <= regfile(to_integer(unsigned(rdaddr2)));
      end if;

      if rd3 = '1' then
        rdout3 <= regfile(to_integer(unsigned(rdaddr3)));
      end if;
    --end if;
  end process;
end;

```

```
        if check = '1' then
            checkout <= regfile(checkcount);
            checkcount := checkcount + 1;
        end if;

    end process;

end;
```

ALU:

--Xiaomin Yuanchang

library ieee;

use ieee.std_logic_1164.all;

use ieee.numeric_std.all;

entity alu is

port(

clk: in std_logic; --not used

rs3: in std_logic_vector(63 downto 0);

rs2: in std_logic_vector(63 downto 0);

rs1: in std_logic_vector(63 downto 0);

sg235: in std_logic_vector(18 downto 0);

rd: out std_logic_vector(63 downto 0)

);

end alu;

architecture behavioral of alu is

begin

process(rs1,rs2,rs3,sg235)

variable rs3s: signed(63 downto 0);

variable rs2s: signed(63 downto 0);

variable rs1s: signed(63 downto 0);

variable rs3us: unsigned(63 downto 0);

variable rs2us: unsigned(63 downto 0);

variable rs1us: unsigned(63 downto 0);

variable rs3std: std_logic_vector(63 downto 0);

variable rs2std: std_logic_vector(63 downto 0);

variable rs1std: std_logic_vector(63 downto 0);

```

variable tmp16_3s: signed(15 downto 0);
variable tmp16_2s: signed(15 downto 0);
variable tmp16_1s: signed(15 downto 0);

variable tmp16_1std: std_logic_vector(15 downto 0);
variable tmp32_1std: std_logic_vector(31 downto 0);

variable tmp16_2us: unsigned(15 downto 0);
variable tmp16_1us: unsigned(15 downto 0);

variable products: signed(31 downto 0);
variable productus: unsigned(31 downto 0);

variable tempouts: signed(63 downto 0);
variable tempoutus: unsigned(63 downto 0);
variable addsub: signed(31 downto 0);
variable count: integer;
variable rightout: std_logic;
variable shiftcount: integer;

constant add32_0: signed(addsub'range):= (others => '0');
constant compareleft32: signed(addsub'range):= add32_0 + (-2)**31;
constant compareright32: signed(addsub'range):= add32_0 + (2**31)-1;
constant add16_0: signed(15 downto 0):= (others => '0');

constant top : unsigned (7 downto 0) := "11111111";
constant off : unsigned (7 downto 0) := "00000001";
begin

if sg235(18) = '1' then
    if sg235(17 downto 16) = "00" then
        rd(15 downto 0) <= sg235(15 downto 0); --li
    elsif sg235(17 downto 16) = "01" then
        rd(31 downto 16) <= sg235(15 downto 0);
    elsif sg235(17 downto 16) = "10" then
        rd(47 downto 32) <= sg235(15 downto 0);
    elsif sg235(17 downto 16) = "11" then
        rd(63 downto 48) <= sg235(15 downto 0);
    end if;
elsif sg235(17) = '1' then
    if sg235(16 downto 15) = "00" then
        rs3s := signed(rs3); --MA
    end if;
end if;

```

```

rs2s := signed(rs2);
rs1s := signed(rs1);
tmp16_3s := rs3s(15 downto 0);
tmp16_2s := rs2s(15 downto 0);
products := tmp16_3s * tmp16_2s;
addsub := rs1s(31 downto 0) + products;
if products > 0 and rs1s(31 downto 0) >0 and addsub <0 then
    tempouts(31 downto 0) := compareright32;
elsif products < 0 and rs1s(31 downto 0) <0 and addsub >0 then
    tempouts(31 downto 0) := compareleft32;
else
    tempouts(31 downto 0) := addsub;
end if;

tmp16_3s := rs3s(47 downto 32);
tmp16_2s := rs2s(47 downto 32);
products := tmp16_3s * tmp16_2s;
addsub := rs1s(63 downto 32) + products;
if products > 0 and rs1s(63 downto 32) >0 and addsub <0 then
    tempouts(63 downto 32) := compareright32;
elsif products < 0 and rs1s(63 downto 32) <0 and addsub >0 then
    tempouts(63 downto 32) := compareleft32;
else
    tempouts(63 downto 32) := addsub;
end if;

rd <= std_logic_vector(tempouts);

elsif sg235(16 downto 15) = "01" then --MS
    rs3s := signed(rs3);
    rs2s := signed(rs2);
    rs1s := signed(rs1);
    tmp16_3s := rs3s(31 downto 16);
    tmp16_2s := rs2s(31 downto 16);
    products := tmp16_3s * tmp16_2s;
    addsub := rs1s(31 downto 0) + products;
    if products > 0 and rs1s(31 downto 0) >0 and addsub <0 then
        tempouts(31 downto 0) := compareright32;
    elsif products < 0 and rs1s(31 downto 0) <0 and addsub >0 then
        tempouts(31 downto 0) := compareleft32;
    else
        tempouts(31 downto 0) := addsub;
    end if;

```

```
tmp16_3s := rs3s(63 downto 48);
tmp16_2s := rs2s(63 downto 48);
products := tmp16_3s * tmp16_2s;
addsub   := rs1s(63 downto 32) + products;
if products > 0 and rs1s(63 downto 32) >0 and addsub <0 then
    tempouts(63 downto 32) := compareright32;
elsif products < 0 and rs1s(63 downto 32) <0 and addsub >0 then
    tempouts(63 downto 32) := compareleft32;
else
    tempouts(63 downto 32) := addsub;
end if;
```

```
rd <= std_logic_vector(tempouts);
elsif sg235(16 downto 15) = "10" then --l
    rs3s := signed(rs3);
    rs2s := signed(rs2);
    rs1s := signed(rs1);
    tmp16_3s := rs3s(15 downto 0);
    tmp16_2s := rs2s(15 downto 0);
    products := tmp16_3s * tmp16_2s;
    addsub   := rs1s(31 downto 0) - products;
    if products < 0 and rs1s(31 downto 0) >0 and addsub <0 then
        tempouts(31 downto 0) := compareright32;
    elsif products > 0 and rs1s(31 downto 0) <0 and addsub >0 then
        tempouts(31 downto 0) := compareleft32;
    else
        tempouts(31 downto 0) := addsub;
    end if;
```

```
tmp16_3s := rs3s(47 downto 32);
tmp16_2s := rs2s(47 downto 32);
products := tmp16_3s * tmp16_2s;
addsub   := rs1s(63 downto 32) - products;
if products < 0 and rs1s(63 downto 32) >0 and addsub <0 then
    tempouts(63 downto 32) := compareright32;
elsif products > 0 and rs1s(63 downto 32) <0 and addsub >0 then
    tempouts(63 downto 32) := compareleft32;
else
    tempouts(63 downto 32) := addsub;
end if;
```

```

        rd <= std_logic_vector(tempouts);
    elsif sg235(16 downto 15) = "11" then --h
        rs3s := signed(rs3);
        rs2s := signed(rs2);
        rs1s := signed(rs1);
        tmp16_3s := rs3s(31 downto 16);
        tmp16_2s := rs2s(31 downto 16);
        products := tmp16_3s * tmp16_2s;
        addsub := rs1s(31 downto 0) - products;
        if products < 0 and rs1s(31 downto 0) > 0 and addsub < 0 then
            tempouts(31 downto 0) := compareright32;
        elsif products > 0 and rs1s(31 downto 0) < 0 and addsub > 0 then
            tempouts(31 downto 0) := compareleft32;
        else
            tempouts(31 downto 0) := addsub;
        end if;

        tmp16_3s := rs3s(63 downto 48);
        tmp16_2s := rs2s(63 downto 48);
        products := tmp16_3s * tmp16_2s;
        addsub := rs1s(63 downto 32) - products;
        if products < 0 and rs1s(63 downto 32) > 0 and addsub < 0 then
            tempouts(63 downto 32) := compareright32;
        elsif products > 0 and rs1s(63 downto 32) < 0 and addsub > 0 then
            tempouts(63 downto 32) := compareleft32;
        else
            tempouts(63 downto 32) := addsub;
        end if;

        rd <= std_logic_vector(tempouts);
    end if;
    elsif sg235(13 downto 10) = "0001" then --bcw
        rs1s := signed(rs1);
        tempouts(31 downto 0) := rs1s(31 downto 0);
        tempouts(63 downto 32) := rs1s(31 downto 0);
        rd <= std_logic_vector(tempouts);
    elsif sg235(13 downto 10) = "0010" then --and
        rs1std := rs1;
        rs2std := rs2;
        rs1std := rs1std and rs2std;
        rd <= rs1std;
    elsif sg235(13 downto 10) = "0011" then --or
        rs1std := rs1;

```

```

rs2std := rs2;
rs1std := rs1std or rs2std;
rd <= rs1std;
elsif sg235(13 downto 10) = "0100" then    --popcnth
    rs1std := rs1;
    --15-0
    tmp16_1std := rs1std(15 downto 0);
    count := 0;
    for i in tmp16_1std' range loop
        if tmp16_1std(i) = '1' then
            count := count + 1;
        end if;
    end loop;
    tempouts(15 downto 0) := to_signed(count, 16);
    --31-16
    tmp16_1std := rs1std(31 downto 16);
    count := 0;
    for i in tmp16_1std' range loop
        if tmp16_1std(i) = '1' then
            count := count + 1;
        end if;
    end loop;
    tempouts(31 downto 16) := to_signed(count, 16);
    --47-32
    tmp16_1std := rs1std(47 downto 32);
    count := 0;
    for i in tmp16_1std' range loop
        if tmp16_1std(i) = '1' then
            count := count + 1;
        end if;
    end loop;
    tempouts(47 downto 32) := to_signed(count, 16);
    --63-48
    tmp16_1std := rs1std(63 downto 48);
    count := 0;
    for i in tmp16_1std' range loop
        if tmp16_1std(i) = '1' then
            count := count + 1;
        end if;
    end loop;
    tempouts(63 downto 48) := to_signed(count, 16);

rd <= std_logic_vector(tempouts);

```

```

elseif sg235(13 downto 10) = "0101" then    --clz
    rs1std := rs1;
    --31-0
    tmp32_1std := rs1std(31 downto 0);
    count := 0;
    for i in tmp32_1std' range loop
        if tmp32_1std(i) = '1' then
            exit;
        else
            count := count + 1;
        end if;
    end loop;
    tempouts(31 downto 0) := to_signed(count, 32);
    --63-32
    tmp32_1std := rs1std(63 downto 32);
    count := 0;
    for i in tmp32_1std' range loop
        if tmp32_1std(i) = '1' then
            exit;
        else
            count := count + 1;
        end if;
    end loop;
    tempouts(63 downto 32) := to_signed(count, 32);

    rd <= std_logic_vector(tempouts);

elseif sg235(13 downto 10) = "0110" then    --rot
    rs1std := rs1;
    rs2std := rs2;
    shiftcount := to_integer(unsigned(rs2std(5 downto 0)));

    for i in 0 to shiftcount - 1 loop
        rightout := rs1std(0);
        for j in 0 to 62 loop
            rs1std(j) := rs1std(j+1);
        end loop;
        rs1std(63) := rightout;
    end loop;

    rd <= rs1std;

elseif sg235(13 downto 10) = "0111" then    --shlhi
    rs1std := rs1;

```



```

    shiftcount := to_integer(unsigned(sg235(9 downto 5)));
    for i in 0 to shiftcount - 1 loop
        tmp16_1std := rs1std(63 downto 48);
        rs1std(63 downto 48) := rs1std(47 downto 32);
        rs1std(47 downto 32) := rs1std(31 downto 16);
        rs1std(31 downto 16) := rs1std(15 downto 0);
        rs1std(15 downto 0) := tmp16_1std;
    end loop;
    rd <= rs1std;

elsif sg235(13 downto 10) = "1000" then    --a
    rs1us := unsigned(rs1);
    rs2us := unsigned(rs2);
    tempoutus(63 downto 32) := rs1us(63 downto 32) + rs2us(63 downto 32);
    tempoutus(31 downto 0) := rs1us(31 downto 0) + rs2us(31 downto 0);
    rd <= std_logic_vector(tempoutus);

elsif sg235(13 downto 10) = "1001" then    --sfw
    rs1us := unsigned(rs1);
    rs2us := unsigned(rs2);
    tempoutus(63 downto 32) := rs1us(63 downto 32) - rs2us(63 downto 32);
    tempoutus(31 downto 0) := rs1us(31 downto 0) - rs2us(31 downto 0);
    rd <= std_logic_vector(tempoutus);

elsif sg235(13 downto 10) = "1010" then    --ah
    rs1us := unsigned(rs1);
    rs2us := unsigned(rs2);
    tempoutus(63 downto 48) := rs1us(63 downto 48) + rs2us(63 downto 48);
    tempoutus(47 downto 32) := rs1us(47 downto 32) + rs2us(47 downto 32);
    tempoutus(31 downto 16) := rs1us(31 downto 16) + rs2us(31 downto 16);
    tempoutus(15 downto 0) := rs1us(15 downto 0) + rs2us(15 downto 0);
    rd <= std_logic_vector(tempoutus);

elsif sg235(13 downto 10) = "1011" then    --sfh
    rs1us := unsigned(rs1);
    rs2us := unsigned(rs2);
    tempoutus(63 downto 48) := rs1us(63 downto 48) - rs2us(63 downto 48);
    tempoutus(47 downto 32) := rs1us(47 downto 32) - rs2us(47 downto 32);
    tempoutus(31 downto 16) := rs1us(31 downto 16) - rs2us(31 downto 16);
    tempoutus(15 downto 0) := rs1us(15 downto 0) - rs2us(15 downto 0);
    rd <= std_logic_vector(tempoutus);

elsif sg235(13 downto 10) = "1100" then    --ahs
    rs1s := signed(rs1);

```

```

        rs2s := signed(rs2);
        tempouts(63 downto 48) := rs1s(63 downto 48) + rs2s(63 downto 48);
        if rs1s(63 downto 48)>0 and rs2s(63 downto 48)>0 and tempouts(63 downto 48)<0
then
            tempouts(63 downto 48) := add16_0 + (32767);
        elsif rs1s(63 downto 48)<0 and rs2s(63 downto 48)<0 and tempouts(63 downto
48)>0 then
            tempouts(63 downto 48) := add16_0 + (-32768);
        end if;
        tempouts(47 downto 32) := rs1s(47 downto 32) + rs2s(47 downto 32);
        if rs1s(47 downto 32)>0 and rs2s(47 downto 32)>0 and tempouts(47 downto 32)<0
then
            tempouts(47 downto 32) := add16_0 + (32767);
        elsif rs1s(47 downto 32)<0 and rs2s(47 downto 32)<0 and tempouts(47 downto
32)>0 then
            tempouts(47 downto 32) := add16_0 + (-32768);
        end if;
        tempouts(31 downto 16) := rs1s(31 downto 16) + rs2s(31 downto 16);
        if rs1s(31 downto 16)>0 and rs2s(31 downto 16)>0 and tempouts(31 downto 16)<0
then
            tempouts(31 downto 16) := add16_0 + (32767);
        elsif rs1s(31 downto 16)<0 and rs2s(31 downto 16)<0 and tempouts(31 downto
16)>0 then
            tempouts(31 downto 16) := add16_0 + (-32768);
        end if;
        tempouts(15 downto 0) := rs1s(15 downto 0) + rs2s(15 downto 0);
        if rs1s(15 downto 0)>0 and rs2s(15 downto 0)>0 and tempouts(15 downto 0)<0 then
            tempouts(15 downto 0) := add16_0 + (32767);
        elsif rs1s(15 downto 0)<0 and rs2s(15 downto 0)<0 and tempouts(15 downto 0)>0
then
            tempouts(15 downto 0) := add16_0 + (-32768);
        end if;
        rd <= std_logic_vector(tempouts);

    elsif sg235(13 downto 10) = "1101" then    --sfhs
        rs1s := signed(rs1);
        rs2s := signed(rs2);
        tempouts(63 downto 48) := rs1s(63 downto 48) - rs2s(63 downto 48);
        if rs1s(63 downto 48)>0 and rs2s(63 downto 48)<0 and tempouts(63 downto 48)<0
then
            tempouts(63 downto 48) := add16_0 + (32767);
        elsif rs1s(63 downto 48)<0 and rs2s(63 downto 48)>0 and tempouts(63 downto
48)>0 then
            tempouts(63 downto 48) := add16_0 + (-32768);

```

```

        end if;
        tempouts(47 downto 32) := rs1s(47 downto 32) - rs2s(47 downto 32);
        if rs1s(47 downto 32)>0 and rs2s(47 downto 32)<0 and tempouts(47 downto 32)<0
then
            tempouts(47 downto 32) := add16_0 + (32767);
        elsif rs1s(47 downto 32)<0 and rs2s(47 downto 32)>0 and tempouts(47 downto
32)>0 then
            tempouts(47 downto 32) := add16_0 + (-32768);
        end if;
        tempouts(31 downto 16) := rs1s(31 downto 16) - rs2s(31 downto 16);
        if rs1s(31 downto 16)>0 and rs2s(31 downto 16)<0 and tempouts(31 downto 16)<0
then
            tempouts(31 downto 16) := add16_0 + (32767);
        elsif rs1s(31 downto 16)<0 and rs2s(31 downto 16)>0 and tempouts(31 downto
16)>0 then
            tempouts(31 downto 16) := add16_0 + (-32768);
        end if;
        tempouts(15 downto 0) := rs1s(15 downto 0) - rs2s(15 downto 0);
        if rs1s(15 downto 0)>0 and rs2s(15 downto 0)<0 and tempouts(15 downto 0)<0 then
            tempouts(15 downto 0) := add16_0 + (32767);
        elsif rs1s(15 downto 0)<0 and rs2s(15 downto 0)>0 and tempouts(15 downto 0)>0
then
            tempouts(15 downto 0) := add16_0 + (-32768);
        end if;
        rd <= std_logic_vector(tempouts);

    elsif sg235(13 downto 10) = "1110" then    --mpyu
        rs1us := unsigned(rs1);
        rs2us := unsigned(rs2);
        tmp16_1us := rs1us(47 downto 32);
        tmp16_2us := rs2us(47 downto 32);
        productus := tmp16_1us * tmp16_2us;
        tempoutus(63 downto 32) := productus;

        tmp16_1us := rs1us(15 downto 0);
        tmp16_2us := rs2us(15 downto 0);
        productus := tmp16_1us * tmp16_2us;
        tempoutus(31 downto 0) := productus;

        rd <= std_logic_vector(tempoutus);

    elsif sg235(13 downto 10) = "1111" then    --absdb
        rs1us := unsigned(rs1);
        rs2us := unsigned(rs2);

```

```

tempoutus(63 downto 56) := rs1us(63 downto 56) - rs2us(63 downto 56);
if rs1us(63 downto 56) < rs2us(63 downto 56) then
tempoutus(63 downto 56) := top - tempoutus(63 downto 56) + off;
end if;
tempoutus(55 downto 48) := rs1us(55 downto 48) - rs2us(55 downto 48);
if rs1us(55 downto 48) < rs2us(55 downto 48) then
tempoutus(55 downto 48) := top - tempoutus(55 downto 48) + off;
end if;
tempoutus(47 downto 40) := rs1us(47 downto 40) - rs2us(47 downto 40);
if rs1us(47 downto 40) < rs2us(47 downto 40) then
tempoutus(47 downto 40) := top - tempoutus(47 downto 40) + off;
end if;
tempoutus(39 downto 32) := rs1us(39 downto 32) - rs2us(39 downto 32);
if rs1us(39 downto 32) < rs2us(39 downto 32) then
tempoutus(39 downto 32) := top - tempoutus(39 downto 32) + off;
end if;
tempoutus(31 downto 24) := rs1us(31 downto 24) - rs2us(31 downto 24);
if rs1us(31 downto 24) < rs2us(31 downto 24) then
tempoutus(31 downto 24) := top - tempoutus(31 downto 24) + off;
end if;
tempoutus(23 downto 16) := rs1us(23 downto 16) - rs2us(23 downto 16);
if rs1us(23 downto 16) < rs2us(23 downto 16) then
tempoutus(23 downto 16) := top - tempoutus(23 downto 16) + off;
end if;
tempoutus(15 downto 8) := rs1us(15 downto 8) - rs2us(15 downto 8);
if rs1us(15 downto 8) < rs2us(15 downto 8) then
tempoutus(15 downto 8) := top - tempoutus(15 downto 8) + off;
end if;
tempoutus(7 downto 0) := rs1us(7 downto 0) - rs2us(7 downto 0);
if rs1us(7 downto 0) < rs2us(7 downto 0) then
tempoutus(7 downto 0) := top - tempoutus(7 downto 0) + off;
end if;
rd <= std_logic_vector(tempoutus);
--      else
--      rd <= (others => '0');
end if;

end process;
end;

prepare:
library ieee;
use ieee.std_logic_1164.all;

```

```
use ieee.numeric_std.all;
```

```
entity prepare is
```

```
    port(  
        start: in std_logic;  
        loaddone: in std_logic;  
        load: out std_logic;  
        aragstart: out std_logic;  
        clk: in std_logic;  
        loadFinish: in std_logic
```

```
    );
```

```
end;
```

```
architecture behavioral of prepare is
```

```
begin
```

```
    process(loaddone,start,loadFinish)  
    begin  
        --if rising_edge(clk) then  
            if start = '1' then  
                load <= '1';  
            elsif loadFinish = '1' then  
                load <= '0';  
            elsif loaddone = '1' then  
                load <= '0';  
                aragstart <= '1';  
            else  
                aragstart <= '0';  
            end if;  
        --end if;  
    end process;
```

```
end;
```

```
startarag:
```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
```

```
use ieee.numeric_std.all;
```

```
entity startarag is
```

```
    port(  
        aragstart: in std_logic;  
        linestart1: out std_logic;  
        linestart2: out std_logic;  
        linestart3: out std_logic;  
        clk: in std_logic;
```

```
    eod: in std_logic
  );
end;
```

architecture behavioral of startarag is

```
begin
  process(clk)
    variable hold: std_logic;
    variable clkcount: integer range 0 to 4;
  begin
    if rising_edge(clk) then
      if aragstart = '1' then
        hold := '1';
        clkcount := 0;
      end if;

      if eod = '1' then
        hold := '0';
        linestart1 <= '0';
        linestart2 <= '0';
        linestart3 <= '0';
      end if;

      if hold = '1' then
        clkcount := clkcount + 1;
      end if;

      if clkcount = 1 and hold = '1' then
        linestart1 <= '1';
      elsif clkcount = 2 and hold = '1' then
        linestart2 <= '1';
      elsif clkcount = 3 and hold = '1' then
        linestart3 <= '1';
      elsif clkcount = 4 then
        clkcount := 0;
      end if;

    end if;
  end process;
end;
```

edge_det:

library ieee;

use ieee.std_logic_1164.all;

entity edge_det is

port(

rset_bar : in std_logic;

sig: in std_logic;

clk: in std_logic;

sig_edge: out std_logic

);

end;

architecture behavior of edge_det is

begin

process(clk,rset_bar)

variable memory: std_logic := '0';

begin

if rset_bar = '0' then

sig_edge <= '0';

memory := '0';

elsif rising_edge(clk) then

if memory = '0' and sig = '1' then

sig_edge <= '1';

elsif memory = '1' and sig = '1' then

sig_edge <= '0';

end if;

memory := sig;

end if;

end process;

end;

or3to1:

library IEEE;

use IEEE.STD_LOGIC_1164.all;

entity or3to1 is

port(

```

        a : in STD_LOGIC;
        b : in STD_LOGIC;
        c : in std_logic;
        output : out STD_LOGIC
    );
end;

--}} End of automatically maintained section

architecture dataflow of or3to1 is
begin
    output <= a or b or c;
end dataflow;

pipelineunit:
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

use global_signal.all;

entity pipelineunit is
    port(
        status: out std_logic_vector(1 downto 0);
        clk:in std_logic;
        rset_bar:in std_logic;
        eod: in std_logic;
        linestart: in std_logic;
        InstructionF: out std_logic;
        ID: out std_logic;
        rd1: out std_logic;
        rd2: out std_logic;
        rd3: out std_logic;
        wt: out std_logic
    );
end;

architecture behaviroal of pipelineunit is
    --type state is (Idle,InsF,InsD,Exe);
    signal present_state, next_state : std_logic_vector (1 downto 0);
    -- Idle 00, InsF 01, InsD 10, Exe 11
begin
    state_reg: process (clk)
    begin

```



```
if rising_edge(clk) then

    if rset_bar = '0' then
        present_state <= "00";
    else
        present_state <= next_state;
    end if;

    status <= present_state;

end if;
end process;

outputs: process(present_state)
begin
    case present_state is
        when "01" =>
            InstructionF<='1';
            ID <= '0';
            rd1<='0';
            rd2<='0';
            rd3<='0';
            wt<='0';
        when "10" =>
            InstructionF<='0';
            ID <= '1';
            rd1<='0';
            rd2<='0';
            rd3<='0';
            wt<='0';
        when "11"=>
            InstructionF<='0';
            ID <= '0';
            rd1<='1';
            rd2<='1';
            rd3<='1';
            wt<='1';
        when others =>
            InstructionF<='0';
            ID <= '0';
            rd1<='0';
            rd2<='0';
            rd3<='0';
            wt<='0';
    end case;
end process;
```

```
        end case;
    end process;

    nxt_state: process (present_state, eod, linestart)
    begin
        case present_state is
            when "00" =>
                if linestart = '1' then
                    next_state <= "01";
                else
                    next_state <= "00";
                end if;

                when "01" =>
                    next_state <= "10";

                when "10" =>
                    next_state <= "11";

                when "11" =>
                    if eod = '1' then
                        next_state <= "00";
                    else
                        next_state <= "01";
                    end if;

                when others =>
                    next_state <= "00";

            end case;
        end process;
    end;
```

pipelineCore:

```
library ieee;
use ieee.std_logic_1164.all;
```

```
use pack.all;
```

```
entity pipelineCore is
    port(
        rset_bar : in std_logic;
        clk: in std_logic;
        eod: in std_logic;
```

```

    loaddone: in std_logic;
    start: in std_logic;
    loadFinish: in std_logic; -- set , when instruction < 32 finished loading
    load: out std_logic;
    insfetch: out std_logic;
    ID: out std_logic;
    rd1: out std_logic;
    rd2: out std_logic;
    rd3: out std_logic;
    wt: out std_logic
  );
end;

```

architecture structural of pipelineCore is

```

signal aragstart: std_logic;
signal aragstartO: std_logic;
signal linestart1: std_logic;
signal linestart2: std_logic;
signal linestart3: std_logic;
signal linestart11: std_logic;
signal linestart22: std_logic;
signal linestart33: std_logic;
signal insfetch1: std_logic;
signal ID1 : std_logic;
signal rd11 : std_logic;
signal rd21 : std_logic;
signal rd31 : std_logic;
signal wt1 : std_logic;
signal insfetch2: std_logic;
signal ID2 : std_logic;
signal rd12 : std_logic;
signal rd22 : std_logic;
signal rd32 : std_logic;
signal wt2 : std_logic;
signal insfetch3: std_logic;
signal ID3 : std_logic;
signal rd13 : std_logic;
signal rd23 : std_logic;
signal rd33 : std_logic;
signal wt3 : std_logic;
begin

```

```

    prepare: entity prepare
    port map(

```

```
        start => start,  
        loaddone=> loaddone,  
        load=>load,  
        aragstart=>aragstart,  
        clk=>clk,  
        loadFinish=> loadFinish  
    );
```

startarag: entity startarag

```
    port map(  
        aragstart=>aragstartO,  
        linestart1=>linestart1,  
        linestart2=>linestart2,  
        linestart3=>linestart3,  
        clk=>clk,  
        eod=>eod  
    );
```

pipelineunit1: entity pipelineunit

```
    port map(  
        status=> status1,  
        clk=>clk,  
        rset_bar=>rset_bar,  
        eod=>eod,  
        linestart=>linestart1,  
        InstructionF=>insfetch1,  
        ID=>ID1,  
        rd1=>rd11,  
        rd2=>rd21,  
        rd3=>rd31,  
        wt=>wt1  
    );
```

pipelineunit2: entity pipelineunit

```
    port map(  
        status=>status2,  
        clk=>clk,  
        rset_bar=>rset_bar,  
        eod=>eod,  
        linestart=>linestart2,  
        InstructionF=>insfetch2,  
        ID=>ID2,  
        rd1=>rd12,  
        rd2=>rd22,
```

```
        rd3=>rd32,
        wt=>wt2
    );
pipelineunit3: entity pipelineunit
    port map(
        status=>status3,
        clk=>clk,
        rset_bar=>rset_bar,
        eod=>eod,
        linestart=>linestart3,
        InstructionF=>insfetch3,
        ID=>ID3,
        rd1=>rd13,
        rd2=>rd23,
        rd3=>rd33,
        wt=>wt3
    );
edgeD1: entity edge_det
    port map(

        rset_bar=>rset_bar,
        sig=>aragstart,
        clk=>clk,
        sig_edge=>aragstartO
    );

edgeD2: entity edge_det
    port map(
        rset_bar=>rset_bar,
        sig=>linestart1,
        clk=>clk,
        sig_edge=>linestart11
    );
edgeD3: entity edge_det
    port map(
        rset_bar=>rset_bar,
        sig=>linestart2,
        clk=>clk,
        sig_edge=>linestart22
    );
edgeD4: entity edge_det
    port map(
        rset_bar=>rset_bar,
        sig=>linestart3,
```

```
        clk=>clk,
        sig_edge=>linestart33
    );
or3to11: entity or3to1
    port map(
        a => ID1,
        b => ID2,
        c => ID3,
        output => ID
    );
or3to12: entity or3to1
    port map(
        a =>insfetch1,
        b =>insfetch2,
        c =>insfetch3,
        output =>insfetch
    );
or3to13: entity or3to1
    port map(
        a =>wt1,
        b =>wt2,
        c =>wt3,
        output =>wt
    );
or3to14: entity or3to1
    port map(
        a =>rd11,
        b =>rd12,
        c =>rd13,
        output =>rd1
    );
or3to15: entity or3to1
    port map(
        a => rd21,
        b => rd22,
        c => rd23,
        output => rd2
    );
or3to16: entity or3to1
    port map(
        a => rd31,
        b => rd32,
        c => rd33,
        output => rd3
    );
```

```

        );
    --probes
        wt1p<=wt1;
        wt2p<=wt2;
        wt3p<=wt3;

end architecture;

Processor:
library ieee;
use ieee.std_logic_1164.all;

use pack.all;

entity Processor is
    port(
        check: in std_logic;
        checkout: out std_logic_vector(63 downto 0);
        instructionLoad: in std_logic_vector(23 downto 0);
        start: in std_logic;
        loadFinish: in std_logic; -- set , when instruction < 32 finished loading
        clk: in std_logic;
        rset_bar: in std_logic;
        eodo: out std_logic
        --registerRead: in std_logic;
        --registerData: out std_logic_vector(63 downto 0)
    );
end;

architecture structural of Processor is
    signal eod : std_logic;
    signal load : std_logic;
    signal loaddone : std_logic;
    signal insfetch : std_logic;
    signal ID : std_logic;
    signal sg235: std_logic_vector(18 downto 0);
    signal rdaddr3: std_logic_vector(4 downto 0);
    signal rdaddr2: std_logic_vector(4 downto 0);
    signal rdaddr1: std_logic_vector(4 downto 0);
    signal wtaddr: std_logic_vector(4 downto 0);

    signal wt: std_logic;
    signal wtin: std_logic_vector(63 downto 0);
    signal rd1: std_logic;

```

```

signal    rd2: std_logic;
signal    rd3: std_logic;
signal    rdout1: std_logic_vector(63 downto 0);
signal    rdout2: std_logic_vector(63 downto 0);
signal    rdout3: std_logic_vector(63 downto 0);

```

```
begin
```

```

InstructionBuffer: entity InstructionBuffer
  port map(
    rset_bar=>rset_bar,
    clk=>clk,
    eod=>eod,
    load=>load,
    loaddone=>loaddone,
    instructionLoad=>instructionLoad,
    insfetch=>insfetch,
    ID=>ID,
    sg235=>sg235,
    rdaddr3=>rdaddr3,
    rdaddr2=>rdaddr2,
    rdaddr1=>rdaddr1,
    wtaddr=>wtaddr
  );

```

```

registerfile: entity registerfile
  port map(
    check=>check,
    checkout=>checkout,
    wt=>wt,
    wtin=>wtin,
    rd1=>rd1,
    rd2=>rd2,
    rd3=>rd3,
    rdout1=>rdout1,
    rdout2=>rdout2,
    rdout3=>rdout3,
    rdaddr1=>rdaddr1,
    rdaddr2=>rdaddr2,
    rdaddr3=>rdaddr3,
    wtaddr=>wtaddr,
    clk=>clk,

```



```
        rset_bar=>rset_bar
    );

alu: entity alu
    port map(
        clk=>clk,
        rs3=>rdout3,
        rs2=>rdout2,
        rs1=>rdout1,
        sg235=>sg235,
        rd=>wtin
    );

PipelineCore: entity pipelineCore
    port map(
        rset_bar=>rset_bar,
        clk=>clk,
        eod=>eod,
        loaddone=>loaddone,
        start => start,
        loadFinish => loadFinish, -- set , when instruction < 32 finished loading
        load=>load,
        insfetch=>insfetch,
        ID=>ID,
        rd1=>rd1,
        rd2=>rd2,
        rd3=>rd3,
        wt=>wt
    );
--probes
    eodo <= eod;
    opcode <= sg235(13 downto 10);
    r1addrp <= rdaddr1;
    r2addrp <= rdaddr2;
    r3addrp <= rdaddr3;
    r1value <= rdout1;
    r2value <= rdout2;
    r3value <= rdout3;
    writeaddr <= wtaddr;
    writevalue <= wtin;
    wtp <= wt;
end architecture;

pack:
```

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
package pack is
    signal status1: std_logic_vector(1 downto 0);
    signal wt1p: std_logic;
    signal status2: std_logic_vector(1 downto 0);
    signal wt2p:std_logic;
    signal status3: std_logic_vector(1 downto 0);
    signal wt3p: std_logic;
    signal wtp:std_logic;
    signal opcode: std_logic_vector(3 downto 0);
    signal r1addrp: std_logic_vector(4 downto 0);
    signal r2addrp: std_logic_vector(4 downto 0);
    signal r3addrp: std_logic_vector(4 downto 0);
    signal r1value: std_logic_vector(63 downto 0);
    signal r2value: std_logic_vector(63 downto 0);
    signal r3value: std_logic_vector(63 downto 0);
    signal writeaddr: std_logic_vector(4 downto 0);
    signal writevalue: std_logic_vector(63 downto 0);
    signal instructionp: std_logic_vector(23 downto 0);
end pack;

```

processor_tb:

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

```

```

library std;
use std.standard.all;
use STD.TEXTIO.ALL;

```

```

use pack.all;

```

```

entity processor_tb is
end processor_tb;

```

```

architecture tb of processor_tb is
    signal simulationend: std_logic := '0';
    signal start: std_logic;
    signal loadFinish: std_logic; -- set , when instruction < 32 finished loading
    signal rset_bar: std_logic;

```

```
signal clk:          std_logic := '0';
constant clk_period: time := 1 ns;
constant period : time := 1ns;
signal timecount : real := 0.0;
```

```
file file_VECTORS : text;
file file_RESULTS : text;
signal fileopen : std_logic := '0';
signal startwrite: std_logic := '0';
```

```
constant c_WIDTH : natural := 24;
signal instructionLoad: std_logic_vector(c_WIDTH-1 downto 0) := (others => '0');
signal eodo : std_logic := '0';
signal check: std_logic := '0';
signal checkout: std_logic_vector (63 downto 0);
```

```
type memory is array(0 to 31) of std_logic_vector(63 downto 0);
signal regfile : memory;
```

```
function chr(sl: std_logic) return character is
```

```
variable c: character;
```

```
begin
```

```
case sl is
```

```
when 'U' => c:= 'U';
```

```
when 'X' => c:= 'X';
```

```
when '0' => c:= '0';
```

```
when '1' => c:= '1';
```

```
when 'Z' => c:= 'Z';
```

```
when 'W' => c:= 'W';
```

```
when 'L' => c:= 'L';
```

```
when 'H' => c:= 'H';
```

```
when '-' => c:= '-';
```

```
end case;
```

```
return c;
```

```
end chr;
```

```
function str(slv: std_logic_vector) return string is
```

```
variable result : string (1 to slv'length);
```

```
variable r : integer;
```

```
begin
```

```

r := 1;
for i in slv'range loop
result(r) := chr(slv(i));
r := r + 1;
end loop;
return result;
end str;

begin

    target: entity Processor
        port map(
            eodo=>eodo,
            check=>check,
            checkout=>checkout,
            instructionLoad=>instructionLoad,
            start=>start,
            loadFinish=>loadFinish, -- set , when instruction < 32 finished loading
            clk=>clk,
            rset_bar=>rset_bar
        );

    --*****read file

go:process

    variable v_ILINE      : line;
    variable v_OLINE      : line;
    variable v_oppoInstruction : std_logic_vector(c_WIDTH-1 downto 0);
    variable v_Instruction : std_logic_vector(c_WIDTH-1 downto 0);

    begin
        wait until rset_bar = '1';
        file_open(file_VECTORS, "instruction.txt", read_mode);
        file_open(file_RESULTS, "output_results_Wu_Xu.txt", write_mode);
        fileopen<='1';

        start <= '0';
        wait for period;

        start <= '1';
        wait for period;

```

```

while not endfile(file_VECTORS) loop
    readline(file_VECTORS, v_ILINE);

    for i in v_ILINE'range loop
        v_oppolInstruction(i-1 downto i-1) :=
std_logic_vector(to_unsigned(character'pos(v_ILINE(i)),1));
    end loop;

    for i in v_oppolInstruction'range loop
        v_Instruction(23-i) := v_oppolInstruction(i);
    end loop;

    -- Pass the variable to a signal to allow the ripple-carry to use it
    instructionLoad <= v_Instruction;
    -- r_ADD_TERM2 <= v_ADD_TERM2;
    if start = '1' then
        start <= '0';
    end if;

    wait for period;

end loop;

loadFinish<= '1';
wait for period;
loadFinish<= '0';

file_close(file_VECTORS);

wait until eodo = '1';
wait for 5*period;

check <= '1';

for i in 0 to 31 loop
    wait for period/2;
    regfile(i) <= checkout;

end loop;
check<='0';

```

```

wait for period;
for i in 0 to 31 loop
    report "Register "&integer'image(i)&" value: "&str(regfile(i));
end loop;
write(v_OLINE,"Program execution result in Register file:");
writeline(file_RESULTS, v_OLINE);
for i in 0 to 31 loop
    write(v_OLINE,"Register "&integer'image(i)&" value: "&str(regfile(i)));
    writeline(file_RESULTS, v_OLINE);
end loop;

file_close(file_RESULTS);
fileopen<='0';

wait;
end process;

--
*****
****
writestart: process(status1, status2, status3)
begin
    if status1 = status2 and status1 = status3 and status2 = status3 then
        startwrite <= '0';
    else
        startwrite <= '1';
    end if;

end process;

track: process
variable v_OLINE      : line;
begin
    wait until startwrite = '1';
    loop
        wait for period/2;
        if fileopen = '1' then
            -- if ((status1 = "11" and wt1p = '0')) or ((status2 = "11" and wt2p = '0')) or ((status3 = "11"
and wt3p = '0')) then

                write(v_OLINE,"PERIOD: "&real'image(timecount)&" ns ");
                writeline(file_RESULTS, v_OLINE);

```

```
if status1 = "00" then
    write(v_OLINE,"Pipeline stage 1 status: Idle");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"waiting to start");
    writeline(file_RESULTS, v_OLINE);
elsif status1 = "01" then
    write(v_OLINE,"Pipeline stage 1 status: InsF");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"Exe result: ");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"next instruction fetched, will be decoded in next cycle");
    writeline(file_RESULTS, v_OLINE);
elsif status1 = "10" then
    write(v_OLINE,"Pipeline stage 1 status: InsD");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"Exe result: ");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"current instruction "&str(instructionp)&" decoded, generate
opcode and operands for next cycle");
    writeline(file_RESULTS, v_OLINE);
elsif status1 = "11" then
    write(v_OLINE,"Pipeline stage 1 status: Exe");
    writeline(file_RESULTS, v_OLINE);

    write(v_OLINE,"Exe result: ");
    writeline(file_RESULTS, v_OLINE);

    write(v_OLINE,"value: "&str(writevalue)&" wrote in address "&str(writeaddr));
    writeline(file_RESULTS, v_OLINE);
end if;
```

```
if status2 = "00" then
    write(v_OLINE,"Pipeline stage 2 status: Idle");
    writeline(file_RESULTS, v_OLINE);
    write(v_OLINE,"waiting to start");
    writeline(file_RESULTS, v_OLINE);
elsif status2 = "01" then
    write(v_OLINE,"Pipeline stage 2 status: InsF");
    writeline(file_RESULTS, v_OLINE);
```

```

        write(v_OLINE,"Exe result: ");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"next instruction fetched, will be decoded in next cycle");
        writeline(file_RESULTS, v_OLINE);
    elsif status2 = "10" then
        write(v_OLINE,"Pipeline stage 2 status: InsD");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"Exe result: ");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"current instruction "&str(instructionp)&" decoded, generate
opcode and oprands for next cycle");
        writeline(file_RESULTS, v_OLINE);
    elsif status2 = "11" then
        write(v_OLINE,"Pipeline stage 2 status: Exe");
        writeline(file_RESULTS, v_OLINE);

        write(v_OLINE,"Exe result: ");
        writeline(file_RESULTS, v_OLINE);

        write(v_OLINE,"value: "&str(writevalue)&" wrote in address "&str(writeaddr));
        writeline(file_RESULTS, v_OLINE);
    end if;

    if status3 = "00" then
        write(v_OLINE,"Pipeline stage 3 status: Idle");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"waiting to start");
        writeline(file_RESULTS, v_OLINE);
    elsif status3 = "01" then
        write(v_OLINE,"Pipeline stage 3 status: InsF");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"Exe result: ");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"next instruction fetched, will be decoded in next cycle");
        writeline(file_RESULTS, v_OLINE);
    elsif status3 = "10" then
        write(v_OLINE,"Pipeline stage 3 status: InsD");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"Exe result: ");
        writeline(file_RESULTS, v_OLINE);
        write(v_OLINE,"current instruction "&str(instructionp)&" decoded, generate
opcode and oprands for next cycle");

```



```
writeline(file_RESULTS, v_OLINE);
elsif status3 = "11" then
    write(v_OLINE, "Pipeline stage 3 status: Exe");
    writeline(file_RESULTS, v_OLINE);

    write(v_OLINE, "Exe result: ");
    writeline(file_RESULTS, v_OLINE);

    write(v_OLINE, "value: "&str(writevalue)&" wrote in address "&str(writeaddr));
    writeline(file_RESULTS, v_OLINE);
end if;

write(v_OLINE, "This cycle writing register? "&chr(wtp));
writeline(file_RESULTS, v_OLINE);

--instruction
write(v_OLINE, "current cycle instruction: "&str(instructionp));
writeline(file_RESULTS, v_OLINE);

--opcode
write(v_OLINE, "current cycle opcode: "&str(opcode));
writeline(file_RESULTS, v_OLINE);

--r1
write(v_OLINE, "current cycle Register Read 1 address: "&str(r1addrp));
writeline(file_RESULTS, v_OLINE);
write(v_OLINE, "current cycle Register Read 1 value: "&str(r1value));
writeline(file_RESULTS, v_OLINE);

--r2
write(v_OLINE, "current cycle Register Read 2 address: "&str(r2addrp));
writeline(file_RESULTS, v_OLINE);
write(v_OLINE, "current cycle Register Read 2 value: "&str(r2value));
writeline(file_RESULTS, v_OLINE);

--r3
write(v_OLINE, "current cycle Register Read 3 address: "&str(r3addrp));
writeline(file_RESULTS, v_OLINE);
write(v_OLINE, "current cycle Register Read 3 value: "&str(r3value));
writeline(file_RESULTS, v_OLINE);

--line brker
```

```

        write(v_OLINE,"*****");
        writeline(file_RESULTS, v_OLINE);
    --end if;
end if;
exit when startwrite = '0';
end loop;

    wait;
end process;

rset: process
    begin
        rset_bar <='0';
        wait until rising_edge(clk);
        wait until rising_edge(clk);
        rset_bar<='1';
        wait;
    end process;

clock: process
    begin
        clk <= '0';
        loop
            wait for period/2;
            clk <= not clk;
            timecount <= timecount + 0.5;
            exit when simulationend = '1';
        end loop;
        wait;
    end process;

end architecture;

```

Instruction convertor in python:

#Xiaomin Yuanchang

import sys

file_name = 'C:/Users/wxm/Desktop/input.txt'

file_input = open(file_name, "r")

output = ""

for line in file_input:

line=line.strip('\n')

tempList = line.split(",")

```
result = ""

if tempList[0] == "li":
    result = result + "1"
    temp = str(bin(int(tempList[1])))[2:]
    temp = temp.zfill(2)
    result = result + str(temp)
    temp = str(bin(int(tempList[2])))[2:]
    temp = temp.zfill(16)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output = output + result + '\n'
#     print (output)
#     #print (result)
if tempList[0] == "MA":
    result = result + "0100"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[4][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     # print (result)
if tempList[0] == "MS":
    result = result + "0101"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
```

```

        temp = str(bin(int(tempList[4][1:])))[2:]
        temp = temp.zfill(5)
        result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "l":
    result = result + "0110"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[4][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "h":
    result = result + "0111"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[4][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "bcw":
    result = result + "000000001"
    result = result + "00000"
    temp = str(bin(int(tempList[2][1:])))[2:]

```

```

        temp = temp.zfill(5)
        result = result + str(temp)
        temp = str(bin(int(tempList[3][1:])))[2:]
        temp = temp.zfill(5)
        result = result + str(temp)
    if tempList[0] == "nop":
        result = result + "000000000000000000000000"

# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "and":
    result = result + "000000010"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "or":
    result = result + "000000011"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "popcntn":
    result = result + "000000100"
    result = result + "00000"
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)

```

```

        result = result + str(temp)
        temp = str(bin(int(tempList[3][1:])))[2:]
        temp = temp.zfill(5)
        result = result + str(temp)
#   output =output + result + '\n'
#       print (output)
#       print (result)
if tempList[0] == "clz":
    result = result + "000000101"
    result = result + "00000"
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
#   output =output + result + '\n'
#       print (output)
#       print (result)
if tempList[0] == "rot":
    result = result + "000000110"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
#   output =output + result + '\n'
#       print (output)
#       print (result)
if tempList[0] == "shlhi":
    result = result + "000000111"
    temp = str(bin(int(tempList[1][0:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)

```

```

# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "a":
    result = result + "000001000"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "sfw":
    result = result + "000001001"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "ah":
    result = result + "000001010"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#     print (output)

```

```

#    print (result)
if tempList[0] == "sfh":
    result = result + "000001011"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
#    output =output + result + '\n'
#    print (output)
#    print (result)
if tempList[0] == "ahs":
    result = result + "000001100"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)

#    print (output)
#    print (result)
#    output =output + result + '\n'
if tempList[0] == "sfhs":
    result = result + "000001101"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output =output + result + '\n'
#    print (output)
#    print (result)

```



```
if tempList[0] == "mpyu":
    result = result + "000001110"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
# output = output + result + '\n'
#     print (output)
#     print (result)
if tempList[0] == "absdb":
    result = result + "000001111"
    temp = str(bin(int(tempList[1][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[2][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)
    temp = str(bin(int(tempList[3][1:])))[2:]
    temp = temp.zfill(5)
    result = result + str(temp)

output = output + result + '\n'

#     print (result)

def save(filename, contents):
    fh = open(filename, 'w')
    fh.write(contents)
    fh.close()
save('C:/My_Designs/ese345/ese345/instruction.txt', output)
```

Testing 1: matrix multiplication**Math principle:**

$$\begin{bmatrix} 4 & 7 \\ 3 & 6 \end{bmatrix} \times \begin{bmatrix} 8 & 10 \\ 9 & 11 \end{bmatrix} = \begin{bmatrix} 95 & 117 \\ 78 & 96 \end{bmatrix}$$

Handwritten diagram showing the calculation of matrix multiplication using registers. The registers are organized as follows:

- r_2 : $\begin{bmatrix} 4 & 7 \end{bmatrix}$
- r_3 : $\begin{bmatrix} 8 & 8 \end{bmatrix}$
- r_4 : $\begin{bmatrix} 10 & 10 \end{bmatrix}$
- r_0 : $\begin{bmatrix} 0 & 0 \end{bmatrix}$
- r_1 : $\begin{bmatrix} 0 & 0 \end{bmatrix}$
- r_5 : $\begin{bmatrix} 32 & 24 \end{bmatrix}$ (with 24 crossed out)
- r_6 : $\begin{bmatrix} 40 & 30 \end{bmatrix}$
- r_2 : $\begin{bmatrix} 7 & 6 \end{bmatrix}$
- r_3 : $\begin{bmatrix} 9 & 9 \end{bmatrix}$
- r_4 : $\begin{bmatrix} 11 & 11 \end{bmatrix}$
- r_7 : $\begin{bmatrix} 95 & 78 \end{bmatrix}$
- r_8 : $\begin{bmatrix} 117 & 96 \end{bmatrix}$

Arrows indicate the flow of data: r_2 and r_3 are used to calculate r_5 and r_6 . r_5 and r_6 are then used to calculate r_7 and r_8 . The final result matrix is shown as $\begin{bmatrix} 95 & 117 \\ 78 & 96 \end{bmatrix}$.

Codes load in:

li,1,0,r2	--clear second half word of r2
li,0,3,r2	--load 3 into first half word of r2
li,3,0,r2	--clear fourth (most left) half word of r2
li,2,4,r2	--load 4 into third half word of r2
li,0,8,r3	--load 8 into first half word of r3
li,1,0,r3	--load 0 into second half word of r3
bcw,r0,r3,r3	--bcw r3 right word to both left and right word
li,0,10,r4	--load 10 into first half word of r4
li,1,0,r4	--load 0 into second half word of r4
bcw,r0,r4,r4	--bcw r4 right word to both left and right word
MA,r2,r3,r0,r5	--multiply r2,r3 each word and add them on each word in r0 save r5
MA,r2,r4,r1,r6	--multiply r2,r4 each word and add them on each word in r1 save r6
li,2,7,r2	--load 7 into third HW of r2
li,1,0,r2	--load 0 into second HW of r2
li,0,6,r2	--load 6 into first HW of r2
li,3,0,r2	--load 0 into fourth HW of r2
li,0,9,r3	--load 9 into first HW of r3
li,1,0,r3	--load 0 into second HW of r3
bcw,r0,r3,r3	--bcw r3 right word to both left and right word
li,0,11,r4	--load 11 into first HW of r4
li,1,0,r4	--load 0 into second HW of r4
bcw,r0,r4,r4	--bcw r4 right word to both left and right word
MA,r2,r3,r5,r7	--multiply r2,r3 each word and add them on each word in r5 save r7
MA,r2,r4,r6,r8	--multiply r2,r4 each word and add them on each word in r6 save r8

Expected result:

R7 holds first column : 95d(5Fh) 78d(4Eh)

R8 holds second column : 117d(75h) 96d(60h)

Time sequence:

2.5ns:

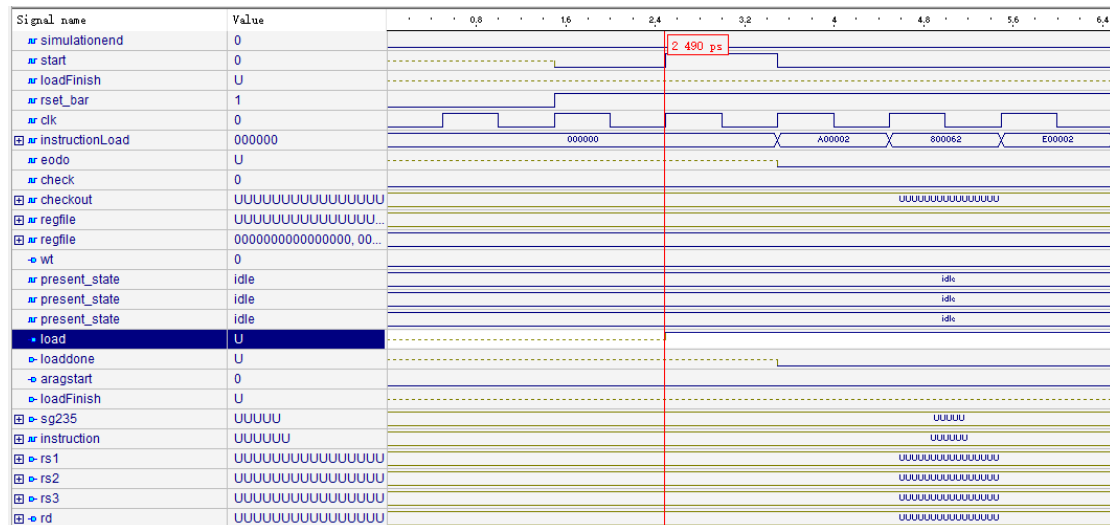
Start = '1' load = '1'

Pipeline1 = idle

Pipeline2 = idle

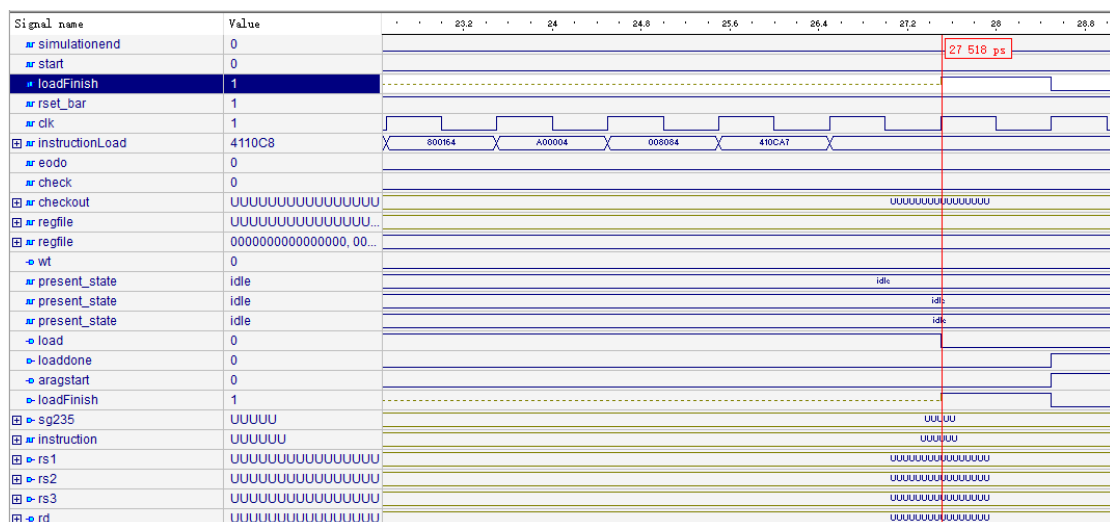
Pipeline3 = idle

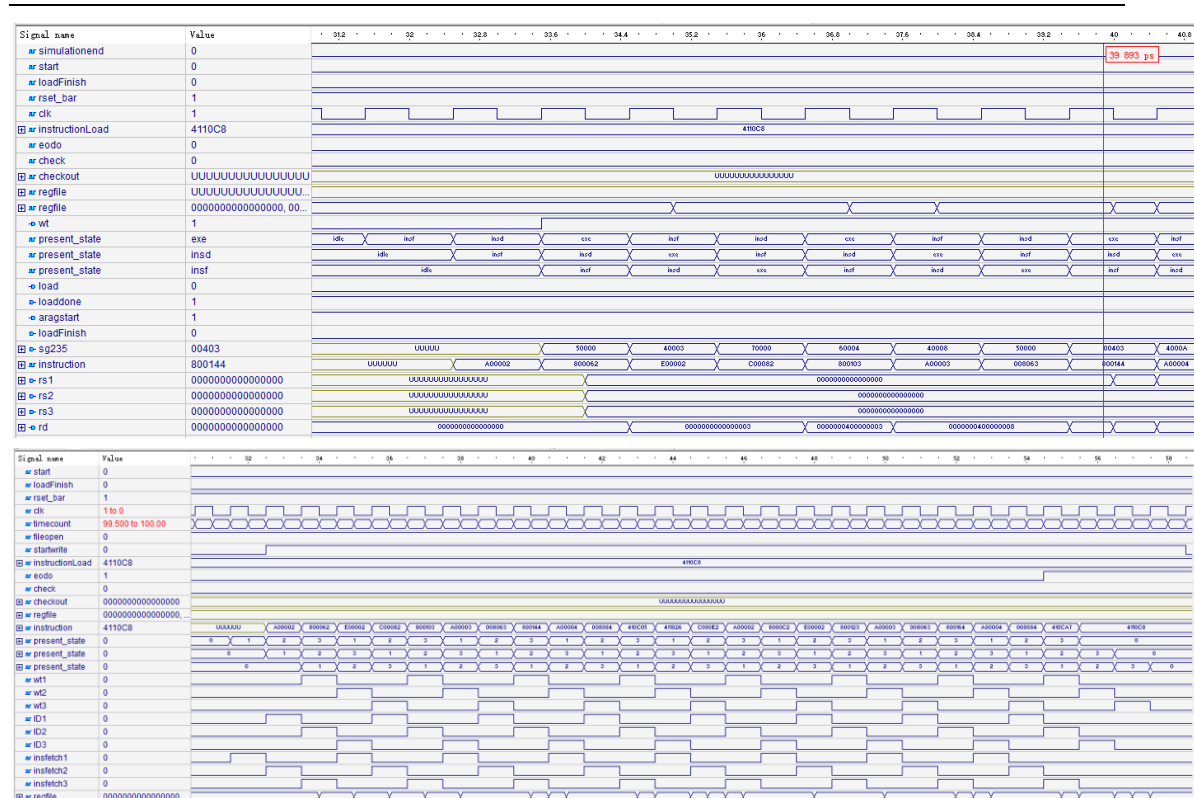
Instruction start loading into instruction buffer



27.5ns:

Instruction loading complete, start to sequencing pipeline





[illegible]

[illegible]

Exe result:

current instruction 11000000000000010000010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 11000000000000010000010

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.600000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000000UUUUUUUUUUUUUUUUUU000000000000000000000000000011

wrote in address 00010

Pipeline stage 3 status: InsD

Exe result:

current instruction 11000000000000010000010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 11000000000000010000010

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.650000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.750000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 10100000000000000000000011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 10100000000000000000000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.800000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 10100000000000000000000011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 10100000000000000000000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01000

current	cycle	Register	Read	1	value:
00					
current cycle Register Read 2 address: 00000					
current	cycle	Register	Read	2	value:
00					
current cycle Register Read 3 address: 00000					
current	cycle	Register	Read	3	value:
00					

PERIOD: 3.850000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000001100011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000001100011

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.900000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000001100011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000001100011

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.950000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 100000000000000101000100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 100000000000000101000100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.000000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 100000000000000101000100 decoded, generate opcode and oprands for next

address 00100

This cycle writing register? 1

current cycle instruction: 010000010000110000000101

current cycle opcode: 0001

current cycle Register Read 1 address: 00100

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.300000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 010000010000110000000101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00100

This cycle writing register? 1

current cycle instruction: 010000010000110000000101

current cycle opcode: 0001

current cycle Register Read 1 address: 00100

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.350000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00101

PERIOD: 4.450000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00000000000000000000000010000000000000000000000000000000000011000 wrote in address 00110

Pipeline stage 3 status: InsD

Exe result:

current instruction 110000000000000011100010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 110000000000000011100010

current cycle opcode: 0010

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00100

current	cycle	Register	Read	2	value:
0000000000000000000000000000100000000000000000000000000000001000					

current cycle Register Read 3 address: 00010

current	cycle	Register	Read	3	value:
00000000000000000000000000001000000000000000000000000000000011					

PERIOD: 4.500000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000000000000001010000000000000000000000000000000011110 wrote in address 00110

Pipeline stage 3 status: InsD

Exe result:

current instruction 110000000000000011100010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 110000000000000011100010

current cycle opcode: 0010

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00					

This cycle writing register? 1

current cycle instruction: 10100000000000000000000010

current cycle opcode: 0000

current cycle Register Read 1 address: 00111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.650000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00010

Pipeline stage 2 status: InsD

Exe result:

current instruction 1000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 1000

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.700000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00010

Pipeline stage 2 status: InsD

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.900000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 10000000000000100100011 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00010

This cycle writing register? 1

current cycle instruction: 10000000000000100100011

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 4.950000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 101000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 1010000000000000000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01001

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.000000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 101000000000000000000011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 101000000000000000000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01001

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.050000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in

Pipeline stage 1 status: InsD

Exe result:

current instruction 100000000000000101100100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 100000000000000101100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.200000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 100000000000000101100100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 100000000000000101100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle opcode: 0000

current cycle Register Read 1 address: 01011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.350000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00100

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000010000100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000010000100

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.400000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00100

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000010000100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000010000100

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.450000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 010000010000110010100111 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00 wrote in address 00100

This cycle writing register? 1

current cycle instruction: 010000010000110010100111

current cycle opcode: 0001

current cycle Register Read 1 address: 00100

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.500000e+001 ns

Pipeline stage 1 status: InsD

Register	22	value:
00		
Register	23	value:
00		
Register	24	value:
00		
Register	25	value:
00		
Register	26	value:
00		
Register	27	value:
00		
Register	28	value:
00		
Register	29	value:
00		
Register	30	value:
00		
Register	31	value:
00		

Conclusion:

Real result:

R7:

000000000000000000000000101111000000000000000000000000001001110

X	0000005F0000004E
---	------------------

R8:

000000000000000000000000111010100000000000000000000000001100000

X	0000007500000060
---	------------------

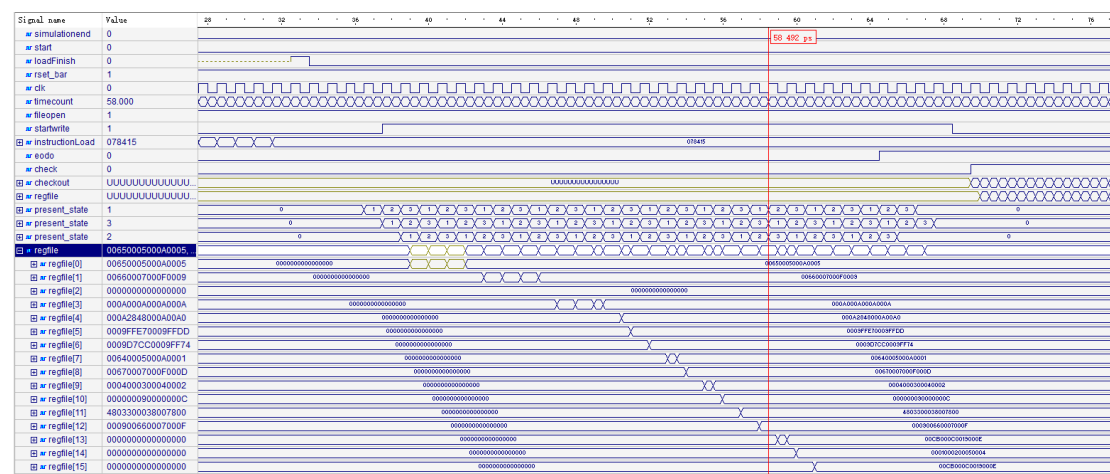
Result correct.

Testing 2, General operation testing:**Instruction loaded:**

```

li,1,10,r0
li,0,5,r0
li,3,101,r0
li,2,5,r0
li,1,15,r1
li,0,9,r1
li,3,102,r1
li,2,7,r1
li,1,10,r3
li,0,10,r3
bcw,r3,r3,r3
MS,r0,r1,r3,r4
l,r0,r1,r3,r5
h,r0,r1,r3,r6
and,r1,r0,r7
or,r1,r0,r8
popcnth,r0,r1,r9
clz,r0,r1,r10
rot,r0,r1,r11
shlhi,3,r1,r12
a,r0,r1,r13
sfw,r0,r1,r14
ah,r0,r1,r15
sfh,r0,r1,r16
ahs,r0,r1,r17
sfhs,r0,r1,r18
mpyu,r0,r1,r19
absdb,r0,r1,r20
absdb,r1,r0,r21

```



Printed running status and result:

[illegible]

[illegible]

PERIOD: 3.850000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 10000000000000010100000 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 1

```
current cycle instruction: 100000000000000010100000
```

```
current cycle opcode: 0000
```

current cycle Register Read 1 address: 01010

[illegible]

current cycle Register Read 2 address: 00000

[illegible]

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 3.900000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 100000000000000010100000 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 1

```
current cycle instruction: 1000000000000000010100000
```

current cycle opcode: 0000

current cycle Register Read 1 address: 01010

[illegible]

PERIOD: 3.950000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

[illegible]

wrote in address 00000

Pipeline stage 2 status: InsD

Exe result:

current instruction 111000000000110010100000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

```
current cycle instruction: 111000000000110010100000
```

current cycle opcode: 0000

current cycle Register Read 1 address: 00101

[illegible]

current cycle Register Read 2 address: 00000

[illegible]

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 4.000000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

[illegible]

wrote in address 00000

Pipeline stage 2 status: InsD

Exe result:

current instruction 111000000000110010100000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

PERIOD: 4.550000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000011001100000000000000111000000000001111000000000001001 wrote in address 00001

Pipeline stage 2 status: InsD

Exe result:

current instruction 10100000000000101000011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 10100000000000101000011

current cycle opcode: 0000

current cycle Register Read 1 address: 00111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
000000000110010100000000000001010000000000010100000000000000101					

PERIOD: 4.600000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000011001100000000000000111000000000001111000000000001001 wrote in address 00001

Pipeline stage 2 status: InsD

Exe result:

current instruction 10100000000000101000011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 10100000000000101000011

current cycle opcode: 0000

current cycle Register Read 1 address: 00111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.650000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000110011000000000000001110000000000001010000000000001001 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 100000000000000101000011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 100000000000000101000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01010

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.700000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000110011000000000000001110000000000001010000000000001001 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 100000000000000101000011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 100000000000000101000011

current cycle opcode: 0000

current cycle Register Read 1 address: 01010

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.750000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000000001000110001100011 decoded, generate opcode and operands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 000000000110011000000000000001110000000000001010000000000001010 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 000000001000110001100011

current cycle opcode: 0000

current cycle Register Read 1 address: 01010

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.800000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000000001000110001100011 decoded, generate opcode and operands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00000000011001100000000000000111000000000001010000000000001010 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 000000001000110001100011

current cycle opcode: 0000

current cycle Register Read 1 address: 01010

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.850000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 010100000000010001100100 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 010100000000010001100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00011

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
0000000001100101000000000000010100000000000010100000000000000101					

PERIOD: 4.900000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000000010100000000000001010000000000001010000000000001010 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 01010000000010001100100 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 01010000000010001100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000010100000000000001010					

current cycle Register Read 2 address: 00011

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000010100000000000001010					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
0000000001100110000000000000011100000000000011100000000000001001					

PERIOD: 4.950000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00100

Pipeline stage 3 status: InsD

Exe result:

current instruction 01100000000010001100101 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 01100000000010001100101

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000001100110000000000000011100000000000011110000000000001001					

PERIOD: 5.000000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000001010001010000100100000000000001010000000010100000 wrote in address 00100

Pipeline stage 3 status: InsD

Exe result:

current instruction 01100000000010001100101 decoded, generate opcode and operands for next cycle

This cycle writing register? 1

current cycle instruction: 01100000000010001100101

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
0000000000010100000000000001010000000000001010000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
000000000110011000000000000001110000000000011110000000000001001					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00000000011001010000000000000101000000000001010000000000000101					

PERIOD: 5.050000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 01110000000010001100110 decoded, generate opcode and operands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 000000000001001111111111100111000000000001001111111111011101 wrote in address 00101

This cycle writing register? 1

current cycle instruction: 01110000000010001100110

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
000000000000	1010000000000000	0101000000000000	1010000000000000	1010	

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
00000000011001	1000000000000000	0111000000000000	1111000000000000	1001	

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00000000011001	1010000000000000	0101000000000000	1010000000000000	101	

PERIOD: 5.100000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 01110000000010001100110 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000000010011111111111001110000000000100111111111011101 wrote in address 00101

This cycle writing register? 1

current cycle instruction: 01110000000010001100110

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
000000000000	1010000000000000	0101000000000000	1010000000000000	1010	

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
00000000011001	1000000000000000	0111000000000000	1111000000000000	1001	

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
00000000011001	1010000000000000	0101000000000000	1010000000000000	101	

PERIOD: 5.150000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000001001110101111100110000000000010011111111101110100 wrote in address 00110

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000010000010000000111 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000010000010000000111

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
00000000110011000000000000001110000000000011110000000000001001					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000011001010000000000000101000000000001010000000000000101					

PERIOD: 5.200000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001001110101111100110000000000001001111111101110100 wrote in address 00110

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000010000010000000111 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000010000010000000111

current cycle opcode: 0000

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
00000000110011000000000000001110000000000011110000000000001001					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
0000000011001010000000000000101000000000001010000000000000101					

PERIOD: 5.250000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00000000000001000000000000001000000000000100000000000001000 wrote in address 00111

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000011000010000001000 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000011000010000001000

current cycle opcode: 0010

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00000000000010100000000000001010000000000001010000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
000000000110011000000000000001110000000000011110000000000001001					

current cycle Register Read 3 address: 00010

current	cycle	Register	Read	3	value:
000000000110010100000000000001010000000000010100000000000000101					

PERIOD: 5.300000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000001100100000000000000010100000000000101000000000000001 wrote in address 00111

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000011000010000001000 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000011000010000001000

current cycle opcode: 0010

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
000000000110010100000000000001010000000000010100000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:

0000000001100110000000000000011100000000000011110000000000001001

current cycle Register Read 3 address: 00010

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.350000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000000100000000000101001 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000001100111000000000000011100000000000011110000000000001101 wrote in address 01000

This cycle writing register? 1

current cycle instruction: 000000100000000000101001

current cycle opcode: 0011

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 3 address: 00011

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.400000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000000100000000000101001 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000001100111000000000000011100000000000011110000000000001101 wrote in address 01000

This cycle writing register? 1

current cycle instruction: 000000100000000000101001

current cycle opcode: 0011

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
000000000110010100000000000001010000000000000101000000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000001111000000000000001001					

current cycle Register Read 3 address: 00011

current	cycle	Register	Read	3	value:
0000000000001010000000000000010100000000000001010000000000000001010					

PERIOD: 5.450000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001000000000000000010000000000000010000000000000010 wrote in address 01001

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000101000000000101010 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000101000000000101010

current cycle opcode: 0100

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
000000000110010100000000000001010000000000000101000000000000000101					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000001111000000000000001001					

current cycle Register Read 3 address: 00100

current	cycle	Register	Read	3	value:
0000000000001010000000000000010100000000000001010000000000000001010					

PERIOD: 5.500000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001000000000000000011000000000000010000000000000010 wrote in address 01001

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000101000000000101010 decoded, generate opcode and oprands for next

cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000101000000000101010

current cycle opcode: 0100

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 00100

current	cycle	Register	Read	3	value:
00000000000101000101000010010000000000000010100000000010100000					

PERIOD: 5.550000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000000000000000000000001001000000000000000000000000001100 wrote in address 01010

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000110000000000101011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000110000000000101011

current cycle opcode: 0101

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 00101

current	cycle	Register	Read	3	value:
00000000000101000101000010010000000000000010100000000010100000					

PERIOD: 5.600000e+001 ns

Pipeline stage 1 status: InsF

[illegible]

current cycle Register Read 3 address: 00110

current	cycle	Register	Read	3	value:
0000000000001001111111111100111000000000001001111111111011101					

PERIOD: 5.700000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000000111000110000101100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 010010000000001100110000000000001110000000000011110000000000 wrote in address 01011

This cycle writing register? 1

current cycle instruction: 000000111000110000101100

current cycle opcode: 0110

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 00110

current	cycle	Register	Read	3	value:
000000000000100111010111110011000000000000010011111111101110100					

PERIOD: 5.750000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000000010010000000001100110000000000000111000000000001111 wrote in address 01100

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001000000000000101101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001000000000000101101

current cycle opcode: 0111

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00011

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 00111

current	cycle	Register	Read	3	value:
000000000000100111010111110011000000000000010011111111101110100					

PERIOD: 5.800000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000000100100000000011001100000000000001110000000000001111 wrote in address 01100

Pipeline stage 2 status: InsD

Exe result:

current instruction 0000010000000000000101101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 0000010000000000000101101

current cycle opcode: 0111

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00011

current	cycle	Register	Read	2	value:
0000000000001010000000000000010100000000000010100000000000001010					

current cycle Register Read 3 address: 00111

current	cycle	Register	Read	3	value:
0000000001100100000000000000010100000000000010100000000000000001					

PERIOD: 5.850000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000001110000000000000001000100000000000110010000000000010011 wrote in address 01101

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001001000000000101110 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001001000000000101110

current cycle opcode: 1000

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00000000000010100000000000000010100000000000001010000000000001010					

current cycle Register Read 3 address: 01000

current	cycle	Register	Read	3	value:
00000000011001000000000000000010100000000000010100000000000000001					

PERIOD: 5.900000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00000000110010110000000000000110000000000000110010000000000001110 wrote in address 01101

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001001000000000101110 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001001000000000101110

current cycle opcode: 1000

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00000000011001010000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 01000

current	cycle	Register	Read	3	value:
00000000011001110000000000000011100000000000011110000000000001101					

PERIOD: 5.950000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001010000000000101111 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 01110

This cycle writing register? 1

current cycle instruction: 000001010000000000101111

current cycle opcode: 1001

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 01001

current	cycle	Register	Read	3	value:
0000000001100111000000000000011100000000000011110000000000001101					

PERIOD: 6.000000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001010000000000101111 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 01110

This cycle writing register? 1

current cycle instruction: 000001010000000000101111

current cycle opcode: 1001

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 01001

current	cycle	Register	Read	3	value:
00000000000001000000000000000110000000000001000000000000000010					

PERIOD: 6.050000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000001100101100000000000011000000000000110010000000000001110 wrote in address 01111

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001011000000000110000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001011000000000110000

current cycle opcode: 1010

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000010100000000000000101					

current cycle Register Read 3 address: 01010

current	cycle	Register	Read	3	value:
00000000000001000000000000000110000000000001000000000000000010					

PERIOD: 6.100000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000001100101100000000000011000000000000110010000000000001110 wrote in address 01111

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001011000000000110000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001011000000000110000

current cycle opcode: 1010

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					
current cycle Register Read 2 address: 00000					
current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					
current cycle Register Read 3 address: 01010					
current	cycle	Register	Read	3	value:
0000000000000000000000000000010010000000000000000000000000001100					

PERIOD: 6.150000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 10000

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001100000000000110001 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001100000000000110001

current cycle opcode: 1011

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					
current cycle Register Read 2 address: 00000					
current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					
current cycle Register Read 3 address: 01011					
current	cycle	Register	Read	3	value:
0000000000000000000000000000010010000000000000000000000000001100					

PERIOD: 6.200000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 10000

Pipeline stage 3 status: InsD

Exe result:

current instruction 0000011000000000000110001 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 0000011000000000000110001

current cycle opcode: 1011

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000111000000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000001010000000000000101					

current cycle Register Read 3 address: 01011

current	cycle	Register	Read	3	value:
01001000000000110011000000000000011100000000000111100000000000					

PERIOD: 6.250000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001101000000000110010 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00000000110010110000000000001100000000000011001000000000001110 wrote in address 10001

This cycle writing register? 1

current cycle instruction: 000001101000000000110010

current cycle opcode: 1100

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000111000000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000010100000000000001010000000000000101					

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
01001000000000110011000000000000011100000000000111100000000000					

PERIOD: 6.300000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001101000000000110010 decoded, generate opcode and oprands for next

cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 000000001100101100000000000011000000000000110010000000000001110 wrote in address 10001

This cycle writing register? 1

current cycle instruction: 000001101000000000110010

current cycle opcode: 1100

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
0000000000001001000000000110011000000000000001110000000000001111					

PERIOD: 6.350000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000000000100000000000000100000000000001010000000000000100 wrote in address 10010

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001110000000000110011 decoded, generate opcode and operands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001110000000000110011

current cycle opcode: 1101

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
0000000001100101000000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:

0000000000001001000000000110011000000000000001110000000000001111

PERIOD: 6.400000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000000000010000000000000100000000000001010000000000000100 wrote in address 10010

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001110000000000110011 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001110000000000110011

current cycle opcode: 1101

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

00000000011001100000000000000111000000000000111100000000000001001

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

0000000001100101000000000000010100000000000010100000000000000101

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

000000001100101100000000000011000000000000110010000000000001110

PERIOD: 6.450000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00000000000000000000000001000110000000000000000000000000101101 wrote in address 10011

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001111000000000110100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001111000000000110100

current cycle opcode: 1110

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

00000000011001100000000000000111000000000000011110000000000001001

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

00000000011001010000000000000101000000000000010100000000000000101

current cycle Register Read 3 address: 01110

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

000000000110010110000000000001100000000000000110010000000000001110

PERIOD: 6.500000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00000000000000000000000001000110000000000000000000000000101101 wrote in address 10011

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001111000000000110100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001111000000000110100

current cycle opcode: 1110

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

00000000011001100000000000000111000000000000011110000000000001001

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

00000000011001010000000000000101000000000000010100000000000000101

current cycle Register Read 3 address: 01110

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

0000000000000001000000000000001000000000000001010000000000000100

PERIOD: 6.550000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001111000010000010101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 00000000000000010000000000000100000000000001010000000000000100 wrote in

address 10100

This cycle writing register? 1

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000000111100000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000000101000000000000010100000000000000101					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
0000000000000001000000000000001000000000000001010000000000000100					

PERIOD: 6.600000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001111000010000010101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 0000000000000001000000000000001000000000000001010000000000000100 wrote in address 10100

This cycle writing register? 1

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
00000000011001100000000000000011100000000000000111100000000000001001					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
000000000110010100000000000000101000000000000010100000000000000101					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
00000000110010110000000000000011000000000000001100100000000000001110					

PERIOD: 6.650000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000000001000000000000001000000000000001010000000000000100 wrote in address 10101

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001111000010000010101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 1

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
000000001100101100000000000011000000000000110010000000000001110					

PERIOD: 6.700000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000000000100000000000001000000000000101000000000000100 wrote in address 10101

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001111000010000010101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 1

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
000000000110010100000000000001010000000000001010000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
000000001100101100000000000011000000000000110010000000000001110					

PERIOD: 6.750000e+001 ns

Pipeline stage 1 status: Idle

waiting to start

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 10101

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00000000011001010000000000000101000000000000010100000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
000000001100101100000000000011000000000000110010000000000001110					

PERIOD: 6.800000e+001 ns

Pipeline stage 1 status: Idle

waiting to start

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000000001000000000000010000000000000101000000000000100 wrote in address 10101

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
00000000011001010000000000000101000000000000010100000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
000000001100101100000000000011000000000000110010000000000001110					

PERIOD: 6.850000e+001 ns

Pipeline stage 1 status: Idle

waiting to start

Pipeline stage 2 status: Idle

waiting to start

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001111000010000010101

current cycle opcode: 1111

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
0000000001100101000000000000010100000000000001010000000000000101					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
0000000001100110000000000000011100000000000011110000000000001001					

current cycle Register Read 3 address: 01111

current	cycle	Register	Read	3	value:
000000001100101100000000000011000000000000110010000000000001110					

Program execution result in Register file:

Register 0 value: 0000000001100101000000000000010100000000000001010000000000000101

Register 1 value: 0000000001100110000000000000011100000000000011110000000000001001

Register 2 value: 00

Register 3 value: 0000000000001010000000000000101000000000000010100000000000001010

Register 4 value: 0000000000001010001010000100100000000000000010100000000010100000

Register 5 value: 0000000000001001111111111100111000000000001001111111111011101

Register 6 value: 0000000000001001110101111001100000000000001001111111101110100

Register 7 value: 00000000011001000000000000001010000000000010100000000000000001

Register 8 value: 00000000011001110000000000001110000000000011110000000000001101

Register 9 value: 00000000000001000000000000001100000000000010000000000000000010

Register	10	value:
00000000000000000000000000001001000000000000000000000000000001100		

Register	11	value:
0100100000000011001100000000000011100000000000111100000000000		

Register	12	value:
00000000000010010000000001100110000000000001110000000000001111		

Register	13	value:
00000000110010110000000000011000000000000110010000000000001110		

Register	14	value:
00000000000000001000000000000100000000000001010000000000000100		

Register	15	value:
00000000110010110000000000011000000000000110010000000000001110		

Register	16	value:
00000000000000001000000000000100000000000001010000000000000100		

Register	17	value:
00000000110010110000000000001100000000000011001000000000001110		
Register	18	value:
000000000000000010000000000000100000000000001010000000000000100		
Register	19	value:
000000000000000000000000000010001100000000000000000000000000101101		
Register	20	value:
00000000000000001000000000000010000000000000010100000000000000100		
Register	21	value:
00000000000000001000000000000010000000000000010100000000000000100		
Register	22	value:
00		
Register	23	value:
00		
Register	24	value:
00		
Register	25	value:
00		
Register	26	value:
00		
Register	27	value:
00		
Register	28	value:
00		
Register	29	value:
00		
Register	30	value:
00		
Register	31	value:
00		

Conclusion:

Signal name	Value	39.2	10
regfile	00650005000A0005, ...		
regfile[0]	00650005000A0005	00650005000A0005	
regfile[1]	00660007000F0009	00660007000F0009	
regfile[2]	0000000000000000	0000000000000000	
regfile[3]	000A000A000A000A	000A000A000A000A	
regfile[4]	000A2848000A00A0	000A2848000A00A0	
regfile[5]	0009FFE70009FFDD	0009FFE70009FFDD	
regfile[6]	0009D7CC0009FF74	0009D7CC0009FF74	
regfile[7]	00640005000A0001	00640005000A0001	
regfile[8]	00670007000F000D	00670007000F000D	
regfile[9]	0004000300040002	0004000300040002	
regfile[10]	000000090000000C	000000090000000C	
regfile[11]	4803300038007800	4803300038007800	
regfile[12]	000900660007000F	000900660007000F	
regfile[13]	00CB000C0019000E	00CB000C0019000E	
regfile[14]	0001000200050004	0001000200050004	
regfile[15]	00CB000C0019000E	00CB000C0019000E	
regfile[16]	0001000200050004	0001000200050004	
regfile[17]	00CB000C0019000E	00CB000C0019000E	
regfile[18]	0001000200050004	0001000200050004	
regfile[19]	000000230000002D	000000230000002D	
regfile[20]	0001000200050004	0001000200050004	
regfile[21]	0001000200050004	0001000200050004	
regfile[22]	0000000000000000	0000000000000000	
regfile[23]	0000000000000000	0000000000000000	
regfile[24]	0000000000000000	0000000000000000	
regfile[25]	0000000000000000	0000000000000000	
regfile[26]	0000000000000000	0000000000000000	
regfile[27]	0000000000000000	0000000000000000	
regfile[28]	0000000000000000	0000000000000000	
regfile[29]	0000000000000000	0000000000000000	
regfile[30]	0000000000000000	0000000000000000	
regfile[31]	0000000000000000	0000000000000000	

```

li, 1, 10, r0
li, 0, 5, r0
li, 3, 101, r0
li, 2, 5, r0
li, 1, 15, r1
li, 0, 9, r1
li, 3, 102, r1
li, 2, 7, r1
li, 1, 10, r3
li, 0, 10, r3
bcw, , r3, r3
MS, r0, r1, r3, r4
l, r0, r1, r3, r5
h, r0, r1, r3, r6
and, r1, r0, r7
or, r1, r0, r8
popcnt, , r1, r9
clz, , r1, r10
rot, r0, r1, r11
shlhi, 3, r1, r12
a, r0, r1, r13
sfw, r0, r1, r14
ah, r0, r1, r15
sfh, r0, r1, r16
ahs, r0, r1, r17
sfhs, r0, r1, r18
mpyu, r0, r1, r19
absdb, r0, r1, r20
absdb, r1, r0, r21

```

Comparing the register value result in hex with the input instructions, all instruction results are correct. R20 r21 shows the function of absdb, which is giving the absolute difference of two register's half words.

[illegible]

[illegible]

[illegible]

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 11 wrote in address 00001

This cycle writing register? 1

current cycle instruction: 1001111111111111100001

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.800000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 1001111111111111100001 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 11 wrote in address 00001

This cycle writing register? 1

current cycle instruction: 1001111111111111100001

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.850000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 11 wrote in address 00001

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000001000000000100001 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000000100001

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.900000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 11 wrote in address 00001

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000001000000000100001 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000000100001

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

[illegible]

current cycle Register Read 3 address: 1111

[illegible]

PERIOD: 3.950000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

[illegible]

Pipeline stage 3 status: InsD

Exe result:

current instruction 101000000000000101000010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

```
current cycle instruction: 101000000000000101000010
```

current cycle opcode: 0001

current cycle Register Read 1 address: 00001

[illegible]

current cycle Register Read 2 address: 00000

[illegible]

current cycle Register Read 3 address: 00001

[illegible]

PERIOD: 4.000000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

[illegible]

Pipeline stage 3 status: InsD

Exe result:

current instruction 101000000000000101000010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

[illegible]

[illegible]

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

[illegible]

PERIOD: 4.300000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

```
value: 00000000000010100000000000001010000000000001010000000000001010 wrote in
address 00010
```

Pipeline stage 3 status: InsD

Exe result:

current instruction 01000000000010001000011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

```
current cycle instruction: 010000000000010001000011
```

current cycle opcode: 0001

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

[illegible]

PERIOD: 4.350000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 01010000000010001000100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

[illegible]

This cycle writing register? 1

current cycle instruction: 010100000000010001000100

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.400000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 010100000000010001000100 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 000000000000101000000000000010110000000000001010000000000001011 wrote in address 00011

This cycle writing register? 1

current cycle instruction: 010100000000010001000100

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.450000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000000101000000000000010110000000000001010000000000001011 wrote in address 00100

Pipeline stage 2 status: InsD

Exe result:

current instruction 011000000000010001000101 decoded, generate opcode and oprands for next

cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 01100000000010001000101

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00000000000010100000000000001010000000000001010000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.500000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 00000000000010100000000000001011000000000001010000000000001011 wrote in address 00100

Pipeline stage 2 status: InsD

Exe result:

current instruction 01100000000010001000101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 01100000000010001000101

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00000000000010100000000000001010000000000001010000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.550000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000000101000000000000010010000000000001010000000000001001 wrote in address 00101

Pipeline stage 3 status: InsD

Exe result:

current instruction 011100000000010001000110 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 011100000000010001000110

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

0000000000001010000000000000101000000000000010100000000000001010					
--	--	--	--	--	--

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

11					
--	--	--	--	--	--

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

11					
--	--	--	--	--	--

PERIOD: 4.600000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 000000000000101000000000000010010000000000001010000000000001001 wrote in address 00101

Pipeline stage 3 status: InsD

Exe result:

current instruction 011100000000010001000110 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 011100000000010001000110

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

0000000000001010000000000000101000000000000010100000000000001010					
--	--	--	--	--	--

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

11					
--	--	--	--	--	--

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 4.650000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 1011000000000000000111 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

```
value: 0000000000001010000000000001001000000000001010000000000001001 wrote in
address 00110
```

This cycle writing register? 1

```
current cycle instruction: 1011000000000000000000111
```

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
000000000000101000000000000010100000000000010100000000000001010					

current cycle Register Read 2 address: 00001

[illegible]

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 4.700000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 1011000000000000000111 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

```
value: 000000000000101000000000000010010000000000001010000000000001001 wrote in
address 00110
```

This cycle writing register? 1

```
current cycle instruction: 1011000000000000000000111
```

current cycle opcode: 0000

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00001

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.750000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000000101000000000000010011000000000000000000000000001001 wrote in address 00111

Pipeline stage 2 status: InsD

Exe result:

current instruction 10010000000000000000111 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 10010000000000000000111

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 00000

current	cycle	Register	Read	3	value:
11					

PERIOD: 4.800000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 000000000000101000000000000010011000000000000000000000000001001 wrote in address 00111

Pipeline stage 2 status: InsD

Exe result:

current instruction 10010000000000000000111 decoded, generate opcode and oprands for next cycle


```

next instruction fetched, will be decoded in next cycle
Pipeline stage 2 status: Exe
Exe result:
value: 00000000000010100000000000001001100000000000000100000000000000 wrote in
address 00111
Pipeline stage 3 status: InsD
Exe result:
current instruction 000000001000000011100111 decoded, generate opcode and oprands for next
cycle
This cycle writing register? 1
current cycle instruction: 000000001000000011100111
current cycle opcode: 0000
current cycle Register Read 1 address: 00000
current          cycle          Register          Read           1             value:
111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
current cycle Register Read 2 address: 00000
current          cycle          Register          Read           2             value:
111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
current cycle Register Read 3 address: 00000
current          cycle          Register          Read           3             value:
111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
*****
PERIOD: 4.950000e+001 ns
Pipeline stage 1 status: InsD
Exe result:
current instruction 101011111111111111101000 decoded, generate opcode and oprands for next
cycle
Pipeline stage 2 status: InsF
Exe result:
next instruction fetched, will be decoded in next cycle
Pipeline stage 3 status: Exe
Exe result:
value: 111111111111111111111111111111111111111111111111111111111111111111111111111111111111111 wrote in
address 00111
This cycle writing register? 1
current cycle instruction: 101011111111111111101000
current cycle opcode: 0001
current cycle Register Read 1 address: 00111
current          cycle          Register          Read           1             value:
111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
current cycle Register Read 2 address: 00000
current          cycle          Register          Read           2             value:
111111111111111111111111111111111111111111111111111111111111111111111111111111111111111
current cycle Register Read 3 address: 00001

```


[illegible]

PERIOD: 5.100000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

```
value: 100000000000000010000000000000011111111111110000000000000 wrote in
address 01000
```

Pipeline stage 2 status: InsD

Exe result:

current instruction 100011111111111101000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 1000111111111111101000

current cycle opcode: 1111

current cycle Register Read 1 address: 1111

[illegible]

current cycle Register Read 2 address: 1111

[illegible]

current cycle Register Read 3 address: 11111

[illegible]

PERIOD: 5.150000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

```
value: 1000000000000000100000000000000011111111111101111111111111 wrote in
address 01000
```

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000100001000 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000100001000

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.200000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 10000000000000001000000000000001111111111111011111111111111 wrote in address 01000

Pipeline stage 3 status: InsD

Exe result:

current instruction 000000001000000100001000 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000100001000

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 5.250000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001100010000001001001 decoded, generate opcode and oprands for next


```

cycle
Pipeline stage 2 status: InsF
Exe result:
next instruction fetched, will be decoded in next cycle
Pipeline stage 3 status: Exe
Exe result:
value: 0000000000000000000000000000000000000000000000000000000000000000 wrote in
address 01000
This cycle writing register? 1
current cycle instruction: 000001100010000001001001
current cycle opcode: 0001
current cycle Register Read 1 address: 01000
current          cycle          Register          Read          1          value:
0000000000000000000000000000000000000000000000000000000000000000
current cycle Register Read 2 address: 00000
current          cycle          Register          Read          2          value:
0000000000000000000000000000000000000000000000000000000000000000
current cycle Register Read 3 address: 00001
current          cycle          Register          Read          3          value:
0000000000000000000000000000000000000000000000000000000000000000
*****
PERIOD: 5.300000e+001 ns
Pipeline stage 1 status: InsD
Exe result:
current instruction 000001100010000001001001 decoded, generate opcode and oprands for next
cycle
Pipeline stage 2 status: InsF
Exe result:
next instruction fetched, will be decoded in next cycle
Pipeline stage 3 status: Exe
Exe result:
value: 0111111111111111101111111111111110111111111111110111111111111111 wrote in
address 01000
This cycle writing register? 1
current cycle instruction: 000001100010000001001001
current cycle opcode: 0001
current cycle Register Read 1 address: 01000
current          cycle          Register          Read          1          value:
1000000000000000010000000000000001111111111111110111111111111111
current cycle Register Read 2 address: 00000
current          cycle          Register          Read          2          value:
1111111111111111111111111111111111111111111111111111111111111111
current cycle Register Read 3 address: 00001
current          cycle          Register          Read          3          value:

```

[illegible]

PERIOD: 5.350000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

[illegible]

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001101000100011101010 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001101000100011101010

```
current cycle opcode: 1100
```

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 2 address: 01000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

[illegible]

PERIOD: 5.400000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

```
value: 0111111111111101111111111111011111111111101111111111111 wrote in
address 01001
```

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001101000100011101010 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001101000100011101010

current cycle opcode: 1100

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

0000000000001010000000000000101000000000000010100000000000001010

current cycle Register Read 2 address: 01000

current	cycle	Register	Read	2	value:
0111111111111111	1011111111111111	1011111111111111	1011111111111111	1011111111111111	

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	

PERIOD: 5.450000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 10000000000010111000000000001011100000000001011100000000001011 wrote in address 01010

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001101001110001001011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001101001110001001011

current cycle opcode: 1101

current cycle Register Read 1 address: 00111

current	cycle	Register	Read	1	value:
0000000000001010	0000000000000000	1010000000000000	1010000000000000	1010000000000000	

current cycle Register Read 2 address: 00010

current	cycle	Register	Read	2	value:
0111111111111111	1011111111111111	1011111111111111	1011111111111111	1011111111111111	

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000000000	0000000000000000	0000000000000000	0000000000000000	0000000000000000	

PERIOD: 5.500000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 100000000000000010000000000000100000000000001000000000000000 wrote in address 01010

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001101001110001001011 decoded, generate opcode and oprands for next

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

value: 011111111111111101111111111111110111111111111111101111111111111111 wrote in address 01011

This cycle writing register? 1

current cycle instruction: 000001100000000001001100

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00111

current	cycle	Register	Read	2	value:
1000000000000001000000000000001000000000000001000000000000000					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
000					

PERIOD: 5.650000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 10000000000001010100000000000101010000000000010101000000000001010 wrote in address 01100

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001101000000001001101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001101000000001001101

current cycle opcode: 1100

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
1000000000000001000000000000001000000000000001000000000000000					

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
000					

PERIOD: 5.700000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001001000000000000100100000000000010010000000000001001 wrote in address 01100

Pipeline stage 2 status: InsD

Exe result:

current instruction 000001101000000001001101 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000001101000000001001101

current cycle opcode: 1100

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
000000000000	10	100000000000	0000	1010000000000000	1010

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
111111111111	11	111111111111	1111	111111111111	1111

current cycle Register Read 3 address: 01100

current	cycle	Register	Read	3	value:
000000000000	00	000000000000	0000	000000000000	0000

PERIOD: 5.750000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 0000000000001011000000000000101100000000000010110000000000001011 wrote in address 01101

Pipeline stage 3 status: InsD

Exe result:

current instruction 000001101000000001001101 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
000000000000	10	100000000000	0000	1010000000000000	1010

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000001011000000000000101100000000000010110000000000001011					

PERIOD: 5.900000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 000001101000000001001101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: Idle

waiting to start

Pipeline stage 3 status: Exe

Exe result:

value: 0000000000001011000000000000101100000000000010110000000000001011 wrote in address 01101

This cycle writing register? 1

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000001011000000000000101100000000000010110000000000001011					

PERIOD: 5.950000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001011000000000000101100000000000010110000000000001011 wrote in address 01101

Pipeline stage 2 status: Idle

waiting to start

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
00000000000010100000000000010100000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000001011000000000000101100000000000010110000000000001011					

PERIOD: 6.000000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000001011000000000000101100000000000010110000000000001011 wrote in address 01101

Pipeline stage 2 status: Idle

waiting to start

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000001011000000000000101100000000000010110000000000001011					

PERIOD: 6.050000e+001 ns

Pipeline stage 1 status: Idle

waiting to start

Pipeline stage 2 status: Idle

waiting to start

Pipeline stage 3 status: Idle

waiting to start

This cycle writing register? 0

current cycle instruction: 000001101000000001001101

current cycle opcode: 1101

current cycle Register Read 1 address: 00010

current	cycle	Register	Read	1	value:
0000000000001010000000000000101000000000000010100000000000001010					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
11					

current cycle Register Read 3 address: 01101

current	cycle	Register	Read	3	value:
0000000000001011000000000000101100000000000010110000000000001011					

Program execution result in Register file:

Register 0 value: 11

Register 1 value: 11

Register 2 value: 0000000000001010000000000000101000000000000010100000000000001010

Register 3 value: 0000000000001010000000000000101100000000000010100000000000001011

Register 4 value: 0000000000001010000000000000101100000000000010100000000000001011

Register 5 value: 0000000000001010000000000000100100000000000010100000000000001001

Register 6 value: 0000000000001010000000000000100100000000000010100000000000001001

Register 7 value: 1000000000000000100000000000000010000000000000010000000000000000

Register 8 value: 01111111111111011111111111110111111111111011111111111101111111111111

Register 9 value: 01111111111111011111111111110111111111111011111111111101111111111111

Register	10	value:
1000000000000000100000000000000010000000000000010000000000000000		

Register	11	value:
01111111111111011111111111110111111111111011111111111101111111111111		

Register	12	value:
0000000000001001000000000000100100000000000010010000000000001001		

Register	13	value:
0000000000001011000000000000101100000000000010110000000000001011		

Register	14	value:
00		

Register	15	value:
00		

Register	16	value:
00		

Register	17	value:
00		

Register	18	value:
00		

Register	19	value:
00		

Register	20	value:
----------	----	--------

```

0000000000000000000000000000000000000000000000000000000000000000
Register                21                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                22                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                23                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                24                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                25                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                26                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                27                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                28                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                29                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                30                                value:
0000000000000000000000000000000000000000000000000000000000000000
Register                31                                value:
0000000000000000000000000000000000000000000000000000000000000000

```

Conclusion:

```

li, 1, 65535, r0
li, 0, 65535, r0
bcw, , r0, r0
li, 1, 65535, r1
li, 0, 65535, r1
bcw, , r1, r1
li, 1, 10, r2
li, 0, 10, r2
bcw, , r2, r2
MA, r0, r1, r2, r3
MS, r0, r1, r2, r4
l, r0, r1, r2, r5
h, r0, r1, r2, r6
li, 1, 32768, r7
li, 0, 32768, r7
bcw, , r7, r7
li, 1, 32767, r8
li, 0, 32767, r8
bcw, , r8, r8
ahs, r8, r2, r9
sfhs, r2, r7, r10
sfhs, r7, r2, r11
ahs, r0, r2, r12
sfhs, r0, r2, r13

```

regfile	FFFFFFFFFFFFFFFF, ...	
regfile[0]	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
regfile[1]	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
regfile[2]	000A000A000A000A	000A000A000A000A
regfile[3]	000A000B000A000B	000A000B000A000B
regfile[4]	000A000B000A000B	000A000B000A000B
regfile[5]	000A0009000A0009	000A0009000A0009
regfile[6]	000A0009000A0009	000A0009000A0009
regfile[7]	8000800080008000	8000800080008000
regfile[8]	7FFF7FFF7FFF7FFF	7FFF7FFF7FFF7FFF
regfile[9]	7FFF7FFF7FFF7FFF	7FFF7FFF7FFF7FFF
regfile[10]	8000800080008000	8000800080008000
regfile[11]	7FFF7FFF7FFF7FFF	7FFF7FFF7FFF7FFF
regfile[12]	0009000900090009	0009000900090009
regfile[13]	000B000B000B000B	000B000B000B000B

We can see from the instruction and result in hex that the MA,MS,l,h,abs,sfhs,ahs,sfhs can perform signed math operation well. And the abs and sfhs are limited with minimum value -32768 and maximum value 32767.

[illegible]

[illegible]

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 2.700000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

```
value: UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU10000000000000000000000000000  
wrote in address 00000
```

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000001000000000000000 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

```
current cycle instruction: 000000001000000000000000
```

current cycle opcode: 0000

current cycle Register Read 1 address: 00000

[illegible]

current cycle Register Read 2 address: 00000

[illegible]

current cycle Register Read 3 address: 00000

[illegible]

PERIOD: 2.750000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

```
value: 100000000000000000000000000010000000000000000000000000000 wrote in
address 00000
```

Pipeline stage 3 status: InsD

Exe result:

current instruction 100111111111111100001 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

[illegible]

[illegible]

00

current cycle Register Read 3 address: 1111

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

[illegible]

PERIOD: 3.050000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

[illegible]

Pipeline stage 3 status: InsD

Exe result:

current instruction 10000000000000000100010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

```
current cycle instruction: 1000000000000000000100010
```

current cycle opcode: 0001

current cycle Register Read 1 address: 00001

current	cycle	Register	Read	1	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
---------	-------	----------	------	---	--------

[illegible]

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
---------	-------	----------	------	---	--------

[illegible]

PERIOD: 3.100000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

[illegible]

Pipeline stage 3 status: InsD

Exe result:

current instruction 10000000000000000100010 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

```
current cycle instruction: 1000000000000000000100010
```


[illegible]

[illegible]

current cycle Register Read 3 address: 00001

[illegible]

PERIOD: 3.400000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

```
value: 0000000000000001000000000000000100000000000000010000000000000001 wrote in
address 00010
```

Pipeline stage 3 status: InsD

Exe result:

current instruction 100111111111111100011 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

```
current cycle instruction: 10011111111111111100011
```

current cycle opcode: 0001

current cycle Register Read 1 address: 00010

[illegible]

current cycle Register Read 2 address: 00000

[illegible]

current cycle Register Read 3 address: 00001

[illegible]

PERIOD: 3.450000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 101111111111111100011 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

```
value: 000000000000000100000000000000100000000000000111111111111111 wrote in
address 00011
```

This cycle writing register? 1

```
current cycle instruction: 1011111111111111111100011
```

current cycle opcode: 1111

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000001100011

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.600000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

value: 0000000000000001000000000000000111111111111111111111111111111111 wrote in address 00011

Pipeline stage 2 status: InsD

Exe result:

current instruction 000000001000000001100011 decoded, generate opcode and operands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 000000001000000001100011

current cycle opcode: 1111

current cycle Register Read 1 address: 11111

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 11111

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 11111

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.650000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 00 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 010000010000100000100100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 010000010000100000100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
00					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
00					

PERIOD: 3.700000e+001 ns

Pipeline stage 1 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 2 status: Exe

Exe result:

value: 11 wrote in address 00011

Pipeline stage 3 status: InsD

Exe result:

current instruction 010000010000100000100100 decoded, generate opcode and oprands for next cycle

This cycle writing register? 1

current cycle instruction: 010000010000100000100100

current cycle opcode: 0001

current cycle Register Read 1 address: 00011

current	cycle	Register	Read	1	value:
00					

current cycle Register Read 2 address: 00000

current	cycle	Register	Read	2	value:
1000					

current cycle Register Read 3 address: 00001

current	cycle	Register	Read	3	value:
0	11111111111111111111111111111111	01111111111111111111111111111111			

PERIOD: 3.750000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 010100011000100000000101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

[illegible]

This cycle writing register? 1

```
current cycle instruction: 010100011000100000000101
```

current cycle opcode: 0010

current cycle Register Read 1 address: 00001

[illegible]

current cycle Register Read 2 address: 00010

[illegible]

current cycle Register Read 3 address: 00010

[illegible]

PERIOD: 3.800000e+001 ns

Pipeline stage 1 status: InsD

Exe result:

current instruction 010100011000100000000101 decoded, generate opcode and oprands for next cycle

Pipeline stage 2 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

Pipeline stage 3 status: Exe

Exe result:

[illegible]

This cycle writing register? 1

current cycle instruction: 010100011000100000000101

current cycle opcode: 0010

current cycle Register Read 1 address: 00001

[illegible]

PERIOD: 3.850000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

[illegible]

Pipeline stage 2 status: InsD

Exe result:

current instruction 011000010000100000000110 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

Exe result:

next instruction fetched, will be decoded in next cycle

This cycle writing register? 1

current cycle instruction: 011000010000100000000110

current cycle opcode: 0011

current cycle Register Read 1 address: 00000

[illegible]

PERIOD: 3.900000e+001 ns

Pipeline stage 1 status: Exe

Exe result:

```
value: 1000000000000000000000000000100000000000000000000000000 wrote in
address 00101
```

Pipeline stage 2 status: InsD

Exe result:

current instruction 011000010000100000000110 decoded, generate opcode and oprands for next cycle

Pipeline stage 3 status: InsF

[illegible]

[illegible]

current cycle Register Read 3 address: 00011

Program execution result in Register file:

[illegible]

Register	26	value:
00		
Register	27	value:
00		
Register	28	value:
00		
Register	29	value:
00		
Register	30	value:
00		
Register	31	value:
00		

Conclusion:

```

li, 1, 32768, r0
li, 0, 0, r0
bcw, , r0, r0
li, 0, 65535, r1
li, 1, 32767, r1
bcw, , r1, r1
li, 0, 1, r2
li, 1, 1, r2
bcw, , r2, r2
li, 0, 65535, r3
li, 1, 65535, r3
bcw, , r3, r3
MA, r2, r2, r1, r4
MS, r3, r2, r0, r5
l, r2, r2, r0, r6
h, r3, r2, r1, r7

```

regfile	8000000080000000, ...	
regfile[0]	8000000080000000	8000000080000000
regfile[1]	7FFFFFFF7FFFFFFF	7FFFFFFF7FFFFFFF
regfile[2]	0001000100010001	0001000100010001
regfile[3]	FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF
regfile[4]	7FFFFFFF7FFFFFFF	7FFFFFFF7FFFFFFF
regfile[5]	8000000080000000	8000000080000000
regfile[6]	8000000080000000	8000000080000000
regfile[7]	7FFFFFFF7FFFFFFF	7FFFFFFF7FFFFFFF

Comparing the instruction loaded with the register result in hex, we can easily see that the MA,MS,l,h operations operating under limitation -2^{31} to $+2^{31}$ well. it also shows the ability of MA,MS,l,h to do signed math operation.