



Mid Term Project

Part 1: MIPS Registers (10 Points)

Instruction Set
Architecture
(ISA) - Part V

Vikram
Padman

Mid Term

Part 1
Part 2
Part 3

- ① Why is the instruction and data memory separated in MIPS_SS_v2 CPU? (2.5)
- ② Explain the advantage and disadvantage of separate instruction and data memory (2.5)
- ③ MIPS_SS_v2's clock rate (5):
 - ① What is the PLL's clock rate or frequency?
 - ② What is the highest clock rate that could be achieved without any modifications?
 - ③ What limits the clock rate in the design?



Mid Term Project

Part 2: Understanding Simple CPU (mips_ss_v2.qar) (20 Points)

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Part 1

Part 2

Part 3

Understanding Simple CPU (mips_ss_v2) is important to complete the rest of the midterm project. In this part you will write an assembly programs in binary and execute it in mips_ss_v2 CPU running in DE0-Nano.

Triangular Number Generator: (20)

- 1 Write a program that generates Triangular numbers up to $n=20$ and count backwards to 0.
- 2 Your program should display 8 least significant bits of each number you generate in the above part through the LEDs.
- 3 While counting back you should blink the LEDs whenever the count reaches 0 or 20

For this part you must submit the programs you wrote and signal tap II capture file.



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Part 3: Advanced Addressing modes (mips_ss_v2.qar) (70 Points)

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Part 1

Part 2

Part 3

As implemented, mips_ss_v2 only supports register and immediate addressing modes. For this part add the following addressing modes to mips_ss_v2:

- 1 Displacement (30)
- 2 Register indirect (40)

You report should at least contain, but not limited to, the following: Instruction formats, implementation details, modification to control unit and signal, detailed description of any new modules you implemented.¹

Refer to the last years midterm project report to understand what your report should contain.

¹Partial credit (75% max) will awarded for a reasonable non-functional