Final Exam

CS6133 - Computer Architecture I

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Digital Design
Part 1 - 25 Points

- Consider the 4 x 4 multiplier described in Digital Design and Computer Architecture, chapter 5 section 5.2.6 and answer the following questions:
  1. Redesign the multiplier such that it is synchronize to a 1Ghz clock source.
  2. Prove, by calculating the worse case combinatorial propagation delays, that your synchronize multiplier works reliably over $0\,^{\circ}\mathrm{C}$ to $100\,^{\circ}\mathrm{C}$ temperature range.
- Assume the following propagation delays:

Temp. \ L.E.	Gate	ALU
$100\,^{\circ}\mathrm{C}$	310ps $\pm$10ps	600ps $\pm$10ps
$50\,^{\circ}\mathrm{C}$	260ps $\pm$10ps	500ps $\pm$10ps
$0\,^{\circ}\mathrm{C}$	210ps $\pm$10ps	400ps $\pm$10ps

Simple CPU

Part 2 - 25 Points

Considering the MIPS_SS_v2 (Simple CPU) and its ISA for this part.

1. How does the simple CPU handle illegal instructions? Describe, with details, what Simple CPU does when an undefined opcode and/or funct code is presented.
2. Redesign Simple CPU's ALU to support the following instructions:
   - ble rx, ry, offset: pc += (rx < ry) ? (offset + 4) : 4
   - bge rx, ry, offset: pc += (rx > ry) ? (offset + 4) : 4

Note: You are only required to show modification to Simple CPU's ALU for question 2.

Pipelined CPU

Part 3 - 25 Points

Considering the MIPS_SS_v2 and its ISA for this part.

1. Assume the Simple CPU is pipelined, as described in lecture, what type of hazards would you encounter in Simple CPU. Remember you only have to consider instructions supported by Simple CPU.
2. Could a "NOP" inserter mitigate all hazards you listed above? Support your answer with details.

Memory
Part 4 - 25 Points

Consider the following code:

```
1| char *a, *b, *c;
2| <allocate 2^29 bytes of memory to a,b>
3| <allocate 2^12 bytes of memory to c>
4| for(i=0; i<=2^29; i++)
5|   a[i] = b[i] + c[(i mod 2^12)];
```

Assume the following cache requirements :

- DDR memory's smallest transfer size is 512 bits or 64 bytes.
- L2 cache is 16MB and is composed of 4096 4KB cache lines. A cache line is the smallest unit that could be transferred between DDR and L2 cache.
- The memory subsystem is aligned to 4KB memory boundaries. Assume that memory allocation confirms to 4KB alignment.

Answer the following questions:

1. Find an optimal cache architecture (direct, n-way associative or fully associative) that would yield the best performance with lowest implementation complexity.
2. What type of replacement algorithm would yield the lowest miss rate?

I/O Connectivity and Technology

Part 5 - 25 Extra Points

Consider Parallel BUS and Serial links described in I/O lecture for this part. State which I/O architecture (serial or parallel) is optimal for each of the following scenarios:

1. Lots of random 32-bit word transfers between CPU and I/O peripherals
2. Large amount contiguous burst transfers occur between I/O peripherals and a few burst transfer between I/O peripherals and CPU
3. Both burst transfers and few 32-bit word transfers between CPU and I/O peripherals.

You should support your answers with sufficient details. [1]

[1] Consider overhead associated with parallel and serial links