Xiaoyang Wang

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Education

Dec 2017 **Northwestern University**, U.S.
Master of Science in Computer Engineering
Gpa: 3.9/4.0

Jun 2016 **Central South University**, China
Bachelor of Engineering in Automation
Gpa: 87.8/100

Research Experience

Nov 2017 – Present | Optimizing Non-Deterministic Parallel Programs
Implementing control and data flow analysis in LLVM to identify the function affected by rand().

Sep 2017 – Present | Predicting Optimizations to Reduce Energy Consumption
Collected and read related papers, verified the innovation of the research idea.
Analyzed performance and power behaviors of a multi-CPU system running HPC benchmark compiled with different GCC optimization options.

Mar 2017 – Present | Bringing Hard Real-Time to the Parallel Hybrid Runtime in Nautilus AeroKernel
Brainstormed and discussed the parallel thread implementation ideas with research advisor and partner.
Contributed to public code repositories: thread group functionality and group scheduling capability as well as group scheduling test and shell support.
Found and killed bugs in an existing real-time scheduler and other related modules.
Measured the performance and the synchronization across different cores of the new functionalities and narrowed down the potential asynchronous issues.
Combining OpenMP runtime with our group thread APIs.

Apr-Aug 2017 | Minimizing Thermal Variation Across Heterogeneous HPC Nodes Utilizing FPGAs
Analyzed thermal behaviors of a multi-FPGA system running HPC tasks.
Developed a machine learning-based task-placement method to reduce the temperature of the system.
Delivered an oral presentation at Chameleon User Meeting, Argonne National Lab.
Submitted a paper to DAC(Design Automation Conference) Conference.

Jan-Mar 2017 | Porting Unified Parallel C(UPC) Language to Nautilus AeroKernel
Wrote makefiles, hacked the UPC compiler script to compile and link the UPC source code to Nautilus.
Modified the UPC and GASNet source code, implemented missing Linux system calls in Nautilus AeroKernel.
Led the team.

Course Projects

May 2017 | Distributed Hash Table
Implemented a Kademlia DHT with Vanish in Go language.

Mar 2017 | Neural Networks on CUDA
Wrote a back-propagate neural network to recognize hand-written digits pictures on CUDA.

Feb 2017 | Network Stacks
Wrote HTTP protocol stack, TCP protocol stack and implemented routing algorithms in C/C++.

Publications

P. Dinda, **X. Wang**, J. Wang, C. Beauchene, C. Hetland, "Bringing Hard Real-Time to the Parallel Hybrid Runtime", *International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*. ACM, 2018. [In Preparation]

Y. Luo, **X. Wang**, G. Memik, S. Ogrenci-Memik, K. Yoshii, P. Beckman, "Title Not Included due to Double-Blind Review", *Design Automation Conference (DAC)*. IEEE, 2018.[Submitted]

Skills

Programming: C/C++, Go, VHDL, Racket, Perl, Python, Shell, SQL, Assembly
System Tool: GNU make, LLVM, Flex, Bison, GDB, Git