Xiaoyang Wang

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Education

Present **University of Illinois at Urbana–Champaign**, U.S.
Ph.D student in Computer Science

Dec 2017 **Northwestern University**, U.S.
M.S. in Computer Engineering
Gpa: 3.9/4.0

Jun 2016 **Central South University**, China
B.E. in Automation
Gpa: 87.8/100

Research Experience

Mar-Dec 2017 | Hard Real-time Scheduling for Parallel Run-time Systems in Nautilus AeroKernel

Developed a parallel thread concept for a kernel and contributed to public code repositories: thread group functionality and group scheduling capability as well as group scheduling test and shell support.

Found and fixed bugs in an existing real-time scheduler and other related modules.

Measured the performance and the synchronization across different cores of the new functionalities and narrowed down the potential asynchronous issues.

Combining OpenMP runtime with our group thread APIs.

Apr-Aug 2017 | Minimizing Thermal Variation Across Heterogeneous HPC Nodes with FPGAs

Analyzed thermal behaviors of a multi-FPGA system running HPC tasks.

Developed a machine learning-based task-placement method to reduce the temperature of the system.

Jan-Mar 2017 | Porting Unified Parallel C(UPC) Language to Nautilus AeroKernel

Wrote makefiles, hacked the UPC compiler script to compile and link the UPC source code to Nautilus.

Modified the UPC and GASNet(Global-Address Space Networking) source code, implemented missing Linux system calls in Nautilus AeroKernel.

Course Projects

Dec 2017 | Code Analysis and Transformation

Implemented intra- and inter-procedure analysis, constant propagation and loop unrolling in LLVM.

May 2017 | Distributed Hash Table

Implemented a Kademlia DHT with Vanish in Go language.

Mar 2017 | Neural Networks on CUDA

Wrote a back-propagate neural network to recognize hand-written digits pictures on CUDA.

Feb 2017 | Databases

Built logic layer of web service (based on DBI) to process data and Query between client and Oracle database.

Implemented B-Tree in C/C++ that runs on top of a buffer cache which runs on top of a simulated disk system.

Feb 2017 | Network Stacks

Wrote HTTP protocol stack, TCP protocol stack and implemented routing algorithms in C/C++.

Dec 2016 | Pipeline Processor

Wrote a five-stage pipeline processor with stall, forward and kill hazard handling in VHDL.

Publications

P. Dinda, **X. Wang**, J. Wang, C. Beauchene, C. Hetland, "Hard Real-time Scheduling for Parallel Run-time Systems", *International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*. ACM, 2018.

Y. Luo, **X. Wang**, G. Memik, S. Ogrenci-Memik, K. Yoshii, P. Beckman, "Minimizing Thermal Variation in Heterogeneous HPC Systems with FPGA Nodes", *International Conference on Computer Design (ICCD)*. IEEE, 2018.

Skills

Programming: C/C++, Go, VHDL, Racket, Perl, Python, Shell, SQL, Assembly
System Tool: GNU make, LLVM, Flex, Bison, GDB, Git