Xiaoyang Wang

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Education

Present **University of Illinois at Urbana–Champaign**, U.S.
Ph.D student in Computer Science
Gpa: 4.0/4.0

Dec 2017 **Northwestern University**, U.S.
M.S. in Computer Engineering
Gpa: 3.9/4.0

Jun 2016 **Central South University**, China
B.E. in Automation
Gpa: 87.8/100

Research Experience

Present | Unified High-performance Collective Messaging Library
Implementing virtual hyper-cube based dimensional exchange AllGather algorithm in Charm++.

Mar-Dec 2017 | Hard Real-time Scheduling for Parallel Run-time Systems in Nautilus AeroKernel
Developed a parallel thread concept for a kernel and contributed to public code repositories: thread group functionality and group scheduling capability as well as group scheduling test and shell support.
Measured the performance and the synchronization across different cores of the new functionalities and narrowed down the potential asynchronous issues.
Found the asynchronization can be limited within 4,000 cycles/3 μs among 255 parallel threads on Intel Xeon Phi.

Apr-Aug 2017 | Minimizing Thermal Variation in Heterogeneous HPC Systems with FPGA Nodes
Analyzed thermal behaviors of a multi-FPGA system running HPC tasks.
Developed a machine learning-based task-placement method to reduce the temperature of the system.
Reduced the system's peak temperature by 4.21°C and peak power by 1.50 W on average.

Selected Projects

Dec 2018 | Exploring Effects of Local Clock Skew in Deep Learning Frameworks
Profiled distributed deep learning with Horovod based Tensorflow and analyzed systems tracing.

Dec 2017 | Code Analysis and Transformation
Implemented intra- and inter-procedure analysis, constant propagation and loop unrolling in LLVM.

May 2017 | Distributed Hash Table
Implemented a Kademlia DHT with Vanish in Go language.

Mar 2017 | Neural Networks on CUDA
Wrote a back-propagate neural network to recognize hand-written digits pictures on CUDA.

Feb 2017 | Database
Implemented B-Tree in C/C++ that runs on top of a buffer cache which runs on top of a simulated disk system.

Feb 2017 | Network Stacks
Wrote HTTP protocol stack, TCP protocol stack and implemented routing algorithms in C/C++.

Publications

P. Dinda, **X. Wang**, J. Wang, C. Beauchene, C. Hetland, "Hard Real-time Scheduling for Parallel Run-time Systems", *International Symposium on High-Performance Parallel and Distributed Computing (HPDC)*. ACM, 2018.

Y. Luo, **X. Wang**, G. Memik, S. Ogrenci-Memik, K. Yoshii, P. Beckman, "Minimizing Thermal Variation in Heterogeneous HPC Systems with FPGA Nodes", *International Conference on Computer Design (ICCD)*. IEEE, 2018.

Skills

Programming: C/C++, Java, Go, Python, SQL, MPI, OpenMP
System Tool: GNU make, LLVM, Git