Pre-Lab for Lab 1

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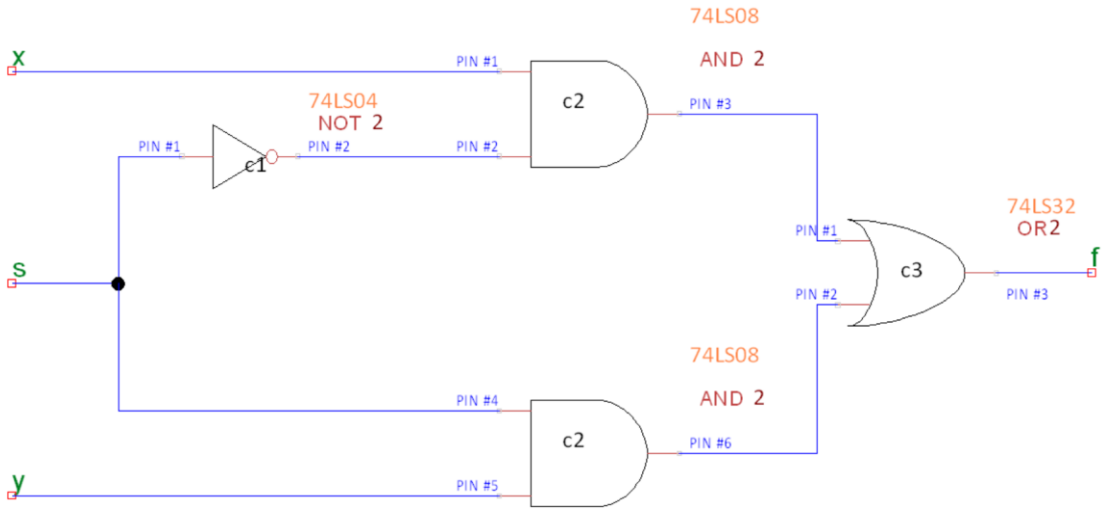
Part I

$$f = xs' + ys$$

1. Draw a 2-to-1 multiplexer design using the gates specified above.



CHIPS USED:

C1 – 74LS04

C2 – 74LS08

C3 – 74LS32

CONNCETED TO ALL CHIPS:

PIN#7 – Gnd

PIN#14 – Vcc

2. Write out the truth table for the design and show that to the TA as well as part of the prelab.

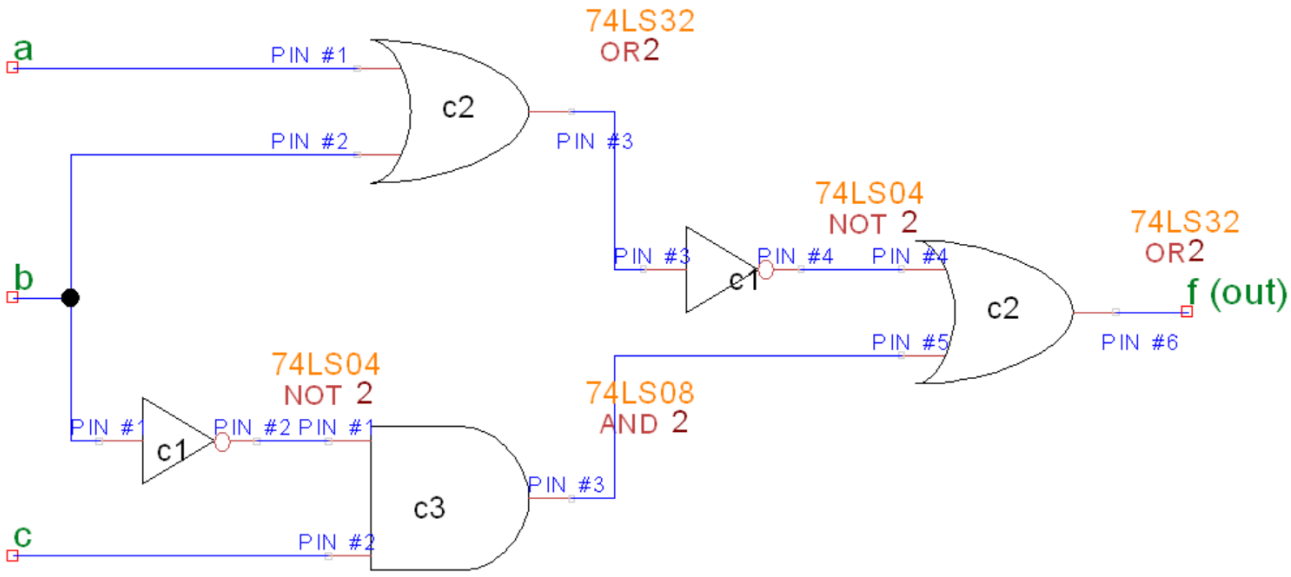
x	y	s	xs' + ys

0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Part II

$$f = (a + b)' + cb'$$

1. Draw the function shown above using the gates specified in the lab preparation..



CHIPS USED:

C1 – 74LS04

C2 – 74LS32

C3 – 74LS08

CONNCETED TO ALL CHIPS:

PIN#7 – Gnd

PIN#14 – Vcc

2. Write out the truth table for the design and show that to the TA as well as part of the prelab.

a	b	c	f = (a + b)’ + cb’
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

3. Wire your design on the protoboard and demonstrate the functionality to the TA. Your results should match your truth table from the prelab.
4. Is there a cheaper implementation for your design, assuming you are still limited to using the same three chip types? If yes, explain by rewriting the

boolean function. For this question we consider a given implementation cheaper if it uses fewer gates or if it uses the same number of gates but fewer chips.

Yes, there exists a cheaper implementation.

$$f = (a + b)' + cb'$$

$$= (a'b') + cb'$$

$$= b'(a' + c)$$