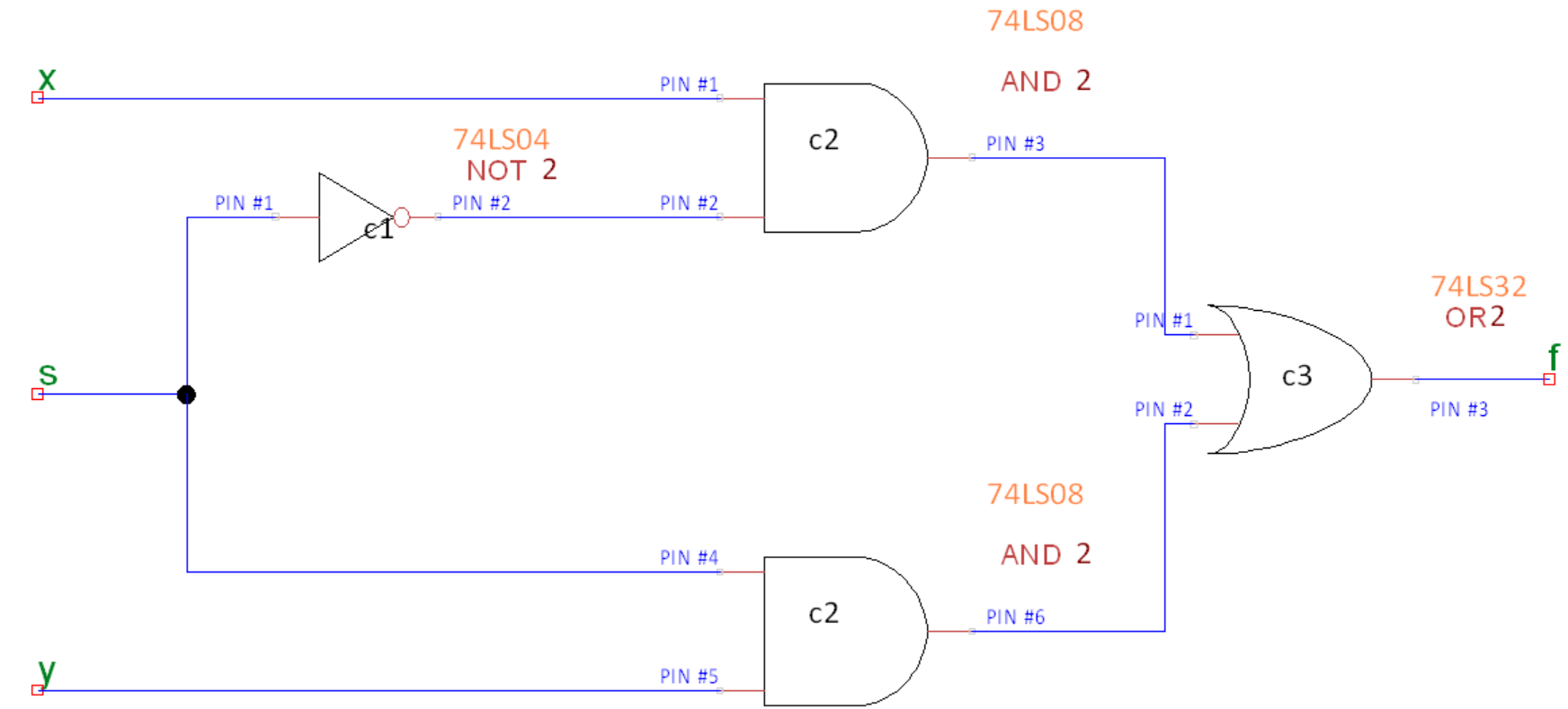
*f = xs’ + ys*

1. Draw a 2-to-1 multiplexer design using the gates specified above.



**CHIPS USED:**

C1 – 74LS04

C2 – 74LS08

C3 – 74LS32

**CONNCETED TO ALL CHIPS:**

PIN#7 – Gnd

PIN#14 – Vcc

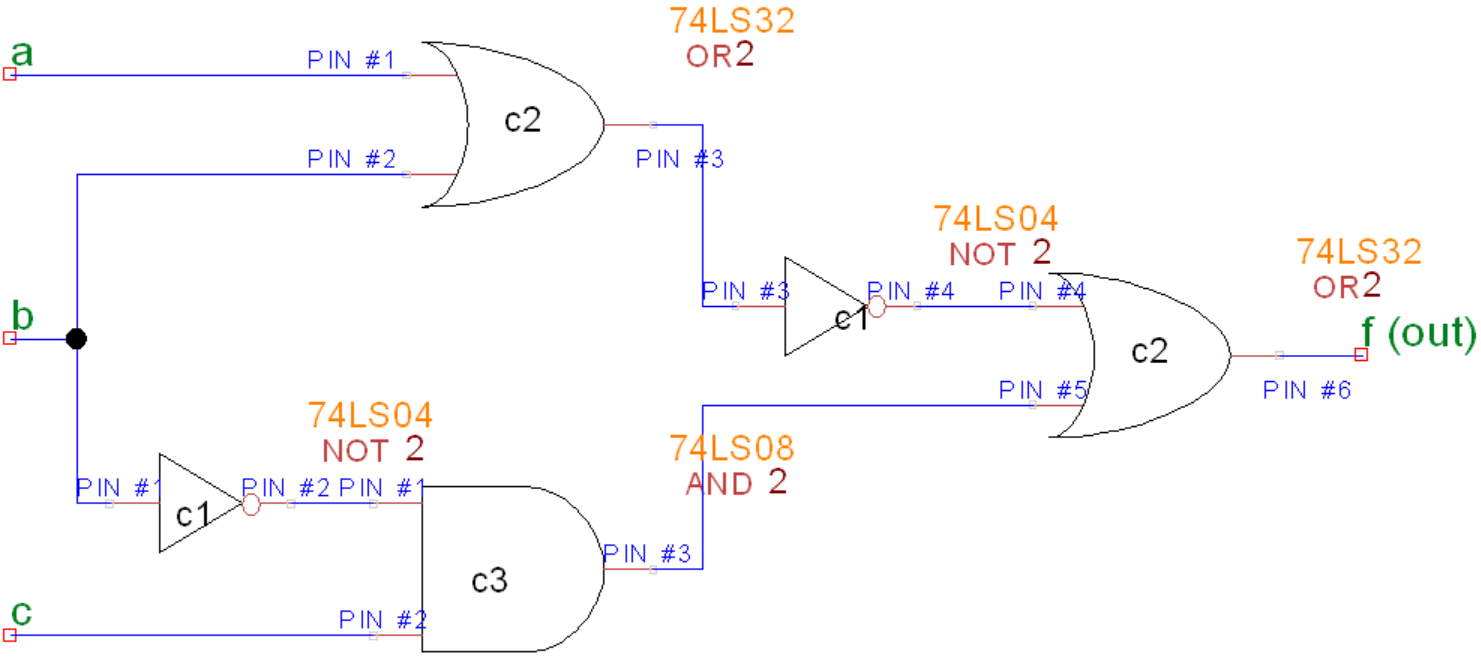
1. Write out the truth table for the design and show that to the TA as well as part of the prelab.

|  |  |  |  |
| --- | --- | --- | --- |
| x | y | s | xs’ + ys |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

**Part II**

*f = (a + b)’ + cb’*

1. Draw the function shown above using the gates specified in the lab preparation..



**CHIPS USED:**

C1 – 74LS04

C2 – 74LS32

C3 – 74LS08

**CONNCETED TO ALL CHIPS:**

PIN#7 – Gnd

PIN#14 – Vcc

1. Write out the truth table for the design and show that to the TA as well as part of the prelab.

|  |  |  |  |
| --- | --- | --- | --- |
| a | b | c | f = (a + b)’ + cb’ |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |